

## **CHAPTER 1**

### *Introduction to Power Semiconductors*

*1.1 General*

*1.2 Power MOSFETS*

*1.3 High Voltage Bipolar Transistors*



*General*



## 1.1.1 An Introduction To Power Devices

Today's mains-fed switching applications make use of a wide variety of active power semiconductor switches. This chapter considers the range of power devices on the market today, making comparisons both in terms of their operation and their general areas of application. The P-N diode will be considered first since this is the basis of all active switches. This will be followed by a look at both 3 layer and 4 layer switches.

Before looking at the switches let's briefly consider the various applications in which they are used. Virtually all mains fed power applications switch a current through an inductive load. This is the case even for resonant systems where the operating point is usually on the "inductive" side of the resonance curve. The voltage that the switch is normally required to block is, in the majority of cases, one or two times the maximum rectified input voltage depending on the configuration used. Resonant applications are the exception to this rule with higher voltages being generated by the circuit. For 110-240 V mains, the required voltage ratings for the switch can vary from 200 V to 1600 V.

Under normal operating conditions the off-state losses in the switch are practically zero. For square wave systems, the on-state losses (occurring during the on-time), are primarily determined by the on-state resistance which gives rise to an on-state voltage drop,  $V_{ON}$ . The (static) on-state losses may be calculated from:

$$P_{STATIC} = \delta \cdot V_{ON} \cdot I_{ON} \quad (1)$$

At the end of the "ON" time the switch is turned off. The turn-off current is normally high which gives rise to a loss dependent on the turn-off properties of the switch. The process of turn-on will also involve a degree of power loss so it is important not to neglect the turn-on properties either. Most applications either involve a high turn-on current or the current reaching its final value very quickly (high  $di/dt$ ). The total dynamic power loss is proportional to both the frequency and to the turn-on and turn-off energies.

$$P_{DYNAMIC} = f \cdot (E_{ON} + E_{OFF}) \quad (2)$$

The total losses are the sum of the on-state and dynamic losses.

$$P_{TOT} = \delta \cdot V_{ON} \cdot I_{ON} + f \cdot (E_{ON} + E_{OFF}) \quad (3)$$

The balance of these losses is primarily determined by the switch used. If the on-state loss dominates, operating frequency will have little influence and the maximum frequency of the device is limited only by its total delay time (the sum of all its switching times). At the other extreme a device whose on-state loss is negligible compared with the switching loss, will be limited in frequency due to the increasing dynamic losses.

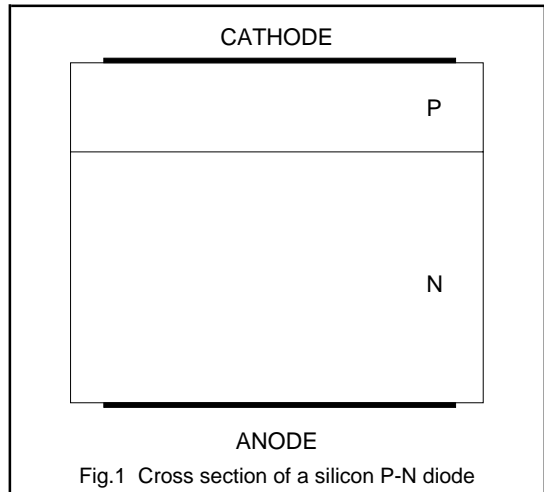
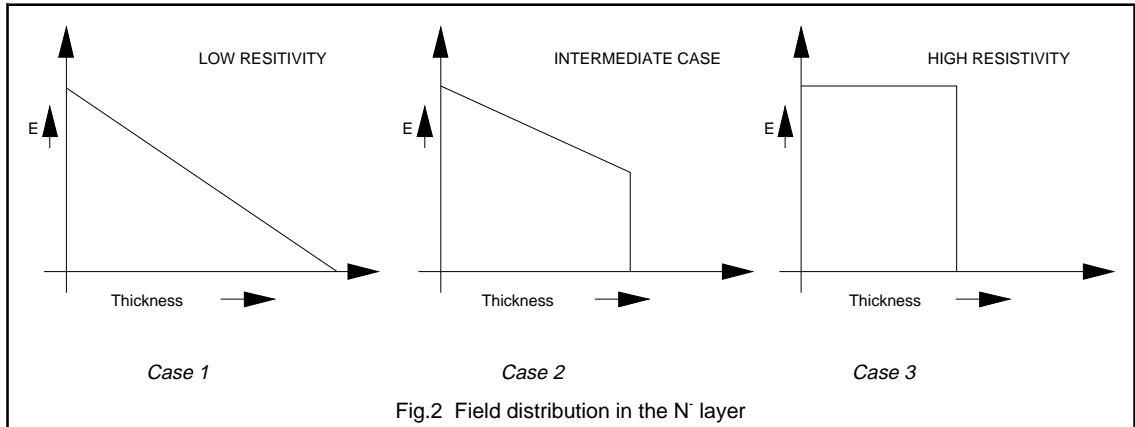


Fig.1 Cross section of a silicon P-N diode

**High frequency switching** When considering frequency limitation it is important to realise that the real issue is not just the frequency, but also the minimum on-time required. For example, an SMPS working at 100 kHz with an almost constant output power, will have a pulse on-time  $t_p$  of about 2-5  $\mu$ s. This can be compared with a high performance UPS working at 10 kHz with low distortion which also requires a minimum on-time of 2  $\mu$ s. Since the 10 kHz and 100 kHz applications considered here, require similar short on-times, both may be considered high frequency applications.

**Resonant systems** have the advantage of relaxing turn-on or turn-off or both. This however tends to be at the expense of V-A product of the switch. The relaxed switching conditions imply that in resonant systems switches can be used at higher frequencies than in non resonant systems. When evaluating switches this should be taken into account.



At higher values of *throughput power*, the physical size of circuits increases and as a consequence, the stray inductances will also tend to increase. Since the required currents are higher, the energy stored in the stray inductances rises significantly, which in turn means the induced peak voltages also rise. As a result such applications force the use of longer pulse times, to keep losses down, and protection networks to limit overshoot or networks to slow down switching speeds. In addition the use of larger switches will also have consequences in terms of increasing the energy required to turn them on and off and drive energy is very important.

So, apart from the voltage and current capabilities of devices, it is necessary to consider static and dynamic losses, drive energy,  $dV/dt$ ,  $dI/dt$  and Safe Operating Areas.

### The silicon diode

Silicon is the semiconductor material used for all power switching devices. Lightly doped N<sup>-</sup> silicon is usually taken as the starting material. The resistance of this material depends upon its resistivity, thickness and total area.

$$R = \rho \cdot \frac{l}{A} \quad (4)$$

A resistor as such does not constitute an active switch, this requires an extra step which is the addition of a P-layer. The result is a diode of which a cross section is drawn in Fig.1

### The blocking diode

Since all active devices contain a diode it is worth considering its structure in a little more detail. To achieve the high blocking voltages required for active power switches necessitates the presence of a thick N<sup>-</sup> layer. To withstand a given voltage the N<sup>-</sup> layer must have the right

combination of thickness and resistivity. Some flexibility exists as to what that combination is allowed to be, the effects of varying the combination are described below.

#### Case 1: Wide N<sup>-</sup> layer and low resistivity

Figure 2 gives the field profile in the N<sup>-</sup> layer, assuming the junction formed with the P layer is at the left. The maximum field at the P-N junction is limited to 22 kV/cm by the breakdown properties of the silicon. The field at the other end is zero. The slope of the line is determined by the resistivity. The total voltage across the N<sup>-</sup> layer is equal to the area underneath the curve. Please note that increasing the thickness of the device would not contribute to its voltage capability in this instance. This is the normal field profile when there is another P-layer at the back as in 4 layer devices (described later).

#### Case 2: Intermediate balance

In this case the higher resistivity material reduces the slope of the profile. The field at the junction is the same so the same blocking voltage capability (area under the profile) can be achieved with a thinner device.

The very steep profile at the right hand side of the profile indicates the presence of an N<sup>+</sup> layer which often required to ensure a good electrical contact

#### Case 3: High resistivity material

With sufficiently high resistivity material a near horizontal slope to the electric field is obtained. It is this scenario which will give rise to the thinnest possible devices for the same required breakdown voltage. Again an N<sup>+</sup> layer is required at the back.

An optimum thickness and resistivity exists which will give the lowest possible resistance for a given voltage capability. Both case 1 (very thick device) and case 3 (high resistivity) give high resistances, the table below shows the thickness and resistivity combinations possible for a 1000 V diode.

The column named RA gives the resistance area product. (A device thickness of less than 50  $\mu\text{m}$  will never yield 1000 V and the same goes for a resistivity of less than 26  $\Omega\text{cm}$ .) The first specification is for the thinnest device possible and the last one is for the thickest device, (required when a P layer is present at the back). It can be seen that the lowest resistance is obtained with an intermediate value of resistivity and material thickness.

Thickness ( $\mu\text{m}$ )	Resistivity ( $\Omega\text{cm}$ )	RA $\Omega\text{cm}^2$	Comments
50	80	0.400	case 3
60	34	0.204	
65	30	0.195	
70	27	0.189	min. R
75	26	0.195	
80	26	0.208	
90	26	0.234	
100	26	0.260	case 1

To summarise, a designer of high voltage devices has only a limited choice of material resistivity and thickness with which to work. The lowest series resistance is obtained for a material thickness and resistivity intermediate between the possible extremes. This solution is the optimum for all majority carrier devices such as the PowerMOSFET and the J-FET where the on-resistance is uniquely defined by the series resistance. Other devices make use of charge storage effects to lower their on-state voltage. Consequently to optimise switching performance in these devices the best choice will be the thinnest layer such that the volume of stored charge is kept to a minimum. Finally as mentioned earlier, the design of a 4 layer device requires the thickest, low resistivity solution.

### The forward biased diode

When a diode is forward biased, a forward current will flow. Internally this current will have two components: an electron current which flows from the N layer to the P layer and a hole current in the other direction. Both currents will generate a charge in the opposite layer (indicated with  $Q_p$  and  $Q_n$  in Fig.3). The highest doped region will deliver most of the current and generate most of the charge. Thus in a  $P^+N^-$  diode the current will primarily be made up of holes flowing from P to N and there will be a significant volume of hole charge in the N<sup>-</sup> layer. This point is important when discussing active devices: whenever a diode is forward biased (such as a base-emitter diode) there will be a charge stored in the lowest doped region.

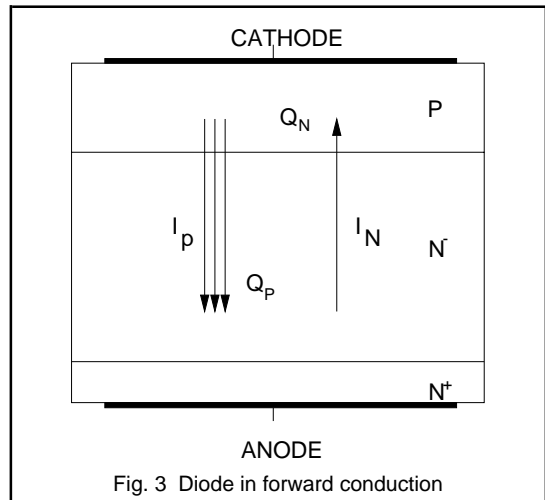


Fig. 3 Diode in forward conduction

The exact volume of charge that will result is dependent amongst other things on the minority carrier lifetime,  $\tau$ . Using platinum or gold doping or by irradiation techniques the value of  $\tau$  can be decreased. This has the effect of reducing the volume of stored charge and causing it to disappear more quickly at turn-off. A side effect is that the resistivity will increase slightly.

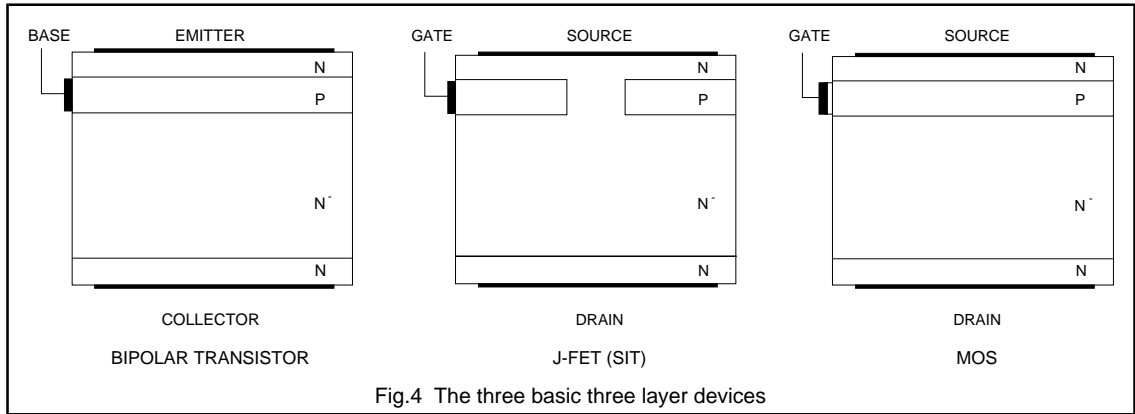
### Three Layer devices

The three basic designs, which form the basis for all derived 3 layer devices, are given in Fig.4. It should be emphasised here that the discussion is restricted to high voltage devices only as indicated in the first section. This means that all relevant devices will have a *vertical structure*, characterised by a wide N-layer.

The figure shows how a three layer device can be formed by adding an N type layer to the P-N diode structure. Two back to back P-N diodes thus form the basis of the device, where the P layer provides a means to control the current when the device is in the on-state.

There are three ways to use this P-layer as a control terminal. The first is to feed current into the terminal itself. The current through the main terminals is now proportional to the drive current. This device is called a *High Voltage Transistor* or *HVT*.

The second one is to have openings in the P-layer and permit the main current to flow between them. When reverse biasing the gate-source, a field is generated which blocks the opening and pinches off the main current. This device is known as the *J-FET* (junction FET) or *SIT* (Static Induction Transistor).



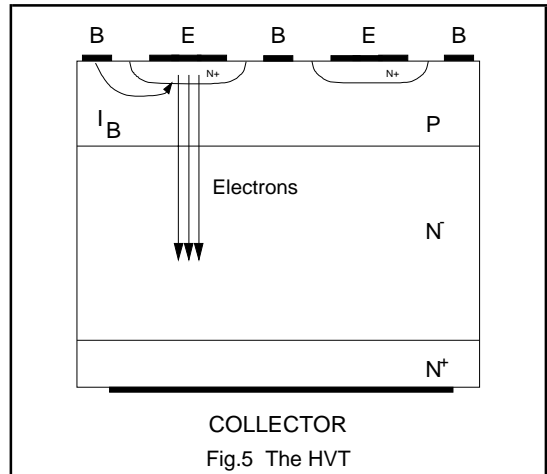
The third version has an electrode (gate) placed very close to the P-layer. The voltage on this gate pushes away the holes in the P-area and attracts electrons to the surface beneath the gate. A channel is thus formed between the main terminals so current can flow. The well known name for this device is *MOS transistor*.

In practice however, devices bear little resemblance to the constructions of Fig.4. In virtually all cases a planar construction is chosen i.e. the construction is such that one main terminal (emitter or source) and the drive contact are on the surface of the device. Each of the devices will now be considered in some more detail.

### The High Voltage Transistor (HVT)

The *High Voltage Transistor* uses a positive base current to control the main collector current. The relation is:  $I_C = H_{FE} \cdot I_B$ . The base drive forward biases the base emitter P-N junction and charge (holes and electrons) will pass through it. Now the base of a transistor is so thin that the most of the electrons do not flow to the base but into the collector - giving rise to a collector current. As explained previously, the ratio between the holes and electrons depend on the doping. So by correctly doping the base emitter junction, the electron current can be made much larger than the hole current, which means that  $I_C$  can be much larger than  $I_B$ .

When enough base drive is provided it is possible to forward bias the base-collector P-N junction also. This has a significant impact on the resistance of the N<sup>+</sup> layer; holes now injected from the P type base constitute stored charge causing a substantial reduction in on-state resistance, much lower than predicted by equation 4. Under these conditions the collector is an effective extension of the base. Unfortunately the base current required to maintain this



condition causes the current gain to drop. For this reason one cannot use a HVT at a very high current density because then the gain would become impractically low.

The on-state voltage of an HVT will be considerably lower than for a MOS or J-FET. This is its main advantage, but the resulting charge stored in the N<sup>+</sup> layer has to be delivered and also to be removed. This takes time and the speed of a bipolar transistor is therefore not optimal. To improve speed requires optimisation of a fine emitter structure in the form of fingers or cells.

Both at turn-on and turn-off considerable losses may occur unless care is taken to optimise drive conditions. At turn-on a short peak base current is normally required. At turn-off a negative base current is required and negative drive has to be provided.

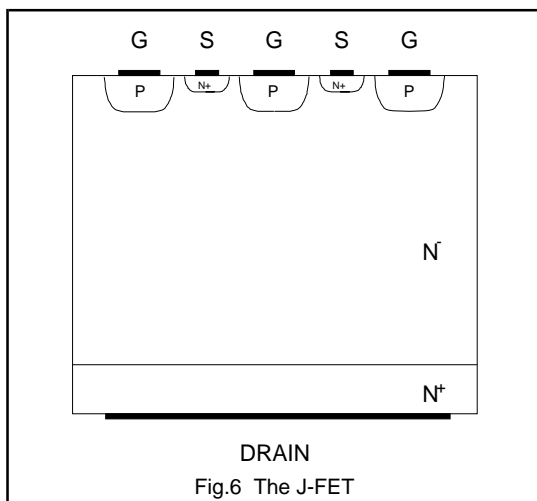


A serious limitation of the HVT is the occurrence of *second breakdown* during switch off. The current contracts towards the middle of the emitter fingers and the current density can become very high. The RBSOAR (Reverse Bias Safe Operating Area) graph specifies where the device can be used safely. Device damage may result if the device is not properly used and one normally needs a snubber (dV/dt network) to protect the device. The price of such a snubber is normally in the order of the price of the transistor itself. In resonant applications it is possible to use the resonant properties of the circuit to have a slow dV/dt.

So, the bipolar transistor has the advantage of a very low forward voltage drop, at the cost of lower speed, a considerable energy is required to drive it and there are also limitations in the RBSOAR.

### The J-FET.

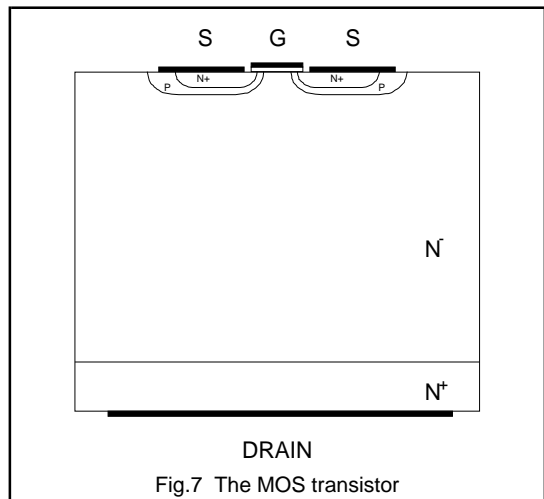
The *J-FET* (Junction Field Effect Transistor) has a direct resistance between the Source and the Drain via the opening in the P-layer. When the gate-source voltage is zero the device is on. Its on-resistance is determined by the resistance of the silicon and no charge is present to make the resistance lower as in the case of the bipolar transistor. When a negative voltage is applied between Gate and Source, a depletion layer is formed which pinches off the current path. So, the current through the switch is determined by the voltage on the gate. The drive energy is low, it consists mainly of the charging and discharging of the gate-source diode capacitance. This sort of device is normally very fast.



Its main difficulty is the opening in the P-layer. In order to speed up performance and increase current density, it is necessary to make a number of openings and this implies fine geometries which are difficult to manufacture. A solution exists in having the P-layer effectively on the surface, basically a diffused grid as shown in Fig.6. Unfortunately the voltages now required to turn the device off may be very large: it is not uncommon that a voltage of 25 V negative is needed. This is a major disadvantage which, when combined with its "normally-on" property and the difficulty to manufacture, means that this type of device is not in mass production.

### The MOS transistor.

The *MOS* (*Metal Oxide Semiconductor*) transistor is normally off: a positive voltage is required to induce a channel in the P-layer. When a positive voltage is applied to the gate, electrons are attracted to the surface beneath the gate area. In this way an "inverted" N-type layer is forced in the P-material providing a current path between drain and source.



Modern technology allows a planar structure with very narrow cells as shown in Fig.7. The properties are quite like the J-FET with the exception that the charge is now across the (normally very thin) gate oxide. Charging and discharging the gate oxide capacitance requires drive currents when turning on and off. Switching speeds can be controlled by controlling the amount of drive charge during the switching interval. Unlike the J-FET it does not require a negative voltage although a negative voltage may help switch the device off quicker.

The MOSFET is the preferred device for higher frequency switching since it combines fast speed, easy drive and wide commercial availability.

## Refinements to the basic structure

A number of techniques are possible to improve upon behaviour of the basic device.

First, the use of *finer geometries* can give lower on-state voltages, speed up devices and extend their energy handling capabilities. This has led to improved "Generation 3" devices for bipolars and to lower  $R_{DS(ON)}$  for PowerMOS. Secondly, *killing the lifetime*  $\tau$  in the device can also yield improvements. For bipolar devices, this positively effects the switching times. The gain, however, will drop, and this sets a maximum to the amount of lifetime killing. For MOS a lower value for  $\tau$  yields the so-called FREDFETs, with an intrinsic diode fast enough for many half bridge applications such as in AC Motor Controllers. The penalty here is that  $R_{DS(ON)}$  is adversely effected (slightly). Total losses, however, are decreased considerably.

## Four layer devices

The three basic designs from the previous section can be extended with a  $P^+$ -layer at the back, thereby generating three basic Four Layer Devices. The addition of this extra layer creates a PNP transistor from the  $P^+$ -N-P-layers. In all cases the 3 layer NPN device will now deliver an electron current into the back  $P^+$ -layer which acts as an emitter. The PNP transistor will thus become active which results in a hole current flowing from the  $P^+$ -layer into the high resistive region. This in its turn will lead to a *hole charge* in the high resistive region which lowers the on-state voltage considerably, as outlined above for High Voltage Transistors. Again, the penalty is in the switching times which will increase.

All the devices with an added  $P^+$ -layer at the back will inject holes into the N-layer. Since the  $P^+$ -layer is much heavier doped than the N-layer, this hole current will be the major contributor to the main current. This means that the charge in the N-layer, especially near the N- $P^+$ -junction, will be large. Under normal operation the hole current will be large enough to influence the injection of electrons from the top  $N^+$ -layer. This results in extra electron current being injected from the top, leading to extra hole current from the back etc. This situation is represented in the schematic of Fig.8.

An important point is *latching*. This happens when the internal currents are such that we are not able to turn off the device using the control electrode. The only way to turn it off is by externally removing the current from the device.

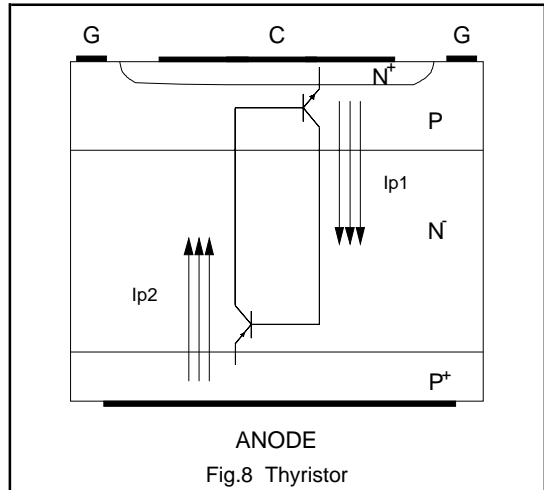
The switching behaviour of all these devices is affected by the behaviour of the PNP: as long as a current is flowing through the device, the back will inject holes into the N-layer. This leads to switching tails which contribute heavily to switching losses. The tail is strongly affected by the lifetime  $\tau$  and by the application of negative drive current

when possible. As previously explained, adjustment of the lifetime affects the on-state voltage. Carefully adjusting the lifetime  $\tau$  will balance the on-state losses with the switching losses.

All four layer devices show this trade-off between switching losses and on-state losses. When minimising switching losses, the devices are optimised for high frequency applications. When the on-state losses are lowest the current density is normally highest, but the device is only useful at low frequencies. So two variants of the four layer device generally exist. In some cases intermediate speeds are also useful as in the case of very high power GTOs.

## The Thyristor

A *thyristor* (or SCR, Silicon Controlled Rectifier) is essentially an HVT with an added  $P^+$ -layer. The resulting P-N- $P^+$  transistor is on when the whole device is on and provides enough base current to the  $N^+$ -P-N transistor to stay on. So after an initial kick-on, no further drive energy is required.

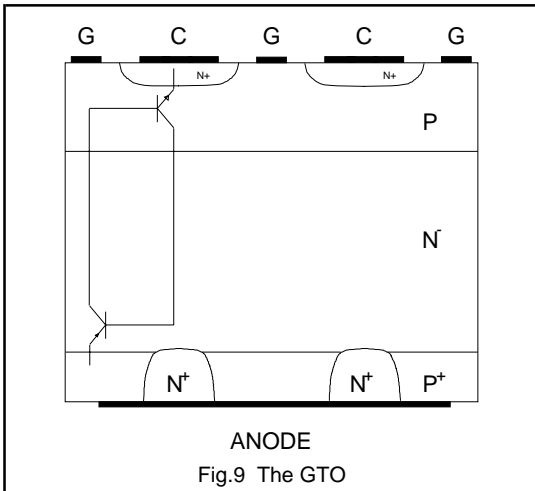


The classical thyristor is thus a latching device. Its construction is normally not very fine and as a result the gate contact is too far away from the centre of the active area to be able to switch it off. Also the current density is much higher than in a bipolar transistor. The switching times however are very long. Its turn-on is hampered by its structure since it takes quite a while for the whole crystal to become active. This seriously limits its  $di/dt$ .

Once a thyristor is on it will only turn-off after having zero current for a few microseconds. This is done by temporarily forcing the current via a so-called commutation circuit.

The charge in the device originates from two sources: The standard NPN transistor structure injects holes in the N-layer ( $I_{P1}$  in Fig.8) and the PNP transistor injects a charge from the back ( $I_{P2}$  in Fig.8). Therefore the total charge is big and switching performance is very poor. Due to its slow switching a normal thyristor is only suitable up to a few kHz.

A major variation on the thyristor is the *GTO* (Gate Turn Off Thyristor). This is a thyristor where the structure has been tailored to give better speed by techniques such as accurate lifetime killing, fine finger or cell structures and "anode shorts" (short circuiting  $P^+$  and  $N^-$  at the back in order to decrease the current gain of the PNP transistor). As a result, the product of the gain of both NPN and PNP is just sufficient to keep the GTO conductive. A negative gate current is enough to sink the hole current from the PNP and turn the device off.

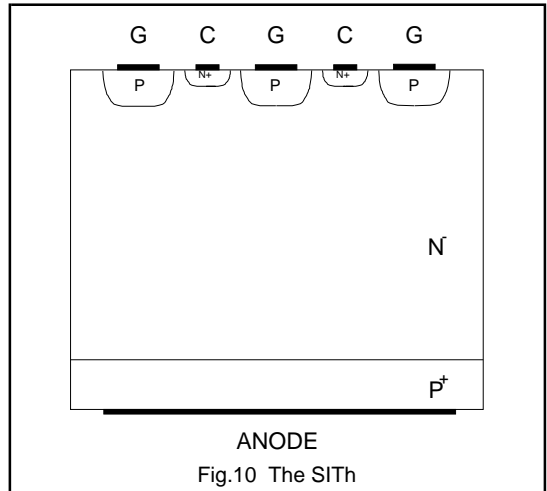


A GTO shows much improved switching behaviour but still has the tail as described above. Lower power applications, especially resonant systems, are particularly attractive for the GTO because the turn-off losses are virtually zero.

### The SITH

The *SITH* (Static Induction Thyristor) sometimes also referred to as *FCT* (Field Controlled Thyristor) is essentially a J-FET with an added  $P^+$  back layer. In contrast to the standard thyristor, charge is normally only injected from the back, so the total amount of charge is limited. However, a positive gate drive is possible which will reduce on-state resistance.

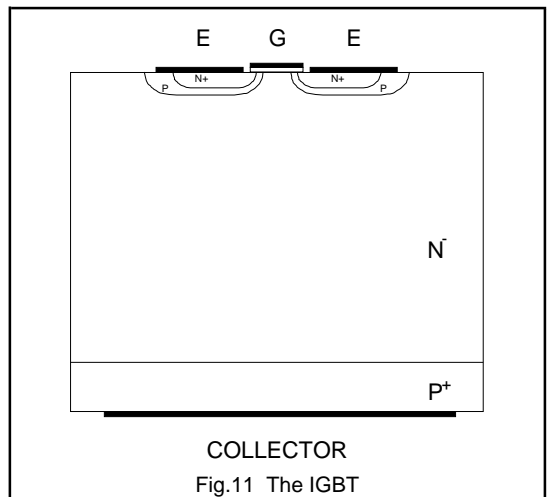
Active extraction of charge via the gate contact is possible and switching speeds may be reduced considerably by applying an appropriate negative drive as in the case of an HVT. As for the SIT the technological complexity is a severe



drawback, as is its negative drive requirements. Consequently mass production of this device is not available yet.

### The IGBT

An *IGBT* (Insulated Gate Bipolar Transistor) is an MOS transistor with  $P^+$  at the back. Charge is injected from the back only, which limits the total amount of charge. Active charge extraction is not possible, so the carrier lifetime  $\tau$  should be chosen carefully, since that determines the switching losses. Again two ranges are available with both fast and slow IGBTs.



The speed of the fast IGBT is somewhat better than that of a GTO because a similar technology is used to optimise the IGBT but only the back P<sup>+</sup>-layer is responsible for the charge.

The IGBT is gaining rapidly in popularity since its manufacturing is similar to producing PowerMOS and an increasing market availability exists. Although the latching of IGBTs was seen as a problem, modern optimised devices don't suffer from latch-up in practical conditions.

### Refinements to the basic structure

The refinements outlined for 3 layer devices also apply to 4 layer structures. In addition to these, an N<sup>+</sup>-layer may be inserted between the P<sup>+</sup> and N<sup>-</sup>-layer. Without such a layer the designer is limited in choice of starting material to Case 3 as explained in the diode section. Adding the extra N<sup>+</sup>-layer allows another combination of resistivity and thickness to be used, improving device performance. An example of this is the ASCR, the Asymmetric SCR, which is much faster than normal thyristors. The reverse blocking capability, however, is now reduced to a value of 10-20 V.

### Comparison of the Basic Devices.

It is important to consider the properties of devices mentioned when choosing the optimum switch for a particular application. Table 2 gives a survey of the essential device properties of devices capable of withstanding 1000 V. IGBTs have been classed in terms of fast and slow devices, however only the fast GTO and slow thyristor are represented. The fast devices are optimised for speed, the slow devices are optimised for On voltage.

#### Comments

This table is valid for 1000 V devices. Lower voltage devices will always perform better, higher voltage devices are worse.

A dot means an average value in between "+" and "-"

The "--" for a thyristor means a "--" in cases where forced commutation is used; in case of natural commutation it is "+"

Most figures are for reference only: in exceptional cases better performance has been achieved, but the figures quoted represent the state of the art.

	HVT	J-FET	MOS	THY	GTO	IGBT slow	IGBT fast	Unit
V(ON)	1	10	5	1.5	3	2	4	V
Positive Drive Requirement	-	+	+	+	+	+	+	+ = Simple to implement
Turn-Off requirement	-	-	+	(--)	-	+	+	+ = Simple to implement
Drive circuit complexity	-	.	+	(-)	.	+	+	- = complex
Technology Complexity	+	.	.	+	-	-	-	- = complex
Device Protection	-	.	+	+	-	-	-	+ = Simple to implement
Delay time (ts, tq)	2	0.1	0.1	5	1	2	0.5	µs
Switching Losses	.	++	++	--	-	-	.	+ = good
Current Density	50	12	20	200	100	50	50	A/cm <sup>2</sup>
Max dv/dt (Vin = 0)	3	20	10	0.5	1.5	3	10	V/ns
di/dt	1	10	10	1	0.3	10	10	A/ns
Vmax	1500	1000	1000	5000	4000	1000	1000	V
Imax	1000	10	100	5000	3000	400	400	A
Over Current factor	5	3	5	15	10	3	3	

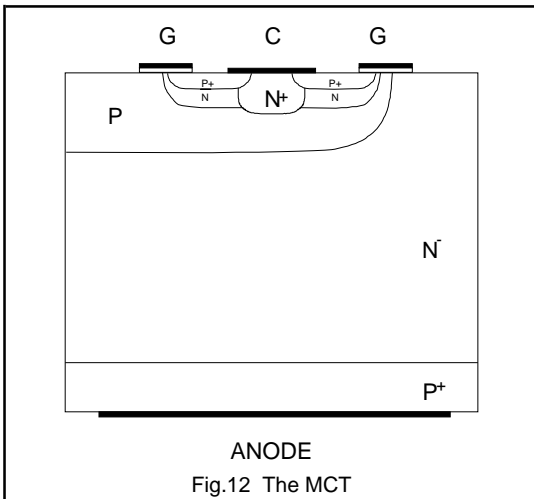
## Merged devices

Merged devices are the class of devices composed of two or more of the above mentioned basic types. They don't offer any breakthrough in device performance. This is understandable since the basic properties of the discussed devices are not or are hardly effected. They may be beneficial for the user though, primarily because they may result in lower positive and/or negative drive requirements.

## Darlington's and BiMOS

A darlington consists of two bipolar transistors. The emitter current of the first (the driver) forms the base current of the output transistor. The advantages of darlington's may be summarised as follows. A darlington has a higher gain than a single transistor. It also switches faster because the input transistor desaturates the output transistor and lower switching losses are the result. However, the resulting  $V_{CE(sat)}$  is higher. The main issue, especially for higher powers is the savings in drive energy. This means that darlington's can be used at considerably higher output powers than standard transistors. Modern darlington's in high power packages can be used in 20 kHz motor drives and power supplies.

A BiMOS consists of a MOS driver and a bipolar output transistor. The positive drive is the same as MOS but turn-off is generally not so good. Adding a "speed-up" diode coupled with some negative drive improves things.



## MCT

MCT stands for *MOS Controlled Thyristor*. This device is effectively a GTO with narrow tolerances, plus a P-MOS transistor between gate and source (P<sup>+</sup>-N-P MOS, the left hand gate in Fig.12) and an extra N-MOS to turn it on, the N-P-N-MOS shown underneath the right hand gate.

Where the GTO would like to be switched off with a negative gate, the internal GTO in an MCT can turn off by short circuiting its gate-cathode, due to its fine structure. Its drive therefore is like a MOS transistor and its behaviour similar to a GTO. Looking closely at the device it is obvious that a GTO using similar fine geometries with a suitable external drive can always perform better, at the cost of some drive circuitry. The only plus point seems to be its ease of drive.

## Application areas of the various devices

The following section gives an *indication* of where the various devices are best placed in terms of applications. It is possible for circuit designers to use various tricks to integrate devices and systems in innovative manners, applying devices far outside their 'normal' operating conditions. As an example, it is generally agreed that above 100 kHz bipolars are too difficult to use. However, a 450 kHz converter using bipolars has been already described in the literature.

As far as the maximum frequency is concerned a number of arguments must be taken into account.

First the *delay times*, either occurring at turn-on or at turn-off, will limit the maximum operating frequency. A reasonable rule of thumb for this is  $f_{MAX} = 3 / t_{DELAY}$ . (There is a danger here for confusion: switching times tend to depend heavily on circuit conditions, drive of the device and on current density. This may lead to a very optimistic or pessimistic expectation and care should be taken to consider reasonable conditions.)

Another factor is the *switching losses* which are proportional to the frequency. These power losses may be influenced by optimising the drive or by the addition of external circuits such as  $dV/dt$  or  $dI/dt$  networks. Alternatively the heatsink size may be increased or one may choose to operate devices at a lower current density in order to decrease power losses. It is clear that this argument is very subjective.

A third point is *manufacturability*. The use of fine structures for example, which improves switching performance, is possible only for small silicon chip sizes: larger chips with very fine MOS-like structures will suffer from unacceptable low factory yields. Therefore high power systems requiring large chip areas are bound to be made with less fine structures and will consequently be slower.

The *operating current density* of the device will influence its physical size. A low current density device aimed at high power systems would need a large outline which tends to be expensive. Large outlines also increase the physical size of the circuit, which leads to bigger parasitic inductances and associated problems.

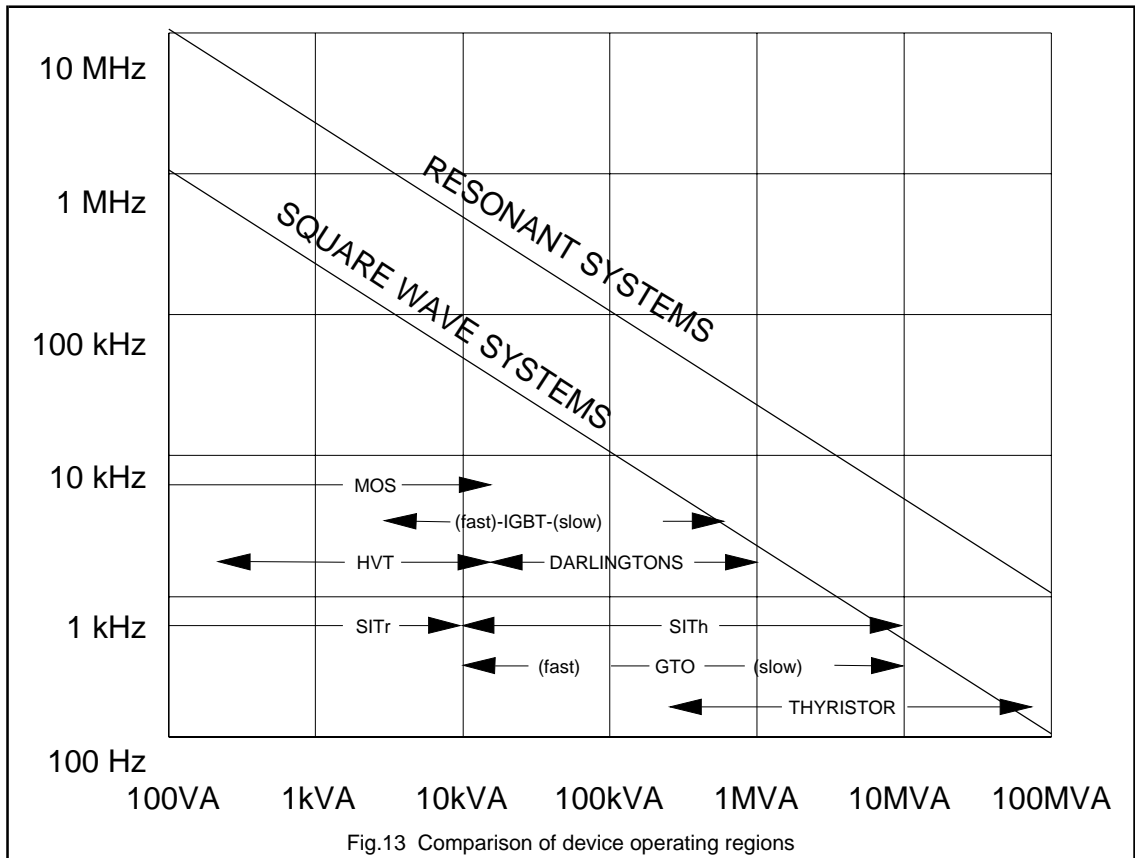


Fig.13 Comparison of device operating regions

*High power systems* will, because of the mechanical size, be restricted in speed as explained earlier in the text. This coincides well with the previously mentioned slower character of higher power devices.

Last but not least it is necessary to take the *application topology* into account. Resonant systems allow the use of considerably higher frequencies, since switching losses are minimised. Square wave systems cause more losses in the devices and thus restrict the maximum frequency. To make a comparison of devices and provide insight into which powers are realistic for which devices we have to take all the above mentioned criteria into account.

Figure 13 shows the optimum working areas of the various switching devices as a function of switchable power and frequency. The *switchable power* is defined as  $I_{AV}$  times  $V_{MAX}$  as seen by the device.

As an example, darlington's will work at powers up to 1 MVA i.e. 1000 V devices will switch 1000 A. The frequency is then limited to 2.5 kHz. At lower powers higher frequencies

can be achieved however above 50 kHz, darlington's are not expected to be used. One should use this table only as guidance; using special circuit techniques, darlington's have actually been used at higher frequencies. Clearly operation at lower powers and frequencies is always possible.

## Conclusions

The starting material for active devices aimed at high voltage switching are made on silicon of which the minimum resistivity and thickness are limited. This essentially determines device performance, since all active switches incorporate such a layer. Optimisation can be performed for either minimum thickness, as required in the case of HVTs, or for minimum resistance, as required for MOS and J-FETs. The thickest variation (lowest resistivity) is required in the case of some 4 layer devices.

Basically three ways exist to control current through the devices: feeding a base current into a P-layer (transistor),

using a voltage to pinch-off the current through openings in the P-layer (J-FET) and by applying a voltage onto a gate which inverts the underlying P-layer (MOS).

The HVT is severely limited in operating frequency due to its stored hole charge, but this at the same time allows a greater current density and a lower on-state voltage. It also requires more drive energy than both MOS and J-FET.

When we add a P<sup>+</sup>-layer at the back of the three basic three layer devices we make three basic four layer devices. The P<sup>+</sup>-layer produces a PNP transistor at the back which exhibits hole storage. This leads to much improved current densities and lower on-state losses, at the cost of switching speed. The four layer devices can be optimised for low on-state losses, in which case the switching will be poor, or for fast switching, in which case the on-state voltage will

be high.

The properties of all six derived basic devices are determined to a large extent by the design of the high resistive area and can be optimised by applying technological features in the devices such as lifetime killing and fine geometries.

Resonant systems allow devices to be used at much higher frequencies due to the lower switching losses and the minimum on-times which may be longer, compared to square wave switching systems. Figure 13 gives the expected maximum frequency and switching power for the discussed devices. The difference for square wave systems and resonant systems is about a factor of 10.





*Power MOSFET*



## 1.2.1 PowerMOS Introduction

### Device structure and fabrication

The idea of a vertical channel MOSFET has been known since the 1930s but it was not until the mid 1970s that the technology of diffusion, ion implantation and material treatment had reached the level necessary to produce DMOS on a commercial scale. The vertical diffusion technique uses technology more commonly associated with the manufacture of large scale integrated circuits than with traditional power devices. Figure 1(a) shows the vertical double implanted (DIMOS) channel structure which is the basis for all Philips power MOSFET devices.

An N-channel PowerMOS transistor is fabricated on an N<sup>+</sup> substrate with a drain metallization applied to its underside. Above the N<sup>+</sup> substrate is an N<sup>-</sup> epi layer, the thickness and resistivity of which depends on the required drain-source breakdown voltage. The channel structure, formed from a double implant in to the surface epi material, is laid down in a cellular pattern such that many thousands of cells go to make a single transistor. The N<sup>+</sup> polysilicon gate which is embedded in an isolating silicon dioxide layer, is a single structure which runs between the cells across the entire active region of the device. The source metallization also covers the entire structure and thus

parallels all the individual transistor cells on the chip. The layout of a typical low voltage chip is shown in Fig.1(b). The polysilicon gate is contacted by bonding to the defined pad area while the source wires are bonded directly to the aluminium over the cell array. The back of the chip is metallized with a triple layer of titanium/nickel/silver and this enables the drain connection to be formed using a standard alloy bond process.

The active part of the device consists of many cells connected in parallel to give a high current handling capability where the current flow is vertical through the chip. Cell density is determined by photolithographic tolerance requirements in defining windows in the polysilicon and gate-source oxide and also by the width of the polysilicon track between adjacent cells. The optimum value for polysilicon track width and hence cell density varies as a function of device drain-source voltage rating, this is explained in more detail further in the section. Typical cell densities are 1.6 million cells per square inch for low voltage types and 350,000 cells per square inch for high voltage types. The cell array is surrounded by an edge termination structure to control the surface electric field distribution in the device off-state.

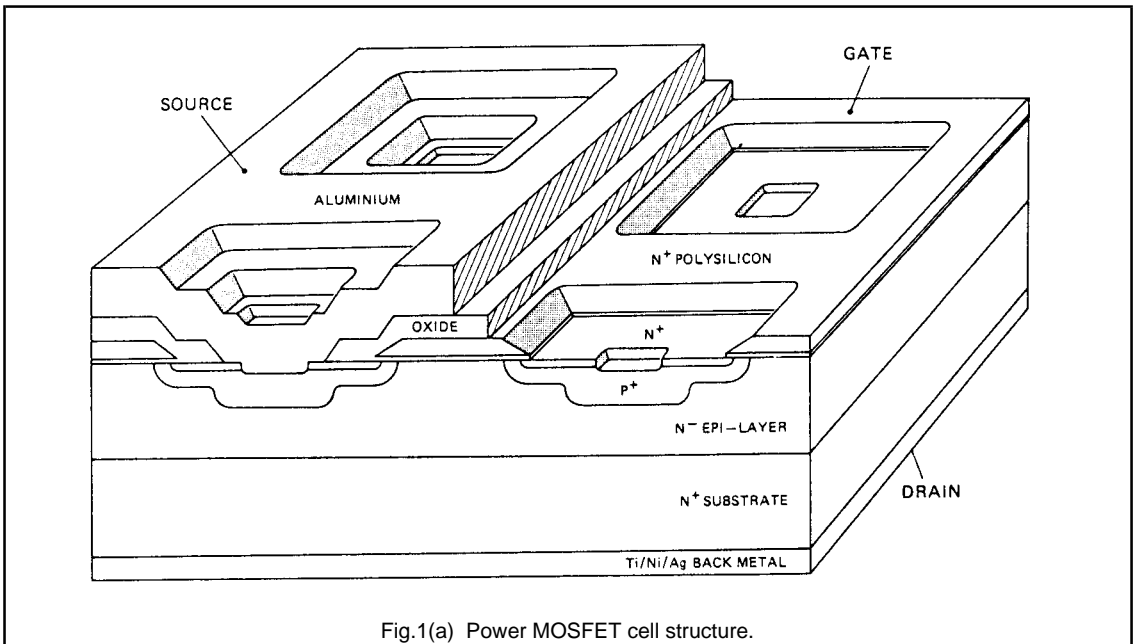


Fig.1(a) Power MOSFET cell structure.

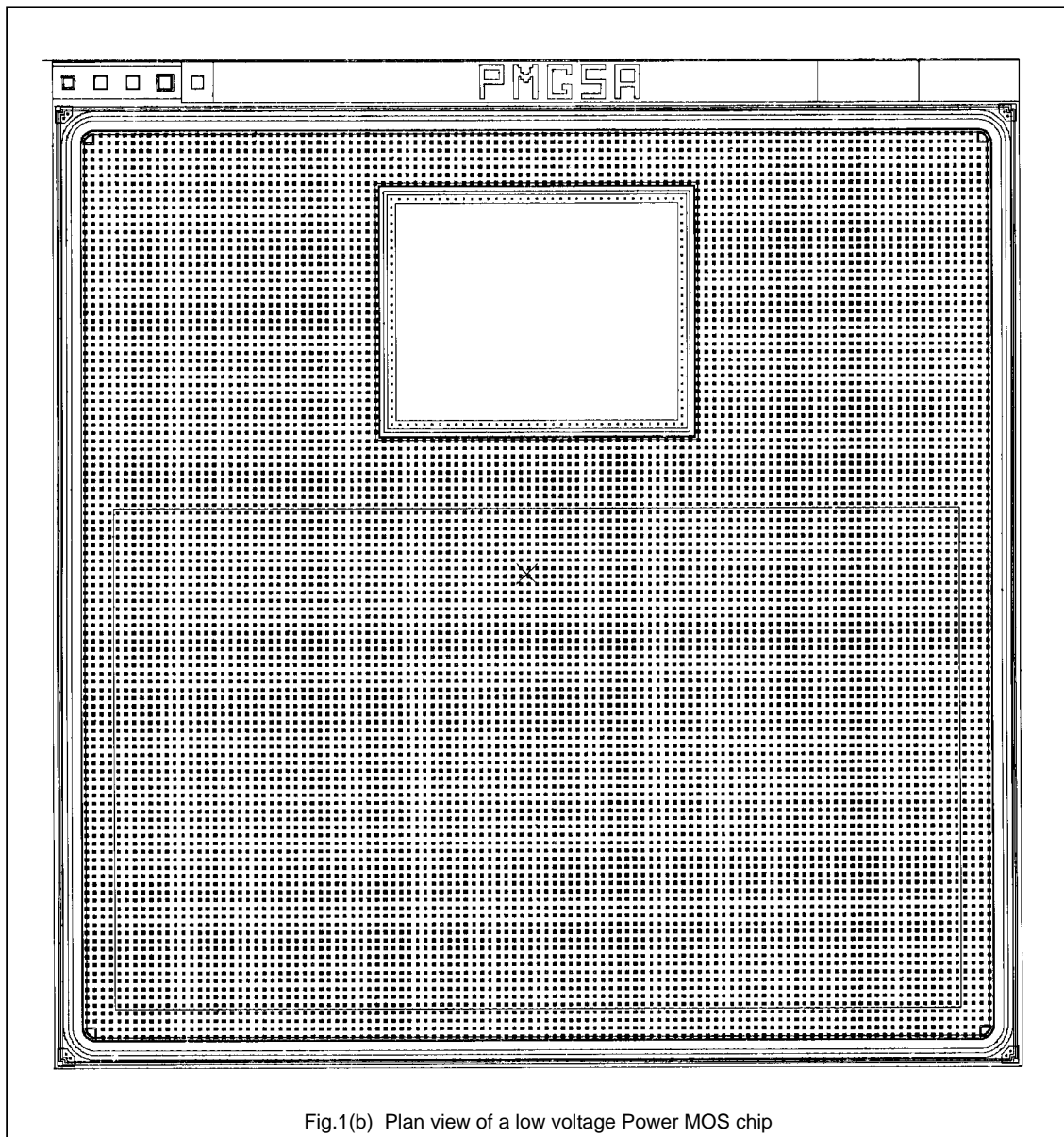
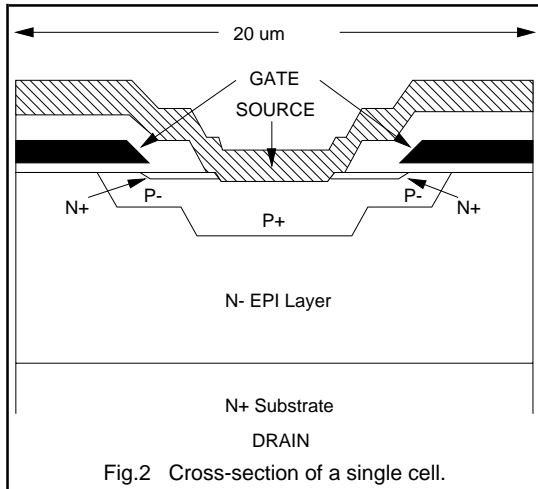


Fig.1(b) Plan view of a low voltage Power MOS chip

A cross-section through a single cell of the array is shown in Fig.2. The channel length is approximately 1.5 microns and is defined by the difference in the sideways diffusion of the N<sup>+</sup> source and the P-body. Both these diffusions are auto-aligned to the edge of the polysilicon gate during the fabrication process. All diffusions are formed by ion implantation followed by high temperature anneal/drive-in to give good parameter reproducibility. The gate is electrically isolated from the silicon by an 800 Angstrom layer of gate oxide (for standard types, 500 Angstrom for Logic level and from the overlying aluminium by a thick layer of phosphorus doped oxide. Windows are defined in the latter oxide layer to enable the aluminium layer to contact the N<sup>+</sup> source and the P<sup>+</sup> diffusion in the centre of each cell. The P<sup>+</sup> diffusion provides a low resistance connection between the P<sup>-</sup> body and ground potential, thus inhibiting turn-on of the inherent parasitic NPN bipolar structure.



## Device operation

Current flow in an enhancement mode power MOSFET is controlled by the voltage applied between the gate and source terminals. The P<sup>-</sup> body isolates the source and drain regions and forms two P-N junctions connected back-to-back. With both the gate and source at zero volts there is no source-drain current flow and the drain sits at the positive supply voltage. The only current which can flow from source to drain is the reverse leakage current.

As the gate voltage is gradually made more positive with respect to the source, holes are repelled and a depleted region of silicon is formed in the P<sup>-</sup> body below the silicon-gate oxide interface. The silicon is now in a 'depleted' state, but there is still no significant current flow between the source and drain.

When the gate voltage is further increased a very thin layer of electrons is formed at the interface between the P<sup>-</sup> body and the gate oxide. This conductive N-type channel enhanced by the positive gate-source voltage, now permits current to flow from drain to source. The silicon in the P<sup>-</sup> body is referred to as being in an 'inverted' state. A slight increase in gate voltage will result in a very significant increase in drain current and a corresponding rapid decrease in drain voltage, assuming a normal resistive load is present.

Eventually the drain current will be limited by the combined resistances of the load resistor and the  $R_{DS(ON)}$  of the MOSFET. The MOSFET resistance reaches a minimum when  $V_{GS} = +10$  volts (assuming a standard type). Subsequently reducing the gate voltage to zero volts reverses the above sequence of events. There are no stored charge effects since power MOSFETS are majority carrier devices.

## Power MOSFET parameters

### Threshold voltage

The threshold voltage is normally measured by connecting the gate to the drain and then determining the voltage which must be applied across the devices to achieve a drain current of 1.0 mA. This method is simple to implement and provides a ready indication of the point at which channel inversion occurs in the device.

The P<sup>-</sup> body is formed by the implantation of boron through the tapered edge of the polysilicon followed by an anneal and drive-in. The main factors controlling threshold voltage are gate oxide thickness and peak surface concentration in the channel, which is determined by the P-body implant dose. To allow for slight process variation a window is usually defined which is 2.1 to 4.0 volts for standard types and 1.0 to 2.0 volts for logic level types.

Positive charges in the gate oxide, for example due to sodium, can cause the threshold voltage to drift. To minimise this effect it is essential that the gate oxide is grown under ultra clean conditions. In addition the polysilicon gate and phosphorus doped oxide layer provide a good barrier to mobile ions such as sodium and thus help to ensure good threshold voltage stability.

### Drain-source on-state resistance

The overall drain-source resistance,  $R_{DS(ON)}$ , of a power MOSFET is composed of several elements, as shown in Fig.3.

The relative contribution from each of the elements varies with the drain-source voltage rating. For low voltage devices the channel resistance is very important while for

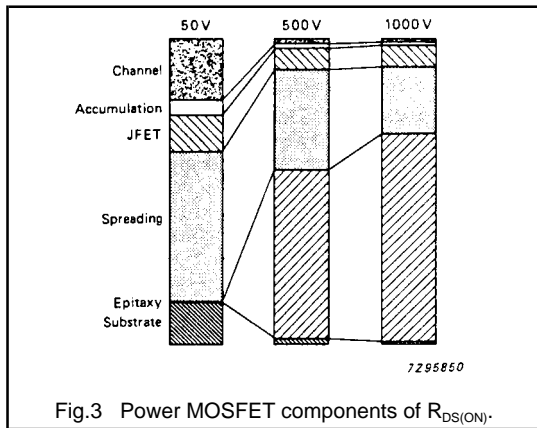


Fig.3 Power MOSFET components of  $R_{DS(ON)}$ .

the high voltage devices the resistivity and thickness of the epitaxial layer dominates. The properties of the various resistive components will now be discussed:

**Channel.** The unit channel resistance is determined by the channel length, gate oxide thickness, carrier mobility, threshold voltage, and the actual gate voltage applied to the device. The channel resistance for a given gate voltage can be significantly reduced by lowering the thickness of the gate oxide. This approach is used to fabricate the Logic Level MOSFET transistors and enables a similar value  $R_{DS(ON)}$  to be achieved with only 5 volts applied to the gate. Of course, the gate-source voltage rating must be reduced to allow for the lower dielectric breakdown of the thinner oxide layer.

The overall channel resistance of a device is inversely proportional to channel width, determined by the total periphery of the cell windows. Channel width is over 200  $\mu\text{m}$  for a 20  $\text{mm}^2$  low voltage chip. The overall channel resistance can be significantly reduced by going to higher cell densities, since the cell periphery per unit area is reduced.

**Accumulation layer.** The silicon interface under the centre of the gate track is 'accumulated' when the gate is biased above the threshold voltage. This provides a low resistance path for the electrons when they leave the channel, prior to entering the bulk silicon. This effect makes a significant contribution towards reducing the overall  $R_{DS(ON)}$ .

**Parasitic JFET.** After leaving the accumulation layer the electrons flow vertically down between the cells into the bulk of the silicon. Associated with each P-N junction there is a depletion region which, in the case of the high voltage devices, extends several microns into the N epitaxial region, even under zero bias conditions. Consequently the current path for the electrons is restricted by this parasitic JFET structure. The resistance of the JFET structure can be reduced by increasing the polysilicon track width. However this reduces the cell density. The need for compromise

leads to an optimum value for the polysilicon track width for a given drain-source voltage rating. Since the zero-bias depletion width is greater for low doped material, then a wider polysilicon track width is used for high voltage chip designs.

**Spreading resistance.** As the electrons move further into the bulk of the silicon they are able to spread sideways and flow under the cells. Eventually paths overlap under the centre of each cell.

**Epitaxial layer.** The drain-source voltage rating requirements determine the resistivity and thickness of the epitaxial layer. For high voltage devices the resistance of the epitaxial layer dominates the overall value of  $R_{DS(ON)}$ .

**Substrate.** The resistance of the  $N^+$  substrate is only significant in the case of 50 V devices.

**Wires and leads.** In a completed device the wire and lead resistances contribute a few milli-ohms to the overall resistance.

For all the above components the actual level of resistance is a function of the mobility of the current carrier. Since the mobility of holes is much lower than that of electrons the resistance of P-Channel MOSFETs is significantly higher than that of N-Channel devices. For this reason P-Channel types tend to be unattractive for most applications.

## Drain-source breakdown voltage

The voltage blocking junction in the PowerMOS transistor is formed between the P-body diffusion and the  $N^+$  epi layer. For any P-N junction there exists a maximum theoretical breakdown voltage, which is dependent on doping profiles and material thickness. For the case of the N-channel PowerMOS transistor nearly all the blocking voltage is supported by the  $N^+$  epi layer. The ability of the  $N^+$  epi layer to support voltage is a function of its resistivity and thickness where both must increase to accommodate a higher breakdown voltage. This has obvious consequences in terms of drain-source resistance with  $R_{DS(ON)}$  being approximately proportional to  $B_{VDSS}^{2.5}$ . It is therefore important to design PowerMOS devices such that the breakdown voltage is as close as possible to the theoretical maximum otherwise thicker, higher resistivity material has to be used. Computer models are used to investigate the influence of cell design and layout on breakdown voltage. Since these factors also influence the 'on-state' and switching performances a degree of compromise is necessary.

To achieve a high percentage of the theoretical breakdown maximum it is necessary to build edge structures around the active area of the device. These are designed to reduce the electric fields which would otherwise be higher in these regions and cause premature breakdown.

For low voltage devices this structure consists of a field plate design, Fig.4. The plates reduce the electric field intensity at the corner of the P<sup>+</sup> guard ring which surrounds the active cell area, and spread the field laterally along the surface of the device. The polysilicon gate is extended to form the first field plate, whilst the aluminium source metallization forms the second plate. The polysilicon termination plate which is shorted to the drain in the corners of the chip (not shown on the diagram) operates as a channel stopper. This prevents any accumulation of positive charge at the surface of the epi layer and thus improves stability. Aluminium overlaps the termination plate and provides a complete electrostatic screen against any external ionic charges, hence ensuring good stability of blocking performance.

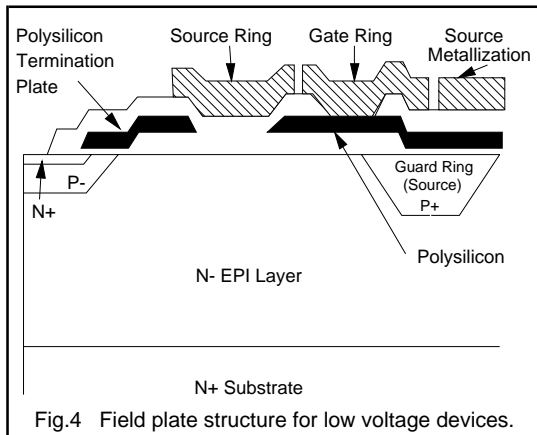


Fig.4 Field plate structure for low voltage devices.

For high voltage devices a set of floating P<sup>+</sup> rings, see Fig.5, is used to control the electric field distribution around the device periphery. The number of rings in the structure depends on the voltage rating of the device, eight rings are used for a 1000 volt type such as the BUK456-1000A. A three dimensional computer model enables the optimum ring spacing to be determined so that each ring experiences a similar field intensity as the structure approaches avalanche breakdown. The rings are passivated with polydox which acts as an electrostatic screen and prevents external ionic charges inverting the lightly doped N<sup>-</sup> interface to form P<sup>-</sup> channels between the rings. The polydox is coated with layers of silicon nitride and phosphorus doped oxide.

All types have a final passivation layer of plasma nitride, which acts as a further barrier to mobile charge and also gives anti-scratch protection to the top surface.

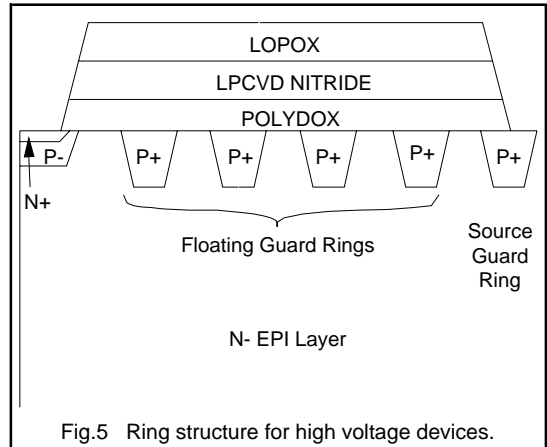


Fig.5 Ring structure for high voltage devices.

## Electrical characteristics

### The DC characteristic

If a dc voltage source is connected across the drain and source terminals of an N channel enhancement mode MOSFET, with the positive terminal connected to the drain, the following characteristics can be observed. With the gate to source voltage held below the threshold level negligible current will flow when sweeping the drain source voltage positive from zero. If the gate to source voltage is taken above the threshold level, increasing the drain to source voltage will cause current to flow in the drain. This current will increase as the drain-source voltage is increased up to a point known as the pinch off voltage. Increasing the drain-source terminal voltage above this value will not produce any significant increase in drain current.

The pinch off voltage arises from a rapid increase in resistance which for any particular MOSFET will depend on the combination of gate voltage and drain current. In its simplest form, pinch off will occur when the ohmic drop across the channel region directly beneath the gate becomes comparable to the gate to source voltage. Any further increase in drain current would now reduce the net voltage across the gate oxide to a level which is no longer sufficient to induce a channel. The channel is thus pinched off at its edge furthest from the source N<sup>+</sup> (see Fig.6).

A typical set of output characteristics is shown in Fig.7. The two regions of operation either side of the pinch off voltage can be seen clearly. The region at voltages lower than the pinch off value is usually known as the ohmic region. Saturation region is the term used to describe that part of the characteristic above the pinch-off voltage. (NB This definition of saturation is different to that used for bipolar devices.)

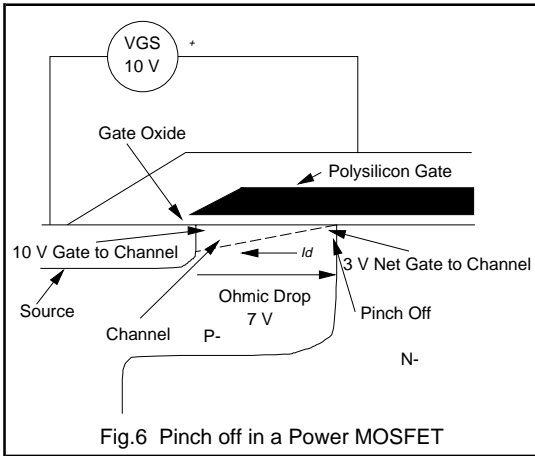


Fig.6 Pinch off in a Power MOSFET

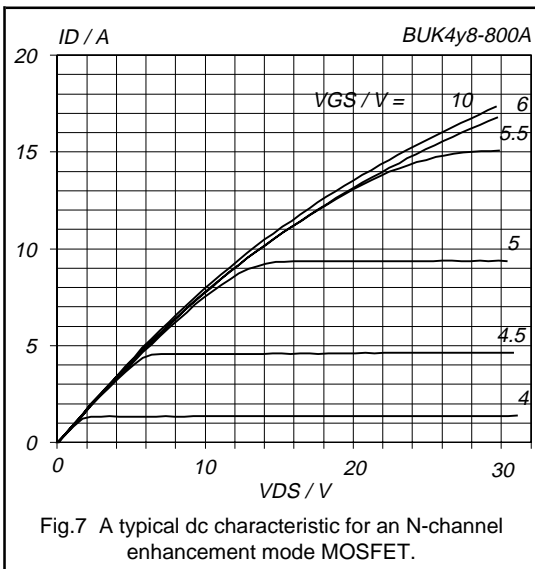


Fig.7 A typical dc characteristic for an N-channel enhancement mode MOSFET.

### The switching characteristics

The switching characteristics of a Power MOSFET are determined largely by the various capacitances inherent in its' structure. These are shown in Fig.8.

To turn the device on and off the capacitances have to be charged and discharged, the rate at which this can be achieved is dependent on the impedance and the current sinking/sourcing capability of the drive circuit. Since it is only the majority carriers that are involved in the conduction process, MOSFETs do not suffer from the same storage time problems which limit bipolar devices where minority carriers have to be removed during turn-off. For most applications therefore the switching times of the Power

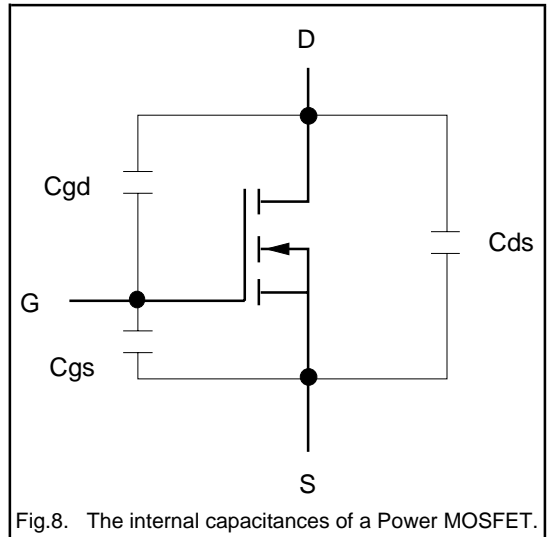
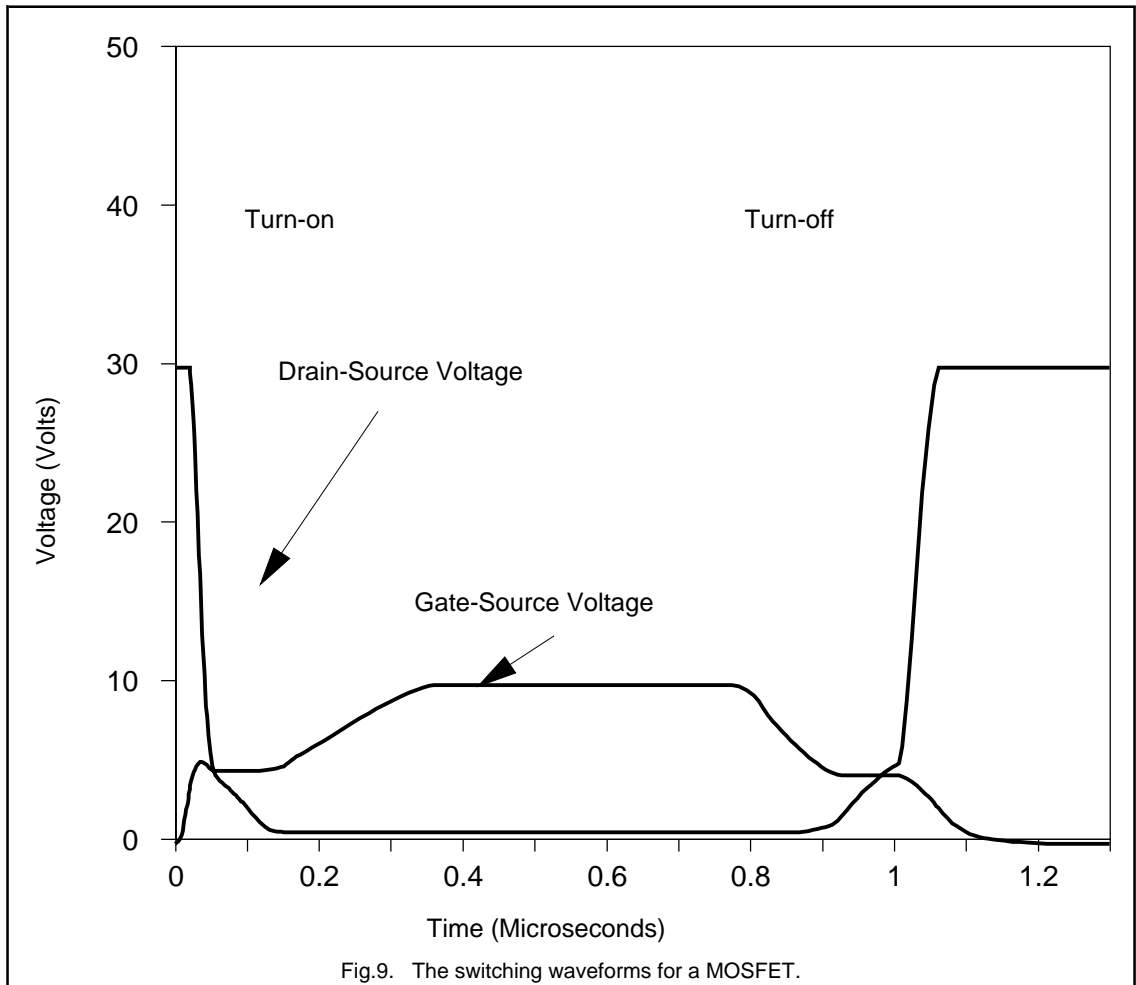


Fig.8. The internal capacitances of a Power MOSFET.

MOSFET are limited only by the drive circuit and can be very fast. Temperature has only a small effect on device capacitances therefore switching times are independent of temperature.

In Fig.9 typical gate-source and drain-source voltages for a MOSFET switching current through a resistive load are shown. The gate source capacitance needs to be charged up to a threshold voltage of about 3 V before the MOSFET begins to turn on. The time constant for this is  $C_{GS}(R_{DR}+R_G)$  and the time taken is called the turn-on delay time ( $t_{D(ON)}$ ). As  $V_{GS}$  starts to exceed the threshold voltage the MOSFET begins to turn on and  $V_{DS}$  begins to fall.  $C_{GD}$  now needs to be discharged as well as  $C_{GS}$  being charged so the time constant is increased and the gradient of  $V_{GS}$  is reduced. As  $V_{DS}$  becomes less than  $V_{GS}$  the value of  $C_{GD}$  increases sharply since it is depletion dependent. A plateau thus occurs in the  $V_{GS}$  characteristic as the drive current goes into the charging of  $C_{GD}$ .





When  $V_{DS}$  has collapsed  $V_{GS}$  continues to rise as overdrive is applied. Gate overdrive is necessary to reduce the on-resistance of the MOSFET and thereby keep power loss to a minimum.

To turn the MOSFET off the overdrive has first to be removed. The charging path for  $C_{GD}$  and  $C_{DS}$  now contains the load resistor ( $R_L$ ) and so the turn-off time will be generally longer than the turn-on time.

### The Safe Operating Area

Unlike bipolar devices Power MOSFETs do not suffer from second breakdown phenomena when operated within their voltage rating. Essentially therefore the safe operating area of a Power MOSFET is determined only by the power

necessary to raise its junction temperature to the rated maximum of 150 °C or 175 °C (which  $T_{JMAX}$  depends on package and voltage rating). Whether a MOSFET is being operated safely with respect to thermal stress can thus be determined directly from knowledge of the power function applied and the thermal impedance characteristics.

A safe operating area calculated assuming a mounting base temperature of 25 °C is shown in Fig.10 for a BUK438-800 device. This plot shows the constant power curves for a variety of pulse durations ranging from dc to 10 μs. These curves represent the power levels which will raise  $T_j$  up to the maximum rating. Clearly for mounting base temperatures higher than 25 °C the safe operating area is smaller. In addition it is not usually desirable to operate the

device at its  $T_{jMAX}$  rating. These factors can be taken into account quite simply where maximum power capability for a particular application is calculated from:

$$P_{max} = \frac{(T_j - T_{mb})}{Z_{th}}$$

$T_j$  is the desired operating junction temperature (must be less than  $T_{jmax}$ )

$T_{mb}$  is the mounting base temperature

$Z_{th}$  is the thermal impedance taken from the data curves

The safe operating area is bounded by a peak pulse current limit and a maximum voltage. The peak pulse current is based on a current above which internal connections may be damaged. The maximum voltage is an upper limit above which the device may go into avalanche breakdown.

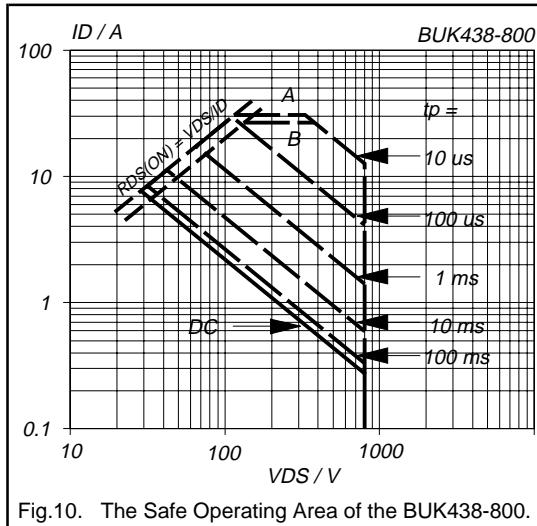


Fig.10. The Safe Operating Area of the BUK438-800.

In a real application the case temperature will be greater than 25 °C because of the finite thermal impedance of practical heatsinks. Also a junction temperature of between 80 °C and 125 °C would be preferable since this improves reliability. If a nominal junction temperature of 80 °C instead of 150 °C is used then the ability of the MOSFET to withstand current spikes is improved.

## Causes of Power Loss

There are four main causes of power dissipation in MOSFETs.

**Conduction losses** - The conduction losses ( $P_C$ ) are given by equation (1).

$$P_C = I_D^2 \cdot R_{DS(ON)} \quad (1)$$

It is important to note that the on-resistance of the MOSFET when it is operated in the Ohmic region is dependent on the junction temperature. On-resistance roughly doubles between 25 °C and 150 °C, the exact characteristics are shown in the data sheets for each device.

**Switching losses** - When a MOSFET is turned on or off it carries a large current and sustains a large voltage at the same time. There is therefore a large power dissipation during the switching interval. Switching losses are negligible at low frequencies but are dominant at high frequencies. The cross-over frequency depends on the circuit configuration. For reasons explained in the section on switching characteristics, a MOSFET usually turns off more slowly than it turns on so the losses at turn-off will be larger than at turn-on. Switching losses are very dependent on circuit configuration since the turn-off time is affected by the load impedance.

Turn-off losses may be reduced by the use of snubber components connected across the MOSFET which limit the rate of rise of voltage. Inductors can be connected in series with the MOSFET to limit the rate of rise of current at turn-on and reduce turn-on losses. With resonant loads switching can take place at zero crossing of voltage or current so switching losses are very much reduced.

**Diode losses** - These losses only occur in circuits which make use of the antiparallel diode inherent in the MOSFET structure. A good approximation to the dissipation in the diode is the product of the diode voltage drop which is typically less than 1.5 V and the average current carried by the diode. Diode conduction can be useful in such circuits as pulse width modulated circuits used for motor control, in some stepper motor drive circuits and in voltage fed circuits feeding a series resonant load.

**Gate losses** - The losses in the gate are given in equation 2 where  $R_G$  is the internal gate resistance,  $R_{DR}$  is the external drive resistance,  $V_{GSD}$  is the gate drive voltage and  $C_{IP}$  is the capacitance seen at the input to the gate of the MOSFET.

$$P_G = \frac{C_{IP} \cdot V_{GSD}^2 \cdot f \cdot R_G}{(R_G + R_{DR})} \quad (2)$$

The input capacitance varies greatly with the gate drain voltage so the expression in equation 3 is more useful.

$$P_G = \frac{Q_G \cdot V_{GSD} \cdot f \cdot R_G}{(R_G + R_{DR})} \quad (3)$$

(3)

Where  $Q_G$  is the peak gate charge.

## Parallel Operation

If power requirements exceed those of available devices then increased power levels can be achieved by paralleling devices. Paralleling of devices is made easier using

MOSFETs because they have a positive temperature coefficient of resistance. If one paralleled MOSFET carries more current than the others it becomes hotter. This causes the on-resistance of that particular device to become greater than that of the others and so the current in it reduces. This mechanism opposes thermal runaway in one of the devices. The positive temperature coefficient also helps to prevent hot spots within the MOSFET itself.

### **Applications of Power MOSFETs**

Power MOSFETs are ideally suited for use in many applications, some of which are listed below. Further information on the major applications is presented in

subsequent chapters.

Chapter 2: Switched mode power supplies (SMPS)

Chapter 3: Variable speed motor control.

Chapter 5: Automotive switching applications.

### **Conclusions**

It can be seen that the operation of the Power MOSFET is relatively easy to understand. The advantages of fast switching times, ease of parallelling and low drive power requirements make the device attractive for use in many applications.



## 1.2.2 Understanding Power MOSFET Switching Behaviour

Power MOSFETs are well known for their ease of drive and fast switching behaviour. Being majority carrier devices means they are free of the charge storage effects which inhibit the switching performance of bipolar products. How fast a Power MOSFET will switch is determined by the speed at which its internal capacitances can be charged and discharged by the drive circuit. MOSFET switching times are often quoted as part of the device data however as an indication as to the true switching capability of the device, these figures are largely irrelevant. The quoted values are only a snapshot showing what will be achieved under the stated conditions.

This report sets out to explain the switching characteristics of Power MOSFETs. It will consider the main features of the switching cycle distinguishing between what is device determinant and what can be controlled by the drive circuit. The requirements for the drive circuit are discussed in terms of the energy that it must supply as well as the currents it is required to deliver. Finally, how the drive circuit influences switching performance, in terms of switching times,  $dV/dt$  and  $dI/dt$  will be reviewed.

### Voltage dependent capacitance

The switching characteristics of the Power MOSFET are determined by its capacitances. These capacitances are not fixed but are a function of the relative voltages between each of the terminals. To fully appreciate Power MOSFET switching, it is necessary to understand what gives rise to this voltage dependency.

Parallel plate capacitance is expressed by the well known equation

$$C = E \frac{a}{d} \quad 1$$

where 'a' is the area of the plates, d is the separating distance and E is the permittivity of the insulating material between them. For a parallel plate capacitor, the plates are surfaces on which charge accumulation / depletion occurs in response to a change in the voltage applied across them. In a semiconductor, static charge accumulation / depletion can occur either across a PN junction or at semiconductor interfaces either side of a separating oxide layer.

#### i) P-N junction capacitance

The voltage supporting capability of most power semiconductors is provided by a reverse biased P-N junction. The voltage is supported either side of the junction by a region of charge which is exposed by the applied voltage. (Usually referred to as the depletion region because it is depleted of majority carriers.) Fig.1 shows how the electric field varies across a typical P-N junction

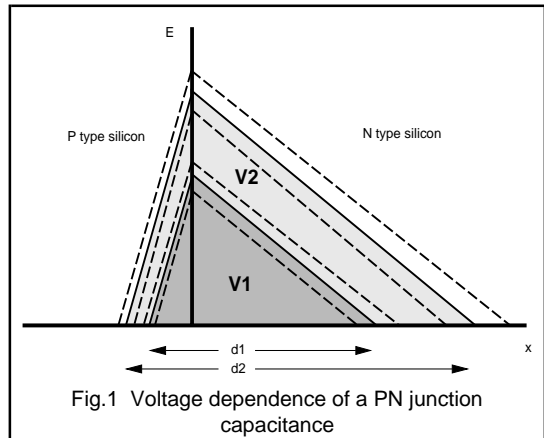
for a fixed dc voltage. The shaded area beneath the curve must be equal to the applied voltage. The electric field gradient is fixed, independent of the applied voltage, according to the concentration of exposed charge. (This is equal to the background doping concentration used during device manufacture.) A slight increase in voltage above this dc level will require an extension of the depletion region, and hence more charge to be exposed at its edges, this is illustrated in Fig.1. Conversely a slight reduction in voltage will cause the depletion region to contract with a removal of exposed charge at its edge. Superimposing a small ac signal on the dc voltage thus causes charge to be added and subtracted at either side of the depletion region of width  $d1$ . The effective capacitance per unit area is

$$C1 = \frac{E}{d1} \quad 2$$

Since the depletion region width is voltage dependent it can be seen from Fig.1 that if the dc bias is raised to say  $V2$ , the junction capacitance becomes

$$C2 = \frac{E}{d2} \quad 3$$

Junction capacitance is thus dependent on applied voltage with an inverse relationship.



#### ii) Oxide capacitance

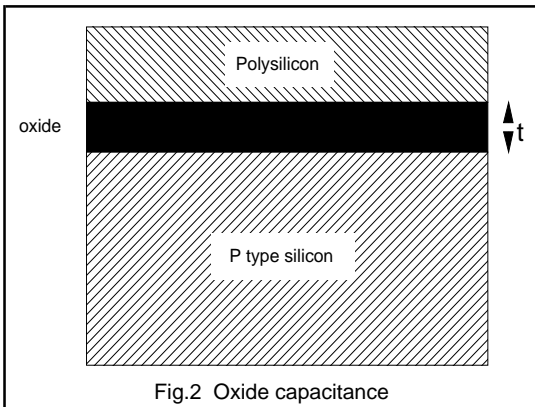
Fig.2 shows two semiconductor layers separated by an insulating oxide. In this case the surface layer is polysilicon (representative of the PowerMOS gate structure) and the lower layer is a P-type substrate. Applying a negative voltage to the upper layer with respect to the lower will cause positive charge accumulation at the surface of the P-doped

material (positively charged holes of the P material are attracted by the negative voltage). Any changes in this applied voltage will cause a corresponding change in the accumulation layer charge. The capacitance per unit area is thus

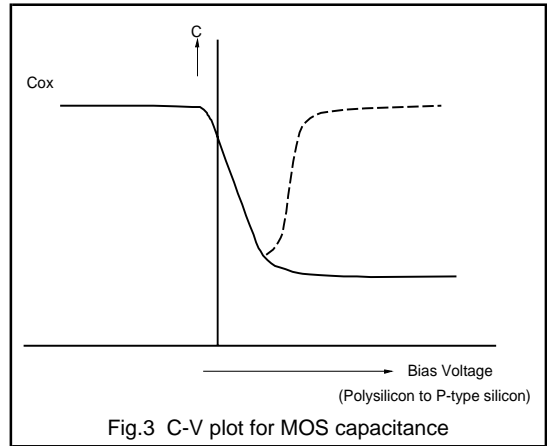
$$C_{ox} = \frac{\epsilon}{t} \quad 4$$

where t = oxide thickness

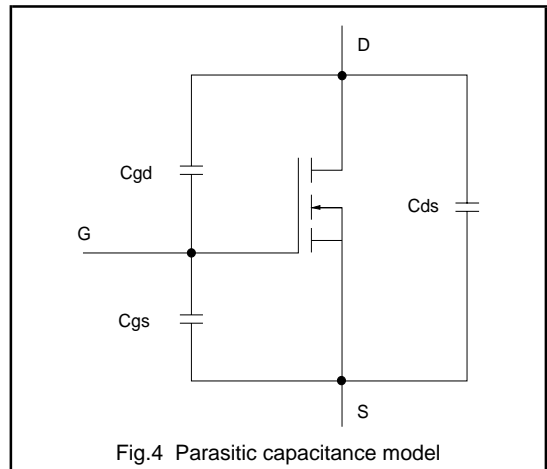
Applying a positive voltage to the gate will cause a depletion layer to form beneath the oxide, (ie the positively charged holes of the P-material are repelled by the positive voltage). The capacitance will now decrease with increasing positive gate voltage as a result of widening of the depletion layer. Increasing the voltage beyond a certain point results in a process known as inversion; electrons pulled into the conduction band by the electric field accumulate at the surface of the P-type semiconductor. (The voltage at which this occurs is the threshold voltage of the power MOSFET.) Once the inversion layer forms, the depletion layer width will not increase with additional dc bias and the capacitance is thus at its minimum value. (NB the electron charge accumulation at the inversion layer cannot follow a high frequency ac signal in the structure of Fig.2, so high frequency capacitance is still determined by the depletion layer width.) The solid line of Fig.3 represents the capacitance-voltage characteristic of an MOS capacitor.



In a power MOSFET the solid line is not actually observed; the formation of the inversion layer in the P-type material allows electrons to move from the neighbouring N<sup>+</sup>-source, the inversion layer can therefore respond to a high frequency gate signal and the capacitance returns to its maximum value, dashed line of Fig.3.



### Power MOSFET capacitances



The circuit model of Fig.4 illustrates the parasitic capacitances of the Power MOSFET. Most PowerMOS data sheets do not refer to these components but to input capacitance C<sub>iss</sub>, output capacitance C<sub>oss</sub> and feedback capacitance C<sub>rss</sub>. The data sheet capacitances relate to the primary parasitic capacitances of Fig.4 as follows:

- C<sub>iss</sub>: Parallel combination of C<sub>gs</sub> and C<sub>gd</sub>
- C<sub>oss</sub>: Parallel combination of C<sub>ds</sub> and C<sub>gd</sub>
- C<sub>rss</sub>: Equivalent to C<sub>gd</sub>

Fig.5 shows the cross section of a power MOSFET cell indicating where the parasitic capacitances occur internally.

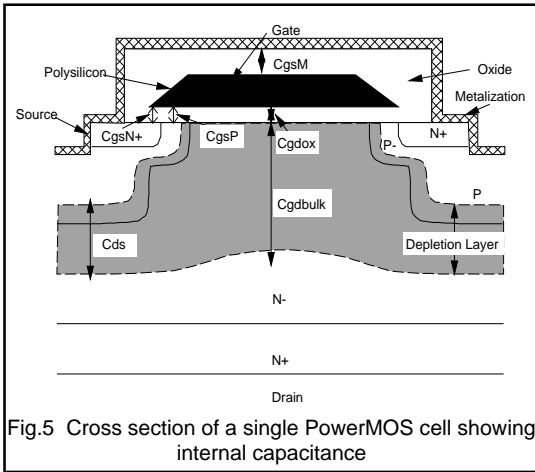


Fig.5 Cross section of a single PowerMOS cell showing internal capacitance

The capacitance between drain and source is a P-N junction capacitance, varying in accordance with the width of the depletion layer, which in turn depends on the voltage being supported by the device. The gate source capacitance consists of the three components, CgsN+, CgsP and CgsM. Of these CgsP is across the oxide which will vary according to the applied gate source voltage as described above.

Of particular interest is the feedback capacitance Cgd. It is this capacitance which plays a dominant role during switching and which is also the most voltage dependent. Cgd is essentially two capacitors in series such that

$$\frac{1}{C_{gd}} = \frac{1}{C_{gdox}} + \frac{1}{C_{gdbulk}}$$

5

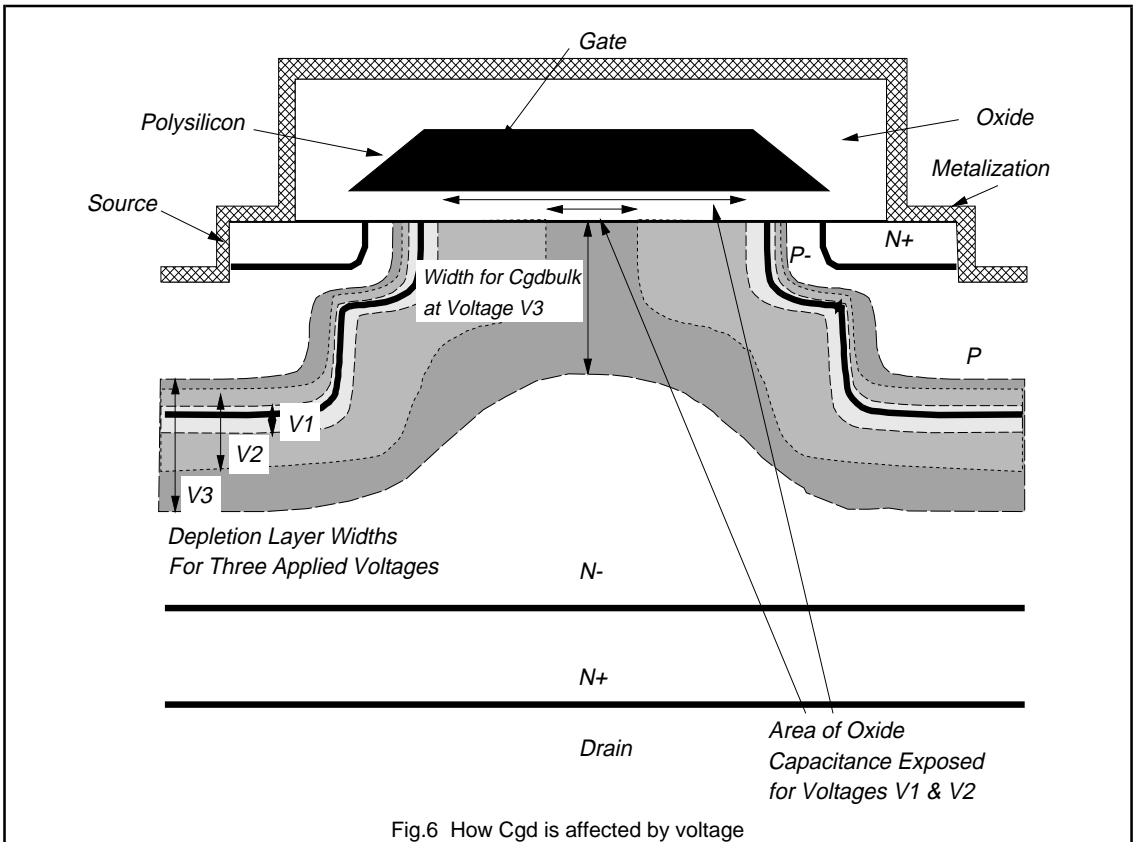


Fig.6 How Cgd is affected by voltage

Fig.6 illustrates how this capacitance is affected by the drain to gate voltage. With a large voltage drain to gate,  $C_{gd_{bulk}}$  is very small due to the wide depletion region and thus maintains  $C_{gd}$  at a low value. As the voltage is reduced the depletion region shrinks until eventually the oxide semiconductor interface is exposed. This occurs as  $V_{dg}$  approaches 0 V.  $C_{gd_{ox}}$  now dominates  $C_{gd}$ . As  $V_{dg}$  is further reduced the drain will become negative with respect to the gate (normal on-state condition) an increasing area of the oxide-semiconductor interface is exposed and an accumulation layer forms at the semiconductor surface. The now large area of exposed oxide results in a large value for  $C_{gd_{ox}}$  and hence  $C_{gd}$ . Fig.7 shows  $C_{gd}$  plotted as a function of drain to gate voltage. This illustrates the almost step increase in capacitance at the point where  $V_{gs} = V_{gd}$ .

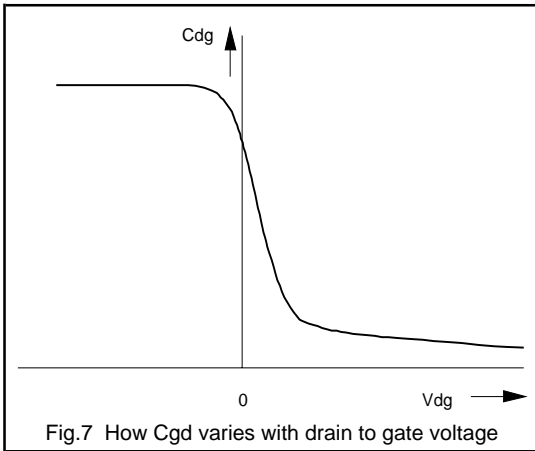


Fig.7 How  $C_{gd}$  varies with drain to gate voltage

### Charging cycle - The Gate Charge Oscillogram

The switching cycle of a power MOSFET can be clearly observed by applying a constant current to the gate and using a constant current source as the load, Fig.8. In this circuit the MOSFET is turned on by feeding a constant current of 1 mA on to the gate, conversely the device is turned off by extracting a constant current of 1 mA from the gate. The gate and drain voltages with respect to source can be monitored on an oscilloscope as a function of time. Since  $Q = it$ , a 1  $\mu$ sec period equates to 1 nC of charge applied to the gate. The gate source voltage can thus be plotted as a function of charge on the gate. Fig.9 shows such a plot for the turn-on of a BUK555-100A, also shown is the drain to source voltage. This gate voltage plot shows the characteristic shape which results from charging of the power MOSFET's input capacitance. This shape arises as follows: (NB the following analysis uses the two circuit models of Fig.10 to represent a MOSFET operating in the active region (a) and the ohmic region (b). In the active

region the MOSFET is a constant current source where the current is a function of the gate-source voltage. In the ohmic region the MOSFET is in effect just a resistance.)

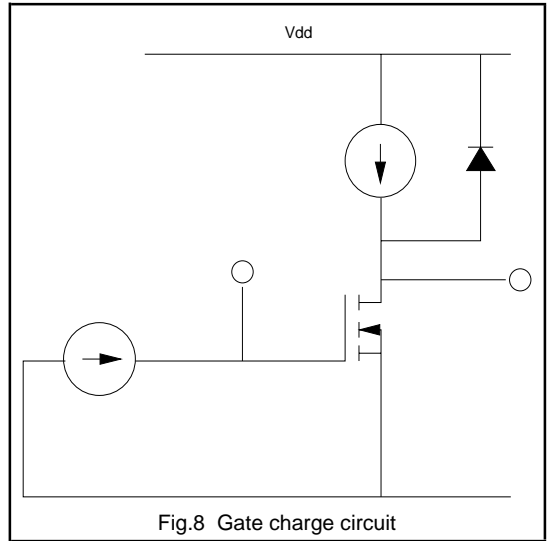


Fig.8 Gate charge circuit

At time,  $t_0$  (Fig.9), the gate drive is activated. Current flows into the gate as indicated in Fig.11(a), charging both  $C_{gs}$  and  $C_{gd}$ . After a short period the threshold voltage is reached and current begins to rise in the MOSFET. The equivalent circuit is now as shown in Fig.11(b). The drain source voltage remains at the supply level as long as  $i_d < I_0$  and the free wheeling diode D is conducting.

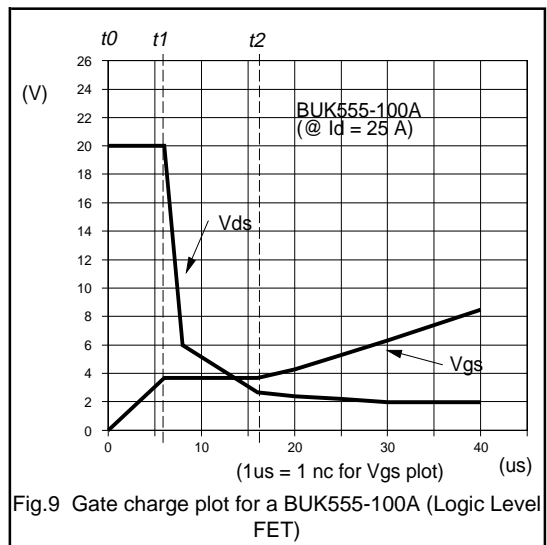


Fig.9 Gate charge plot for a BUK555-100A (Logic Level FET)

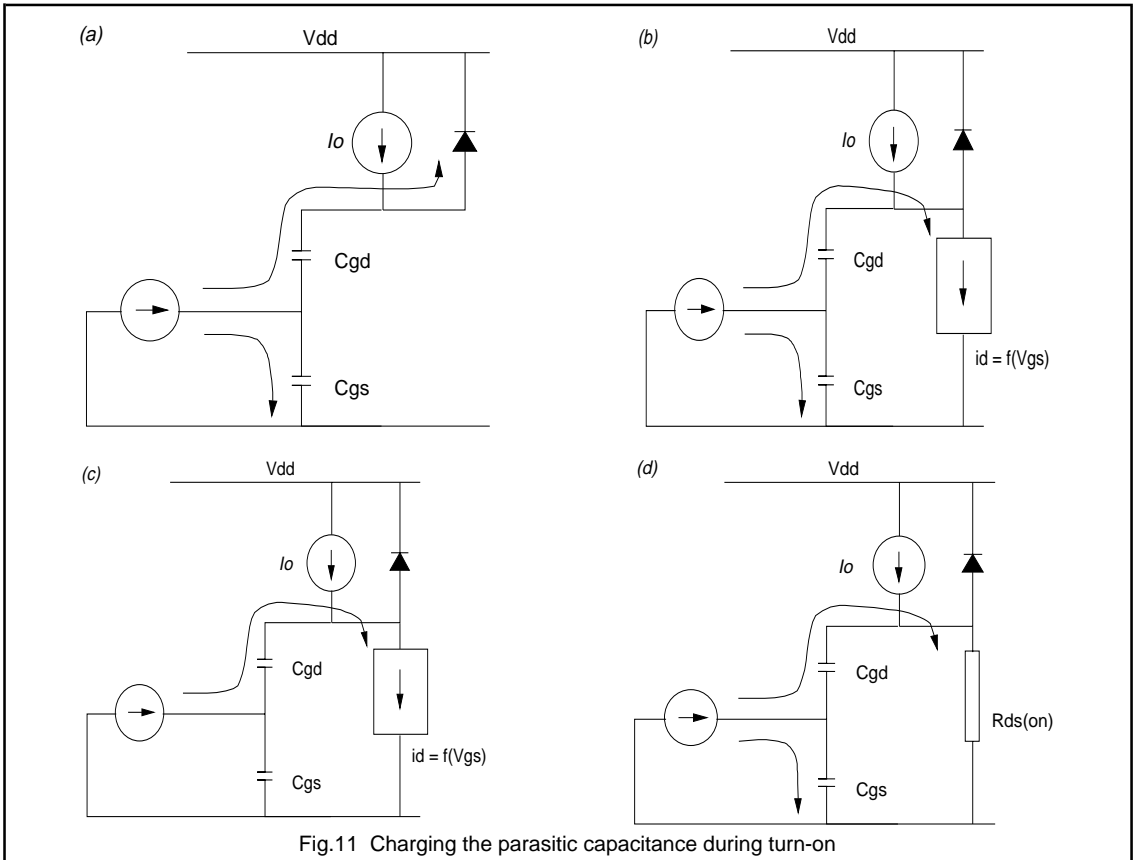
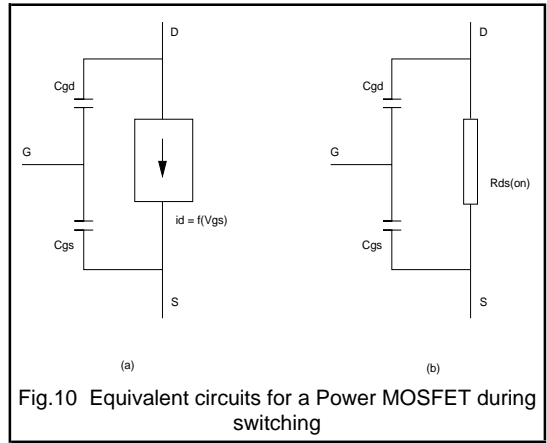


The current in the MOSFET continues to rise until  $i_d = I_0$ , since the device is still in its active region, the gate voltage becomes clamped at this point, ( $t_1$ ). The entire gate current now flows through  $C_{gd}$  causing the drain-source voltage to drop as  $C_{gd}$  is discharged, Fig.11(c). The rate at which  $V_{ds}$  falls is given by:

$$\frac{dV_{ds}}{dt} = \frac{dV_{dg}}{dt} = \frac{i_g}{C_{gd}} \quad 6$$

As  $V_{dg}$  approaches zero,  $C_{gd}$  starts to increase dramatically, reaching its maximum as  $V_{dg}$  becomes negative.  $dV_{ds}/dt$  is now greatly reduced giving rise to the voltage tail.

Once the drain-source voltage has completed its drop to the on-state value of  $I_0 \cdot R_{DS(ON)}$ , (point  $t_2$ ), the gate source voltage becomes unclamped and continues to rise, Fig.11(d). (NB  $dV_{gs}/dQ$  in regions 1 and 3 indicates the input capacitance values.)

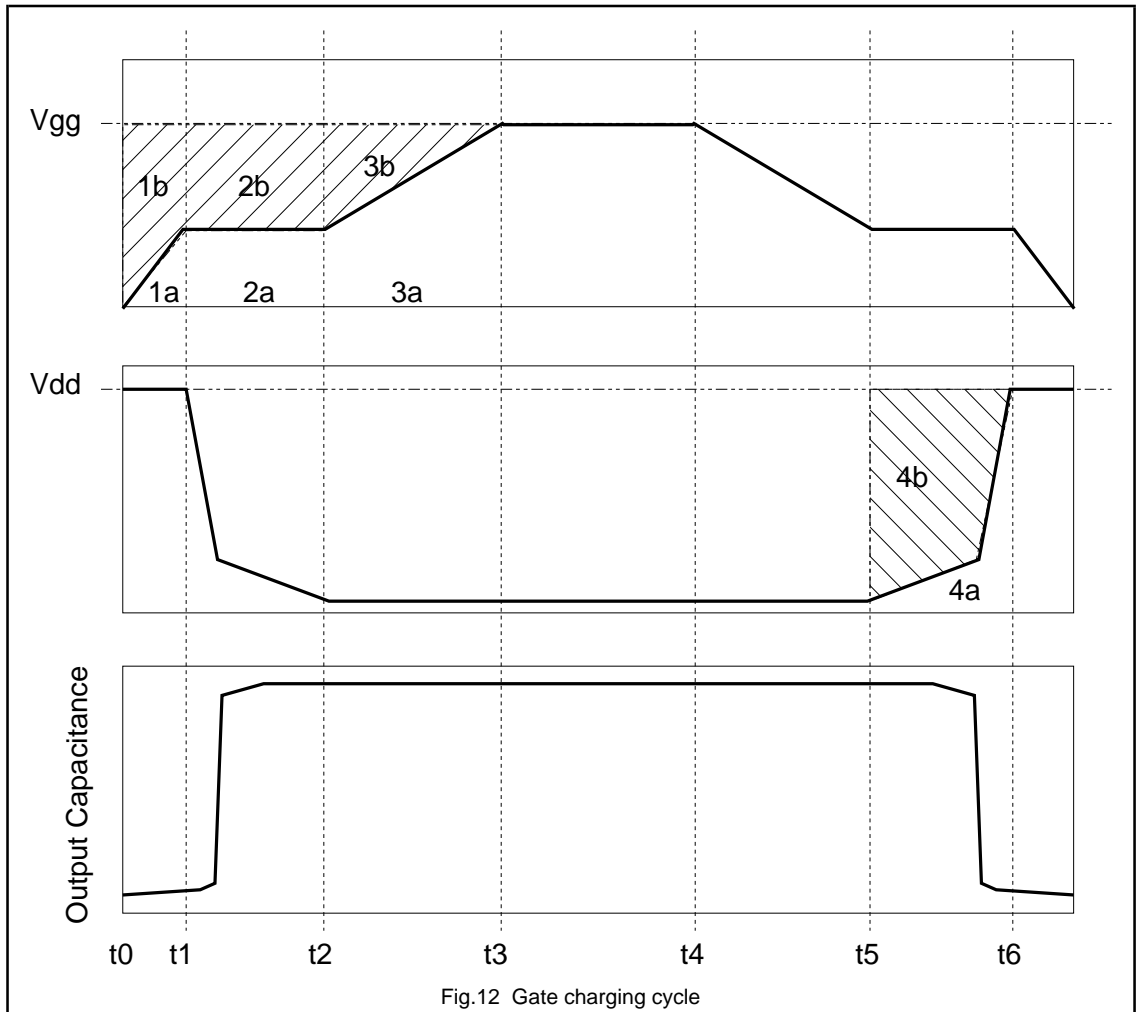


The gate charge oscillogram can be found in the data for all Philips PowerMOS devices. This plot can be used to determine the required average gate drive current for a particular switching speed. The speed is set by how fast the charge is supplied to the MOSFET.

### Energy consumed by the switching event

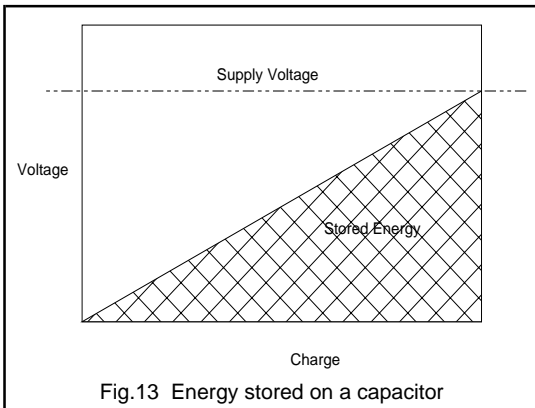
In the majority of applications the power MOSFET will be driven not from a constant current source but via a fixed

gate drive impedance from a voltage source. Fig.13 shows the voltage on a voltage independent capacitor as a function of charge. The area beneath the charge vs voltage curve equals the stored energy ( $E = Q.V/2$ ). The area above the charge vs voltage curve (bounded by the supply voltage) is the amount of energy dissipated during the charging cycle from a fixed voltage source. The total energy delivered by the supply is therefore  $Q.V$ , where  $1/2 Q.V$  is stored on the capacitor to be dissipated during the discharge phase.



Although the voltage vs charge relationship for the MOSFETs gate is not linear, energy loss is easily identified. The following discussion assumes a simple drive circuit consisting of a voltage source and drive resistance.

From  $t_0$  to  $t_1$  energy is stored in the gate capacitance which is equal to the area of region 1a. Since this charge has fallen through a voltage  $V_{gg} - V_{gs}(t)$ , the area of region 1b represents the energy dissipated in the drive resistance during its delivery. Between  $t_1$  and  $t_2$  all charge enters  $C_{gd}$ , the area of region 2a represents the energy stored in  $C_{gd}$  while 2b again corresponds with the energy dissipation in the drive resistor. Finally, between  $t_2$  and  $t_3$  additional energy is stored by the input capacitance equal to the area of region 3a.



The total energy dissipated in the drive resistance at turn-on is therefore equal to the area  $1b + 2b + 3b$ . The corresponding energy stored on the input capacitance is  $1a + 2a + 3a$ , this energy will be dissipated in the drive resistance at turn-off. The total energy expended by the gate drive for the switching cycle is  $Q \cdot V_{gg}$ .

As well as energy expended by the drive circuit, a switching cycle will also require energy to be expended by the drain circuit due to the charging and discharging of  $C_{gd}$  and  $C_{ds}$  between the supply rail and  $V_{DS(ON)}$ . Moving from  $t_5$  to  $t_6$  the drain side of  $C_{gd}$  is charged from  $I_o \cdot R_{DS(ON)}$  to  $V_{dd}$ . The drain circuit must therefore supply sufficient current for this charging event. The total charge requirement is given by the plateau region,  $Q_6 - Q_5$ . The area 4a (Fig.12) under the drain-source voltage curve represents the energy stored by the drain circuit on  $C_{gd}$  during turn-on. Region 4b represents the corresponding energy delivered to the load during this period. The energy consumed from the drain supply to charge and discharge  $C_{gd}$  over one switching cycle is thus given by:

$$W_{DD} = (Q_6 - Q_5) \cdot (V_{DD} - V_{DS(ON)}) \quad 7$$

(The energy stored on  $C_{gd}$  during turn-off is dissipated internally in the MOSFET during turn-on.) Additional energy is also stored on  $C_{ds}$  during turn-off which again is dissipated in the MOSFET at turn-on.

The energy lost by both the gate and drain supplies in the charging and discharging of the capacitances is very small over 1 cycle; Fig.9 indicates 40 nc is required to raise the gate voltage to 10 V, delivered from a 10 V supply this equates to 400 nJ; to charge  $C_{gd}$  to 80 V from an 80 V supply will consume  $12 \text{ nc} \times 80 \text{ V} = 1.4 \mu\text{J}$ . Only as switching frequencies approach 1 MHz will this energy loss start to become significant. (NB these losses only apply to square wave switching, the case for resonant switching is some-what different.)

## Switching performance

### 1) Turn-on

The parameters likely to be of most importance during the turn-on phase are,

- turn-on time
- turn-on loss
- peak  $dV/dt$
- peak  $dI/dt$ .

Turn-on time is simply a matter of how quickly the specified charge can be applied to the gate. The average current that must be supplied over the turn-on period is

$$I_{on} = \frac{Q}{t_{on}} \quad 8$$

For repetitive switching the average current requirement of the drive is

$$I = Q \cdot f \quad 9$$

where  $f$  = frequency of the input signal

Turn-on loss occurs during the initial phase when current flows in the MOSFET while the drain source voltage is still high. To minimise this loss, a necessary requirement of high frequency circuits, requires the turn-on time to be as small as possible. To achieve fast switching the drive circuit must be able to supply the initial peak current, given by equation 10.

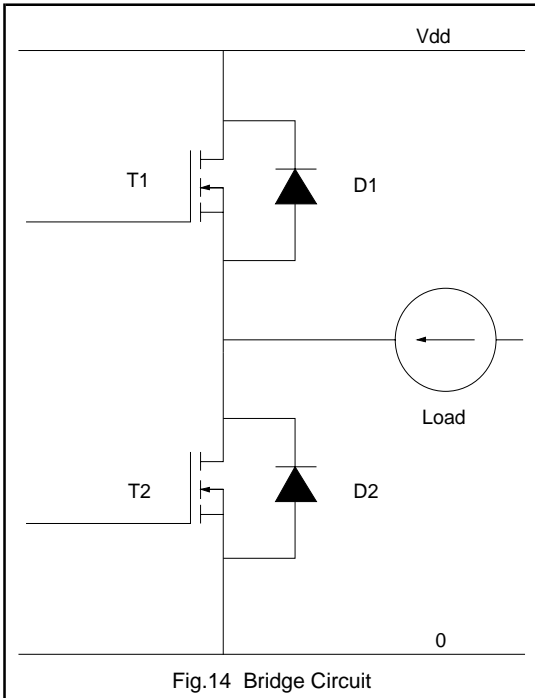


Fig.14 Bridge Circuit

$$I_{pk} = \frac{V_{GG}}{R_g} \quad 10$$

One of the main problems associated with very fast switching MOSFETs is the high rates of change in voltage and current. High values of  $dV/dt$  can couple through parasitic capacitances to give unwanted noise on signal lines. Similarly a high  $dI/dt$  may react with circuit inductance to give problematic transients and overshoot voltages in the power circuit.  $dI/dt$  is controlled by the time taken to charge the input capacitance up to the plateau voltage, while  $dV/dt$  is governed by the rate at which the plateau region is moved through.

$$\frac{dVds}{dt} = \frac{i_g}{C_{gd}} = \frac{V_{GG} - V_{GT}}{R_g \cdot C_{gd}} \quad 11$$

Particular care is required regarding  $dV/dt$  when switching in bridge circuits, (Fig.14). The free wheeling diode will have associated with it a reverse recovery current. When the opposing MOSFET switches on, the drain current rises beyond the load current value  $I_o$  to a value  $I_o + I_{rr}$ . Consequently  $V_{gs}$  increases beyond  $V_{gt}(I_o)$  to  $V_{gt}(I_o + I_{rr})$  as shown in Fig.15. Once the diode has recovered there is a rapid decrease in  $V_{gs}$  to  $V_{gt}(I_o)$  and this rapid decrease provides additional current to  $C_{gd}$  on top of that being supplied by the gate drive. This in turn causes  $V_{dg}$  and  $V_{ds}$  to decrease very rapidly during this recovery period.

The  $dV/dt$  in this period is determined by the recovery properties of the diode in relation to the  $dI/dt$  imposed upon it by the turn-on of the MOSFET, (reducing  $dI/dt$  will reduce this  $dV/dt$ , however it is best to use soft recovery diodes).

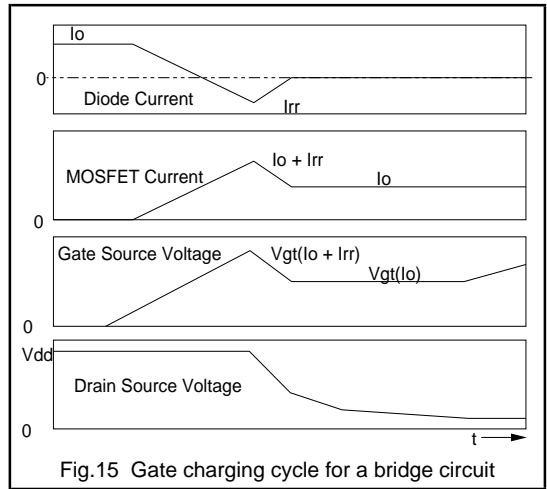


Fig.15 Gate charging cycle for a bridge circuit

ii) Turn-off

The parameters of most importance during the turn-off phase are,

- turn-off time
- turn-off loss
- peak  $dV/dt$
- peak  $dI/dt$ .

Turn-off of a power MOSFET is more or less the inverse of the turn-on process. The main difference is that the charging current for  $C_{gd}$  during turn-off must flow through both the gate circuit impedance and the load impedance. A high load impedance will thus slow down the turn-off speed.

The speed at which the plateau region is moved through determines the voltage rise time. In most applications the charging current for  $C_{gd}$  will be limited by the gate drive circuitry. The charging current, assuming no negative drive, is simply

$$i = \frac{V_{gt}}{R_g} \quad 12$$

and the length of the plateau region will be

$$t_p = \frac{Q \cdot R_g}{V_{gt}} \quad 13$$

The implications for low threshold (Logic Level) MOSFETs are clear from the above equations. The lower value of  $V_{gt}$  will mean a slower turn-off for a given gate impedance when compared to an equivalent standard threshold device. Equivalent switching therefore requires a lower drive impedance to be used.

### Conclusions

In theory the speed of a power MOSFET is limited only by the parasitic inductances of its internal bond wires. The

speed is essentially determined by how fast the internal capacitances can be charged and discharged by the drive circuit. Switching speeds quoted in data should be treated with caution since they only reflect performance for one particular drive condition. The gate charge plot is a more useful way of looking at switching capability since it indicates how much charge needs to be supplied by the drive to turn the device on. How fast that charge should be applied depends on the application and circuit performance requirements.



## 1.2.3 Power MOSFET Drive Circuits

MOSFETs are being increasingly used in many switching applications because of their fast switching times and low drive power requirements. The fast switching times can easily be realised by driving MOSFETs with relatively simple drive circuits. The following paragraphs outline the requirements of MOSFET drive circuits and present various circuit examples. A look at the special requirements of very fast switching circuits is also presented, this can be found in the latter part of this article.

### The requirements of the drive circuit

The switching of a MOSFET involves the charging and discharging of the capacitance between the gate and source terminals. This capacitance is related to the size of the MOSFET chip used typically about 1-2 nF. A gate-source voltage of 6V is usually sufficient to turn a standard MOSFET fully on. However further increases in gate-to-source voltage are usually employed to reduce the MOSFETs on-resistance. Therefore for switching times of about 50 ns, applying a 10 V gate drive voltage to a MOSFET with a 2 nF gate-source capacitance would require the drive circuit to sink and source peak currents of about 0.5 A. However it is only necessary to carry this current during the switching intervals.

The gate drive power requirements are given in equation (1)

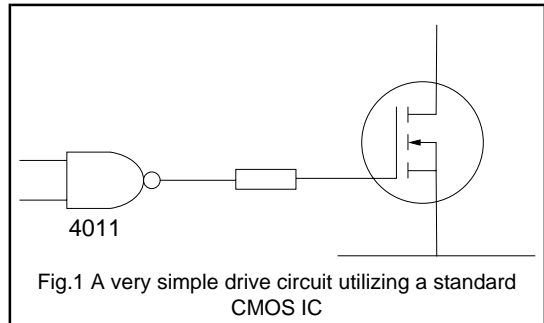
$$P_G = Q_G \cdot V_{GS} \cdot f \quad 1$$

where  $Q_G$  is the peak gate charge,  $V_{GS}$  is the peak gate source voltage and  $f$  is the switching frequency.

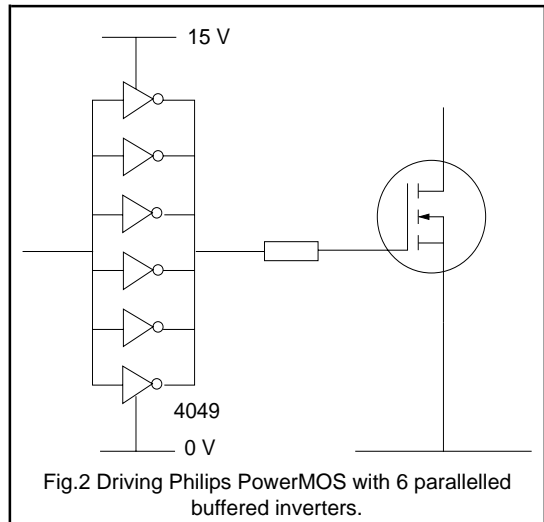
In circuits which use a bridge configuration, the gate terminals of the MOSFETs in the circuit need to float relative to each other. The gate drive circuitry then needs to incorporate some isolation. The impedance of the gate drive circuit should not be so large that there is a possibility of  $dV/dt$  turn on.  $dV/dt$  turn on can be caused by rapid changes of drain to source voltage. The charging current for the gate-drain capacitance  $C_{GD}$  flows through the gate drive circuit. This charging current can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on.

### Non-isolated drive circuits

MOSFETs can be driven directly from a CMOS logic IC as shown in Fig.1.

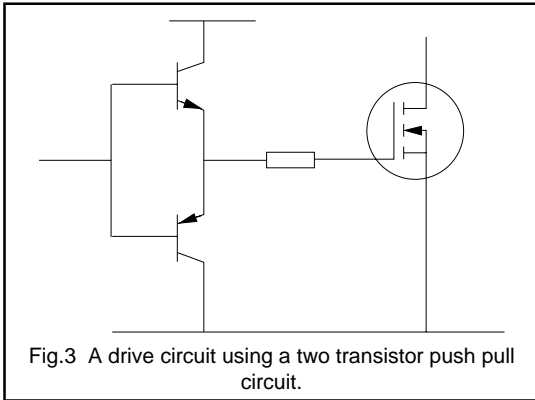


Faster switching speeds can be achieved by parallelling CMOS hex inverting (4049) or non-inverting (4050) buffers as shown in Fig.2.



A push pull circuit can also be used as shown in Fig.3.

The connections between the drive circuit and the MOSFET should be kept as short as possible and twisted together if the shortest switching times are required. If both the drive circuit and the terminals of the MOSFET are on the same PCB, then the inductance of tracks, between the drive transistors and the terminals of the MOSFETs, should be kept as small as possible. This is necessary to reduce the impedance of the drive circuit in order to reduce the switching times and lessen the susceptibility of the circuit



to  $dV/dt$  turn-on of the MOSFET. Attention to layout also improves the immunity to spurious switching by interference.

One of the advantages of MOSFETs is that their switching times can be easily controlled. For example it may be required to limit the rate of change of drain current to reduce overshoot on the drain source voltage waveform. The overshoot may be caused by switching current in parasitic lead or transformer leakage inductance. The slower switching can be achieved by increasing the value of the gate drive resistor.

The supply rails should be decoupled near to fast switching elements such as the push-pull transistors in Fig.3. An electrolytic capacitor in parallel with a ceramic capacitor are recommended since the electrolytic capacitor will not be a low enough impedance to the fast edges of the MOSFET drive pulse.

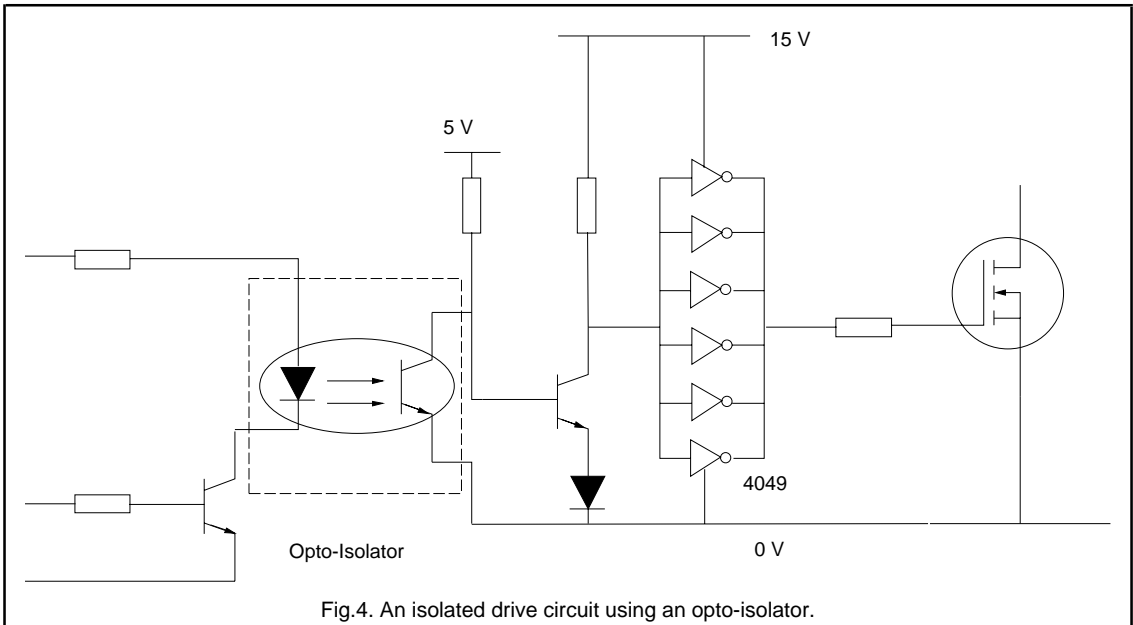
### Isolated drive circuits

Some circuits demand that the gate and source terminals of MOSFETs are floating with respect to those of other MOSFETs in the circuit. Isolated drive to these MOSFETs can be provided in the following way:

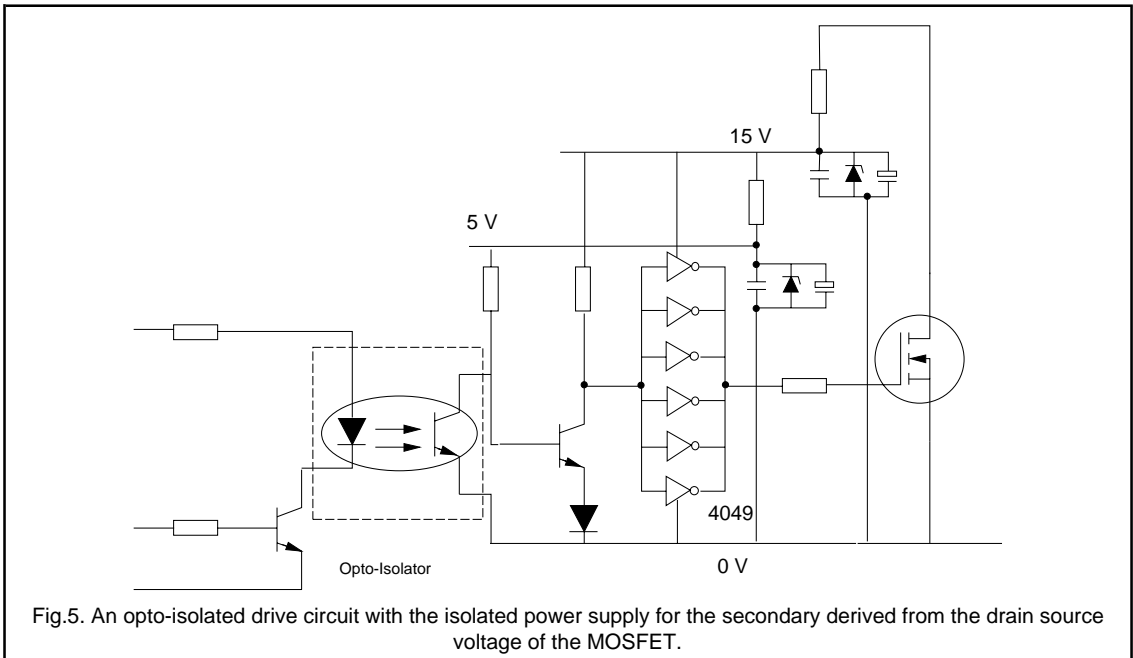
#### (a) Opto-isolators.

A drive circuit using an opto-isolator is shown in Fig.4.

A diode in the primary side of the opto-isolator emits photons when it is forward biased. These photons impinge on the base region of a transistor in the secondary side. This causes photogeneration of carriers sufficient to satisfy the base requirement for turn-on. In this way the opto-isolator provides isolation between the primary and secondary of the opto-isolator. An isolated supply is required for the circuitry on the secondary side of the opto-isolator. This supply can be derived, in some cases, from the drain-to-source voltage across the MOSFET being driven as shown in Fig.5. This is made possible by the low drive power requirements of MOSFETs.







Some opto-isolators incorporate an internal screen to improve the common mode transient immunity. Values as high as 1000 V/μs are quoted for common mode rejection which is equivalent to rejecting a 300V peak-to-peak sine wave.

The faster opto-isolators work off a maximum collector voltage on the secondary side of 5V so some form of level shifting may be required.

**(b) Pulse transformers.**

A circuit using a pulse transformer for isolation is shown in Fig.6(a).

When T2 switches on, voltage is applied across the primary of the pulse transformer. The current through T2 consists of the sum of the gate drive current for T1 and the magnetising current of the pulse transformer. From the waveforms of current and voltage around the circuit shown in Fig.6(b), it can be seen that after the turn off of T2 the voltage across it rises to  $V_D + V_Z$ , where  $V_Z$  is the voltage across the zener diode  $Z_D$ . The zener voltage  $V_Z$  applied across the pulse transformer causes the flux in the core to be reset. Thus the net volt second area across the pulse transformer is zero over a switching cycle. The minimum number of turns on the primary is given by equation (2).

$$N = \frac{V \cdot t}{B \cdot A_e}$$

2

where B is the maximum flux density,  $A_e$  is the effective cross sectional area of the core and t is the time that T2 is on for.

The circuit in Fig.6(a) is best suited for fixed duty cycle operation. The zener diode has to be large enough so that the flux in the core will be reset during operation with the maximum duty cycle. For any duty cycle less than the maximum there will be a period when the voltage across the secondary is zero as shown in Fig.7.

In Fig.8 a capacitor is used to block the dc components of the drive signal.

Drive circuits using pulse transformers have problems if a widely varying duty cycle is required. This causes widely varying gate drive voltages when the MOSFET is off. In consequence there are variable switching times and varying levels of immunity to dV/dt turn on and interference. There are several possible solutions to this problem, some examples are given in Figs.9 - 12.

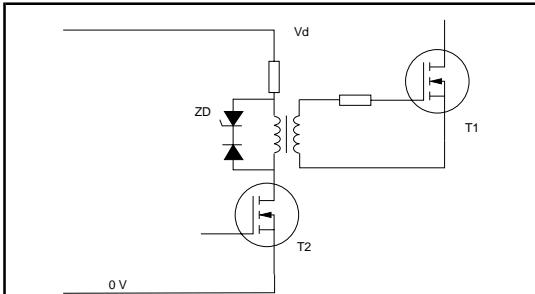


Fig.6(a) A circuit using a pulse transformer for isolation.

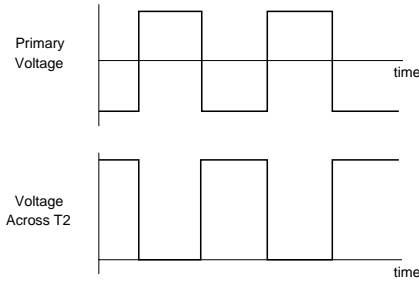


Fig.6(b) Waveforms associated with pulse transformer.

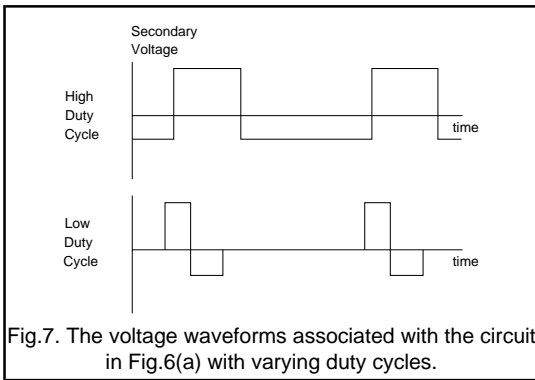


Fig.7. The voltage waveforms associated with the circuit in Fig.6(a) with varying duty cycles.

In the circuit shown in Fig.9 when A is positive with respect to B the input capacitance of T1 is charged through the parasitic diode of T2. The voltage across the secondary of the pulse transformer can then fall to zero and the input capacitance of T1 will remain charged. (It is sometimes necessary to raise the effective input capacitance with an external capacitor as indicated by the dashed lines.) When B becomes positive with respect to A T2 will turn on and the input capacitance of T2 will be discharged. The noise immunity of the circuit can be increased by using another MOSFET as shown in Fig.10.

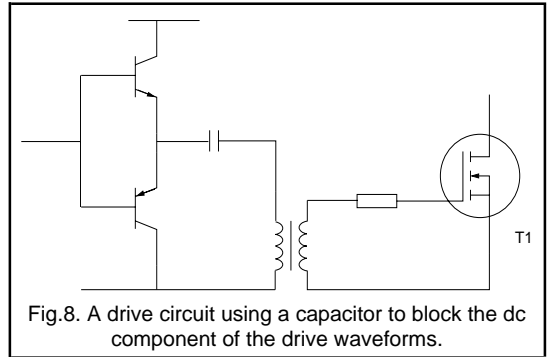


Fig.8. A drive circuit using a capacitor to block the dc component of the drive waveforms.

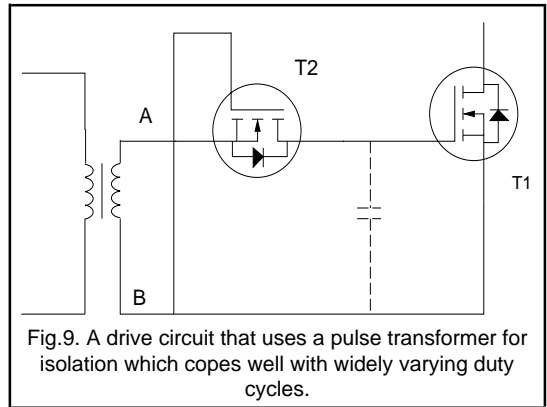


Fig.9. A drive circuit that uses a pulse transformer for isolation which copes well with widely varying duty cycles.

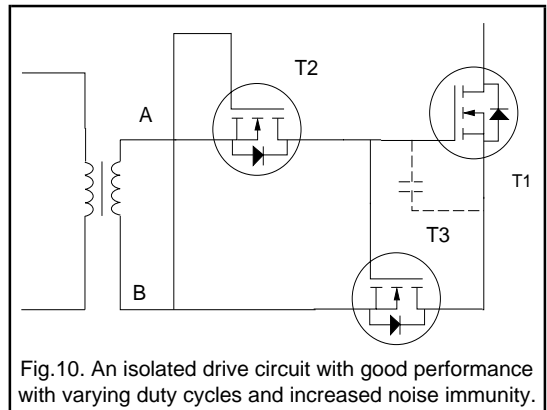


Fig.10. An isolated drive circuit with good performance with varying duty cycles and increased noise immunity.

In Fig.10 the potential at A relative to B has to be sufficient to charge the input capacitance of T3 and so turn T3 on before T1 can begin to turn on.

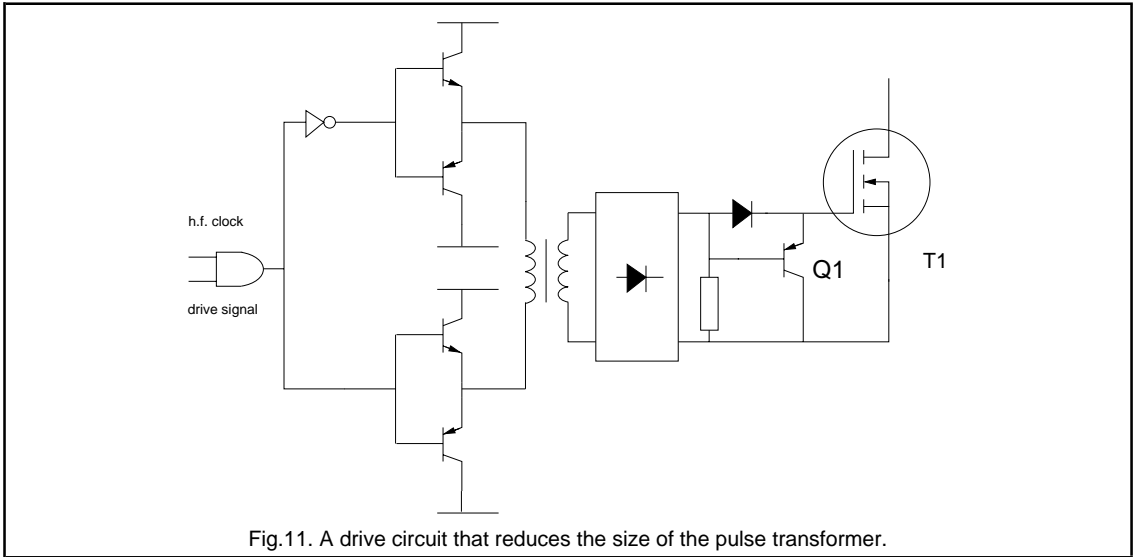


Fig.11. A drive circuit that reduces the size of the pulse transformer.

In Fig.11 the drive signal is ANDed with a hf clock. If the clock has a frequency much higher than the switching frequency of T1 then the size of the pulse transformer is reduced. The hf signal on the secondary of the pulse

transformer is rectified. Q1 provides a low impedance path for discharging the input capacitance of T1 when the hf signal on the secondary of the pulse transformer is absent.

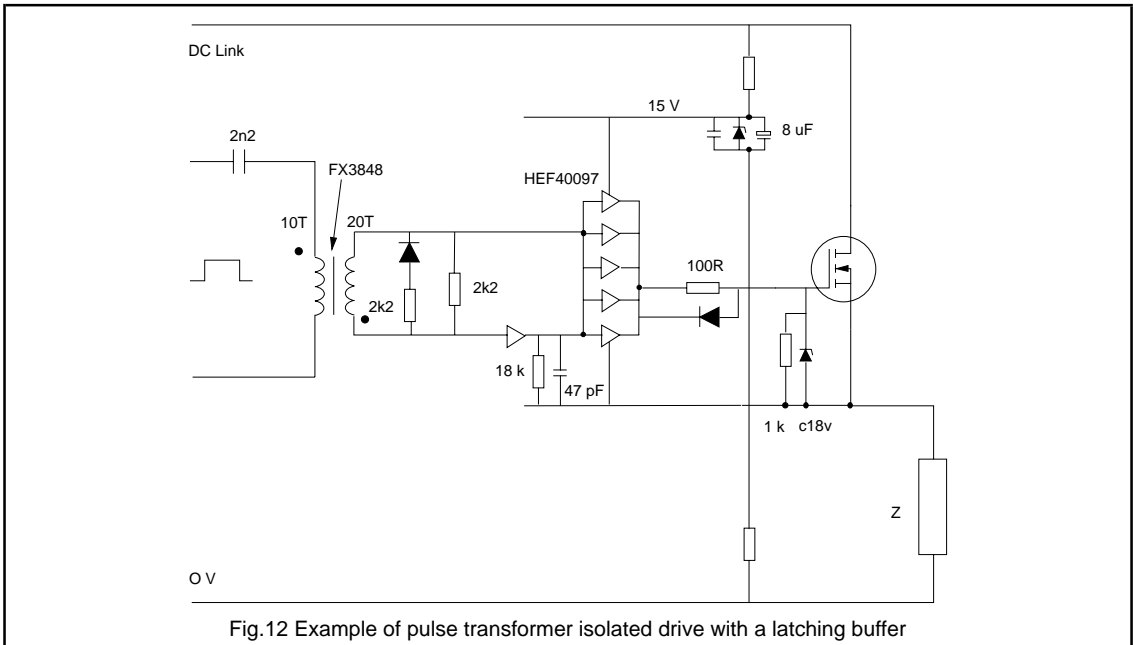


Fig.12 Example of pulse transformer isolated drive with a latching buffer

Figure 12 shows a hex non-inverting buffer connected on the secondary side, with one of the six buffers configured as a latch. The circuit operates such that the positive going edge of the drive pulse will cause the buffers to latch into the high state. Conversely the negative going edge of the drive pulse causes the buffers to latch into the low state. With the component values indicated on the diagram this circuit can operate with pulse on-times as low as 1  $\mu$ s. The impedance Z represents either the low side switch in a bridge circuit (which can be a MOSFET configured with identical drive) or a low side load.

The impedance of the gate drive circuit may be used to control the switching times of the MOSFET. Increasing gate drive impedance however can increase the risk of dV/dt turn-on. To try and overcome this problem it may be necessary to configure the drive as outlined in Fig.13.

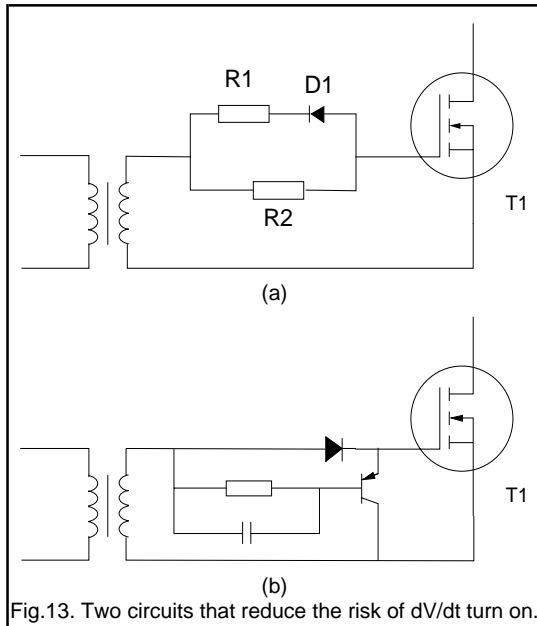


Fig.13. Two circuits that reduce the risk of dV/dt turn on.

The diode in Fig.13(a) reduces the gate drive impedance when the MOSFET is turned off. In Fig.13(b) when the drive pulse is taken away, the pnp transistor is turned on. When the pnp transistor is on it short-circuits the gate to the source and so reduces the gate drive impedance.

### High side drive circuits

The isolated drive circuits in the previous section can be used for either high or low side applications. Not all high side applications however require an isolated drive. Two examples showing how a high side drive can be achieved simply with a boot strap capacitor are shown in Fig.14. Both these circuits depend upon the topping up of the charge on

the boot strap capacitor while the MOSFET is off. For this reason these circuits cannot be used for dc switching. The minimum operating frequency is determined by the size of the boot strap capacitor (and R1 in circuit (a)), as the operating frequency is increased so the value of the capacitor can be reduced. The circuit example in Fig. 14(a) has a minimum operating frequency of 500 Hz.

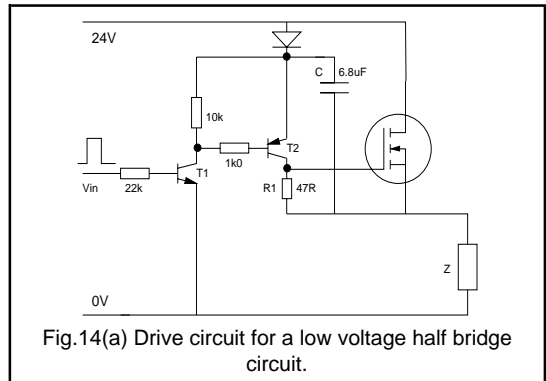


Fig.14(a) Drive circuit for a low voltage half bridge circuit.

At high frequencies it may be necessary to replace R1 with the transistor T3 as shown in Fig.14(b). This enables very fast turn-off times which would be difficult to achieve with circuit (a) since reducing R1 to a low value would cause the boot strap capacitor to discharge during the on-period. The impedance Z represents either the low side switch part of the bridge or the load.

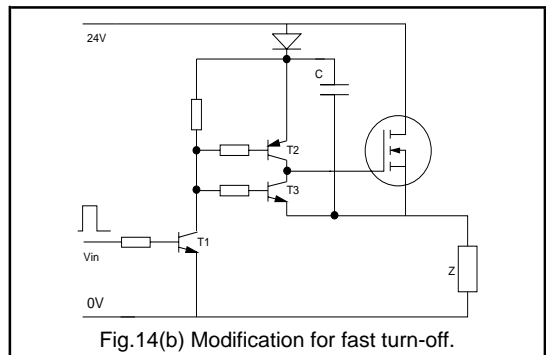


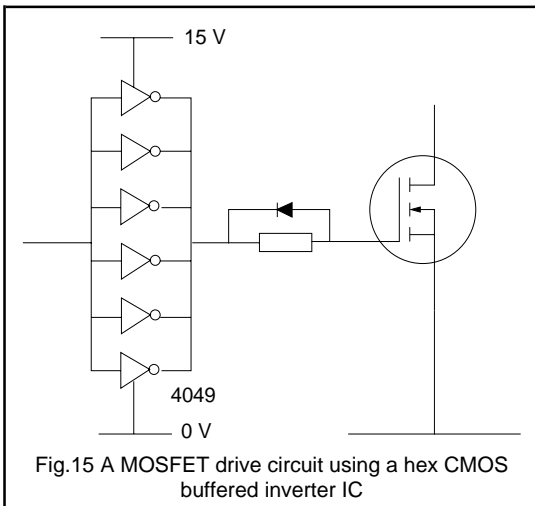
Fig.14(b) Modification for fast turn-off.

### Very fast drive circuits for frequencies up to 1 MHz

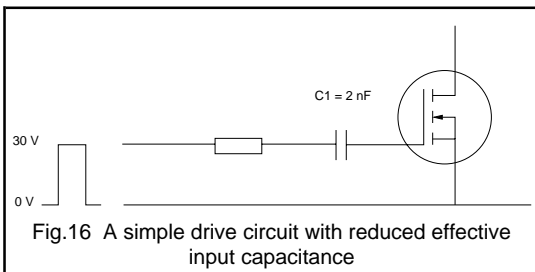
The following drive circuits can charge the gate source capacitance particularly fast and so realise extremely short switching times. These fast transition times are necessary to reduce the switching losses. Switching losses are directly proportional to the switching frequency and are greater than conduction losses above a frequency of about 500 kHz,

although this crossover frequency is dependent on circuit configuration. Thus for operation above 500 kHz it is important to have fast transition times.

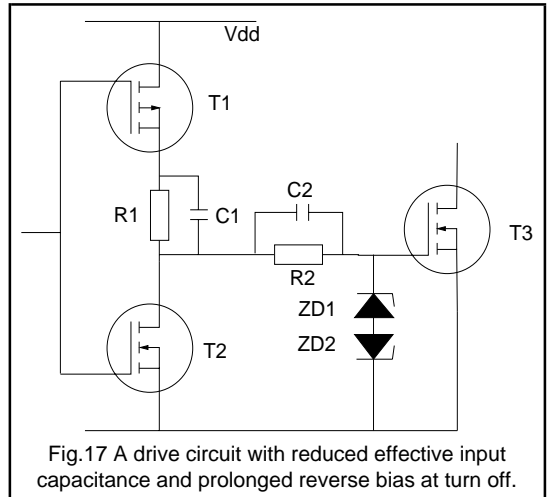
At frequencies below 500 kHz the circuit in Fig.15 is often used. Above 500 kHz the use of the DS0026 instead of the 4049 is recommended. The DS0026 has a high current sinking and sourcing capability of 2.5 A. It is a National Semiconductor device and is capable of charging a capacitance of 100 pF in as short a time as 25 ns.



In Fig.16 the value of capacitor C1 is made approximately equal to the input capacitance of the driven MOSFET. Thus the RC time constant for the charging circuit is approximately halved. The disadvantage of this arrangement is that a drive voltage of 30V instead of 15V is needed because of the potential divider action of C1 and the input capacitance of the driven MOSFET. A small value of C1 would be ideal for a fast turn on time and a large value of C1 would produce a fast turn off. The circuit in Fig.17 replaces C1 by two capacitors and enables fast turn on and fast turn off.



For the circuit in Fig.17 when MOSFET T1 is turned on the driven MOSFET T3 is driven initially by a voltage  $V_{DD}$  feeding three capacitors in series, namely C1, C2 and the input capacitance of T3. Since the capacitors are in series their equivalent capacitance will be low and so the RC time constant of the charging circuit will be low. C1 is made low to make the turn on time very fast.



The voltage across C2 will then settle down to  $(V_{DD} - V_{ZD1}) R2 / (R1 + R2)$ . Therefore the inclusion of resistors R1 and R2 means that C2 can be made larger than C1 and still have a large voltage across it before the turn off of T3. Thus C2 can sustain a reverse voltage across the gate source of T3 for the whole of the turn off time. The initial discharging current will be given by Equation 3,

$$I = \frac{V_{ZD1} + \frac{R_2(V_{DD} - V_{ZD1})}{(R1 + R2)}}{R_{STRAY} + R_{DS(ON)T2}} \quad 3$$

Making  $V_{DD}$  large will make turn on and turn off times very small.

Fast switching speeds can be achieved with the push pull circuit of Fig.19. A further improvement can be made by replacing the bipolar devices by MOSFETs as shown in Fig.20. The positions of the P and N channel MOSFETs may be interchanged and connected in the alternative arrangement of Fig.21. However it is likely that one MOSFET will turn on faster than the other turns off and so the circuit in Fig.21 may cause a current spike during the switching interval. The peak to average current rating of MOSFETs is excellent so this current spike is not usually a problem. In the circuit of Fig.20 the input capacitance of the driven MOSFET is charged up to  $V_{DD} - V_T$ , where  $V_T$  is the threshold voltage, at which point the MOSFET T1 turns off. Therefore when T2 turns on there is no current spike.

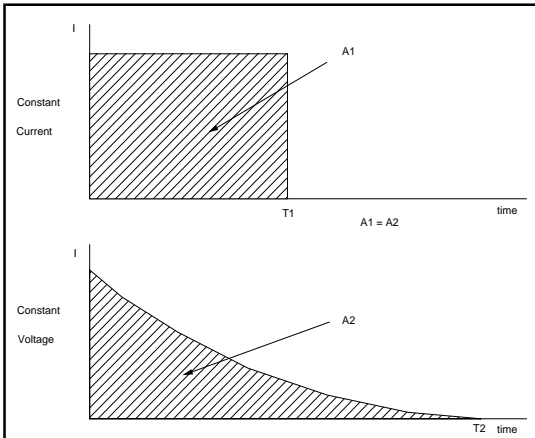


Fig.18 A comparison of the switching times for MOSFETs driven from a constant current source and a constant voltage source.

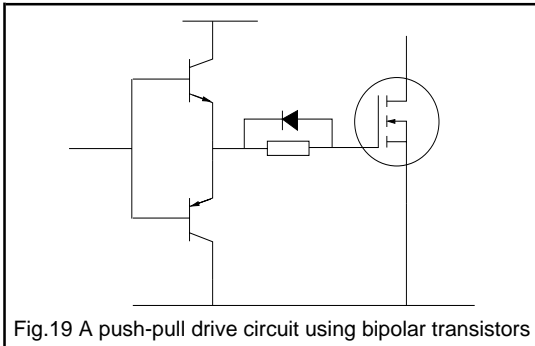


Fig.19 A push-pull drive circuit using bipolar transistors

There may well be some advantages in charging the input capacitance of the MOSFET from a constant current source rather than a constant voltage source. For a given drain source voltage a fixed amount of charge has to be transferred to the input capacitance of a MOSFET to turn it on. As illustrated in Fig.18 this charge can be transferred more quickly with a constant current of magnitude equal to the peak current from a constant voltage source.

A few other points are worthy of note when discussing very fast drive circuits.

(1) SMPS working in the 1 - 15 MHz range sometimes use resonant drive circuits. These SMPS are typically QRC (Quasi Resonant Circuits). The resonant drive circuits do not achieve faster switching by the fact that they are resonant. But by being resonant, they recoup some of the drive energy and reduce the gate drive power. There are two main types of QRC - zero voltage and zero current switching circuits. In one of these types, fall times are not critical and in the other, rise times are not critical. On the

critical switching edge, a normal, fast switching edge is provided by using a circuit similar to those given above. For the non-critical edge there is a resonant transfer of energy. Thus drive losses of  $Q_G \cdot V_{GS} \cdot f$  become  $0.5 \cdot Q_G \cdot V_{GS} \cdot f$ .

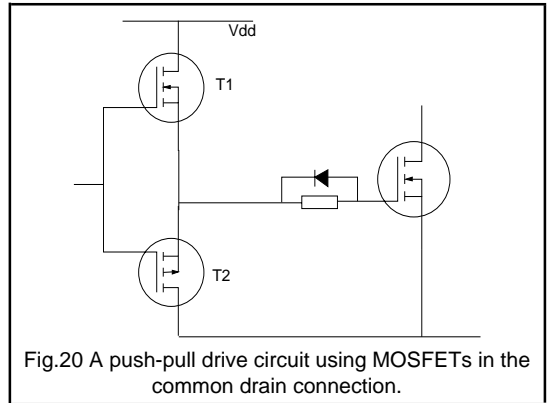


Fig.20 A push-pull drive circuit using MOSFETs in the common drain connection.

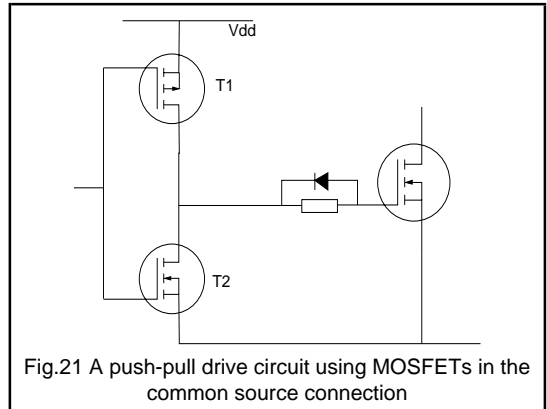


Fig.21 A push-pull drive circuit using MOSFETs in the common source connection

(2) It is usual to provide overdrive of the gate source voltage. This means charging the input capacitance to a voltage which is more than sufficient to turn the MOSFET fully on. This has advantages in achieving lower on-resistance and increasing noise immunity. The gate power requirements are however increased when overdrive is applied. It may well be a good idea therefore to drive the gate with only 12 V say instead of 15 V.

(3) It is recommended that a zener diode be connected across the gate source terminals of a MOSFET to protect against over voltage. This zener can have a capacitance which is not insignificant compared to the input capacitance of small MOSFETs. The zener can thus affect switching times.

## Parallel operation

Power MOSFETs lend themselves readily to operation in parallel since their positive temperature coefficient of resistance opposes thermal runaway. Since MOSFETs have low gate drive power requirements it is not normally necessary to increase the rating of drive circuit components if more MOSFETs are connected in parallel. It is however recommended that differential resistors are used in the drive circuits as shown in Fig.22.

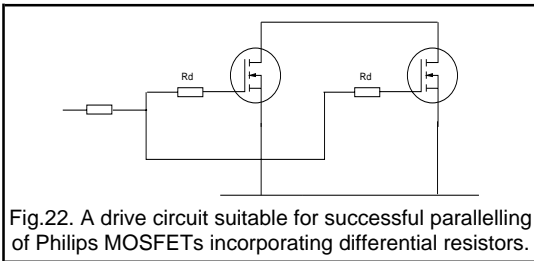


Fig.22. A drive circuit suitable for successful parallelling of Philips MOSFETs incorporating differential resistors.

These differential resistors ( $R_D$ ) damp down possible oscillations between reactive components in the device and in connections around the MOSFETs, with the MOSFETs themselves, which have a high gain even up to 200 MHz.

## Protection against gate-source overvoltages

It is recommended that zener diodes are connected across the gate-source terminals of the MOSFET to protect against voltage spikes. One zener diode or two back-to-back zener diodes are necessary dependent on whether the gate-source is unipolar or bipolar, as shown in Fig.23.

The zener diodes should be connected close to the terminals of the MOSFET to reduce the inductance of the connecting leads. If the inductance of the connecting leads is too large it can support sufficient voltage to cause an overvoltage across the gate-source oxide.

In conclusion the low drive power requirement of Philips PowerMOS make provision of gate drive circuitry a relatively straightforward process as long as the few guide-lines outlined in this note are heeded.

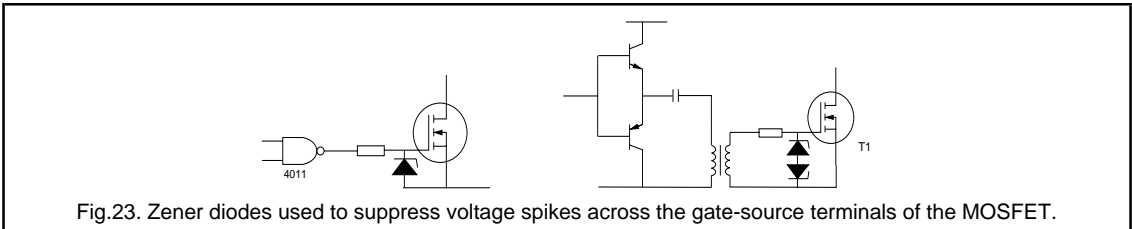


Fig.23. Zener diodes used to suppress voltage spikes across the gate-source terminals of the MOSFET.





## 1.2.4 Parallel Operation of Power MOSFETs

This section is intended as a guide to the successful parallelling of Power MOSFETs in switching circuits.

### Advantages of operating devices in parallel

#### Increased power handling capability

If power requirements exceed those of available devices then increased power levels can be achieved by parallelling devices. The alternative means of meeting the power requirements would be to increase the area of die. The processing of the larger die would have a lower yield and so the relative cost of the die would be increased. The larger die may also require a more expensive package.

#### Standardisation

Parallelling devices can mean that only one package, say the TO220 package, needs to be used. This can result in reduced production costs.

#### Increased operating frequency

Packages are commercially available which contain upto five die connected in parallel. The switching capabilities of these packages are typically greater than 10 kVA. The parasitic inductances of connections to the parallellled dies are different for each die. This means that the current rating of the package has to be derated at high frequencies to allow for unequal current sharing. The voltage rating of the multiple die package has to be derated for higher switching speeds. This is because the relatively large inductances of connections within the package sustain appreciable voltages during the switching intervals. This means that the voltages at the drain connections to the dice will be appreciably greater than voltages at the terminals of the package. By parallelling discrete devices these problems can be overcome.

Faster switching speeds are achieved using parallellled devices than using a multiple die package. This is because switching times are adversely affected by the impedance of the gate drive circuit. When devices are parallellled these impedances are parallellled and so their effect is reduced. Hence faster switching times and so reduced switching losses can be achieved.

Faster switching speeds improve parallelling. During switching intervals one MOSFET may carry more current than other MOSFETs in parallel with it. This is caused by differences in electrical parameters between the parallellled MOSFETs themselves or between their drive circuits. The increased power dissipation in the MOSFET which carries more current will be minimised if switching speeds are

increased. The inevitable inductance in the source connection, caused by leads within the package, causes a negative feedback effect during switching. If the rate of rise of current in one parallellled MOSFET is greater than in the others then the voltage drop across inductances in its drain and source terminals will be greater. This will oppose the build up of current in this MOSFET and so have a balancing effect. This balancing effect will be greater if switching speeds are faster. This negative feedback effect reduces the deleterious effect of unequal impedances of drive circuit connections to parallellled MOSFETs. The faster the switching speeds then the greater will be the balancing effect of the negative feedback. Parallelling devices enables higher operating frequencies to be achieved than using multiple die packages. The faster switching speeds possible by parallelling at the device level promote better current sharing during switching intervals.

#### Increased power dissipation capability

If two devices, each rated for half the total required current, are parallellled then the sum of their individual power dissipation capabilities will be more than the possible power dissipation in a single device rated for the total required current. This is especially useful for circuits operating above 100 kHz where switching losses predominate.

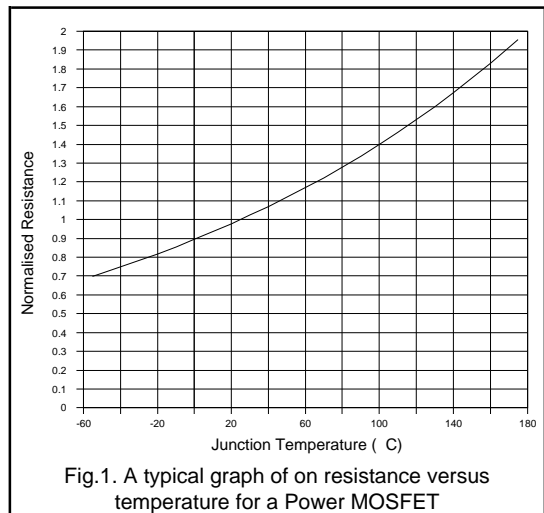


Fig. 1. A typical graph of on resistance versus temperature for a Power MOSFET

## Advantages of power MOSFETs for parallel operation

### Reduced likelihood of thermal runaway

If one of the paralleled devices carries more current than the power dissipation in this device will be greater and its junction temperature will increase. The temperature coefficient of  $R_{DS(ON)}$  for Power MOSFETs is positive as shown in Fig.1. Therefore there will be a rise in  $R_{DS(ON)}$  for the device carrying more current. This mechanism will oppose thermal runaway in paralleled devices and also in paralleled cells in the device.

### Low Drive Power Requirements

The low drive power requirements of power MOSFETs mean that many devices can be driven from the same gate drive that would be used for one MOSFET.

### Very good tolerance of dynamic unbalance

The peak to average current carrying capability of power MOSFETs is very good. A device rated at 8A continuous drain current can typically withstand a peak current of about 30A. Therefore, for the case of three 8A devices in parallel, if one of the devices switches on slightly before the others no damage will result since it will be able to carry the full load current for a short time.

## Design points

### Derating

Since there is a spread in on-resistance between devices from different batches it is necessary to derate the continuous current rating of paralleled devices by about 20%.

### Layout

There are two aspects to successful paralleling which are static and dynamic balance. Static balance refers to equal sharing of current between paralleled devices when they have been turned on. Dynamic balance means equal sharing of current between paralleled transistors during switching intervals.

Unsymmetrical layout of the circuit causes static imbalance. If the connections between individual MOSFETs and the rest of the power circuit have different impedances then there will be static imbalance. The connections need to be kept as short as possible to keep their inductance as small as possible. Symmetrical layout is particularly important in resonant circuits where MOSFETs carry a sinusoidal current e.g. in a voltage fed inverter feeding a series resonant circuit. In a current fed inverter, where switching in the inversion stage causes a rectangular wave of current

to be passed through a parallel resonant tank circuit, the voltage sustained by MOSFETs when they are off will be half sinusoid. A component of the current carried by MOSFETs will be a charging current for snubber capacitors which will be sinusoidal so again symmetrical layout will be important.

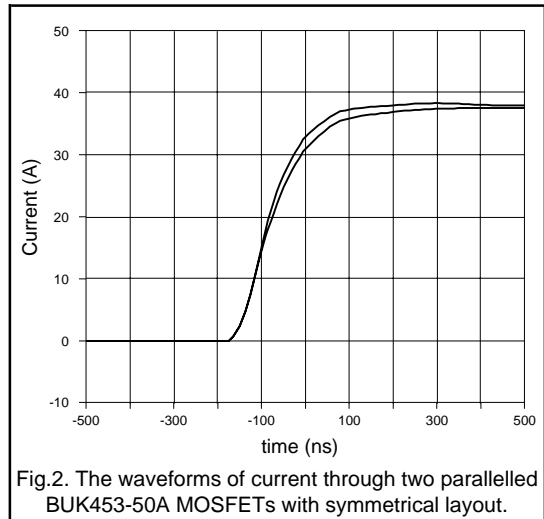


Fig.2. The waveforms of current through two paralleled BUK453-50A MOSFETs with symmetrical layout.

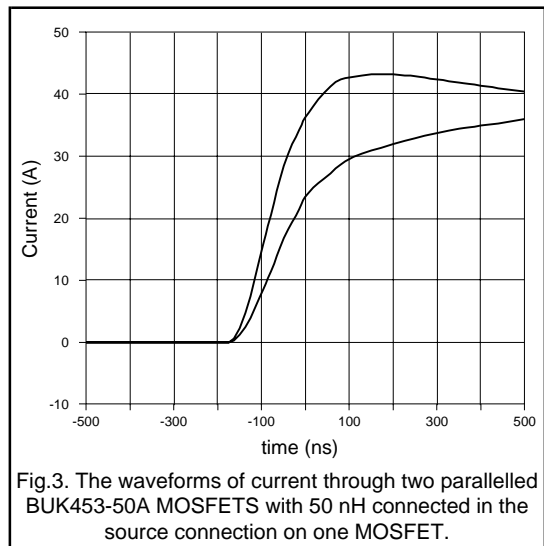


Fig.3. The waveforms of current through two paralleled BUK453-50A MOSFETs with 50 nH connected in the source connection on one MOSFET.

Unsymmetrical layout of the gate drive circuitry causes dynamic imbalance. Connections between the gate drive circuitry and the MOSFETs need to be kept short and twisted together to reduce their inductance. Further to this

the connections between the gate drive circuit and paralleled MOSFETs need to be approximately the same length.

Figures 2 and 3 illustrate the effect of unsymmetrical layout on the current sharing of two paralleled MOSFETs. The presence of 50 nH in the source connection of one of the two paralleled BUK453-50A MOSFETs causes noticeable imbalance. A square shaped loop of 1 mm diameter wire and side dimension only 25 mm is sufficient to produce an inductance of 50 nH.

Symmetrical layout becomes more important if more MOSFETs are paralleled, e.g. if a MOSFET with an  $R_{DS(ON)}$  of 0.7 Ohm was connected in parallel with a MOSFET with an  $R_{DS(ON)}$  of 1 Ohm then the MOSFET with the lower  $R_{DS(ON)}$  would carry 18% more current than if both MOSFETs had an  $R_{DS(ON)}$  of 1 ohm. If the MOSFET with an  $R_{DS(ON)}$  of 0.7 ohm was connected in parallel with a hundred MOSFETs with  $R_{DS(ON)}$  of 1 ohm it would carry 42% more current than if all the MOSFETs had an  $R_{DS(ON)}$  1 Ohm.

## Good Thermal Coupling

There should be good thermal coupling between paralleled MOSFETs. This is achieved by mounting paralleled MOSFETs on the same heatsink or on separate heatsinks which are in good thermal contact with each other.

If poor thermal coupling existed between paralleled MOSFETs and the positive temperature coefficient of resistance was relied on to promote static balance, then the total current carried by the MOSFETs would be less than with good thermal coupling. Some MOSFETs would also have relatively high junction temperatures and so their reliability would be reduced. The temperature coefficient of MOSFETs is not large enough to make poor thermal coupling tolerable.

## The Suppression of Parasitic Oscillations

Parasitic oscillations can occur. MOSFETs have transition frequencies typically in excess of 200 MHz and parasitic reactances are present both in the MOSFET package and circuit connections, so the necessary feedback conditions for parasitic oscillations exist. These oscillations typically occur at frequencies above 100 MHz so a high bandwidth oscilloscope is necessary to investigate them. The likelihood of these parasitic oscillations occurring is very much reduced if small differential resistors are connected in the leads to each paralleled MOSFET. A common gate drive resistor of between 10 and 100 Ohms with differential resistors of about 10 Ohm are recommended as shown in Fig.4.

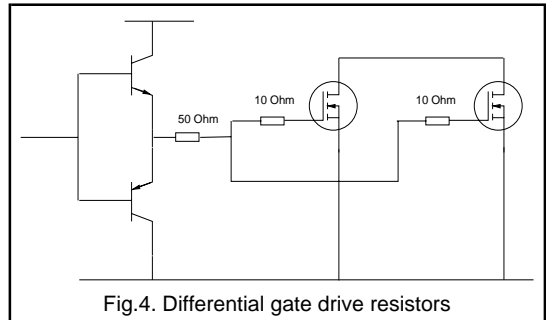


Fig.4. Differential gate drive resistors

The suppression of parasitic oscillations between paralleled MOSFETs can also be aided by passing the connections from the gate drive circuit through ferrite beads. The effect of these beads below 1 MHz is negligible. The ferrite beads however damp the parasitic oscillations which occur at frequencies typically above 100 MHz. An example of parasitic oscillations is shown in Fig.5.

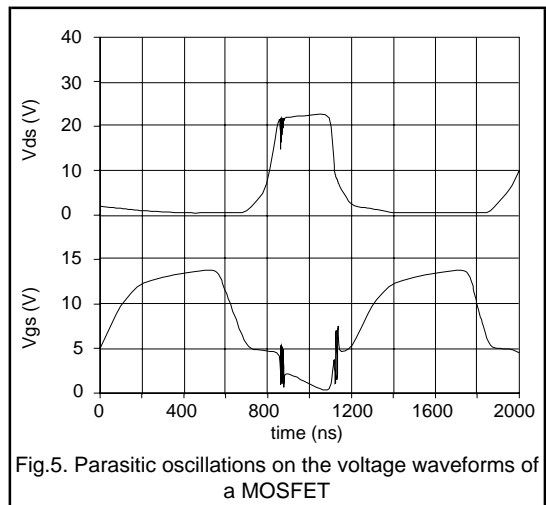


Fig.5. Parasitic oscillations on the voltage waveforms of a MOSFET

If separate drive circuits with closely decoupled power supplies are used for each paralleled device then parasitic oscillations will be prevented. This condition could be satisfied by driving each paralleled MOSFET from 3 buffers in a CMOS Hex buffer ic.

To take this one stage further, separate push pull transistor drivers could be used for each MOSFET. (A separate base resistor is needed for each push-pull driver to avoid a MOSFET with a low threshold voltage clamping the drive voltage to all the push pull drivers). This arrangement also has the advantage that the drive circuits can be positioned very close to the terminals of each MOSFET. The impedance of connections from the drive circuits to the MOSFETs will be minimised and so there will be a reduced

likelihood of spurious turn on. Spurious turn on can occur when there is a fast change in the drain to source voltage. The charging current for the gate drain capacitance inherent in the MOSFET structure can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on. The gate drive impedance needs to be kept as low as possible to reduce the likelihood of spurious turn on.

### Resonant power supplies

If a resonant circuit is used then there will be reduced interference and switching losses. The reduced interference is achieved because sinusoidal waveforms are present in resonant circuits rather than rectangular waveforms. Rectangular waveforms have large high frequency harmonic components.

MOSFETs are able to switch at a zero crossing of either the voltage or the current waveform and so switching losses are ideally zero. For example, in the case of a current fed inverter feeding a parallel resonant load switching can take place at a zero crossing of voltage so switching losses are negligible. In this case the sinusoidal drain source voltage sustained by MOSFETs reduces the likelihood of spurious  $dv/dt$  turn on. This is because the peak charging current for the internal gate to drain capacitance of the MOSFET is reduced.

### The current fed approach

Switch mode power supplies using the current fed topology have a d.c. link which contains a choke to smooth the current in the link. Thus a high impedance supply is presented to the inversion stage. Switching in the inversion stage causes a rectangular wave of current to be passed through the load. The current fed approach has many advantages for switch mode power supplies. It causes reduced stress on devices caused by the slow reverse recovery time of the parasitic diode inherent in the structure of MOSFETs.

The current fed approach can also reduce problems caused by dynamic imbalance. If more than three MOSFETs are paralleled then it is advantageous to use more than one choke in the d.c. link rather than wind a single choke out of thicker gauge wire. One of the connections to each choke

is connected to the output of the rectification stage. The other connection of each choke is connected to a group of three MOSFETs. This means that if one MOSFET switches on before the others it will carry a current less than its peak pulse value even when many MOSFETs are paralleled.

### The parallel operation of MOSFETs in the linear mode

The problems of paralleling MOSFETs which are being used in the linear mode are listed below.

(a) The paralleled devices have different threshold voltages and transconductances. This leads to poor sharing.

(b) MOSFETs have a positive temperature coefficient of gain at low values of gate to source voltage. This can lead to thermal runaway.

The imbalance caused by differences in threshold voltage and transconductance can be reduced by connecting resistors ( $R_s$ ) in the source connections. These resistors are in the gate drive circuit and so provide negative feedback. The negative feedback reduces the effect of different values of  $V_T$  and  $g_m$ . The effective transconductance  $g_m$  of the MOSFET is given in Equation 1.

$$g_m = \frac{1}{R_s + \frac{1}{g_m}} \quad 1$$

$R_s$  must be large compared to  $1/g_m$  to reduce the effects of differences in  $g_m$ . Values of  $1/g_m$  typically vary between 0.1 and 1.0 Ohm. Therefore values of  $R_s$  between 1 ohm and 10 ohm are recommended.

Differential heating usually has a detrimental effect on sharing and so good thermal coupling is advisable.

### Conclusions

Power MOSFETs can successfully be paralleled to realise higher power handling capability if a few guidelines are followed.

## 1.2.5 Series Operation of Power MOSFETs

The need for high voltage switches can be well illustrated by considering the following examples. In flyback converters the leakage inductance of an isolating transformer can cause a large voltage spike across the switch when it switches off. If high voltage MOSFETs are used the snubber components can be reduced in size and in some cases dispensed with altogether.

For industrial equipment operation from a supply of 415 V, 550 V or 660 V is required. Rectification of these supply voltages produces d.c. rails of approximately 550 V, 700 V and 800 V. The need for high voltage switches in these cases is clear.

Resonant topologies are being increasingly used in switching circuits. These circuits have advantages of reduced RFI and reduced switching losses. To reduce the size of magnetic components and capacitors the switching frequency of power supplies is increased. RFI and switching losses become more important at high frequencies so resonant topologies are more attractive. Resonant circuits have the disadvantage that the ratio of peak to average voltage can be large. For example a Parallel Resonant Power Supply for a microwave oven operating off a 240 V supply can be designed most easily using a switch with a voltage rating of over 1000 V.

In high frequency induction heating power supplies capacitors are used to resonate the heating coil. The use of high voltage switches in the inversion bridge can result in better utilisation of the kVAR capability of these capacitors. This is advantageous since capacitors rated at tens of kVAR above 100 kHz are very expensive.

In most TV deflection and monitor circuits peak voltages of up to 1300 V have to be sustained by the switch during the flyback period. This high voltage is necessary to reset the current in the horizontal deflection coil. If the EHT flashes over, the switch will have to sustain a higher voltage so 1500 V devices are typically required.

The Philips range of PowerMOS includes devices rated at voltages up to 1000 V to cater for these requirements. However in circuits, particularly in resonant applications where voltages higher than this are required, it may be necessary to operate devices in series.

Series operation can be attractive for the following reasons:

Firstly, the voltage rating of a PowerMOS transistor cannot be exceeded. A limited amount of energy can be absorbed by a device specified with a ruggedness rating

(eg device can survive some overvoltage transients), but a 1000 V device cannot block voltages in excess of 1000 V.

Secondly, series operation allows flexibility as regards on-resistance and so conduction losses.

The following are problems that have to be overcome for successful operation of MOSFETs in series. If one device turns off before another it may be asked to block a voltage greater than its breakdown voltage. This will cause a reduction in the lifetime of the MOSFET. Also there is a requirement for twice as many isolated gate drive circuits in many circuits.

The low drive power requirements of Philips PowerMOS mean that the provision of more isolated gate drive circuits is made easier. Resonant circuits can have advantages in reducing the problems encountered if one MOSFET turns off before another. The current fed full bridge inverter is one such circuit.

To illustrate how devices can be operated in series, a current fed full bridge inverter is described where the peak voltage requirement is greater than 1200 V.

### **The current fed inverter**

A circuit diagram of the full bridge current fed inverter is shown in Fig.1. A choke in the d.c. link smooths the link current. Switching in the inversion bridge causes a rectangular wave of current to be passed through the load. The load is a parallel resonant tank circuit. Since the Q of the tank circuit is relatively high the voltage across the load is a sinewave. MOSFETs sustain a half sinusoid of voltage when they are off. Thus series operation of MOSFETs is made easier because if one MOSFET turns off before another it only has to sustain a small voltage. To achieve the best sharing, the gate drive to MOSFETs connected in series should be as similar as possible. In particular the zero crossings should be synchronised. The MOSFET drive circuit shown in Fig.2 has been found to be excellent in this respect. For current fed resonant circuits in which the duty cycle varies over large ranges the circuit in Fig.3 will perform well. A short pulse applied to the primary of the pulse transformer is sufficient to turn MOSFET M4 on. This short pulse can be achieved by designing the pulse transformer so that it saturates during the time that M1 is on. The gate source capacitance of M4 will remain charged until M2 is turned on. M3 will then be turned on and the gate source capacitance of M4 will be discharged and so

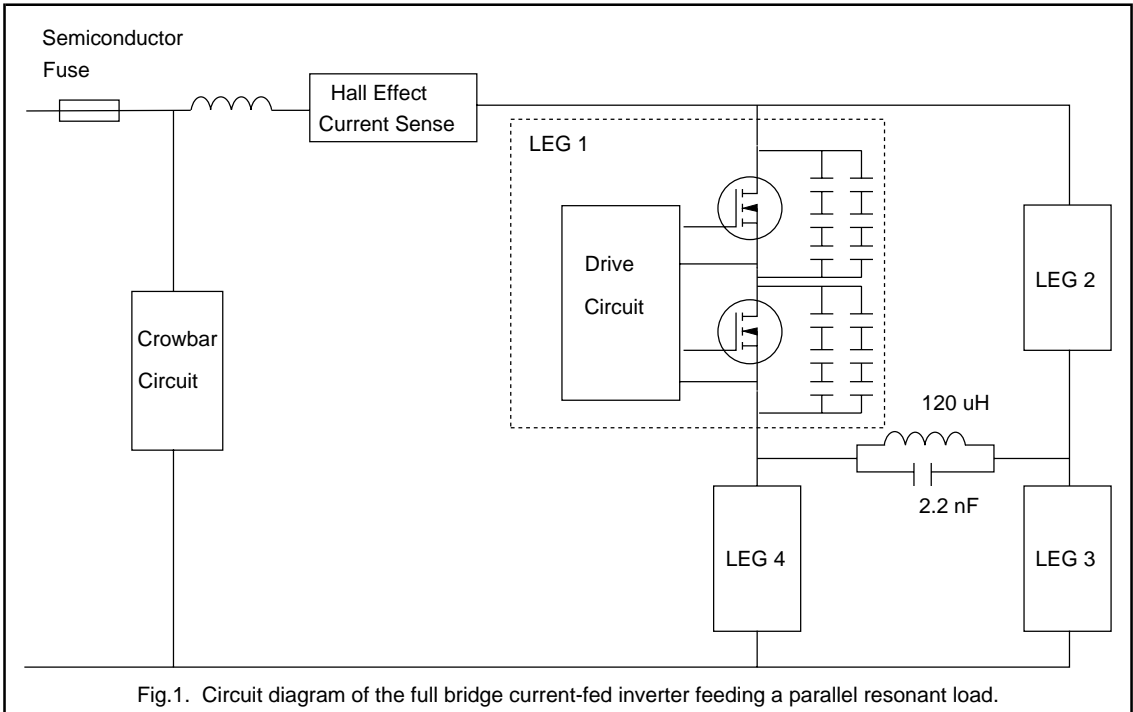


Fig.1. Circuit diagram of the full bridge current-fed inverter feeding a parallel resonant load.

M4 is turned off. Thus this circuit overcomes problems of resetting the flux in the core of the pulse transformer for large duty cycles.

Each leg of the inverter consists of two MOSFETs, type BUK456-800B, connected in series. The ideal rating of the two switches in each leg is therefore 1600 V and 3.5 A. The inverter is fed into a parallel resonant circuit with values of  $L = 120 \mu\text{H}$  ( $Q = 24$  at 150 kHz) and  $C = 2.2 \text{ nF}$ .

Capacitors are shown connected across the drain source terminals of MOSFETs. The value of the capacitor across the drain to source of each MOSFET is 6.6 nF. (Six 10 nF polypropylene capacitors, type 2222 376 92103.) This gives a peak voltage rating of about 850 V at 150 kHz for the capacitor combination across each MOSFET. (This voltage rating takes into account that the capacitors will only have to sustain voltage when the MOSFET is off). The function of these capacitors is twofold. Firstly they suppress spikes caused by switching off current in parasitic lead inductance. Secondly they improve the sharing of voltage between the MOSFETs connected in series. These capacitors are effectively in parallel with the tank circuit capacitor. However only half of the capacitors across MOSFETs are in circuit at any one time. This is because half of the capacitors are shorted out by MOSFETs which have been turned on. The resonant frequency of the tank circuit and drain source capacitors is given by Equation 1.

$$f = \frac{1}{2\pi\sqrt{L \cdot C_{tot}}} \quad 1$$

Where  $C_{tot}$  is the equivalent capacitance of the tank circuit capacitor and the drain source capacitors and is given by Equation 2.

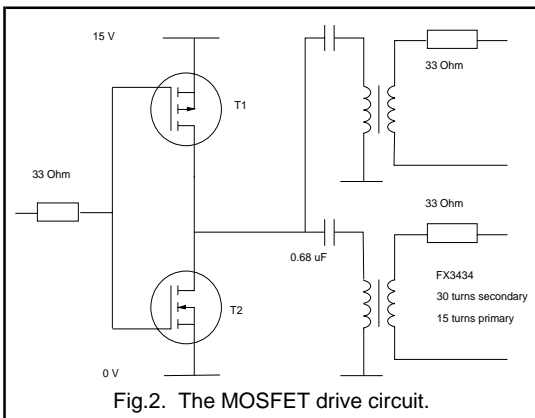


Fig.2. The MOSFET drive circuit.

$$C_{tot} = C_i + C_{DS} \quad 2$$

Therefore the resonant frequency of the tank circuit is 155 kHz.

An expression for the impedance at resonance of the parallel resonant circuit ( $Z_D$ ) is given in Equation 3.

$$Z_D = \frac{L}{C_{tot} \cdot R} \quad 3$$

The Q of the circuit is given by Equation 4.

$$Q = \frac{1}{R} \cdot \sqrt{\frac{L}{C_{tot}}} \quad 4$$

Substituting Equation 3.

$$Z_D = Q \cdot \sqrt{\frac{L}{C_{tot}}} \quad 5$$

Thus  $Z_D$  for the parallel resonant load was 2.7 kOhms.

In a conventional rectangular switching circuit the connection of capacitors across MOSFETs will cause additional losses. These losses are caused because when a MOSFET turns on, the energy stored in the drain source capacitance is dissipated in the MOSFET and in a series resistor. This series resistor is necessary to limit the current

spike in the MOSFET at turn on. These losses are appreciable at 150 kHz, e.g. the connection of 1 nF across a MOSFET switching 600 V would cause losses of more than 25 W at 150 kHz. In the current fed inverter described in this article the MOSFETs turn on when the voltage across the capacitor is ideally zero. Thus there is no need for a series resistor and the turn on losses are ideally zero.

In this case the supply to the inverter was 470 V rms. This means that the peak voltage in the d.c. link was 650 V.

Equating the power flowing in the d.c. link to the power dissipated in the tank circuit produces an expression for the peak voltage across the tank circuit ( $V_T$ ) as given in Equation 6.

$$V_T = 2 \times \sqrt{2} \times 1.11 \times V_{dclink} \quad 6$$

Therefore the peak to peak voltage across the tank circuit was ideally 2050 V

The voltage across each MOSFET should be 512 V.

### Circuit performance

The switching frequency of this circuit is 120 kHz. Thus the load is fed slightly below its resonant frequency. This means that the load looks inductive and ensures that the MOSFETs do not switch on when the capacitors connected across their drain source terminals are charged.

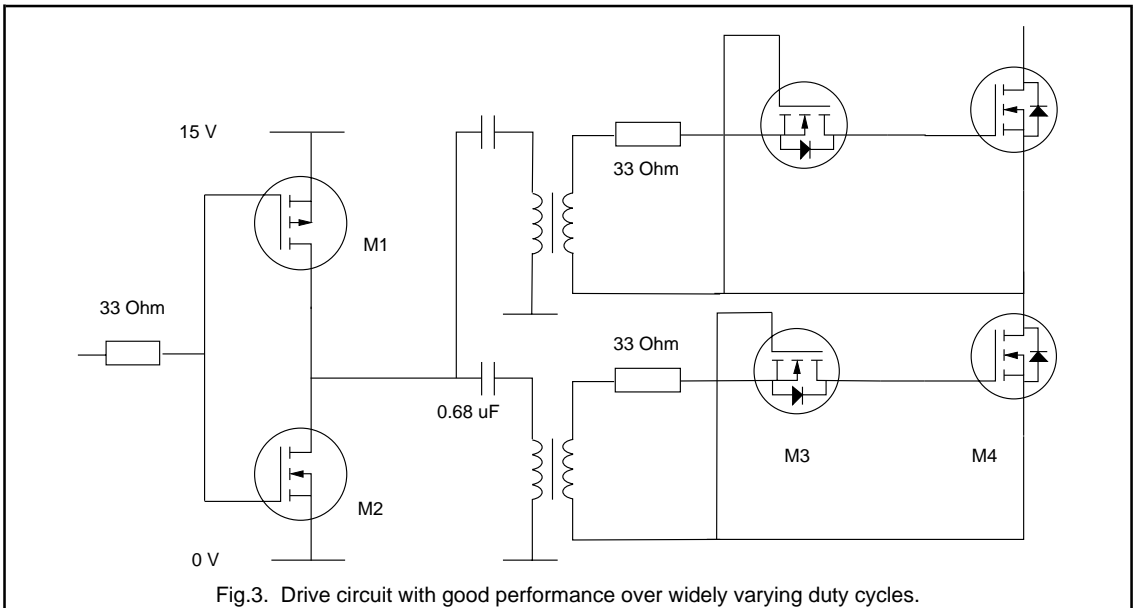


Fig.3. Drive circuit with good performance over widely varying duty cycles.

The waveforms of the voltage across two MOSFETs in series in a leg of the inversion bridge are shown in Fig.4. It can be seen that the sharing is excellent. The peak voltage across each MOSFET is 600 V. This is higher than 512 V because of ringing between parasitic lead inductance and the drain source capacitance of MOSFETs when they switch off.

The MOSFETs carry two components of current. The first component is the d.c. link current. The second component is a fraction of the circulating current of the tank circuit. The size of the second component is dependent on the relative sizes of the drain source capacitance connected across MOSFETs and the tank circuit capacitor.

In this circuit the peak value of charging current for drain source capacitors, which is carried by the MOSFET, is 4 A. The on-resistance of the BUK456-800B is about 5 Ohms at 80 °C. This explains the rise in  $V_{DS(ON)}$  of about 20 V seen in Fig.4 just above the turn off of the MOSFETs.

The sharing of Philips PowerMOS in this configuration is so good that the value of drain source capacitance is not determined by its beneficial effect on sharing. Therefore, the value can be selected solely on the need to control ringing which in turn is dependent on power output and layout. (The increased current level associated with increased power output makes the ringing worse).

In any given configuration there is a maximum output power that single MOSFETs can handle and there will be a value of drain source capacitance associated with it. This value

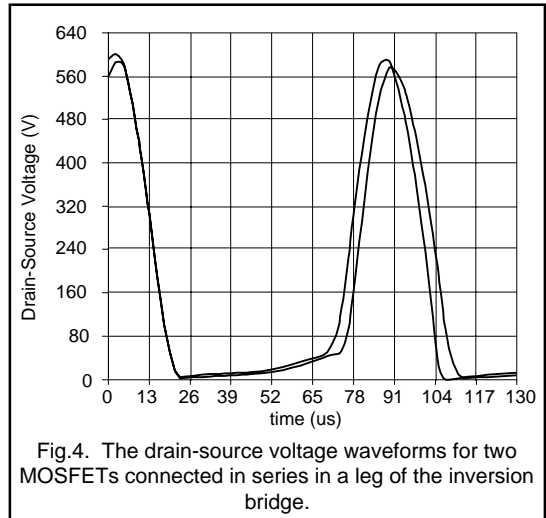


Fig.4. The drain-source voltage waveforms for two MOSFETs connected in series in a leg of the inversion bridge.

can be used as the 'capacitance per MOSFET' in higher power circuits where it becomes necessary to use MOSFETs connected in parallel. A value of between 5 and 10 nF is probably sufficient given a sensible layout.

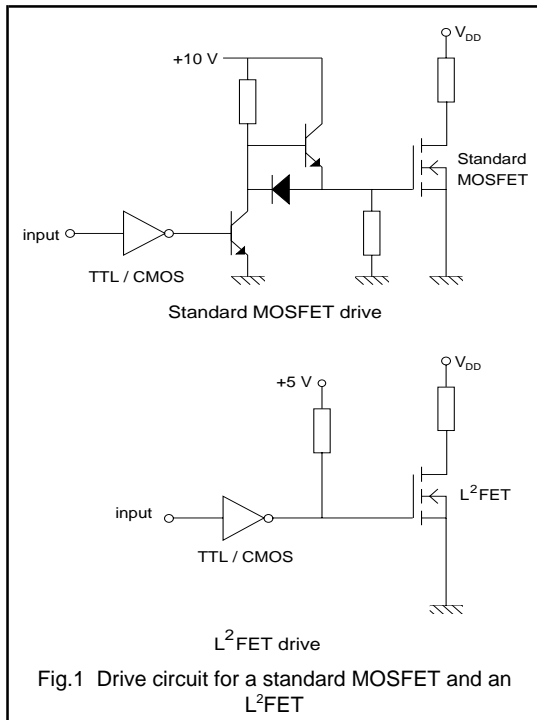
## Conclusions

It has been shown that MOSFETs can be connected in series to realise a switch that is as high as 90% of the sum of the voltage sustaining capabilities of the individual transistors.



## 1.2.6 Logic Level FETs

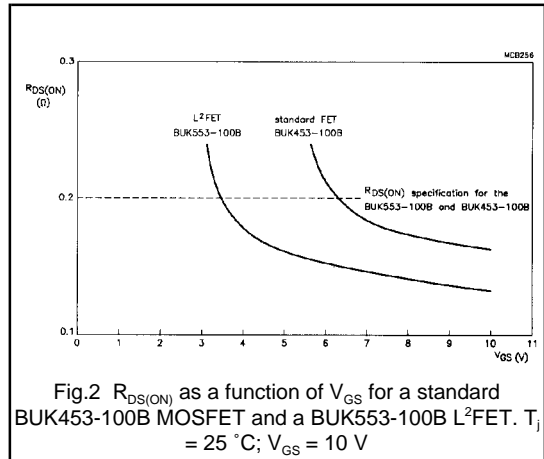
Standard Power MOSFETs require a gate-source voltage of 10 V to be fully ON. With Logic Level FETs ( $L^2$ FETs) however, the same level of conduction is possible with a gate-source voltage of only 5 V. They can, therefore, be driven directly from 5 V TTL/CMOS ICs without the need for the level shifting stages required for standard MOSFETs, see Fig.1. This makes them ideal for today's sophisticated electrical systems, where microprocessors are used to drive switching circuits.



This characteristic of  $L^2$ FETs is achieved by reducing the gate oxide thickness from - 800 Angstroms to - 500 Angstroms, which reduces the threshold voltage of the device from the standard 2.1-4.0 V to 1.0-2.0 V. However the result is a reduction in gate-source voltage ratings, from  $\pm 30$  V for a standard MOSFET to  $\pm 15$  V for the  $L^2$ FET. The  $\pm 15$  V rating is an improvement over the 'industry standard' of  $\pm 10$  V, and permits Philips  $L^2$ FETs to be used in demanding applications such as automotive.

Although a 5 V gate-drive is ideal for  $L^2$ FETs, they can be used in circuits with gate-drive voltages of up to 10 V. Using

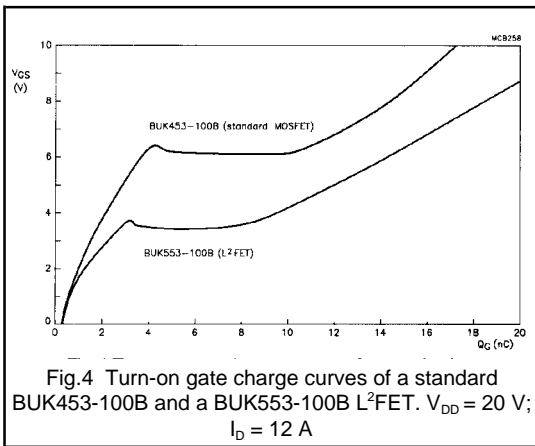
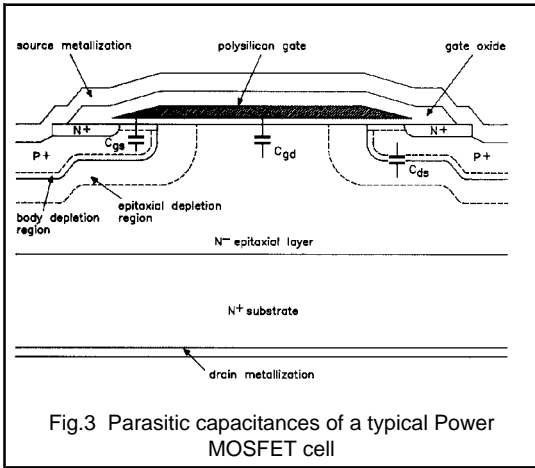
a 10 V gate-drive results in a reduced  $R_{DS(ON)}$  (see Fig.2) but the turn-off delay time is increased. This is due to excessive charging of the  $L^2$ FET's input capacitance.



### Capacitances, Transconductance and Gate Charge

Figure 3 shows the parasitic capacitance areas of a typical Power MOSFET cell. Both the gate-source capacitance  $C_{gs}$  and the gate-drain capacitance  $C_{gd}$  increase due to the reduction in gate oxide thickness, although the increase in  $C_{gd}$  is only significant at low values of  $V_{DS}$ , when the depletion layer is narrow. Increases of the order of 25% in input capacitance  $C_{iss}$ , output capacitance  $C_{oss}$  and reverse transfer capacitance  $C_{rss}$  result for the  $L^2$ FET, compared with a similar standard type, at  $V_{DS} = 0$  V. However at the standard measurement condition of  $V_{DS} = 25$  V the differences are virtually negligible.

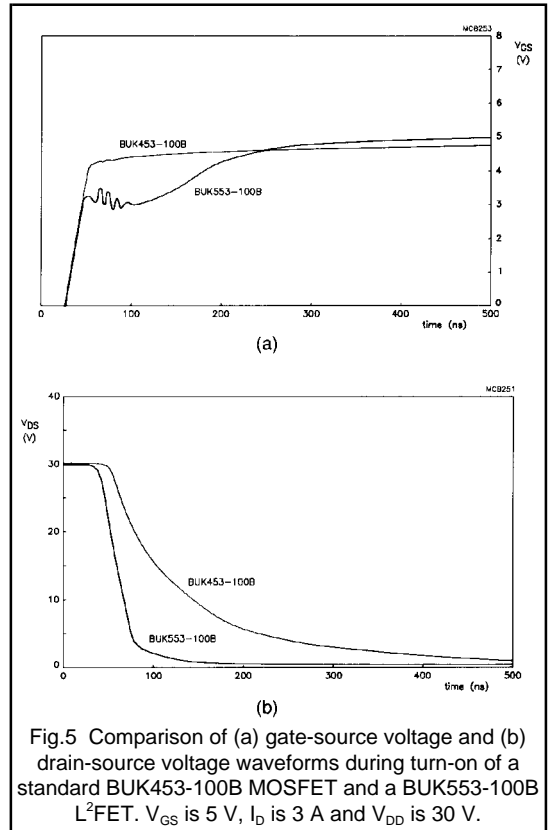
Forward transconductance  $g_{fs}$  is a function of the oxide thickness so the  $g_{fs}$  of an  $L^2$ FET is typically 40% - 50% higher than a standard MOSFET. This increase in  $g_{fs}$  more than offsets the increase in capacitance of an  $L^2$ FET, so the turn on charge requirement of the  $L^2$ FET is lower than the standard type see Fig.4. For example, the standard BUK453-100B MOSFET requires about 17 nC to be fully switched on (at a gate voltage of 10 V) while the BUK553-100B  $L^2$ FET only needs about 12 nC (at a gate source voltage of 5 V).



**Switching speed.**

Figure 5 compares the turn-on performance of the standard BUK453-100B MOSFET and the BUK553-100B L<sup>2</sup>FET, under identical drive conditions of 5 V from a 50 Ω generator using identical loads. Thanks to its lower gate threshold voltage  $V_{GST}$ , the L<sup>2</sup>FET can be seen to turn on in a much shorter time from the low level drive.

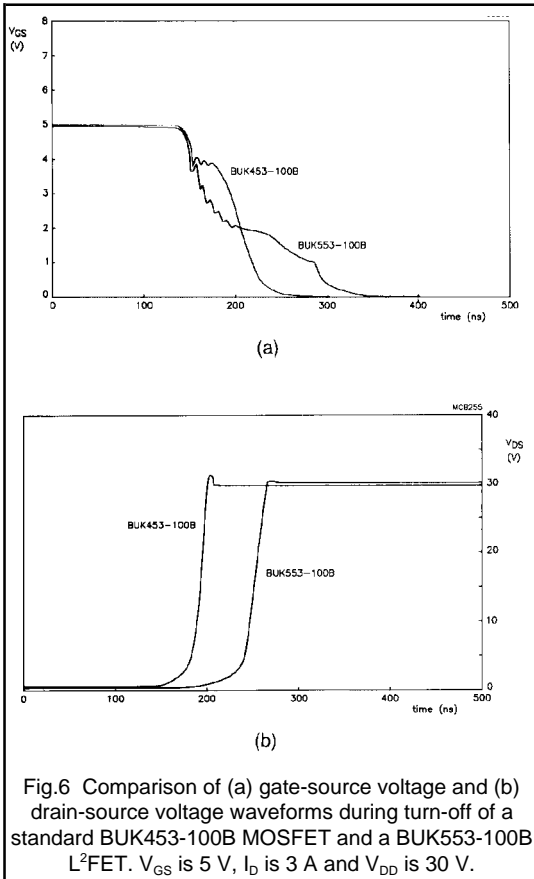
Figure 6 shows the turn-off performance of the standard BUK453-100B MOSFET and the BUK553-100B L<sup>2</sup>FET, again with the same drive. This time the L<sup>2</sup>FET is slower to switch. The turn-off times are determined mainly by the time required for  $C_{gd}$  to discharge. The  $C_{gd}$  is higher for the L<sup>2</sup>FET at low  $V_{DS}$ , and the lower value of  $V_{GST}$  leads to a lower discharging current. The net result is an increase in turn off time.



Fast switching in many applications, for example automotive circuits, is not important. In areas where it is important however the drive conditions should be examined. For example, for a given drive power, a 10 V drive with a 50 Ω source impedance is equivalent to a 5 V drive with a source impedance of only 12 Ω. This results in faster switching for the L<sup>2</sup>FET compared with standard MOSFETs.

**Ruggedness and reliability**

MOSFETs are frequently required to be able to withstand the energy of an unclamped inductive load turn-off. Since this energy is dissipated in the bulk of the silicon, stress is avoided in the gate oxide. This means that the ruggedness performance of L<sup>2</sup>FETs is comparable with that of standard MOSFETs. The use of thinner gate oxide in no way compromises reliability. Good control of key process parameters such as pinhole density, mobile ion content, interface state density ensures good oxide quality. The projected MTBF is 2070 years at 90°C, at a 60% confidence level.



The  $V_{GS}$  rating of an L<sup>2</sup>FET is about half that of a standard MOSFET, but this does not affect the  $V_{DS}$  rating. In principle, an L<sup>2</sup>FET version of any standard MOSFET is feasible.

### Temperature stability

In general threshold voltage decreases with increasing temperature. Although the threshold voltage of L<sup>2</sup>FETs is lower than that of standard MOSFETs, so is their temperature coefficient of threshold voltage (about half in fact), so their temperature stability compares favourably with standard MOSFETs. Philips low voltage L<sup>2</sup>FETs ( $\leq 200V$ ) in TO220 all feature  $T_{jmax}$  of 175°C, rather than the industry standard of 150°C.

### Applications

The Philips Components range of rugged Logic Level MOSFETs enable cost effective drive circuit design without compromising ruggedness or reliability. Since they enable power loads to be driven directly from ICs they may be considered to be the first step towards intelligent power switching. Thanks to their good reliability and 175°C  $T_{jmax}$  temperature rating, they are displacing mechanical relays in automotive body electrical functions and are being designed in to such safety critical areas as ABS.



## 1.2.7 Avalanche Ruggedness

Recent advances in power MOS processing technology now enables power MOS transistors to dissipate energy while operating in the avalanche mode. This feature results in transistors able to survive in-circuit momentary overvoltage conditions, presenting circuit designers with increased flexibility when choosing device voltage grade against required safety margins.

This paper considers the avalanche characteristics of 'rugged' power MOSFETs and presents results from investigations into the physical constraints which ultimately limit avalanche energy dissipation in the VDMOS structure. Results suggest that the maximum sustainable energy is a function of the applied power density waveform, independent of device voltage grade and chip size.

The ability of a rugged device to operate reliably in a circuit subject to extreme interference is also demonstrated.

### Introduction.

Susceptibility to secondary breakdown is a phenomenon which limits the power handling capability of a bipolar transistor to below its full potential. For a power MOSFET, power handling capability is a simple function of thermal resistance and operating temperature since the device is not vulnerable to a second breakdown mechanism. The previous statement holds true provided the device is operated at or below its breakdown voltage rating ( $B_{V_{DSS}}$ ) and not subject to overvoltage. Should the transistor be forced into avalanche by a voltage surge the structure of the device permits possible activation of a parasitic bipolar transistor which may then suffer the consequences of second breakdown. In the past this mechanism was typical of failure in circuits where the device became exposed to overvoltage. To reduce the risk of device failure during momentary overloads improvements have been introduced to the Power MOS design which enable it to dissipate energy while operating in the avalanche condition. The term commonly used to describe this ability is 'Ruggedness', however before discussing in further detail the merits of a rugged Power MOSFET it is worth considering the failure mechanism of non-rugged devices.

### Failure mechanism of a non-rugged Power MOS.

A power MOS transistor is made up of many thousands of cells, identical in structure. The cross section of a typical cell is shown in Fig. 1. When in the off-state or operating in saturation, voltage is supported across the p-n junction as shown by the shaded region. If the device is subjected to over-voltage (greater than the avalanche value of the

device), the peak electric field, located at the p-n junction, rises to the critical value (approx. 200 kV / cm ) at which avalanche multiplication commences.

Computer modelling has shown that the maximum electric field occurs at the corners of the P diffusions. The electron-hole plasma generated by the avalanche process in these regions gives rise to a source of electrons, which are swept across the drain, and a source of holes, which flow through the P- and P regions towards the source metal contact.

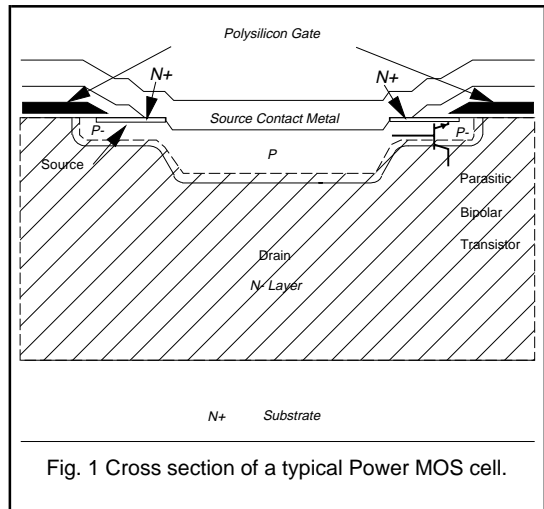


Fig. 1 Cross section of a typical Power MOS cell.

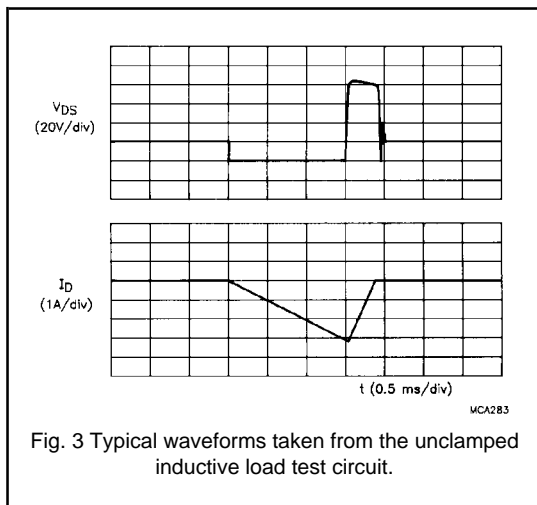
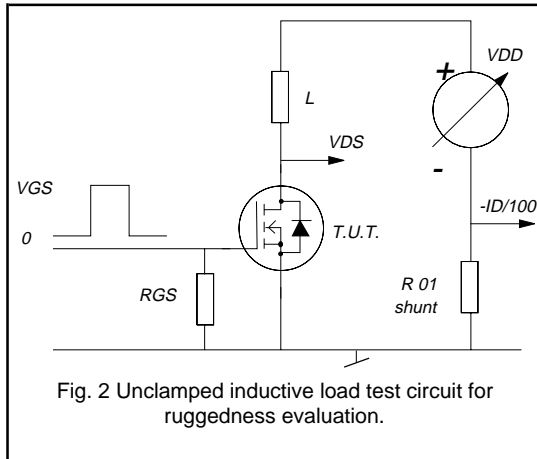
Clearly the P- region constitutes a resistance which will give rise to a potential drop beneath the n+. If this resistance is too large the p-n junction may become forward biased for relatively low avalanche currents.

Also if the manufacturing process does not yield a uniform cell structure across the device or if defects are present in the silicon then multiplication may be a local event within the crystal. This would give rise to a high avalanche current density flowing beneath the source n+ and cause a relatively large potential drop sufficient to forward bias the p-n junction and hence activate the parasitic npn bipolar transistor inherent in the MOSFET structure. Due to the positive temperature coefficient associated with a forward biased p-n junction, current crowding will rapidly ensue with the likely result of second breakdown and eventual device destruction.

In order that a power MOS transistor may survive transitory excursions into avalanche it is necessary to manufacture a device with uniform cell structure, free from defects throughout the crystal and that within the cell the resistance beneath the n+ should be kept to a minimum. In this way a forward biasing potential across the p-n junction is avoided.

### Definition of ruggedness.

The term 'Ruggedness' when applied to a power MOS transistor, describes the ability of that device to dissipate energy while operating in the avalanche condition. To test ruggedness of a device it is usual to use the method of unclamped inductive load turn-off using the circuit drawn in Fig. 2.



### Circuit operation:-

A pulse is applied to the gate such that the transistor turns on and load current ramps up according to the inductor value, L and drain supply voltage,  $V_{DD}$ . At the end of the gate pulse, channel current in the power MOS begins to fall while voltage on the drain terminal rises rapidly in accordance with equation 1.

$$\frac{dv}{dt} = L \frac{d^2I}{dt^2} \quad (1)$$

The voltage on the drain terminal is clamped by the avalanche voltage of the Power MOS for a duration equal to that necessary for dissipation of all energy stored in the inductor. Typical waveforms showing drain voltage and source current for a device undergoing successful test are shown in Fig. 3.

The energy stored in the inductor is given by equation 2 where  $I_D$  is the peak load current at the point of turn-off of the transistor.

$$W_{DSS} = 0.5LI_D^2 \quad (2)$$

All this energy is dissipated by the Power MOS while the device is in avalanche.

Provided the supply rail is kept below 50 % of the avalanche voltage, equation 2 approximates closely to the total energy dissipation by the device during turn-off. However a more exact expression which takes account of additional energy delivered from the power supply is given by equation 3.

$$W_{DSS} = \frac{BV_{DSS}}{BV_{DSS} - V_{DD}} 0.5LI_D^2 \quad (3)$$

Clearly the energy dissipated is a function of both the inductor value and the load current  $I_D$ , the latter being set by the duration of the gate pulse. The 50 Ohm resistor between gate and source is necessary to ensure a fast turn-off such that the device is forced into avalanche.

The performance of a non-rugged device in response to the avalanche test is shown in Fig. 4. The drain voltage rises to the avalanche value followed by an immediate collapse to approximately 30 V. This voltage is typical of the sustaining voltage during Second Breakdown of a bipolar transistor, [1]. The subsequent collapse to zero volts after 12  $\mu$ S signifies failure of the device. The transistor shown here was only able to dissipate a few micro joules at a very low current if a failure of this type was to be avoided.

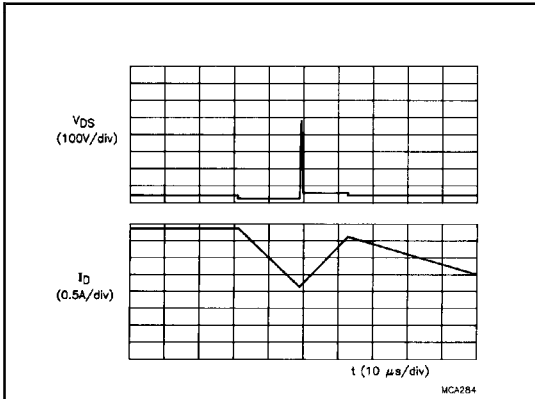


Fig. 4 Failure waveforms of a non rugged Power MOS transistor.

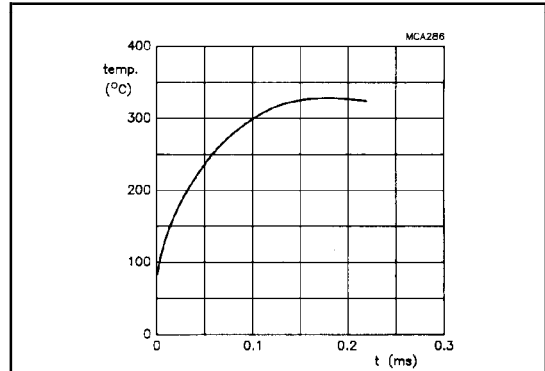


Fig. 6 Junction temperature during the power pulse for the avalanche ruggedness test on a Philips BUK627-500B.

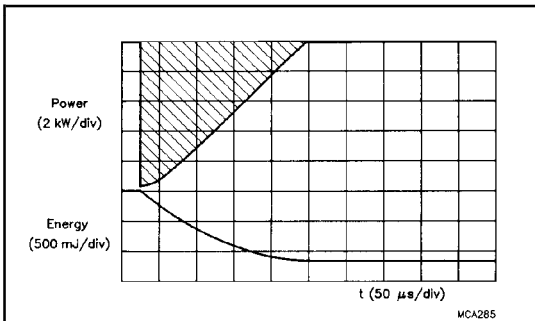


Fig. 5 Power and energy waveforms prior to failure for a typical BUK627-500B

Equation 4 predicts that the junction temperature will pass through a maximum of 325 °C during the test. The calculation of  $Z_{th}(t)$  assumes that the power dissipation is uniform across the active area of the device. When the device operates in the avalanche mode the power will be dissipated more locally in the region of the p-n junction where the multiplication takes place. Consequently a local temperature above that predicted by equation 4 is likely to be present within the device.

Work on bipolar transistors [2] has shown that at a temperature of the order of 400 °C, the voltage supporting p-n region becomes effectively intrinsic as a result of thermal multiplication, resulting in a rapid collapse in the terminal voltage. It is probable that a similar mechanism is responsible for failure of the Power MOS with a local temperature approaching 400 °C resulting in a device short circuit. A subsequent rapid rise in internal temperature will result in eventual device destruction.

Clearly the rise in  $T_j$  is a function of the applied power waveform which is in turn related to circuit current, avalanche voltage of the device and duration of the energy pulse. Thus the energy required to bring about device failure will vary as a function of each of these parameters. The ruggedness of Power MOSFETS of varying crystal size and voltage specification together with dependence on circuit current is considered below.

**Characteristics of a rugged Power MOS.**

**i) The energy limitation of a rugged device**

The power waveform for a BUK627-500B (500 V, 0.8 Ohm) tested at a peak current of 15 A is presented in Fig. 5.

The area within the triangle represents the maximum energy that this particular device type may sustain without failure at the above current. Figure 6 shows the junction temperature variation in response to the power pulse, calculated from the convolution integral as shown in equation 4.

$$T_j(t) = \int_{\tau=0}^{\tau=t} P(t - \tau)Z_{th}(\tau)d\tau \quad (4)$$

where  $Z_{th}(\tau)$  = transient thermal impedance.

**ii) Sustainable avalanche energy as a function of current.**

The typical avalanche energy required to cause device failure is plotted as a function of peak current in Fig. 7 for a BUK553-60A (60 V, 0.085 Ohm Logic Level device). This result was obtained through destructive device testing using the circuit of Fig. 2 and a variety of inductor values.

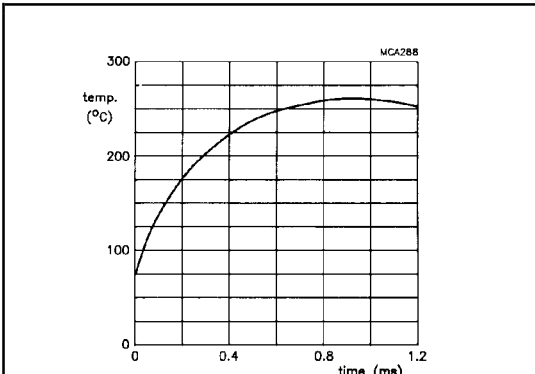
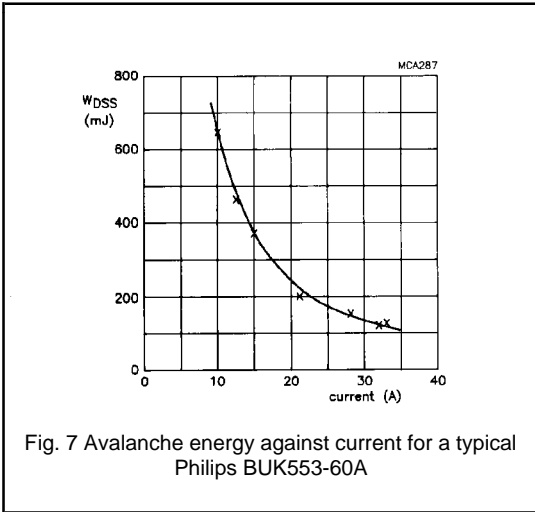


Fig. 8(a) Temperature during avalanche test for a BUK553-60A; ID = 10 A

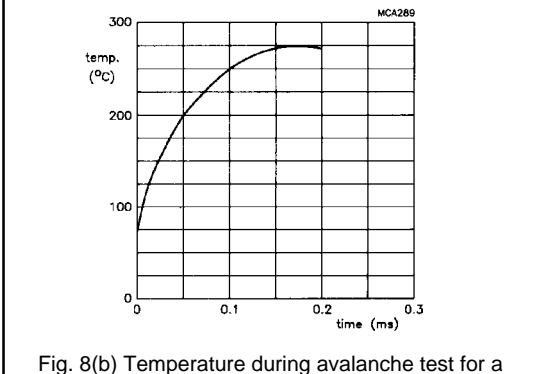


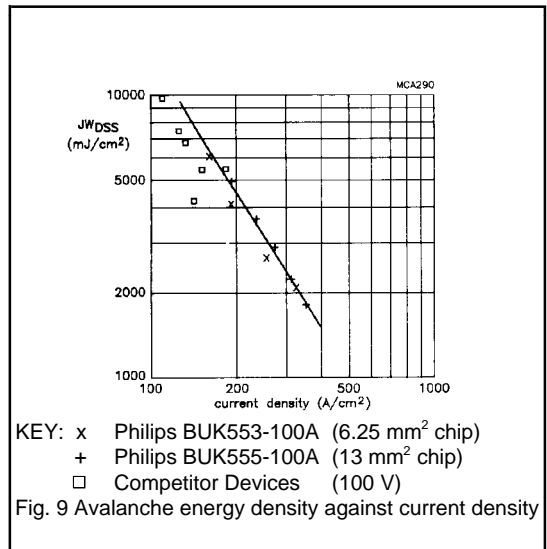
Fig. 8(b) Temperature during avalanche test for a BUK553-60A; ID = 22 A

The plot shows that the effect of reducing current is to permit greater energy dissipation during avalanche prior to failure. This is an expected result since lower currents result in reduced power dissipation enabling avalanche to be sustained over a longer period. Temperature plots (Fig. 8) calculated for the 10 A and 22 A failure points confirm that the maximum junction temperature reached in each case is the same despite the different energy values. (N.B. The critical temperature is again underestimated as previously stated.)

**iii) Effect of crystal size.**

To enable a fair comparison of ruggedness between devices of various chip size it is necessary to normalise the results. Therefore instead of plotting avalanche energy against current, avalanche energy density and current density become more appropriate axes. Figure 9 shows the avalanche energy density against current density failure locus for two 100 V Philips Power MOS types which are different only in silicon area. Also shown on this plot are two competitor devices of different chip areas (B<sub>VDSS</sub> = 100 V). This result demonstrates two points:

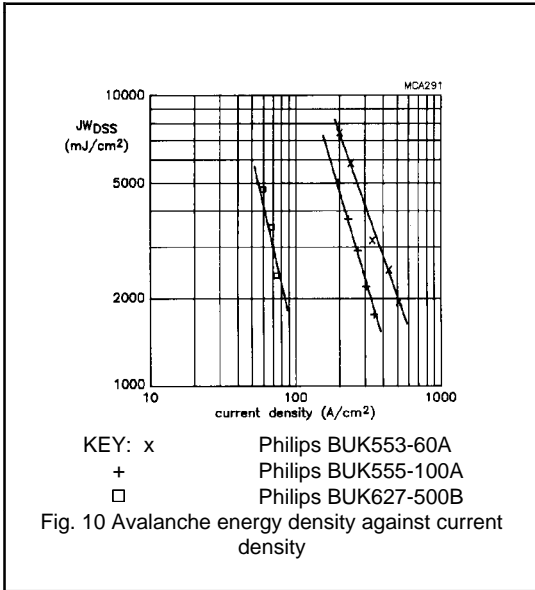
- a) the rise in T<sub>j</sub> to the critical value for failure is dependent on the power density dissipated within the device as a function of time,
- b) the sustainable avalanche energy scales proportional to chip size.



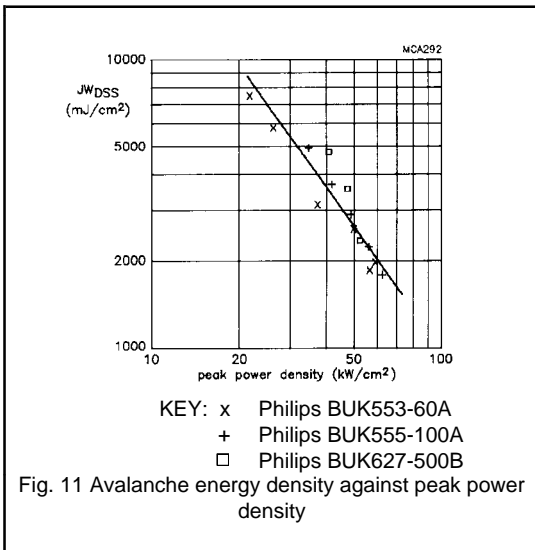
**iv) Dependence on the drain source breakdown voltage rating.**

Energy density against current density failure loci are shown for devices of several different breakdown voltages in Fig. 10.





Presented in this form it is difficult to assess the relative ruggedness of each device since the current density is reduced for increasing voltage. If instead of peak current density, peak power density is used for the x-axis then comparison is made very simple. The data of Fig. 10 has been replotted in Fig. 11 in the above manner. Represented in this fashion the ruggedness of each chip appears very similar highlighting that the maximum energy dissipation of a device while in avalanche is dependent only on the power density function.



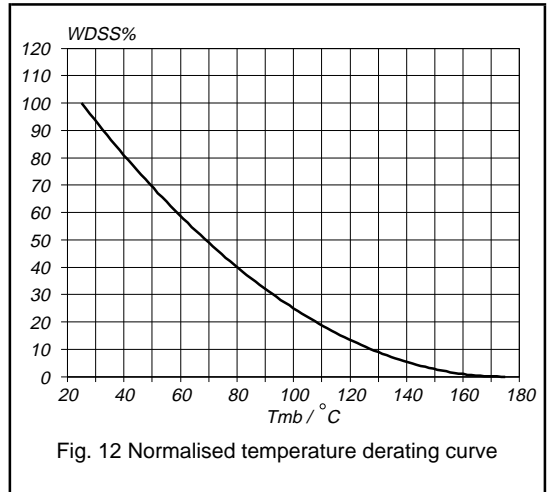
### Ruggedness ratings.

It should be stressed that the avalanche energies presented in the previous section result in a rise of the junction temperature far in excess of the device rating and in practice energies should be kept within the specification. Ruggedness is specified in data for each device in terms of an unclamped inductive load test maximum condition; recommended energy dissipation at a particular current (usually the rated current of the device).

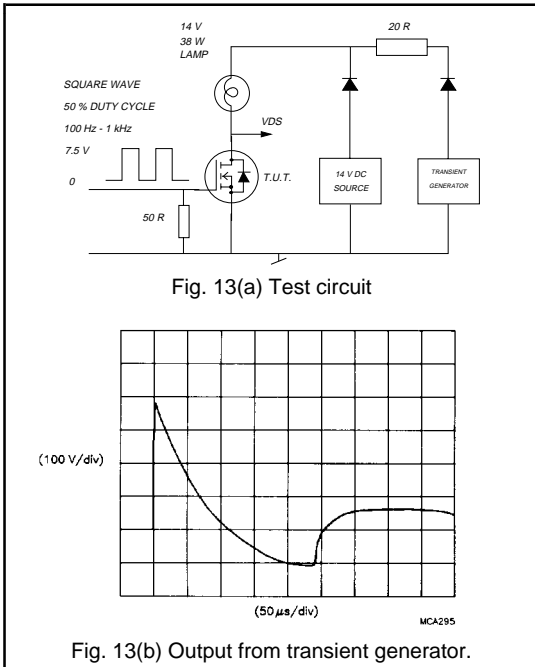
DEVICE	$R_{DS(on)}$	$V_{DS}$	$I_D$	$W_{DSS}$
TYPE	( $\Omega$ )	(V)	(A)	(mJ)
BUK552-60A	0.15	60	14	30
BUK552-100A	0.28	100	10	30
BUK553-60A	0.085	60	20	45
BUK553-100A	0.18	100	13	70

Table 1 Ruggedness Ratings

The ruggedness rating is chosen to protect against a rise in  $T_j$  above the maximum rating. Examples of ruggedness ratings for a small selection of devices are shown in Table 1.



This data is applicable for  $T_j = 25$  C. For higher operating temperatures the permissible rise in junction temperature during the energy test is reduced. Consequently ruggedness needs to be derated with increasing operating temperature. A normalised derating curve for devices with  $T_j$  max 175 °C is presented in Fig. 12.



**Performance of a rugged Power MOS device.**

The ability of a rugged Power MOS transistor to survive momentary power surges results in excellent device reliability. The response of a BUK553-60A to interference spikes while switching a load is presented below. The test

circuit is shown in Fig. 13(a) together with the profile of the interference spike in Fig. 13(b).

The interference generator produces pulses asynchronous to the switching frequency of the Power MOS. Figure 14 shows the drain voltage and load current response at four instances in the switching cycle. Devices were subjected to 5000 interference spikes at a frequency of 5 Hz. No degradation in device performance was recorded.

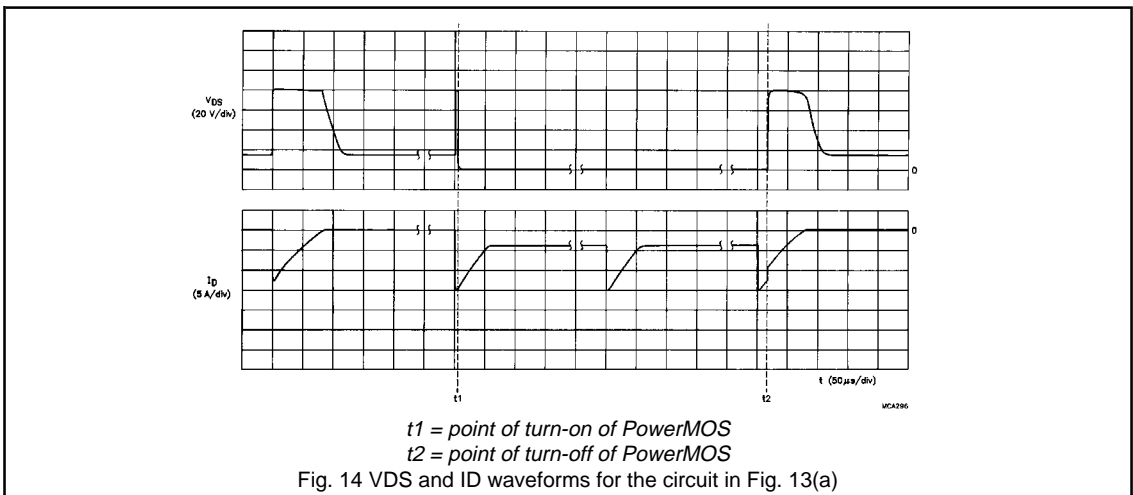
**Conclusions.**

The ability of power MOS devices to dissipate energy in the avalanche mode has been made possible by process optimisation to remove the possibility of turn-on of the parasitic bipolar structure. The failure mechanism of a rugged device is one of excessive junction temperature initiating a collapse in the terminal voltage as the junction area becomes intrinsic. The rise in junction temperature is dictated by the power density dissipation which is a function of crystal size, breakdown voltage and circuit current.

Ruggedness ratings for Philips PowerMOS are chosen to ensure that the specified maximum junction temperature of the device is not exceeded.

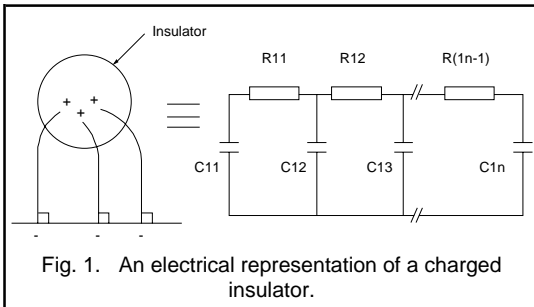
**References.**

1. DUNN and NUTTALL, An investigation of the voltage sustained by epitaxial bipolar transistors in current mode second breakdown. Int.J.Electronics, 1978, vol.45, no.4, 353-372
2. DOW and NUTTALL, A study of the current distribution established in npn epitaxial transistors during current mode second breakdown. Int.J.Electronics, 1981, vol.50, no.2, 93-108



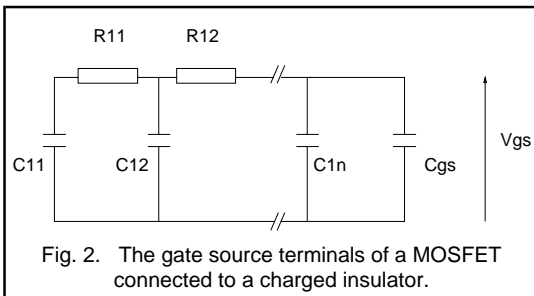
## 1.2.8 Electrostatic Discharge (ESD) Considerations

Charge accumulates on insulating bodies and voltages as high as 20,000 V can be developed by, for example, walking across a nylon carpet. Electrically the insulator can be represented by many capacitors and resistors connected as shown in Fig. 1. The value of the resistors is large and as a consequence it is not possible to discharge an insulator by connecting it straight to ground. An ion source is necessary to discharge an insulator.



Since MOSFETs have a very high input impedance, typically  $> 10^9$  Ohms at dc, there is a danger of static electricity building up on the gate source capacitance of the MOSFET. This can lead to damage of the thin gate oxide. There are two ways in which the voltage across the gate source terminals of a MOSFET can be increased to its breakdown voltage by static electricity.

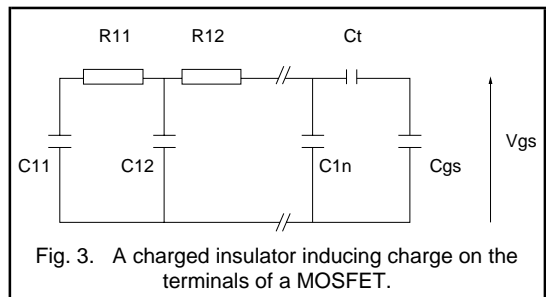
Firstly a charged object can be brought into contact with the MOSFET terminals or with tracks electrically connected to the terminals. This is represented electrically by Fig. 2. Secondly charge can be induced onto the terminals of the MOSFET. Electrically this can be represented by the circuit in Fig. 3.



From Figs. 2 and 3, it can be seen that, as the total area of the gate source region increases then the sensitivity of the devices to ESD will decrease. Hence power MOSFETs are less prone to ESD than CMOS ICs. Also, for a given

voltage rating, MOSFETs with a larger die area (i.e. the devices with lower on-resistance) are less prone to ESD than smaller dice.

To prevent the destruction of MOSFETs through ESD a two pronged approach is necessary. Firstly it is important to minimise the build up of static electricity. Secondly measures need to be taken to prevent the charging up of the input capacitance of MOSFETs by static electric charges.



In the Philips manufacturing facilities many precautions are taken to prevent ESD damage and these are summarised below.

### Precautions taken to prevent the build up of static electricity

1. It is important to ensure that personnel working with MOSFETs are aware of the problems and procedures that have to be followed. This involves the training of staff. Areas in which MOSFETs are handled are designated Special Handling Areas (SHA) and are clearly marked as such. Checks are made every month that anti-static rules are being rigorously implemented.
2. Some materials are more prone to the build up of static electricity than others (e.g. polyester is worse than cotton). Therefore it is important to minimise the use of materials that enhance the likelihood of build up of static electricity. Materials best avoided are acetate, rayon and polyester. The wearing of overclothing made from polycotton with 1% stainless steel fibre is one solution. In clean rooms nylon overalls which have been antistatically treated are worn. The use of insulating materials is avoided.
3. Work benches and floors are covered in a static dissipative material and connected to a common earth. A high conductive material is not used since it would create an electric shock hazard and cause too rapid a discharge of charged material. From the point of view of ESD materials can be classified according to their conductivity as shown below.

insulator ( $>10^{14}$  ohm/square)

antistatic ( $10^9 - 10^{14}$  Ohm/square)

static dissipative ( $10^5 - 10^9$  Ohm/square)

conductor ( $<10^5$  Ohm/square).

4. Conducting straps are used to electrically connect personnel to the point of common earthing. This prevents the build up of static charge on staff. The connection is static dissipative to prevent an electric shock hazard.

5. Air plays an important part in the build up of static electricity.

This is particularly troublesome in a dry atmosphere.

Many of the techniques mentioned above are referred to in BS5783.

### **Precautions taken to prevent damage to MOSFETs by electrostatic build up of charge**

1. When MOSFETs are being transported or stored they

should be in antistatic containers. These containers should be totally enclosed to prevent charges being induced onto the terminals of devices.

2. If MOSFETs have to be left out on the bench, e.g. during a test sequence, they should be in sockets which have the gate and source pins electrically connected together.

The precautions that should be taken at the customers' premises are the same as above. It should be remembered that whenever a MOSFET is touched by someone there is a danger of damage. The precautions should be taken in every area in which MOSFETs are tested or handled. In addition where devices are soldered into circuits with a soldering iron an earthed bit should always be used.

The probability of device destruction caused by ESD is low even if only the most rudimentary precautions are taken. However without such precautions and with large numbers of PowerMOS devices now being designed into equipment a few failures would be inevitable. The adoption of the precautions outlined will mean that ESD will no longer be a problem.

## 1.2.9 Understanding the Data Sheet: PowerMOS

All manufacturers of power MOSFETs provide a data sheet for every type produced. The purpose of the data sheet is primarily to give an indication as to the capabilities of a particular product. It is also useful for the purpose of selecting device equivalents between different manufacturers. In some cases however data on a number of parameters may be quoted under subtly different conditions by different manufacturers, particularly on second order parameters such as switching times. In addition the information contained within the data sheet does not always appear relevant for the application. Using data sheets and selecting device equivalents therefore requires caution and an understanding of exactly what the data means and how it can be interpreted. Throughout this chapter the BUK553-100A is used as an example, this device is a 100 V logic level MOSFET.

### Information contained in the Philips data sheet

The data sheet is divided into 8 sections as follows:

- \* Quick reference data
- \* Limiting values
- \* Thermal resistances
- \* Static characteristics
- \* Dynamic characteristics
- \* Reverse diode limiting values and characteristics
- \* Avalanche limiting value
- \* Graphical data

The information contained within each of these sections is now described.

### Quick reference data

This data is presented for the purpose of quick selection. It lists what is considered to be the key parameters of the device such that a designer can decide at a glance whether the device is likely to be the correct one for the application or not. Five parameters are listed, the two most important are the drain-source voltage  $V_{DS}$  and drain-source on-state resistance,  $R_{DS(ON)}$ .  $V_{DS}$  is the maximum voltage the device will support between drain and source terminals in the off-state.  $R_{DS(ON)}$  is the maximum on-state resistance at the quoted gate voltage,  $V_{GS}$ , and a junction temperature of 25 °C. (NB  $R_{DS(ON)}$  is temperature dependent, see static characteristics). It is these two parameters which provide a first order indication of the devices capability.

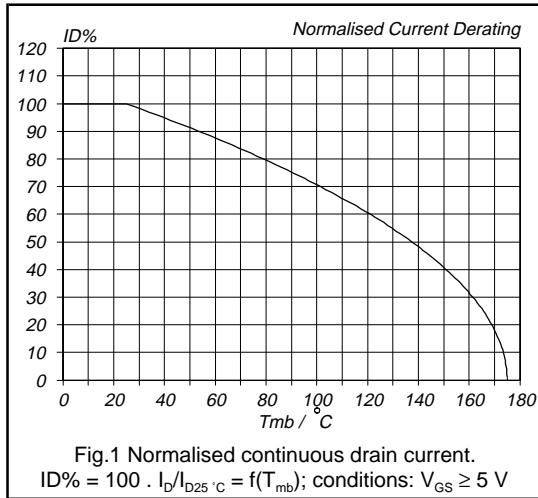
A drain current value ( $I_D$ ) and a figure for total power dissipation are also given in this section. These figures should be treated with caution since they are quoted for conditions that are rarely attainable in real applications. (See limiting values.) For most applications the usable dc current will be less than the quoted figure in the quick reference data. Typical power dissipations that can be tolerated by the majority of designers are less than 20 W (for discrete devices), depending on the heatsinking arrangement used. The junction temperature ( $T_J$ ) is usually given as either 150 °C or 175 °C. It is not recommended that the internal device temperature be allowed to exceed this figure.

### Limiting values

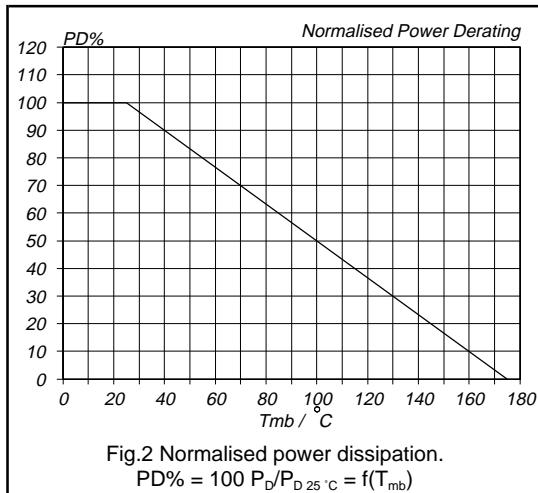
This table lists the absolute maximum values of six parameters. The device may be operated right up to these maximum levels however they must not be exceeded, to do so may incur damage to the device.

Drain-source voltage and drain-gate voltage have the same value. The figure given is the maximum voltage that may be applied between the respective terminals. Gate-source voltage,  $\pm V_{GS}$ , gives the maximum value that may be allowed between the gate and source terminals. To exceed this voltage, even for the shortest period can cause permanent damage to the gate oxide. Two values for the dc drain current,  $I_D$ , are quoted, one at a mounting base temperature of 25 °C and one at a mounting base temperature of 100 °C. Again these currents do not represent attainable operating levels. These currents are the values that will cause the junction temperature to reach its maximum value when the mounting base is held at the quoted value. The maximum current rating is therefore a function of the mounting base temperature and the quoted figures are just two points on the derating curve, see Fig. 1.

The third current level quoted is the pulse peak value,  $I_{DM}$ . PowerMOS devices generally speaking have a very high peak current handling capability. It is the internal bond wires which connect to the chip that provide the final limitation. The pulse width for which  $I_{DM}$  can be applied depends upon the thermal considerations (see section on calculating currents.) The total power dissipation,  $P_{tot}$ , and maximum junction temperature are also stated as for the quick reference data. The  $P_{tot}$  figure is calculated from the simple quotient given in equation 1 (see section on safe operating area). It is quoted for the condition where the mounting base temperature is maintained at 25 °C. As an example, for the BUK553-100A the  $P_{tot}$  figure is 75 W, dissipating this amount of power while maintaining the mounting base at 25 °C would be a challenge! For higher mounting base temperatures the total power that can be dissipated is less.



Obviously if the mounting base temperature was made equal to the max permitted junction temperature, then no power could be dissipated internally. A derating curve is given as part of the graphical data, an example is shown in Fig.2 for a device with a limiting  $T_j$  of 175 °C.



Storage temperature limits are also quoted, usually between -40 /-55 °C and +150 /+175 °C. Both the storage temperature limits and the junction temperature limit are figures at which extensive reliability work is performed by our Quality department. To exceed these figures will cause a reduction in long-term reliability.

## Thermal resistance.

For non-isolated packages two thermal resistance values are given. The value from junction to mounting base ( $R_{thj-mb}$ ) indicates how much the junction temperature will be raised above the temperature of the mounting base when dissipating a given power. Eg a BUK553-100A has a  $R_{thj-mb}$  of 2 K/W, dissipating 10 W, the junction temperature will be 20 °C above the temperature of its mounting base. The other figure quoted is from junction to ambient. This is a much larger figure and indicates how the junction temperature will rise if the device is NOT mounted on a heatsink but operated in free air. Eg for a BUK553-100A,  $R_{thj-a} = 60 K/W$ , dissipating 1 W while mounted in free air will produce a junction temperature 60 °C above the ambient air temperature.

For isolated packages, (F-packs) the mounting base (the metal plate upon which the silicon chip is mounted) is fully encapsulated in plastic. Therefore it is not possible to give a thermal resistance figure junction to mounting base. Instead a figure is quoted from junction to heatsink,  $R_{thj-hs}$ , which assumes the use of heatsink compound. Care should be taken when comparing thermal resistances of isolated and non-isolated types. Consider the following example:

The non-isolated BUK553-100A has a  $R_{thj-mb}$  of 2 K/W. The isolated BUK543-100A has a  $R_{thj-hs}$  of 5 K/W. These devices have identical crystals but mounted in different packages. At first glance the non-isolated type might be expected to offer much higher power (and hence current) handling capability. However for the BUK553-100A the thermal resistance junction to heatsink has to be calculated, this involves adding the extra thermal resistance between mounting base and heatsink. For most applications some isolation is used, such as a mica washer. The thermal resistance mounting base to heatsink is then of the order 2 K/W. The total thermal resistance junction to heatsink is therefore

$$R_{thj-hs} \text{ (non isolated type)} = R_{thj-mb} + R_{thmb-hs} = 4 K/W$$

It can be seen that the real performance difference between the isolated and non isolated types will not be significant.

## Static Characteristics

The parameters in this section characterise breakdown voltage, threshold voltage, leakage currents and on-resistance.

A drain-source breakdown voltage is specified as greater than the limiting value of drain-source voltage. It can be measured on a curve tracer, with gate terminal shorted to the source terminal, it is the voltage at which a drain current of 250  $\mu A$  is observed. Gate threshold voltage,  $V_{GS(FTO)}$ , indicates the voltage required on the gate (with respect to the source) to bring the device into its conducting state. For logic level devices this is usually between 1.0 and 2.0 V and for standard devices between 2.1 and 4 V.

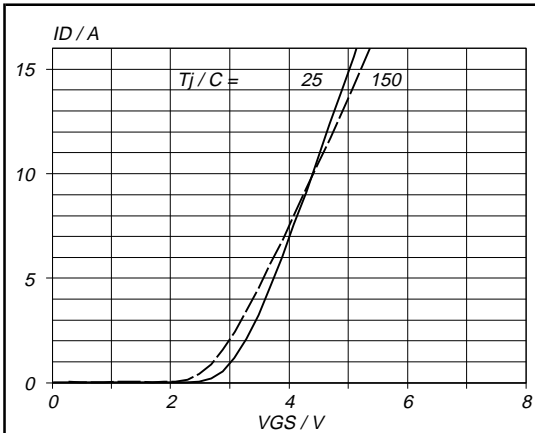


Fig.3 Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25\text{ V}$ ; parameter  $T_j$

Useful plots in the graphical data are the typical transfer characteristics (Fig.3) showing drain current as a function of  $V_{GS}$  and the gate threshold voltage variation with junction temperature (Fig.4). An additional plot also provided is the sub-threshold conduction, showing how the drain current varies with gate-source voltage below the threshold level (Fig.5).

Off-state leakage currents are specified for both the drain-source and gate-source under their respective maximum voltage conditions. Note, although gate-source leakage current is specified in nano-amperes, values are typically of the order of a few pico-amperes.

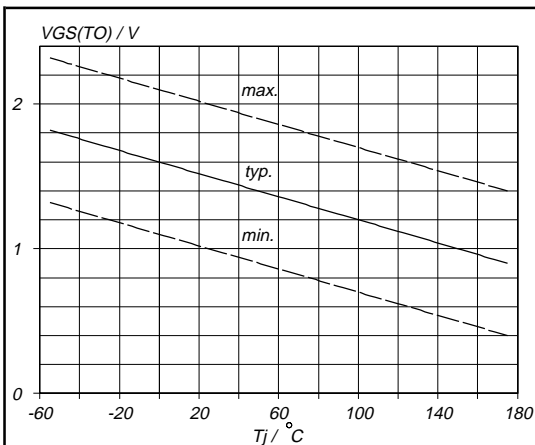


Fig.4 Gate threshold voltage.  
 $V_{GS(T_0)} = f(T_j)$ ; conditions:  $I_D = 1\text{ mA}$ ;  $V_{DS} = V_{GS}$

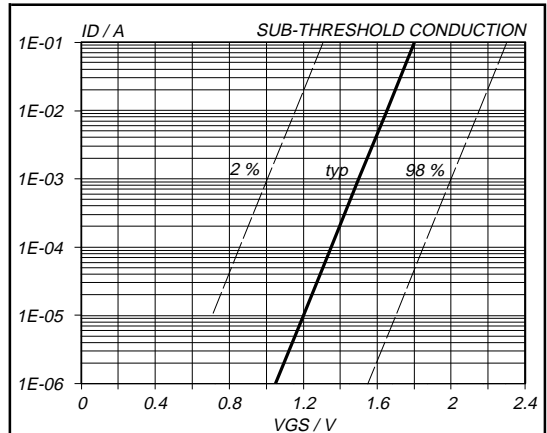


Fig.5 Sub-threshold drain current.  
 $I_D = f(V_{GS})$ ; conditions:  $T_j = 25\text{ °C}$ ;  $V_{DS} = V_{GS}$

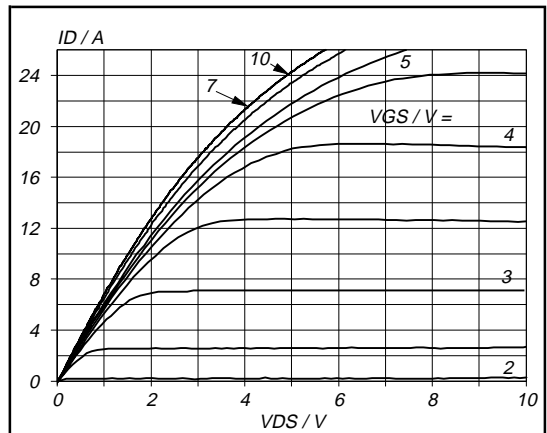
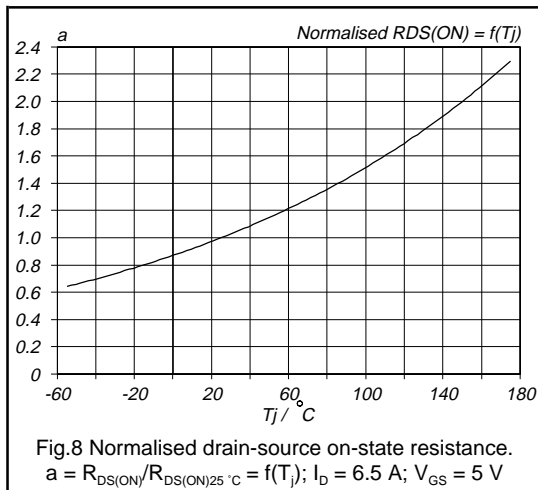
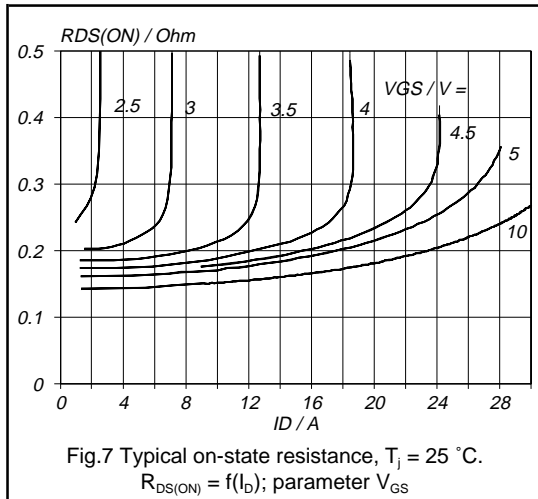


Fig.6 Typical output characteristics,  $T_j = 25\text{ °C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{GS}$

The drain-source on-resistance is very important. It is specified at a gate-source voltage of 5 V for logic level FETs and 10 V for a standard device. The on-resistance for a standard MOSFET cannot be reduced significantly by increasing the gate source voltage above 10 V. Reducing the gate voltage will however increase the on-resistance. For the logic level FET, the on-resistance is given for a gate voltage of 5 V, a further reduction is possible however at gate voltages up to 10 V, this is demonstrated by the output characteristics, Fig.6 and on-resistance characteristics, Fig.7 for a BUK553-100A. .

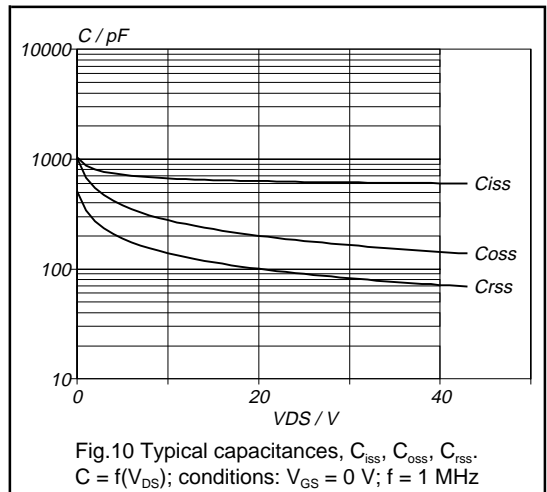
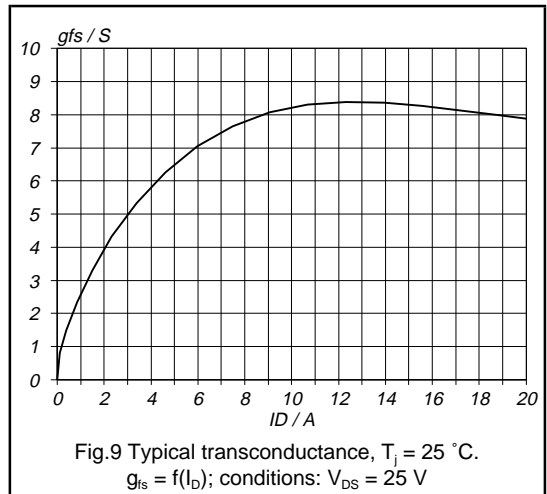
The on-resistance is a temperature sensitive parameter, between 25 °C and 150 °C it approximately doubles in value. A plot of normalised  $R_{DS(ON)}$  versus temperature (Fig.8) is included in each data sheet. Since the MOSFET will normally operate at a  $T_j$  higher than 25 °C, when making estimates of power dissipation in the MOSFET, it is important to take into account the higher  $R_{DS(ON)}$ .



**Dynamic Characteristics**

These include transconductance, capacitance and switching times. Forward transconductance,  $g_{fs}$ , is essentially the gain parameter which indicates the change in drain current that will result from a fluctuation in gate voltage when the device is saturated. (NB saturation of a

MOSFET refers to the flat portion of the output characteristics.) Fig.9 shows how  $g_{fs}$  varies as a function of the drain current for a BUK553-100A.

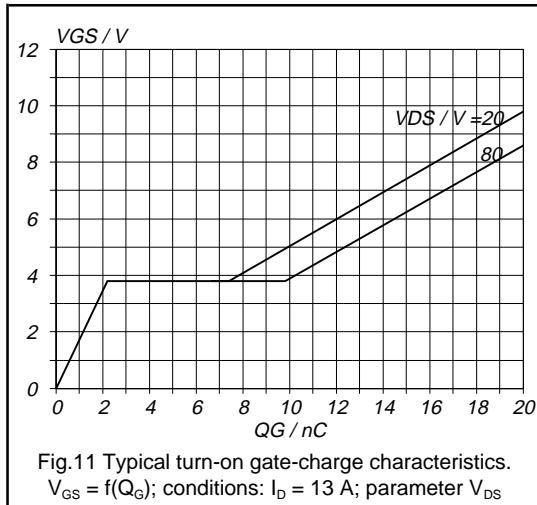


Capacitances are specified by most manufacturers, usually in terms of input, output and feedback capacitance. The values quoted are for a drain-source voltage of 25 V. However this is only part of the story as the MOSFET capacitances are strongly voltage dependent, increasing as drain-source voltage is reduced. Fig.10 shows how these capacitances vary with voltage. The usefulness of the capacitance figures is limited. The input capacitance value gives only a rough indication of the charging required by the drive circuit. Perhaps more useful is the gate charge information an example of which is shown in Fig.11. This plot shows how much charge has to be input to the gate to



reach a particular gate-source voltage. Eg. to charge a BUK553-100A to  $V_{GS} = 5\text{ V}$ , starting from a drain-source voltage of  $80\text{ V}$ , requires  $12.4\text{ ns}$ . The speed at which this charge is to be applied will give the gate circuit current requirements. More information on MOSFET capacitance is given in chapter 1.2.2.

Resistive load switching times are also quoted by most manufacturers, however extreme care should be taken when making comparisons between different manufacturers data. The speed at which a power MOSFET can be switched is essentially limited only by circuit and package inductances. The actual speed in a circuit is determined by how fast the internal capacitances of the MOSFET are charged and discharged by the drive circuit. The switching times are therefore extremely dependent on the circuit conditions employed; a low gate drive resistance will provide for faster switching and vice-versa. The Philips data sheet presents the switching times for all PowerMOS with a resistor between gate and source of  $50\ \Omega$ . The device is switched from a pulse generator with a source impedance also of  $50\ \Omega$ . The overall impedance of the gate drive circuit is therefore  $25\ \Omega$ .

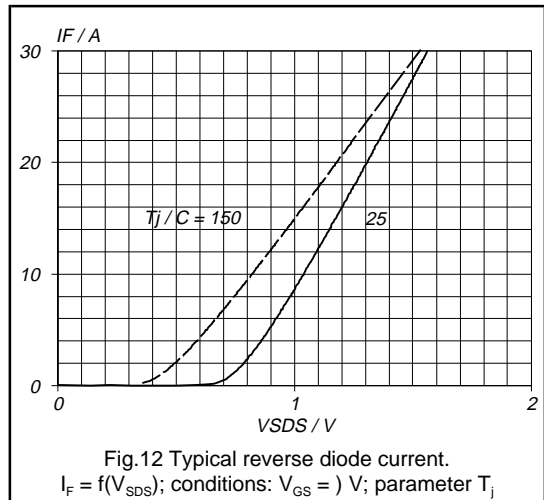


Also presented under dynamic characteristics are the typical inductances of the package. These inductances become important when very high switching speeds are employed such that large  $di/dt$  values exist in the circuit. Eg. turning-on  $30\text{ A}$  within  $60\text{ ns}$  gives a  $di/dt$  of  $0.5\text{ A/ns}$ . The typical inductance of the source lead is  $7.5\text{ nH}$ , from  $V = -L \cdot di/dt$  the potential drop from the source bond pad (point where the source bond wire connects to the chip internally) to the bottom of the source lead would be  $3.75\text{ V}$ . Normally a standard device will be driven with a gate-source voltage of  $10\text{ V}$  applied across the gate and source terminals, the actual voltage gate to source on the

semiconductor however would only be  $6.25\text{ V}$  during the turn-on period! The switching speed is therefore ultimately limited by package inductance.

## Reverse diode limiting values and characteristics

The reverse diode is inherent in the vertical structure of the power MOSFET. In some circuits this diode is required to perform a useful function. For this reason the characteristics of the diode are specified. The forward currents permissible in the diode are specified as 'continuous reverse drain current' and 'pulsed reverse drain current'. The forward voltage drop of the diode is also provided together with a plot of the diode characteristic, Fig.12. The switching capability of the diode is given in terms of the reverse recovery parameters,  $t_{rr}$  and  $Q_{rr}$ .



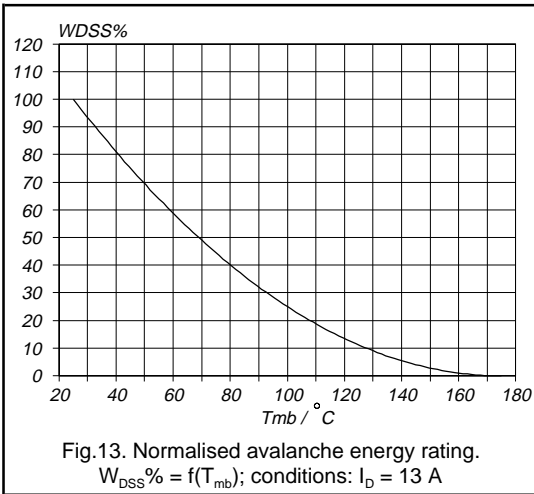
Because the diode operates as a bipolar device it is subject to charge storage effects. This charge must be removed for the diode to turn-off. The amount of charge stored is given by  $Q_{rr}$ , the reverse recovery charge, the time taken to extract the charge is given by  $t_{rr}$ , the reverse recovery time. NB.  $t_{rr}$  depends very much on the  $-di/dt$  in the circuit,  $t_{rr}$  is specified in data at  $100\text{ A}/\mu\text{s}$ .

## Avalanche limiting value

This parameter is an indication as to the ruggedness of the product in terms of its ability to handle a transient overvoltage, ie the voltage exceeds the drain-source voltage limiting value and causes the device to operate in an avalanche condition. The ruggedness is specified in terms of a drain-source non-repetitive unclamped inductive turn-off energy at a mounting base temperature of  $25\ ^\circ\text{C}$ . This energy level must be derated at higher mounting base temperatures as shown in Fig.13. NB. this rating is

non-repetitive which means the circuit should not be designed to force the PowerMOS repeatedly into avalanche. This rating is only to permit the device to survive if exceptional circuit conditions arise such that a transient overvoltage occurs.

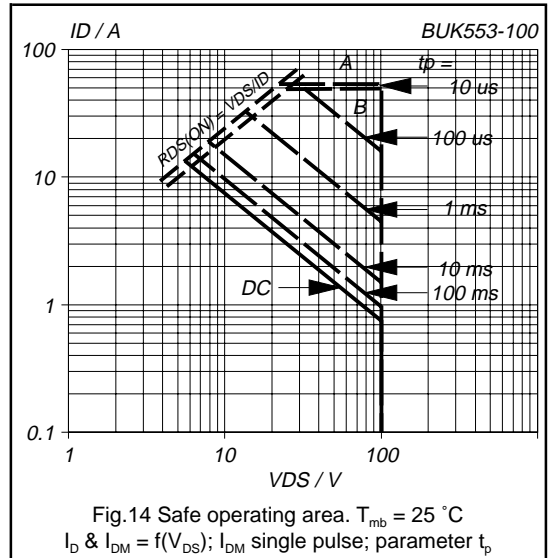
The new generation of Philips Medium Voltage MOSFETs also feature a repetitive ruggedness rating. This rating is specified in terms of a drain-source repetitive unclamped inductive turn-off energy at a mounting base temperature of 25 °C, and indicates that the devices are able to withstand repeated momentary excursions into avalanche breakdown provided the maximum junction temperature is not exceeded. (A more detailed explanation of Ruggedness is given in chapter 1.2.7.)



**Safe Operating Area**

A plot of the safe operating area is presented for every PowerMOS type. Unlike bipolar transistors a PowerMOS exhibits no second breakdown mechanism. The safe operating area is therefore simply defined from the power dissipation that will cause the junction temperature to reach the maximum permitted value.

Fig.14 shows the SOA for a BUK553-100. The area is bounded by the limiting drain source voltage, limiting current values and a set of constant power curves for various pulse durations. The plots in data are all for a mounting base temperature of 25 °C. The constant power curves therefore represent the power that raises the junction temperature by an amount  $T_{jmax} - T_{mb}$ , i.e. 150 °C for a device with a limiting  $T_j$  of 175 °C and 125 °C for a device with a limiting  $T_j$  of 150 °C. Clearly in most applications the mounting base temperature will be higher than 25 °C, the SOA would therefore need to be reduced. The maximum power curves are calculated very simply.



The dc curve is based upon the thermal resistance junction to mounting base (junction to heatsink in the case of isolated packages), which is substituted into equation 1. The curves for pulsed operation assume a single shot pulse and instead of thermal resistance, a value for transient thermal impedance is used. Transient thermal impedance is supplied as graphical data for each type, an example is shown in Fig.15. For calculation of the single shot power dissipation capability, a value at the required pulse width is read from the  $D = 0$  curve and substituted in to equation 2. (A more detailed explanation of transient thermal impedance and how to use the curves can be found in chapter 7.)

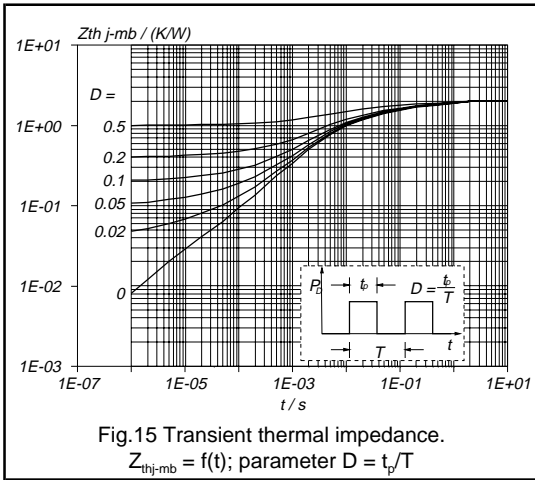
$$P_{tot(dc)} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}} \tag{1}$$

$$P_{tot(pulse)} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}} \tag{2}$$

Examples of how to calculate the maximum power dissipation for a 1 ms pulse are shown below. Example 1 calculates the maximum power assuming a  $T_j$  of 175 °C and  $T_{mb}$  of 25 °C. This power equates to the 1 ms curve on the SOA plot of Fig.14. Example 2 illustrates how the power capability is reduced if  $T_{mb}$  is greater than 25 °C.

**Example 1:** 1 ms pulse at 25 °C for a BUK553-100A

$$Z_{th} = 0.32 K/W, T_{jmax} = 175 °C, T_{mb} = 25 °C$$



$$P_{\max(1\text{ms pulse})} = \frac{175 - 25}{0.32} = 469\text{ W}$$

The 469 W line is observed on Fig.13, (4.69 A @ 100 V and 15.6 A @ 30 V etc)

**Example 2:** 1 ms pulse at 75 °C for a BUK553-100A

$Z_{th} = 0.32\text{ K/W}$ ,  $T_{j\max} = 175\text{ °C}$ ,  $T_{mb} = 75\text{ °C}$

$$P_{\max(1\text{ms pulse})} = \frac{175 - 75}{0.32} = 312\text{ W}$$

Therefore with a mounting base temperature of 75 °C the maximum permissible power dissipation is reduced by one third compared with the 25 °C value on the SOA plot.

### Calculating Currents

The current ratings quoted in the data sheet are derived directly from the maximum power dissipation.

$$I_D(@T_{mb})^2 \cdot R_{DS(ON)}(@T_{j\max}) = P_{tot} \quad 3$$

substituting for  $P_{tot}$  from equation 1

$$I_D(@T_{mb}) = \left\{ \frac{T_{j\max} - T_{mb}}{R_{thj-mb} \cdot R_{DS(ON)}(@T_{j\max})} \right\}^{\frac{1}{2}} \quad 4$$

To calculate a more realistic current it is necessary to replace  $T_{j\max}$  in equation 4 with the desired operating junction temperature and  $T_{mb}$  with a realistic working value. It is generally recommended that devices are not operated continuously at  $T_{j\max}$ . For reasons of long term reliability, 125 °C is a more suitable junction operating temperature. A value of  $T_{mb}$  between 75 °C and 110 °C is also a more typical figure.

As an example a BUK553-100A is quoted as having a dc current rating of 13 A. Assuming a  $T_{mb}$  of 100 °C and operating  $T_j$  of 125 °C the device current is calculated as follows:

From Fig.8

$$R_{DS(ON)}(@125^\circ\text{C}) = 1.75 \cdot R_{DS(ON)}(@25^\circ\text{C}) = 1.75 \cdot 0.18 = 0.315\ \Omega$$

$R_{thj-mb} = 2\text{ K/W}$ , using equation 4

$$I_D = \left\{ \frac{25}{2 \cdot 0.315} \right\}^{\frac{1}{2}} = 6.3\text{ A}$$

The device could therefore conduct 6.3 A under these conditions which equates to a 12.5 W power dissipation.

### Conclusions

The most important information presented in the data sheet is the on-resistance and the maximum voltage drain-source. Current values and maximum power dissipation values should be viewed carefully since they are only achievable if the mounting base temperature is held to 25 °C. Switching times are applicable only for the specific conditions described in the data sheet, when making comparisons between devices from different manufacturers, particular attention should be paid to these conditions.



*High Voltage Bipolar Transistor*



## 1.3.1 Introduction To High Voltage Bipolar Transistors

This section introduces the high voltage bipolar transistor and discusses its construction and technology. Specific transistor properties will be analysed in more detail in subsequent sections and in Chapter 2, section 2.1.2.

### Basic Characteristics

High voltage transistors are almost exclusively used as electronic switches. Therefore, the characteristics of these devices are given for the on state, the off state and the transition between the two i.e. turn-on and turn-off.

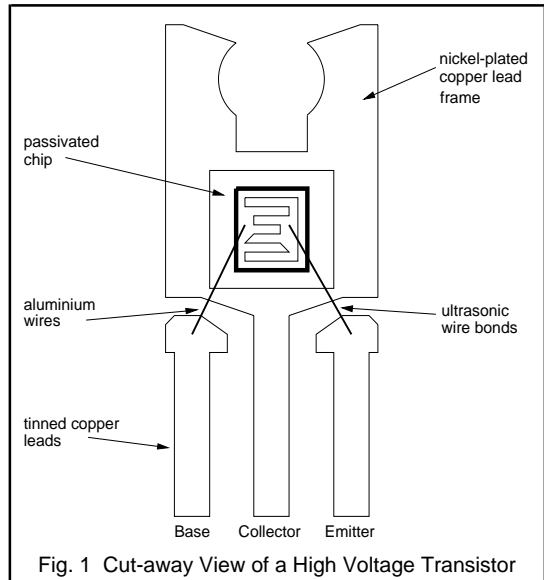
The relative importance of the  $V_{CES}$  and  $V_{CEO}$  ratings usually depends on the application. In a half bridge converter, for instance, the rated  $V_{CEO}$  is the dominant factor, whilst in a forward converter  $V_{CES}$  is important. Which rating is most applicable may also depend on whether a slow rise network or snubber is applied (see section 1.3.3).

The saturation properties in the on state and the switching times are given at a specific collector current called the collector saturation current,  $I_{CSat}$ . It is this current which is normally considered to be the practical working current of the device. If this device is used at higher currents the total dissipation may be too high, while at low currents the storage time is long. At  $I_{CSat}$  the best compromise is present for the total spread of products. The value of the base current used to specify the saturation and switching properties of the device is called  $I_{BSat}$  which is also an important design parameter. As the device requirements can differ per application a universal  $I_{BSat}$  cannot be quoted.

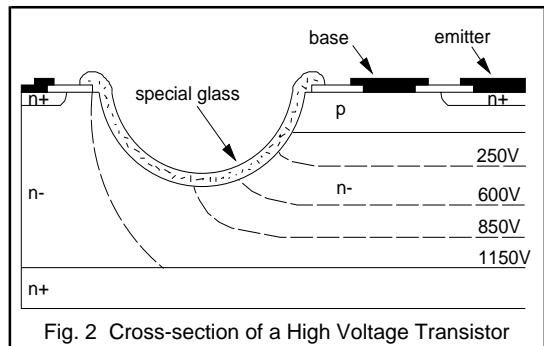
### Device Construction

A drawing of a high voltage transistor, in this case a fully isolated SOT186 F-pack, is shown in Fig. 1 with the plastic encapsulation stripped away. This figure shows the three leads, two of which are connected with wires to the transistor chip. The third lead makes contact with the mounting base on which the crystal is soldered, enabling good thermal contact with a heatsink. It is the transistor package which basically determines the thermal properties of the device. The electrical properties are mainly determined by the design of the chip inside.

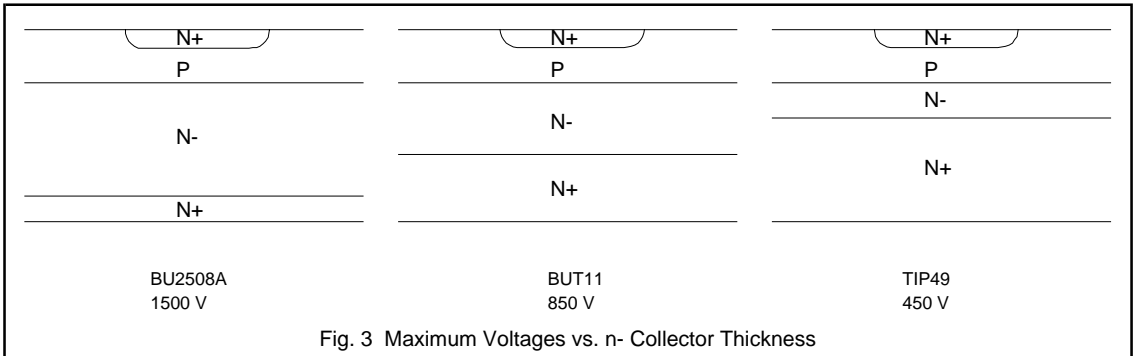
A cross-section of a transistor chip is given in Fig. 2. Here the transistor structure can be recognised with the emitter and the base contacts at the top surface and the collector connected to the mounting base. The thickest part in the drawing is the collector n- region across which the high voltage will be supported in the off state. This layer is of



prime importance in the determination of the characteristics of the device. Below the n- region is an extra n+ layer, needed for a good electrical contact to the heatsink.



Above the collector is the base p layer, and the emitter n+ layer with their respective metallic contacts on top. It is important to realise that the characteristics of the device are determined by the active area, this is the area underneath the emitter where the collector current flows and the high voltage can be developed. The active area of two devices with the same chip size may not be the same.



In addition to the basic collector-base-emitter structure manufacturers have to add electrical contacts, and special measures are needed at the edges of the crystal to sustain the design voltage. This introduces another very important feature, the high voltage passivation. The function of the passivation, (the example shown here is referred to as glass passivation), is to ensure that the breakdown voltage of the device is determined by the collector-base structure and not by the construction at the edges. If no special passivation was used the breakdown voltage might be as low as 50% of the maximum value. Manufacturers optimise the high voltage passivation and much work has also been done to ensure that its properties do not change in time.

**Process Technology**

There are several ways to make the above structure. The starting material can be an n- wafer where first an n+ diffusion is made in the back, followed by the base (p) and emitter (n+) diffusions. This is the well known triple diffused process.

Another way is to start with an n+ wafer onto which an n- layer is deposited using epitaxial growth techniques. A further two diffusions (base and emitter) forms the basic transistor structure. This is called a double diffused epitaxial process.

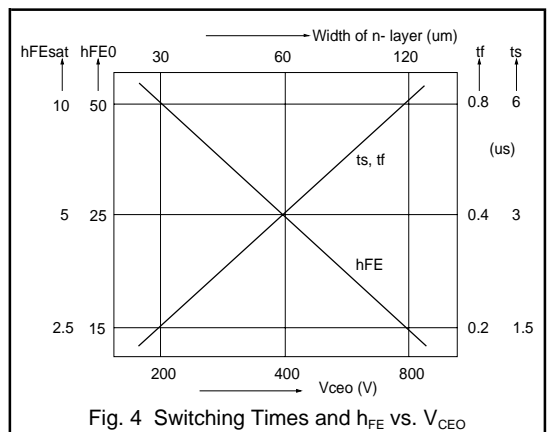
Another little used technology is to grow, epitaxially, the base p-type layer onto an n-/n+ wafer and then diffuse an n+ emitter. This is referred to as a single diffused epi-base transistor.

The question often asked is which is the best technology for high voltage bipolar transistors ? The basic difference in the technologies is the concentration profile at the n-/n+ junction. For epitaxial wafers the concentration gradient is much more steeper from n- to n+ than it is for back diffused wafers. There are more applications where a smoother concentration gradient gives the better performance. Manufacturers utilising epitaxial techniques tend to use buffer layers between the n- and n+ to give smoother

concentration gradients. Another disadvantage of epitaxial processing is cost: back diffused wafers are much cheaper than equivalent high voltage epitaxial wafers.

The process technology used to create the edge passivation is also diverse. The expression "planar" is used to indicate the passivation technique which is most commonly used in semiconductors. This involves the diffusion of additional n-type rings around the active area of the device which give an even electric field distribution at the edge. However, for high voltage bipolar transistors planar passivation is relatively new and the long term reliability has yet to be completely optimised. For high voltage bipolar transistors the most common passivation systems employ a deep trough etched, or cut, into the device with a special glass coating. Like the planar passivation, the glass passivation ensures an even distribution of the electric field around the active area.

**Maximum Voltage and Characteristics**





High voltage and low voltage transistors differ primarily in the thickness and resistivity of the n-layer. As the thickness and resistivity of this layer is increased, the breakdown voltage goes up. The difference over the range of Philips high voltage transistors of different voltages is illustrated in Fig. 3. The TIP49 has a  $V_{CBO} = 450$  V, the BUT11 has a  $V_{CES} = 850$  V, while the BU2508A can be used up to voltages of 1500 V.

The penalty for increasing the n-layer is a decrease in high current  $h_{FE}$  and an increase in switching times. The graph in Fig. 4 points this out by giving both switching times and  $h_{FE}$  as a function of the breakdown voltage. The values given should be used as a guide to illustrate the effect. The effect can be compensated for by having a bigger chip.

### Applications of High Voltage Transistors

High voltage transistors are mainly used as the power switch in energy conversion systems. What is common to

all these systems, is that a current flows through an inductor, thus storing energy in its core. When the current is interrupted by turning off the power switch, the energy must be transferred one way or another. Very often the energy is converted into an electrical output e.g. in switched mode power supplies and battery chargers.

Two special applications are electronic fluorescent lamp ballasts and horizontal deflection of the electron beam in TV's and monitors. In the ballast, an ac voltage is generated to deliver energy to a fluorescent lamp. In the TV and monitor a sawtooth current in the deflection coil sweeps the beam across the screen from left to right and back again in a much shorter blanking, or flyback, period

Other ways to transfer the energy are ac and dc motor control where the output is delivered as movement, or induction heating where the output is delivered in the form of heat.



## 1.3.2 Effects of Base Drive on Switching Times

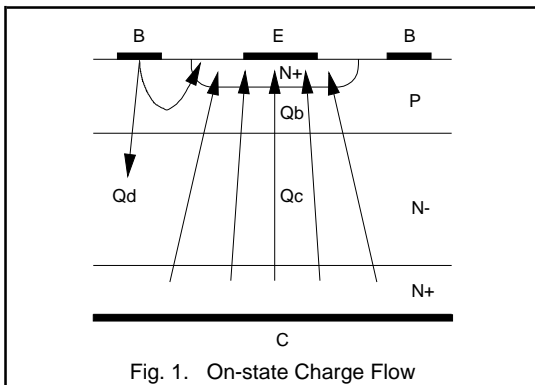
### Introduction

The switching processes that take place within a high voltage transistor are quite different from those in a small signal transistor. This section describes, figuratively, what happens within high voltage transistors under various base drive conditions. After an analysis of the charges that are present in a high voltage transistor, the switch-off process is described. Then comparisons are made of switching for various forward and reverse base drive conditions. A fundamental knowledge of basic semiconductor physics is assumed.

### Charge distribution within a transistor

An off-state transistor has no excess charge, but to enable transistor conduction in the on-state excess charge build up within the device takes place. There are three distinct charge distributions to consider that control the current through the device, see Fig. 1. These charge distributions are influenced by the level of collector-emitter bias,  $V_{CE}$ , and collector current,  $I_C$ , as shown in Fig. 2.

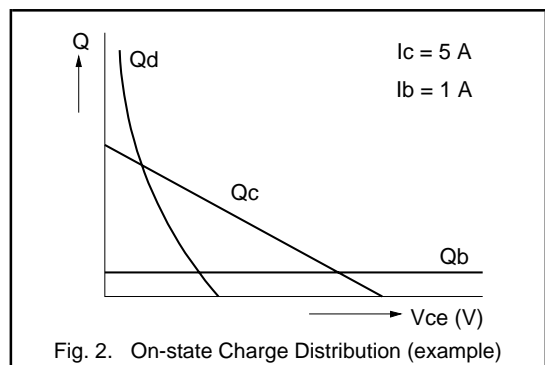
Forward biasing the base-emitter (BE) junction causes a depletion layer to form across the junction. As the bias exceeds the potential energy barrier (work function) for that junction, current will flow. Electrons will flow out of the emitter into the base and out of the base contact. For high voltage transistors the level of BE bias is much in excess of the forward bias for a small signal transistor. The bias generates free electron-hole pairs in the base-emitter leading to a concentration of electrons in the base in excess of the residual hole concentration. This produces an excess charge in the base,  $Q_b$ , concentrated underneath the emitter.



Not only is there an excess charge in the base near the emitter junction but the injection and base width ensure that this excess charge is also present at the collector junction. Applying a load in series with the collector and a dc supply between load and emitter will trigger some sort of collector current,  $I_C$ . The level of  $I_C$  is dependent on the base current,  $I_B$ , the load and supply voltage. For a certain  $I_B$ , low voltage supply and high impedance load there will be a small  $I_C$ . As the supply voltage rises and/or the load impedance falls so  $I_C$  will rise. As  $I_C$  rises so the collector-emitter voltage,  $V_{CE}$ , falls. The  $I_C$  is composed mainly of the excess emitter electrons that reach the base-collector junction (BC). This electron concentration will continue into the collector inducing an excess charge in the collector,  $Q_c$ .

The concentration of electrons decreases only slightly from the emitter-base junction to some way into the collector. In effect, the base width extends into the collector. Decreasing  $V_{CE}$  below  $V_{BE}$  causes the BC junction to become forward biased throughout. This creates a path for electrons from the collector to be driven back into the base and out of the base contact. This electron flow is in direct opposition to the established  $I_C$ . With no change in base drive, the ultimate effect is a reduction in  $I_C$ . This is the classical 'saturation' region of transistor operation. As  $V_{CE}$  falls so the BC forward bias increases leading to an excess of electrons at the depletion layer edge in the collector beneath the base contact. This concentration of electrons leads to an excess charge,  $Q_d$ .

The charge flows and excess charges  $Q_b$ ,  $Q_c$  and  $Q_d$  are shown in Fig. 1. An example of the excess charge distributions for fixed  $I_C$  and  $I_B$  are shown in Fig. 2.



### The switching process of a transistor

Removing the bias voltage,  $V_{BE}$ , will cause the electron-hole pairs to recombine and the excess charge regions to disappear. Allowing this to happen just by removing  $V_{BE}$

takes a long time so usually turn-off is assisted in some way. It is common practice to apply a negative bias (typically 5V) to the base, via a resistor and/or inductor, inducing a negative current that draws the charge out of the transistor. In the sequence that follows, four phases of turn-off can be distinguished (see Fig. 3).

1. First the applied negative bias tries to force a negative bias across the BC junction. The BC electron flow now stops and the charge  $Q_d$  dissipates as the bias now causes the base holes out through the base contact and the collector electrons back into the bulk collector. When the BC was forward biased this current had the effect of reducing the total collector current, so now the negative  $V_{BE}$  can cause the total collector current to increase (this also depends on the load). Although the base has been switched off the load current is maintained by the stored charge effects; this is called the transistor storage time,  $t_s$ .

During this stage the applied negative bias appears as a positive  $V_{BE}$  at the device terminals as the internal charge distributions create an effective battery voltage. Depleting the charge, of course, lowers this effective battery voltage.

2. The next phase produces a reduction in both  $Q_b$ ,  $Q_c$  and, consequently,  $I_c$ . The BC junction is no longer forward biased and  $Q_d$  has dissipated to provide the negative base current. The inductance in series in the base path requires a continuation in the base current. The injection of electrons into the base opposes the established electron flow from emitter to collector via the base. At first the opposing electron flows cancel at the edge of the emitter nearest the base contacts. This reduces both  $Q_b$  and  $Q_c$  in this region.  $Q_b$  and  $Q_c$  become concentrated in the centre of the emitter area. The decrease in  $I_c$  is called the fall time,  $t_f$ .

3. Now there is an extra resistance to the negative base current as the electrons flow through the base under the emitter area. This increase in resistance limits the increase in amplitude of the negative base current. As  $Q_b$  and  $Q_c$  reduce further so the resistance increases and the negative base current reaches its maximum value.

As  $Q_b$  and  $Q_c$  tend to zero the series inductance ensures that negative base current must be continued by other means. The actual mechanism is by avalanche breakdown of the base-emitter junction. This now induces a negative  $V_{BE}$  which is larger than the bias resulting in a reverse in polarity of the voltage across the inductance. This in turn triggers a positive rate of change in base current. The negative base current now quickly rises to zero while the base-emitter junction is in avalanche breakdown. Avalanche breakdown ceases when the base current tends to zero and the  $V_{BE}$  becomes equal to the bias voltage.

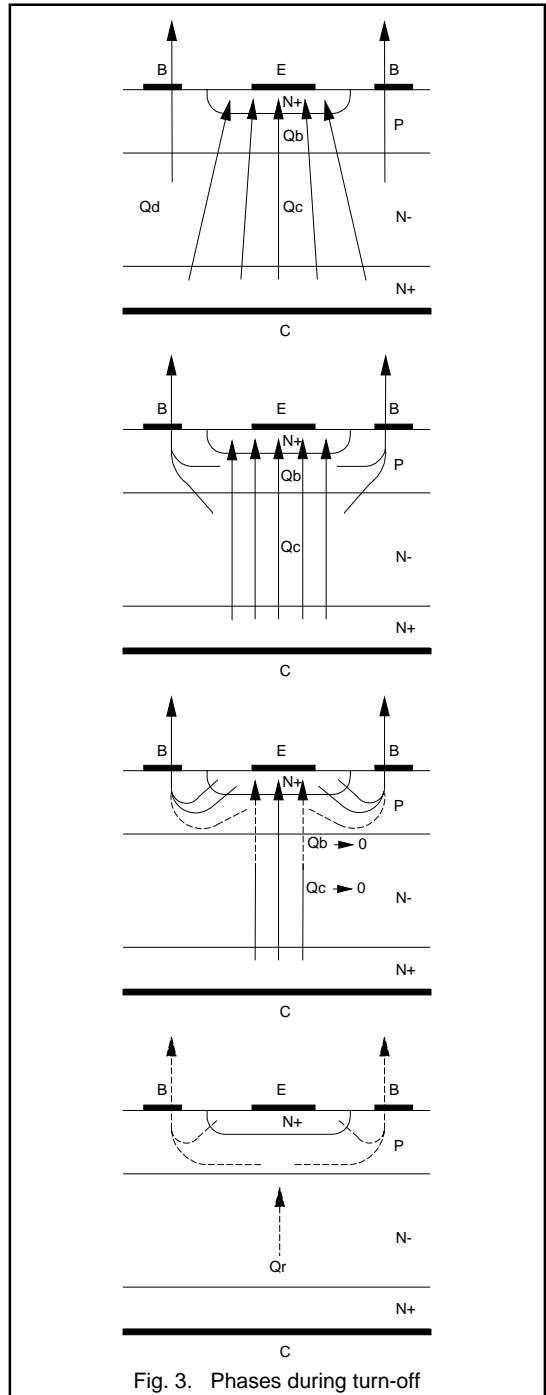


Fig. 3. Phases during turn-off

4. If a very small series base inductor is used with the 5V reverse bias then the base current will have a very fast rate of change. This will speed up the phases 1 to 3 and, therefore, the switching times of the transistor. However, there is a point when reducing the inductor further introduces another phase to the turn-off process. High reverse base currents will draw the charges out closest to the base contact and leave a residual charge trapped deep in the collector regions furthest away from the base. This charge,  $Q_r$ , must be removed before the transistor returns fully to the off-state. This is detected as a tail to  $I_C$  at the end of turn-off with a corresponding tail to the base current as it tends to zero.

The switching waveforms for a BUT11 in a forward converter are given in Fig. 4 where the four phases can easily be recognised. (Because of the small base coil used both phases in the fall time appear clearly!).

- |   |       |
|---|-------|
| 1 - Removal of $Q_d$ until $t \approx 0.7 \mu s$            | $t_s$ |
| 2 - $Q_c$ and $Q_b$ decrease until $t \approx 1.7 \mu s$    | $t_s$ |
| 3 - Removal of $Q_b$ and $Q_c$ until $t \approx 1.75 \mu s$ | $t_f$ |
| 4 - Removal of $Q_r$ until $t \approx 1.85 \mu s$           | $t_f$ |

Note the course of  $V_{BE}$ : first the decrease in voltage due to the base resistance during current contraction and second (because a base coil has been used) the value of  $V_{BE}$  is clamped by the emitter-base breakdown voltage of the transistor. It should be remembered that because breakdown takes place near the surface and not in the active region no harm comes to the transistor.

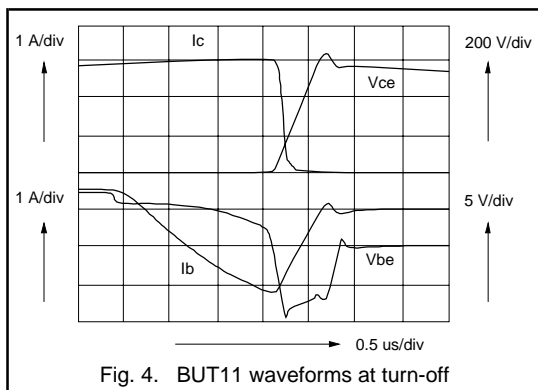


Fig. 4. BUT11 waveforms at turn-off

## The influence of forward drive on stored charge

Fig. 5 shows how, for a transistor in the on-state, at a fixed value of  $I_C$  and  $I_B$  the three charges  $Q_b$ ,  $Q_c$  and  $Q_d$  depend upon  $V_{CE}$ . The base charge,  $Q_b$ , is independent of  $V_{CE}$ , it primarily depends upon  $V_{BE}$ . For normal base drive

conditions, a satisfactory value for  $V_{CEsat}$  is obtained, indicated by N in Fig. 5, and moderate values for  $Q_c$  and  $Q_d$  result.

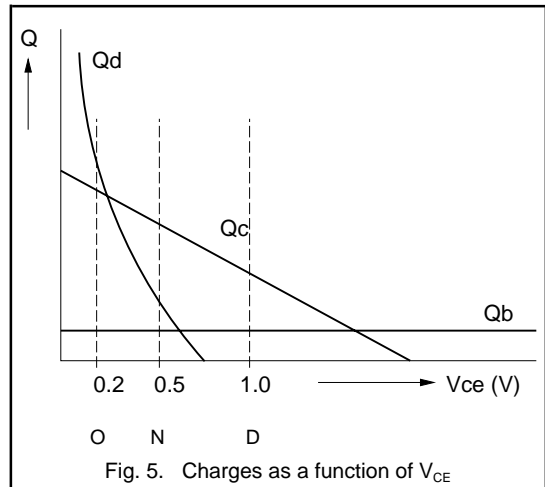


Fig. 5. Charges as a function of  $V_{CE}$

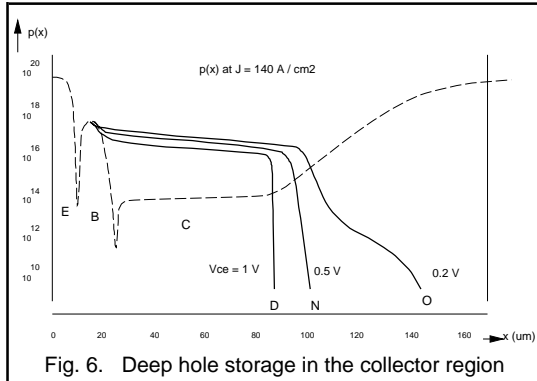
With the transistor operating in the active region, for  $V_{CE} \geq 1V$ , there will be a charge  $Q_c$  but no charge  $Q_d$ . This is indicated by D in Fig. 5. At the other extreme, with the transistor operating in the saturation region  $Q_c$  will be higher and  $Q_d$  will be higher than  $Q_c$ . This is indicated by O in Fig. 5. In this condition there are more excess electron-hole pairs to recombine at switch off.

Increasing  $I_B$  causes  $Q_b$  to increase. Also, for a given  $I_C$ ,  $Q_c$  and  $Q_d$  will be higher as  $V_{CE}$  reduces. Therefore, for a given  $I_C$ , the stored charge in the transistor can be controlled by the level of  $I_B$ . If the  $I_B$  is too low the  $V_{CE}$  will be high with low  $Q_c$  and zero  $Q_d$ , as D in Fig. 5. This condition is called **underdrive**. If the  $I_B$  is too high the  $V_{CE}$  will be low with high  $Q_c$  and  $Q_d$ , as O in Fig. 5. This condition is called **overdrive**. The overdrive condition (high forward drive) gives high stored charge and the underdrive condition (low forward drive) gives low stored charge.

## Deep-hole storage

As the high free electron concentration extends into the base and collector regions there must be an equivalent hole concentration. Fig. 6 shows results obtained from a computer model which illustrates charge storage as a function of  $V_{CE}$ . Here the hole density,  $p(x)$ , is given as a function of depth inside the active area; the doping profile is also indicated. It can be seen that overdrive, O, causes holes to be stored deep in the collector at the collector-substrate junction known as "deep-hole storage", this is the main reason for the increase in residual charge,  $Q_r$ .

During overdrive not only  $Q_d$  becomes very big but also holes are stored far away from the junction: this thus leads not only to a longer storage time, but also to a large  $Q_r$  resulting in tails in the turn-off current.

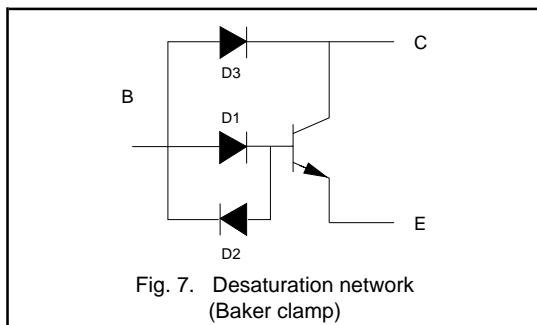


## Desaturation networks

A desaturation network, as shown in Fig. 7, limits the stored charge in the transistor and, hence, aids switching. The series base diode, D1 means that the applied drive voltage now has to be  $V_{BE}$  plus the  $V_F$  of D1. The anti-parallel diode, D2 is necessary for the negative  $I_B$  at turn-off. As  $V_{CE}$  reduces below  $V_{BE} + V_F$  so the external BC diode, D3, becomes forward biased. D3 now conducts any further increase in drive current away from the base and into the collector. Transistor saturation is avoided.

With a desaturation network the charge  $Q_d$  equals zero and the charge  $Q_c$  is minimised. When examining the distribution of the charge in the collector region (see Fig. 6) it can be seen that deep hole storage does not appear. Desaturation networks are a common technique for reducing switching times.

It should be realised that there is a drawback attached to operating out of saturation: increased dissipation during the on-state. Base drive design often requires a trade-off between switching and on-state losses.



## Breakdown voltage vs. switching times

For a higher breakdown voltage transistor the n-layer (see Fig. 1) will be thicker and of higher resistivity (ie a lower donor atom concentration). This means that when comparing identical devices the values for  $Q_d$  and  $Q_c$  will be higher, for a given  $I_C$ , in the device with the higher breakdown voltage.

In general:

- the higher  $BV_{CEO}$  the larger  $Q_d$  and  $Q_c$  will be;
- during overdrive  $Q_d$  is very high and there is a charge located deep in the collector region (deep hole storage);
- when desaturated  $Q_d$  equals zero and there is no deep hole storage:  $Q_c$  is minimised for the  $I_C$ .

## Turn-off conditions

Various ways of turning off a high voltage transistor are used but the base should always be switched to a negative supply via an appropriate impedance. If this is not done, (ie turn-off is attempted by simply interrupting the base current), very long storage times result and the collector voltage increases, while the collector current falls only slowly. A very high dissipation and thus a short lifetime of the transistor are the result. The charges must be removed using a negative base current.

### a) Hard turn-off

The technique widely used, especially for low voltage transistors, is to switch directly to a negative voltage, (see Fig. 8a). In the absence of a negative supply, this can be achieved with an appropriate R-C network (Fig. 8b). Also applying an "emitter-drive" (Fig. 8c) with a large base capacitor in fact is identical to hard-turn-off.

The main drawback for high voltage transistors is that the base charge  $Q_b$  is removed too quickly, leaving a high residual charge. This leads to current tails (long fall times) and high dissipation. It depends upon what state the transistor is in (overdriven or desaturated), whether this way of turn-off is best. It also depends upon the kind of transistor that must be switched off. If it is a lower voltage transistor ( $BV_{CEO} \leq 200V$ ) then this will work very well because the charges  $Q_c$  and  $Q_d$  will be rather low. For transistors with a higher breakdown voltage, hard turn-off will yield the shortest storage time at the cost, however, of higher turn-off dissipation (longer  $t_f$ ).

### b) Smooth turn-off

To properly turn-off a high voltage transistor a storage time to minimise  $Q_d$  and  $Q_c$  is required, and then a large negative base current to give a short fall time.

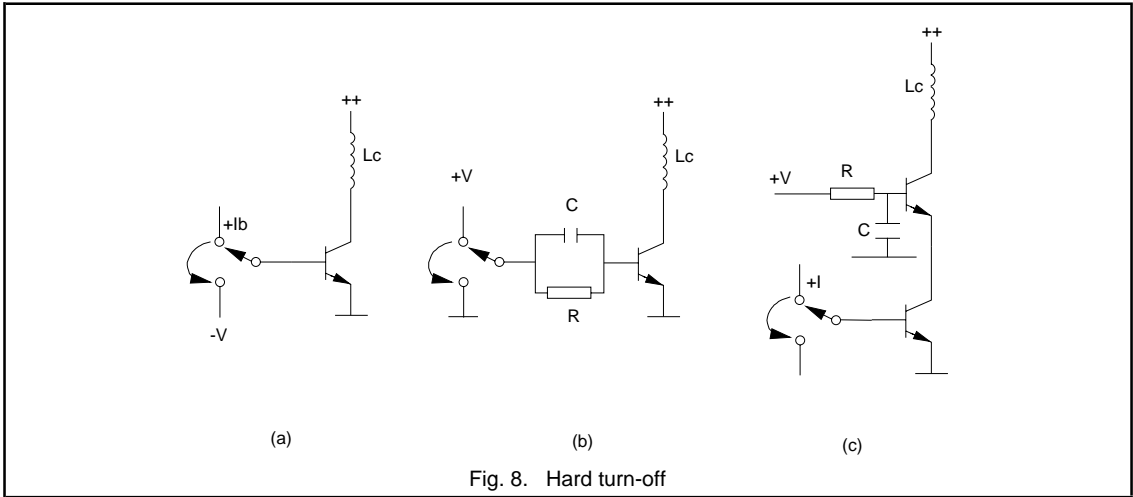


Fig. 8. Hard turn-off

The easiest way to obtain these turn-off requirements is to switch the base to a negative supply via a base coil, see Fig. 9.

The base coil gives a constant  $di_B/dt$  (approx.) during the storage time. When the fall time begins the negative base current reaches its maximum and the  $L_b$  induces the BE junction into breakdown (see Fig. 4).

An optimum value exists for the base coil: if  $L_b = 0$  we have the hard turn-off condition which is not optimum for standard high voltage transistors. If the value of  $L_b$  is too high it slows the switching process so that the transistor desaturates. The  $V_{CE}$  increases too much during the storage time and so higher losses result (see Fig. 10).

For high voltage transistors in typical applications ( $f = 15$  to  $40$  kHz, standard base drive, not overdriven, not desaturated) the following equations give a good indication for the value of  $L_b$ .

$$L_B = \frac{(-V_{dr} + V_{BEsat})}{\left(\frac{dI_B}{dt}\right)}$$

with  $\frac{dI_B}{dt} \approx 0.5 \cdot I_C$  (A/ $\mu$ s) for  $BV_{CEO} = 400V$ ,  $BV_{CES} = 800V$

and  $\frac{dI_B}{dt} \approx 0.15 \cdot I_C$  (A/ $\mu$ s) for  $BV_{CEO} = 700V$ ,  $BV_{CES} = 1500V$

Using  $-V_{dr} = 5V$ ,  $V_{BEsat} = 1V$  and transistors having  $BV_{CEO} = 400V$  it follows that:

$$L_B = \frac{12}{I_C} \text{ H } (I_C \text{ in Amps})$$

c) Other ways of turn-off

Of course, other ways of turn-off are applicable but in general these can be reduced to one of the methods described above, or something in between. The  $BV_{CEO}$  has a strong influence on the method used: the higher  $BV_{CEO}$  the longer the storage time required to achieve proper turn-off. For transistors having a  $BV_{CEO}$  of 200V or less hard turn-off and the use of a base coil yield comparable losses, so hard turn-off works well. For transistors having  $BV_{CEO}$  more than 400V hard turn-off is unacceptable because of the resulting tails.

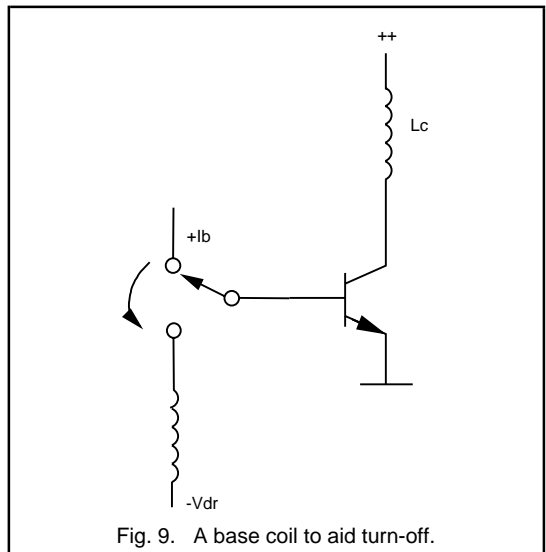


Fig. 9. A base coil to aid turn-off.

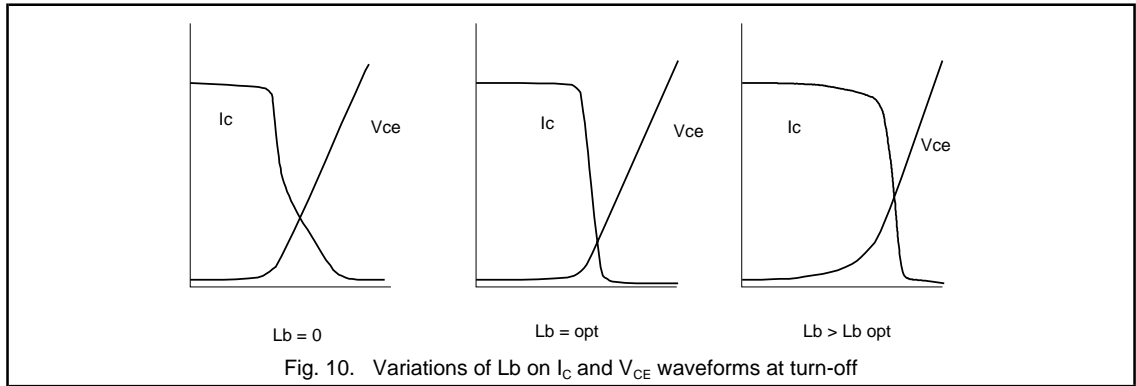


Fig. 10. Variations of  $L_b$  on  $I_C$  and  $V_{CE}$  waveforms at turn-off

### Turn-off for various forward drive conditions

Using the BUT11 as an example, turn-off characteristics are discussed for optimum drive, underdrive and overdrive with hard and smooth turn-off.

#### a) Optimum drive

The optimum  $I_B$  and  $L_b$  for a range of  $I_C$  is given in Fig. 11 for the BUT11. The  $I_B$  referred to is  $I_{B\text{end}}$  which is the value of  $I_B$  at the end of the on-state of the applied base drive signal. In most applications during the on-state the  $I_B$  will not be constant, hence the term  $I_{B\text{end}}$  rather than  $I_{B\text{on}}$ . For optimum drive the level of  $I_{B\text{end}}$  increases with  $I_C$ . For smooth turn-off the level of  $L_b$  decreases with increasing  $I_C$ .

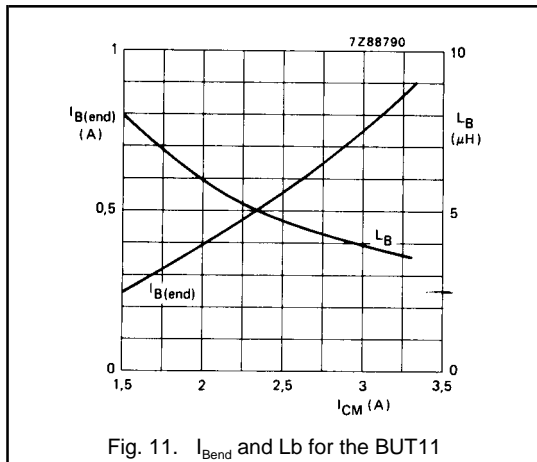


Fig. 11.  $I_{B\text{end}}$  and  $L_b$  for the BUT11

Deviations from Fig. 11 will generally lead to higher power dissipation. If a short storage time is a must in a certain application then  $L_b$  can be reduced but this will lead to longer fall times and current tails.

With hard turn-off  $I_B$  reaches its peak negative value as all the charge is removed from the base. For continuity this current must be sourced from elsewhere. It has been shown that the BE junction now avalanches, giving instantaneous continuity followed by a positive  $dI_B/dt$ . However, for hard turn-off the current is sourced by the residual collector charge without BE avalanche, see Fig. 12. The small negative  $V_{BE}$  ensures a long tail to  $I_C$  and  $I_B$ .

#### b) Underdrive (Desaturated drive)

As has been indicated previously, desaturating, or underdriving, a transistor results in less internal charge.  $Q_d$  will be zero and  $Q_c$  is low and located near the junction.

If the application requires such a drive then steps should be taken to optimise the characteristics. One simple way of obtaining underdrive is to increase the series base resistance with smooth turn-off. The same effect can be achieved with optimum  $I_{B\text{end}}$  and a base coil having half the value used for optimum drive, ie hard turn-off. Both methods give shorter  $t_s$  and  $t_r$ . For 400V  $BV_{CE0}$  devices (like the Philips BUT range) such a harder turn-off can lead to reasonable results.

Fig. 13 compares the use of the optimum base coil with hard turn-off for an undriven BUT11. For underdrive the final  $I_C$  is less and hence the collector charge is less. Therefore, underdrive and hard turn-off gives less of a tail than for a higher  $I_{B\text{end}}$ . Underdrive with smooth turn-off gives longer  $t_s$  but reduced losses.

#### c) Overdrive

When a transistor is severely overdriven the BC charge,  $Q_d$ , becomes so large that a considerable tail will result even with smooth turn-off. In general, deliberately designing a drive circuit to overdrive a transistor is not done: it has no real value. However, most circuits do have variable collector loads which can result in extreme conditions when the circuit is required to operate with the transistor in overdrive.



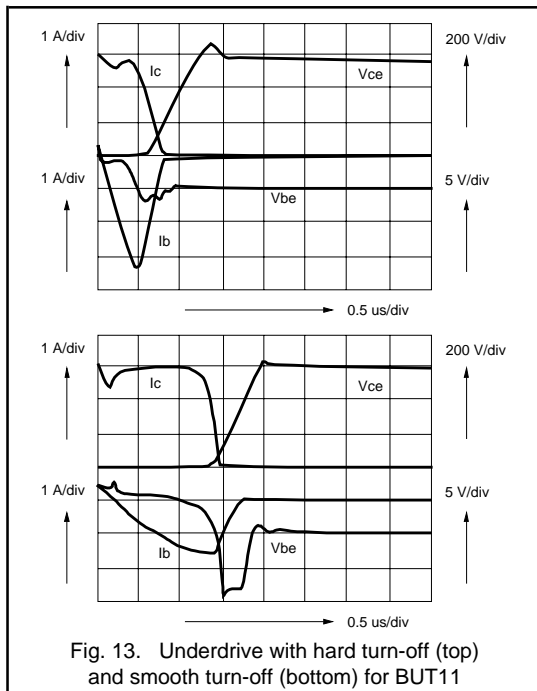
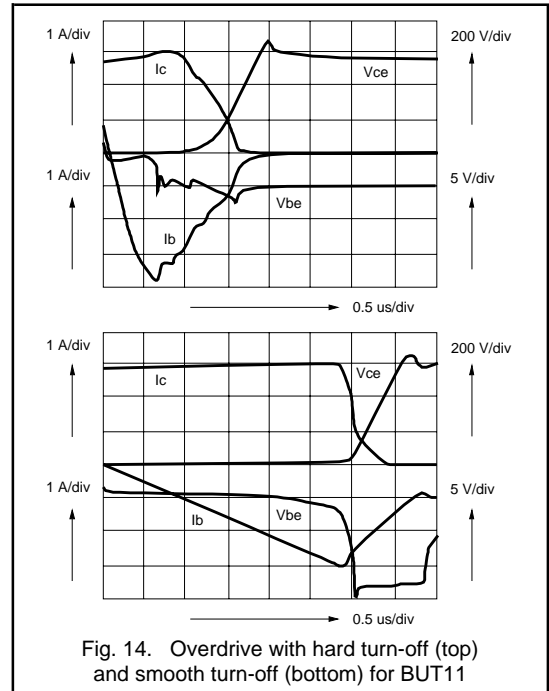
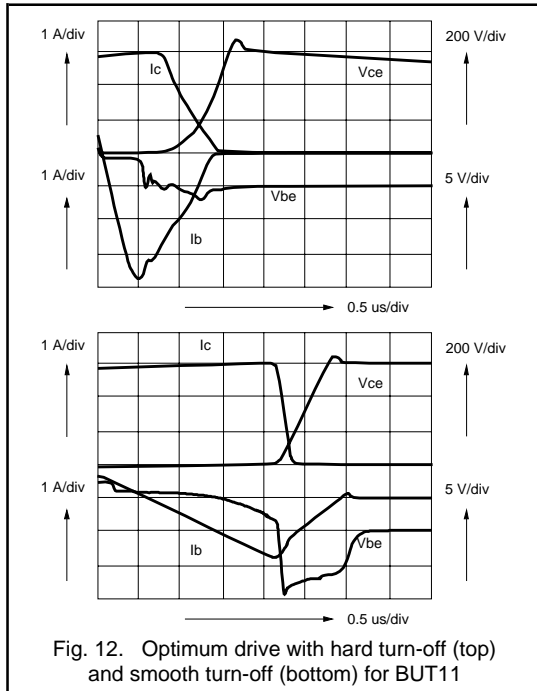


Fig. 14 compares the use of the optimum base coil with hard turn-off for an overdriven BUT11. For overdrive there is more base charge, also the final collector current will be higher and, hence, there will be more collector charge. The overdriven transistor is then certain to have longer switching times as there are more electron-hole pairs in the device that need to recombine before the off-state is reached.

## Conclusions

Two ways of turning off a high voltage transistor, hard turn-off and the use of a base coil, were examined in three conditions of the on-state: optimum drive, overdrive and underdrive.

For transistors having  $BV_{CEO} \sim 400$  V the use of a base coil yields low losses compared to hard turn-off. As a good approximation the base coil should have the value:

$$L_B = \frac{12}{I_C} \mu H$$

for optimum drive.

When using a desaturation circuit the value for  $L_B$  can be halved with acceptable results.

Overdrive should be prevented as much as possible because considerable tails in the collector current cause unacceptable losses.



### 1.3.3 Using High Voltage Bipolar Transistors

This section looks at some aspects of using high voltage bipolar transistors in switching circuits. It highlights points such as switching, both turn-on and turn-off, Safe Operating Areas and the need for snubber circuits. Base drive design curves for the BUT11, BUW12 and BUW13 are discussed under 'Application Information' at the end of this section.

#### Transistor switching: turn-on

To make optimum use of today's high voltage transistors, one should carefully choose the correct value for both the positive base current when the transistor is on and the negative base current when the device is switched off (see Application Information section).

When a transistor is in the off-state, there are no carriers in the thick n- collector, effectively there is a resistor with a relatively high value in the collector. To obtain a low on-state voltage, a base current is applied such that the collector area is quickly filled with electron - hole pairs causing the collector resistance to decrease. In the transition time, the so called turn-on time, the voltage and current may both be high, especially in forward converters, and high turn-on losses may result. Initially, all the carriers in the collector will be delivered via the base contact and, therefore, the base current waveform should have a peak at the beginning. In this way the carriers quickly fill the collector area so the voltage is lower and the losses decrease.

In flyback converters the current to be turned on is normally low, but in forward converters this current is normally high. The collector current,  $I_C$ , reaches its on-state value in a short time which is normally determined by the leakage inductance of the transformer.

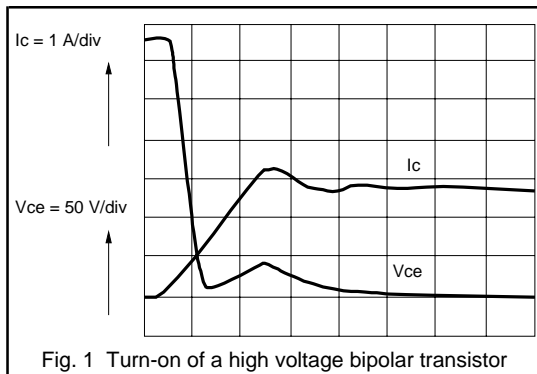


Fig. 1 Turn-on of a high voltage bipolar transistor

In Fig. 1 the characteristic 'hump' which often occurs at turn-on in forward converters due to the effect of the collector series resistance is observed.

The turn-on losses are strongly dependent on the value of the leakage inductance and the applied base drive. It is generally advised to apply a high initial  $+I_B$  for a short time in order to minimise turn on losses.

A deeper analysis can be found in sections 1.3.2, 2.1.2 and 2.1.3. Turn on losses are generally low for flyback converters but are the most important factor in forward converter types.

#### Turn-off of high voltage transistors

All charge stored in the collector when the transistor is on should be removed again at turn-off. To ensure a quick turn-off a negative base current is applied. The time needed to remove the base - collector charge is called the storage time. A short storage time is needed to minimise problems within the control loop in SMPS and deflection applications.

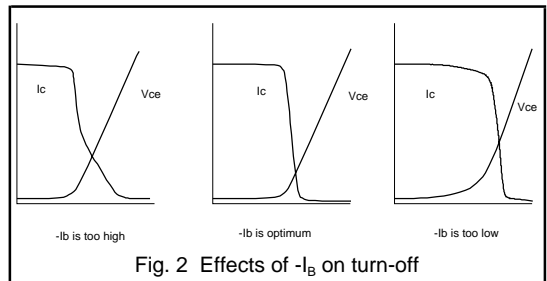


Fig. 2 Effects of  $-I_B$  on turn-off

Care is needed to implement the optimum drive. First overdrive should be prevented by keeping  $+I_B$  to a minimum. Overdrive results in current tails and long storage times. But, decreasing  $I_B$  too much results in high on-state losses.

Second, the negative base current should be chosen carefully. A small negative base current ( $-I_B$ ) will give a long storage time and a high  $V_{CEsat}$  at the end of the storage time, while the current is still high. As a consequence, the turn-off losses will be high. If, however, a large negative base current is used, the danger exists that tails will occur in the collector current, again resulting in high losses. There is an optimum as shown in Fig. 2.

A circuit which is worth considering, especially for higher frequencies, is the Baker Clamp or desaturation circuit. This circuit prevents saturation of the transistor and, hence, faster switching times are achieved.

The total losses depend on the base drive and the collector current. In Fig.3 the total losses are shown for a BUW133 as a function of the positive base current, for both the saturated and the desaturated case. Note that when different conditions are being used the picture will change. The application defines the acceptable storage time which then determines the base drive requirements.

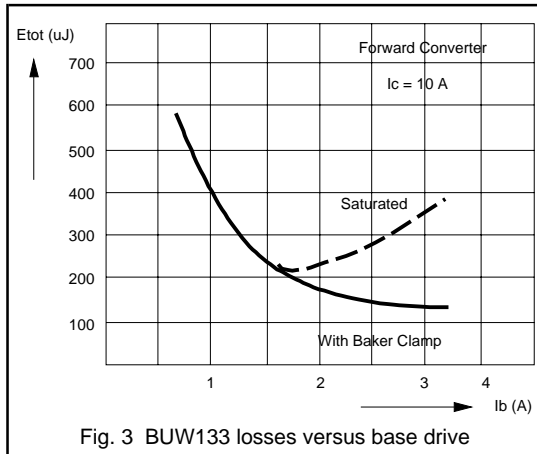


Fig. 3 BUW133 losses versus base drive

The total number of variables is too large to give unique base drive advice for each application. As a first hint the device data sheets give  $I_C$  and  $I_B$  values for  $V_{CEsat}$ ,  $V_{BEsat}$  and switching. However, it is more important to appreciate the ways to influence base drive and the consequences of a non-optimised circuit.

For a flyback converter the best value of  $I_{Bend}$  to start with is about 2/3 of the  $I_B$  value given in data for  $V_{CEsat}$  and  $V_{BEsat}$ . In this application the forward base current is proportional to the collector current (triangular shaped waveforms) and this  $I_{Bend}$  value will give low on-state losses and fast switching.

The best turn-off base current depends on the breakdown voltage of the transistor. As a guide, Table 1 gives reasonable values for the target storage time and may be used to begin optimising the base drive:

f (kHz)	tp (μs)	target ts (μs)
25	20	2.0
150	10	1.5
100	5	1.0

Table 1 Target ts for varying frequency and pulse width

The above table holds for transistors with a  $V_{CE0max}$  rating of 400-450V and  $V_{CESmax}$  between 850-1000V. Transistors with higher voltages require longer storage times, eg.

transistors with  $V_{CE0max} = 700V$  and  $V_{CESmax} = 1500V$  need a storage time which is approximately double the value in the table.

A recommended way to control the storage time is by switching the base to a negative voltage rail via a base coil. The leakage inductance of a driver transformer may serve as an excellent base coil. As a guide, the base coil should be chosen such that the peak value of the negative base current equals half the value of the collector current.

## Specific problems and solutions

A high voltage transistor needs protection circuits to ensure that the device will survive all the currents and voltages it will see during its life in an application.

### a) Over Current

Exceeding current ratings normally does not lead to immediate transistor failure. In the case of a short circuit, the protection is normally fast enough for problems to be avoided. Most devices are capable of carrying very high currents for short periods of time. High currents will raise the junction temperature and if  $T_{jmax}$  is exceeded the reliability of the device may be weakened.

### b) Over Voltage

In contrast with over current, it is NOT allowed to exceed the published voltage ratings for  $V_{CEO}$  and  $V_{CES}$  (or  $V_{CBO}$ ). In switching applications it is common for the base - emitter junction to be taken into avalanche, this does not harm the device. For this reason  $V_{EBO}$  limits are not given in data.

Exceeding  $V_{CEO}$  and  $V_{CES}$  causes high currents to flow in very small areas of the device. These currents may cause immediate damage to the device in very short times (nanoseconds). So, even for very short times it is not allowed to have voltages above data for the device.

In reality  $V_{CEO}$  and  $V_{CES}$  are unlikely to occur in a circuit. If  $V_{BE} = 0V$  there will probably still be a path between the base and the emitter. In fact the situation is  $V_{CEX}$ , where X is the impedance of this path. To cover for all values of X, the limit is  $X = \infty$ , ie  $V_{CEO}$ . For all  $V_{BE} < 0V$ , ie  $V_{CEV}$ , the limit case is  $V_{BE} = 0V$ , ie  $V_{CES}$ .

If voltage transients that exceed the voltage limits are detected then a snubber circuit may limit the voltage to a safe value. If the over voltage states last greater than a few μs a higher voltage device is required.

### c) Forward Bias Safe Operating Areas (FBSOA)

The FBSOA is valid for positive values of  $V_{BE}$ . There is a time limit to  $V_{CE} - I_C$  operating points beyond which device failure becomes a risk. At certain values of  $V_{CE}$  and  $I_C$  there is a risk of secondary breakdown; this is likely to lead to the immediate failure of the device. The FBSOA curve should only be considered during drastic change sequences; for example, start-up, s/c or o/c load.

**d) Reverse Bias Safe Operating Area (RBSOA)**

The RBSOA is valid for negative values of  $V_{BE}$ . During turn-off with an inductive load the  $V_{CE}$  will rise as the  $I_C$  falls. For each device type there is a  $V_{CE} - I_C$  boundary which, if exceeded, will lead to the immediate failure of the device. To limit the  $V_{CE} - I_C$  path at turn-off snubber circuits are used, see Fig. 4.

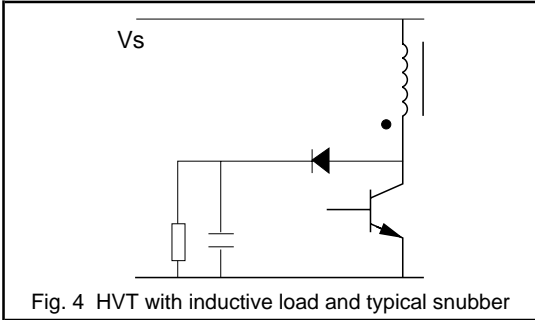


Fig. 4 HVT with inductive load and typical snubber

At turn-off, as the  $V_{CE}$  rises the diode starts conducting charging the capacitor. The additional diode current means that the total load current does not decrease so fast at turn-off. This slower current tail in turn ensures a slower  $V_{CE}$  rise. The slower  $V_{CE}$  rise takes the transistor through a safer  $V_{CE} - I_C$  path away from the limit, see Fig. 5.

As a handy guide, the snubber capacitor in a 20-40 kHz converter is about 1nF for each 100W of throughput power (this is the power which is being transferred via the transformer). This value may be reduced empirically as required.

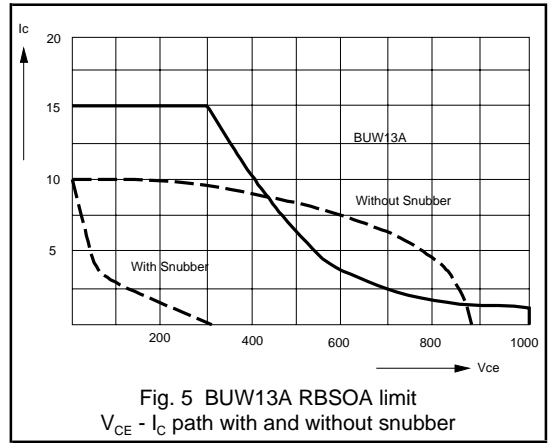


Fig. 5 BUW13A RBSOA limit  
 $V_{CE} - I_C$  path with and without snubber

The following table may serve as a guide to the value of  $dV_{CE}/dt$  for some switching frequencies

f (kHz)	25	50	100
$dV_{CE}/dt$ (kV/ $\mu$ s)	1	2	4

The snubber resistor should be chosen so that the capacitor will be discharged in the shortest occurring on-time of the switch.

In some cases the losses in the snubber may be considerable. Clever designs exist to feed the energy stored in the capacitor back into the supply capacitor, but this is beyond the scope of this report.

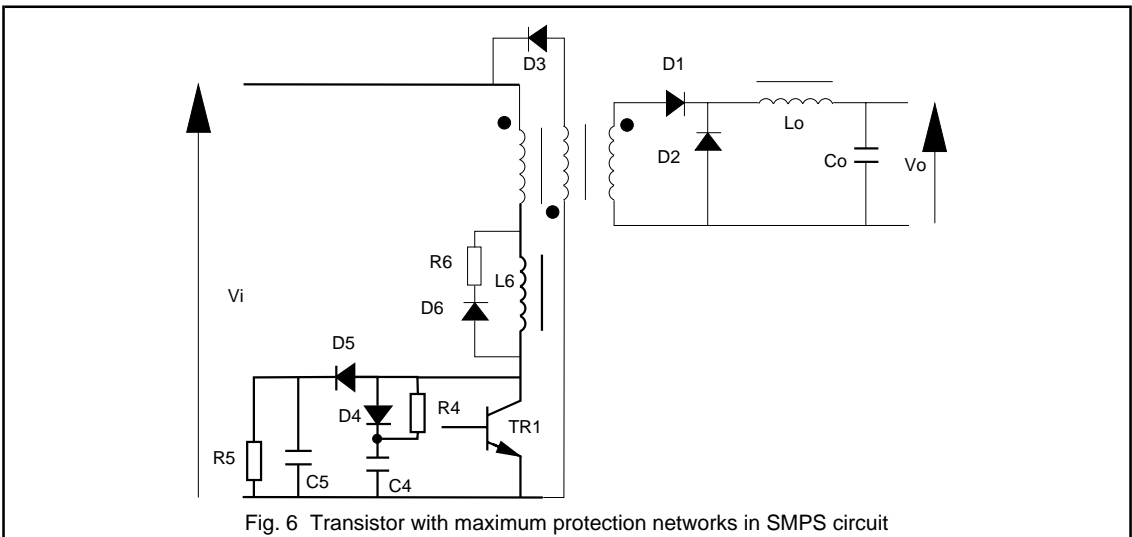


Fig. 6 Transistor with maximum protection networks in SMPS circuit

**d) Other protection networks**

In Fig. 6 a "maximum protection" diagram is shown with various networks connected. R4, C4, and D4 form the snubber to limit the rate of rise of  $V_{CE}$ . The network with D5, R5 and C5 forms a "peak detector" to limit the peak  $V_{CE}$ .

The inductor L6 serves to limit the rate of rise of  $I_C$  which may be very high for some transformer designs. The slower  $dI_C/dt$  leads to considerably lower turn-on losses. Added to L6 is a diode D6 and resistor R6, with values chosen so that L6 loses its energy during the off-time of the power switch.

While the snubber is present in almost all SMPS circuits where transistors are used above  $V_{CE0max}$ , the  $dI_C/dt$  limiter is only needed when the transformer leakage inductance is extremely low. The peak detector is applied in circuits which have bad coupling between primary and secondary windings.

**Application Information**

Important design factors of SMPS circuits are the maximum power losses, heatsink requirements and base drive conditions of the switching transistor. The power losses are very dependent on the operating frequency, the

maximum collector current amplitude and shape.

The operating frequency is usually between 15 and 50 kHz. The collector current shape varies from rectangular in a forward converter to sawtooth in a flyback converter.

Examples of base drive and losses are given in Appendix 1 for the BUT11, BUW12 and BUW13. In these figures  $I_{CM}$  represents the maximum repetitive peak collector current, which occurs during overload. The information is derived from limit-case transistors at a mounting base temperature of 100 °C under the following conditions (see also Fig. 7):

- collector current shape  $I_{C1} / I_{CM} = 0.9$
- duty factor  $(t_p / T) = 0.45$
- rate of rise of  $I_C$  during turn-on = 4 A/ $\mu$ s
- rate of rise  $V_{CE}$  during turn-off = 1 kV/ $\mu$ s
- reverse drive voltage during turn-off = 5 V
- base current shape  $I_{B1} / I_{Be} = 1.5$

The required thermal resistance of the heatsink can be calculated from

$$R_{th(mb-amb)} < \frac{100 - T_{amb}}{P_{tot}} \text{ K/W}$$

To ensure thermal stability a maximum value of the ambient temperature,  $T_{amb}$ , is assumed:  $T_{amb} \leq 40^\circ\text{C}$ .

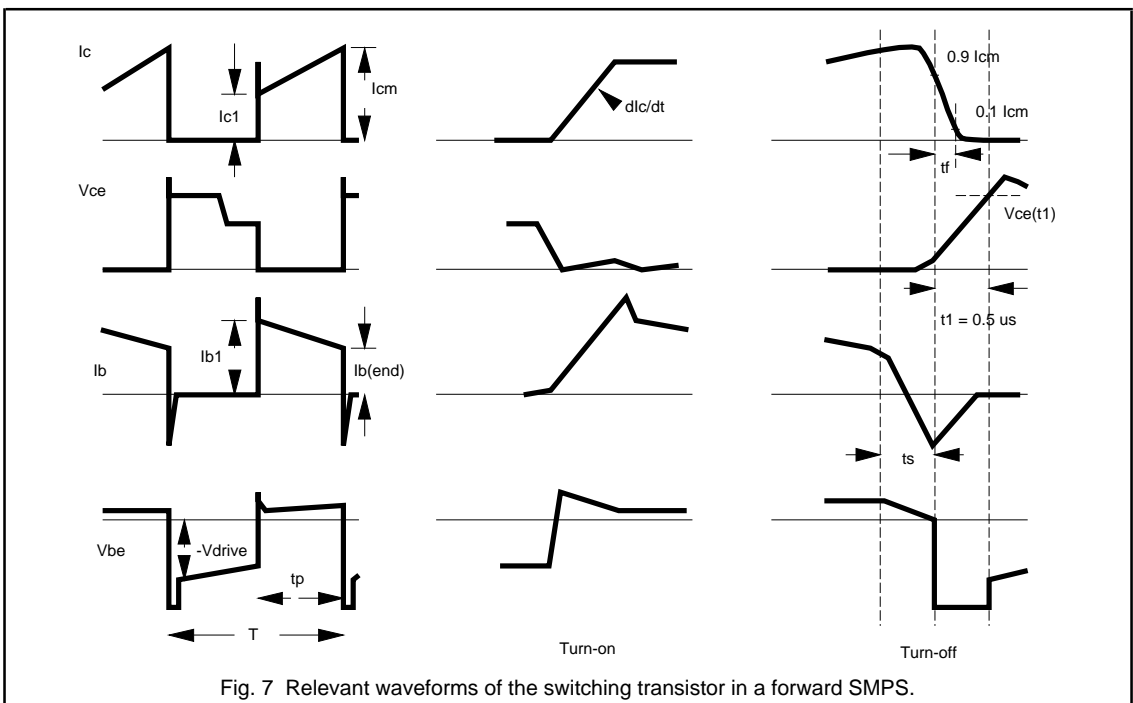


Fig. 7 Relevant waveforms of the switching transistor in a forward SMPS.

As a base coil is normally advised and a negative drive voltage of -5V is rather common, the value for the base coil,  $L_B$ , is given for these conditions. For other values of  $-V_{drive}$  (-3 to -7 volt) the base coil follows from:

$$L_B = L_{Bnom} \cdot \frac{(-V_{drive} + 1)}{6}$$

Where  $L_{Bnom}$  is the value given in Appendix 1.

It should be noted, that this advice yields acceptable power losses for the whole spread in the product. It is not just for typical products as is sometimes thought ! This is demonstrated in Fig. 8, where limit and typical devices are compared (worst-case saturation and worst-case switching).

It appears that the worst-case fall time devices have losses P0 for  $I_{Bend} = (I_b \text{ adv}) + 20\%$ , while the saturation worst-case devices have the same losses at  $(I_b \text{ adv}) - 20\%$ . A typical device now has losses P1 at  $I_b \text{ adv}$ , while the optimum  $I_{Bend}$  for the typical case might yield losses P2 at an approximately 15% lower  $I_{Bend}$  (NB: this is not a rule, it is an example).

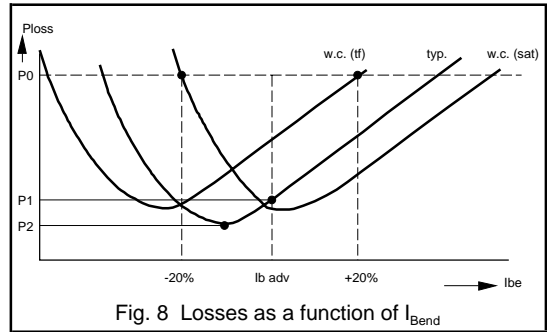
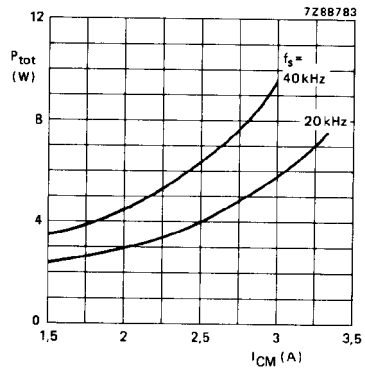
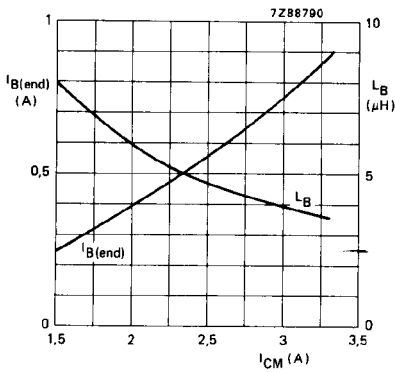


Fig. 8 Losses as a function of  $I_{Bend}$

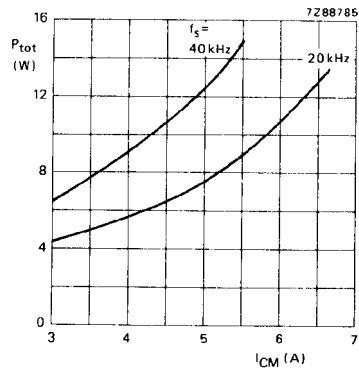
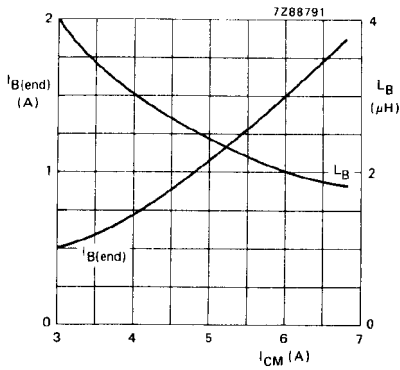
## Conclusion

To avoid exceeding the RBSOA of an HVT, snubbers are a requirement for most circuits. To minimise both switching and on-state losses, particular attention should be given to the design of the base drive circuit. It is generally advised that a high initial base current is applied for a short time to minimise turn-on loss. As a guide-line for turn-off, a base coil should be chosen such that the peak value of the negative base current equals half the value of the collector current.

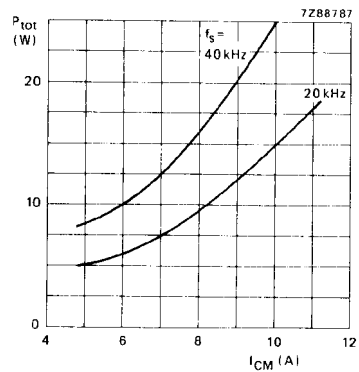
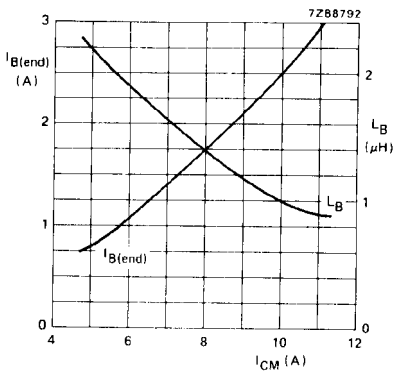
Appendix 1 Base Drive Design Graphs



BUT11 Base Drive Design Information



BUW12 Base Drive Design Information



BUW13 Base Drive Design Information



## 1.3.4 Understanding The Data Sheet: High Voltage Transistors

### Introduction

Being one of the most important switching devices in present day switched mode power supplies and other fast switching applications, the high voltage transistor is a component with many aspects that designers do not always fully understand. In spite of its "age" and the variety of papers and publications by manufacturers and users of high voltage transistors, data sheets are somewhat limited in the information they give. This section deals with the data sheets of high voltage transistors and the background to their properties. A more detailed look at the background to transistor specifications can be found in chapter 2.1.2.

Fig. 1 shows the cross section of a high voltage transistor. The active part of the transistor is highlighted (the area underneath the emitter) and it is this part of the silicon that determines the primary properties of the device: breakdown voltages,  $h_{FE}$ , switching times. All the added parts can only make these properties worse: a bad passivation scheme can yield a much lower collector-base breakdown voltage, too thin wires may seriously decrease the current capability, a bad die bond (solder layer) leads to a high thermal resistance leading to poor thermal fatigue behaviour.

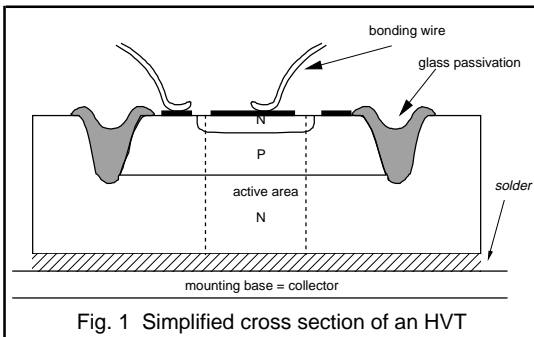


Fig. 1 Simplified cross section of an HVT

### The Data Sheet

The data sheet of a high voltage transistor can specify -

\* Limiting Values / Ratings: the maximum allowable currents through and voltages across terminals, as well as temperatures that must not be exceeded.

\* Characteristics: describing properties in the on and off state (static) as well as dynamic, both in words and in figures.

\* SOA: Safe Operating Area both in forward and reverse biased conditions.

Data sheets are intended to be a means of presenting the essentials of a device and, at the same time, to give an overview of the guaranteed specification points. This data is checked as a final measurement of the device and customers may wish to use it for their incoming inspection. For this reason the data is such that it can be inspected rather easily in relatively simple test circuits. This somewhat application unfriendly way of presenting data is unavoidable if cheap devices are a must, and they are !

Each of the above mentioned items will now be discussed in more detail, in some instances parts of the data for a BUT11 will be used as an example. The BUT11 is intended for 3A applications and has a maximum  $V_{CES}$  of 850V.

### Limiting Values / Maximum Ratings

There is a significant difference between current and voltage ratings. Exceeding voltage ratings can lead to breakdown phenomena which are possibly destructive within fractions of a second. The avalanche effects normally take place within a very small volume and, therefore, only a little energy can be absorbed. Surge voltages, that are sometimes allowed for other components, are out of the question for high voltage transistors.

There is, however, no reason to have a derating on voltages: using the device up to its full voltage ratings - in worst case situations - is allowed. The life tests, carried out in Philips quality laboratories, clearly show that no voltage degradation takes place and excellent reliability is maintained.

From the above, it should be clear that the habit of derating is not a good one. If, in a particular application, the collector-emitter voltage never exceeds, say 800V, the required device should be an 850V device not a 1500V device. Higher voltage devices not only have lower  $h_{FE}$ , but also slower switching speeds and higher dissipation.

The rating for the emitter-base voltage is a special case: to allow a base coil to be used, the base-emitter diode may be brought into breakdown; in some cases a  $-I_{Bav}$  is given to prevent excessive base-emitter dissipation. The only effect of long term repetitive base-emitter avalanche breakdown that has been observed is a slight decrease in  $h_{FE}$  at very low values of collector current (approximately 10% at  $\leq 5\text{mA}$ ); at higher currents the effects can be neglected completely.

The maximum value for  $V_{CE0}$  is important if no snubber is applied; it sets a firm boundary in applications with a very fast rising collector voltage and a normal base drive (see also section on SOA).

Currents above a certain value may be destructive if they last long enough: bonding wires fuse due to excessive heating. Therefore, short peak currents are allowed well above the rated  $I_{CSat}$  with values up to five times this value being published for  $I_{CM}$ . Exceeding the published maximum temperatures is not immediately destructive, but may seriously affect the useful life of the device. It is well known, that the useful life of a semiconductor device doubles for each 10K decrease in working junction temperature. Another factor that should be kept in mind is the thermal fatigue behaviour, which strongly depends on the die-bonding technology used. Philips high voltage devices are capable of 10,000 cycles with a temperature rise of 90K without any degradation in performance.

This kind of consideration leads to the following advice: under worst case conditions the maximum case-temperature should not exceed 115 °C for reliable operation. This advice is valid regardless of the maximum temperature being specified. Of course, for storage the published values remain valid.

The maximum total power dissipation  $P_{tot}$  is an industry standard, but not very useful, parameter. It is the quotient of  $T_{jmax} - T_{mb}$  and  $R_{th(j-mb)}$  ( $R_{th(j-mb)}$  is the thermal resistance from junction to mounting base and  $T_{mb}$  is assumed to be 25°C). This implies a rather impractical infinite heatsink, kept at 25°C !

## Electrical Characteristics

Static parameters characterise leakage currents,  $h_{FE}$ , saturation voltages; dynamic parameters and switching times, but also include transition frequency and collector capacitance.

To start:  $I_{CSat}$ , the collector saturation current, is that value of the collector current where both saturation and switching properties of the devices are specified.  $I_{CSat}$  is not a characteristic that can be measured, but it is used as an indication of the of the peak working current allowed through a device.

In the off-state various leakage currents are specified, however, these are of little use as they indicate the low level of dissipation in the off state. Also a  $V_{CE0sust}$  is specified, usually being equal to the max.  $V_{CE0}$ . For switching purposes it is the RBSOA that is important (see next section).

In the on state the saturation voltages  $V_{CEsat}$  and, to a lesser extent,  $V_{BEsat}$  are important.  $V_{CEsat}$  is an indication of the saturation losses and  $V_{BEsat}$  normally influences base drive. Sometimes worst case  $V_{CEsat}$  is given as a function of both  $I_c$  and  $I_b$ . It is not possible to precisely relate these curves

to a real circuit; in practice, currents and voltages will vary over the switching cycle. The dynamic performance is different to the static performance. However, a reasonable indication can be obtained from these curves.

Both the transition frequency ( $f_T$ ) and the collector capacitance ( $C_c$  or  $C_{ob}$ ) are minor parameters relating to the design and processing technology used.

Switching times may be given in circuits with an inductive or a resistive collector load. See Figs. 2a-b for simplified test circuits and Figs. 3a-b for waveforms.

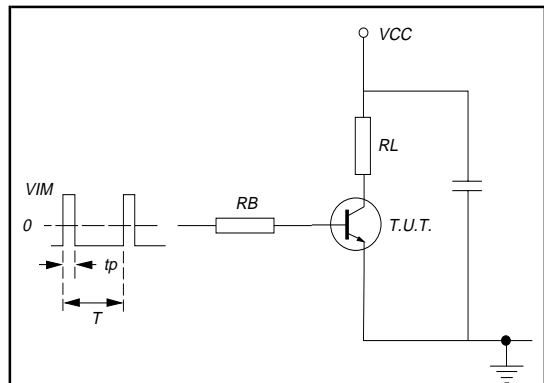


Fig. 2a Test circuit for resistive load

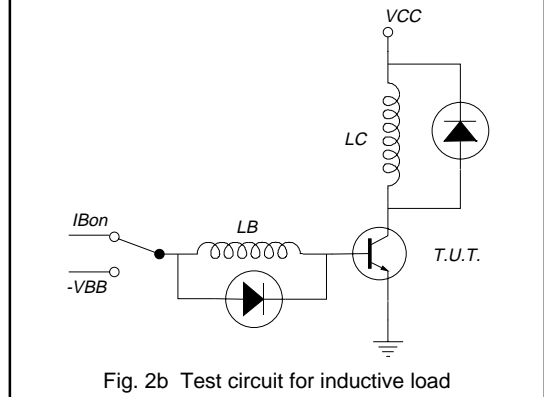


Fig. 2b Test circuit for inductive load

When comparing similar devices from different manufacturers one is confronted with a great variety of base drive conditions. The positive base current ( $+I_b$ ) may be the same as the one used in the  $V_{CEsat}$  spec. but also lower values (up to 40% lower) or desaturation networks may be used, yielding better  $t_s$  and  $t_f$  values. The negative base drive,  $-I_b$ , may equal  $+I_b$  or it may be twice this value, yielding a shorter  $t_s$ , and sometimes it is determined by switching the base to a negative voltage, possibly via a base coil. Altogether it is quite confusing and when comparing switching times one should be well aware of all the differences!

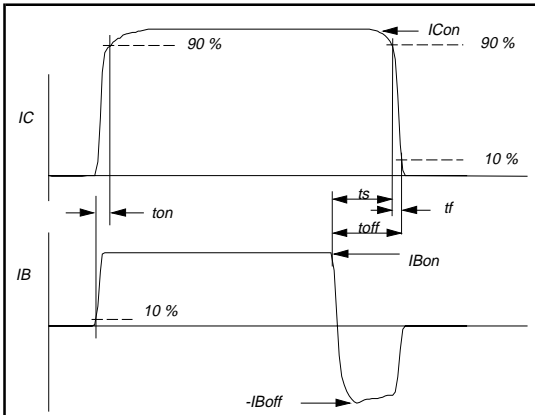


Fig. 3a Waveforms for Resistive Switching.

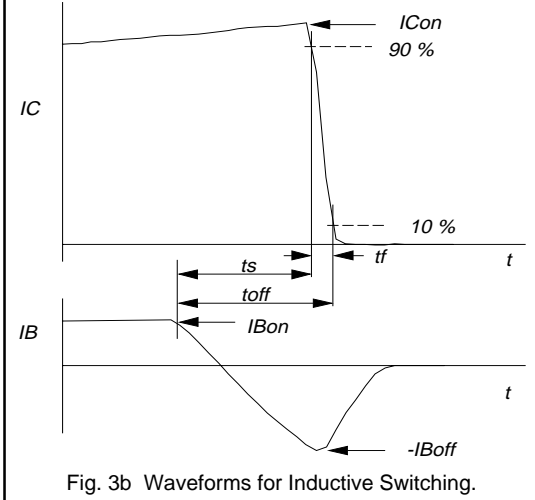


Fig. 3b Waveforms for Inductive Switching.

As an example a BUT11 has been measured at  $I_C = 3\text{ A}$  in a resistive test circuit varying both  $+I_B$  and  $-I_B$ . The results in Table 1 show that it is possible to turn a normal transistor into a super device by simple specmanship!

$I_C = 3\text{ A}$	$t_s$ ( $\mu\text{s}$ )	$t_f$ (ns)
$+I_B = 0.6\text{ A}; -I_B = 0.6\text{ A}$ (normal case)	2.5	260
$+I_B = 0.36\text{ A}; -I_B = 0.72\text{ A}$ (underdriven)	1.6	210
$+I_B = 0.36\text{ A}; -V_{BE} = -5\text{ V}$ (underdriven, hard turn-off)	0.8	50

Table 1 Switching times and base drive for the BUT11

The effect of base drive variations on storage and fall times is given in Table 2. The reference is the condition that both  $+I_B$  as well as  $-I_B$  equals the value for  $I_B$  given for the  $V_{CEsat}$  specification in the data sheet.

	$t_s$	$t_f$	comments
$+I_B = \text{ref.}$	normal	normal	reference
$+I_B = 40\% \text{ less}$	↓	↓	
Desaturated	↓	↓	
$-I_B = \text{ref.}$	normal	normal	reference
$-I_B = 2 \times +I_B$	↓	↓	
Directly to -5 V	↓	↑	with normal base drive!
Directly to -5 V	↓	↓	if underdriven
Via L to -5 V	↓	↓	

Table 2 Switching times and base drive variations.

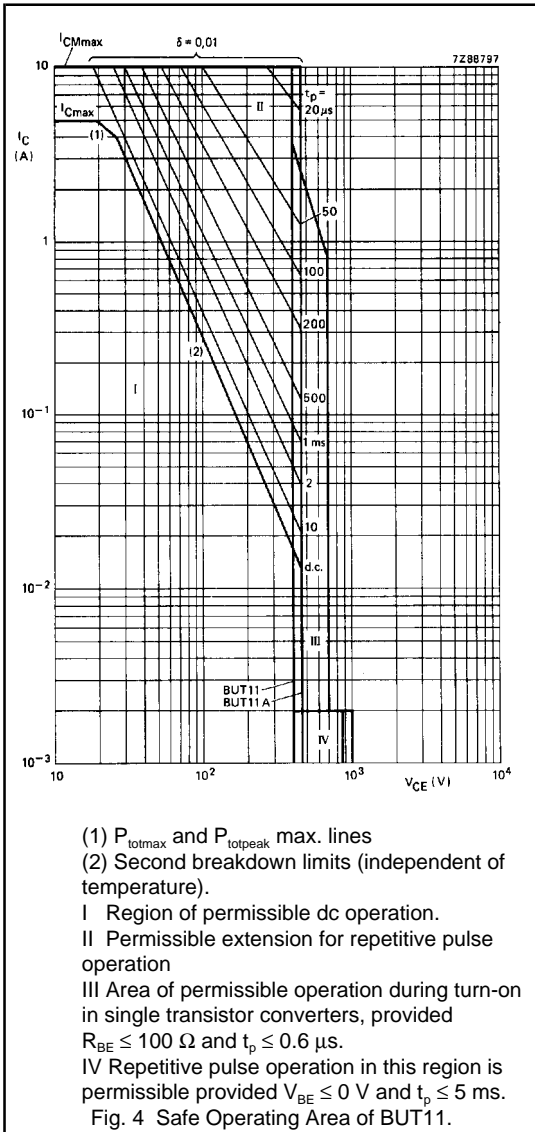
The turn-on time is a parameter which only partially correlates with dissipation as it is usually the behaviour directly after the turn-on time which appears to be most significant. Both inductive and resistive load test circuits are only partially useful, as resistive loads are seldom used and very often some form of slow-rise network is used with inductive loads. Both circuits provide easy lab. measurements and the results can be guaranteed. The alternative of testing the devices in a real switched mode power supply would be too costly!

### Safe Operating Area

The difference between forward bias safe operating area (FBSOA) and reverse bias safe operating area (RBSOA) is in the device  $V_{BE}$ : if  $V_{BE} > 0\text{ V}$  it is FBSOA and if  $V_{BE} < 0\text{ V}$  it is RBSOA. Chapter 2.1.3 deals with both subjects in more detail, a few of the main points are covered below.

FBSOA gives boundaries for dc or pulsed operation. In switching applications, where the transistor is "on" or "off", normally the excursion in the  $I_C$ - $V_{CE}$  plane is fast enough to allow the designer to use the whole plane, with the boundaries  $I_{Cmax}$  and  $V_{CEO}$ , as given in the ratings. This is useful for snubberless applications and for overload, fault conditions or at switch-on of the power supply

Fig. 4 gives the FBSOA of the BUT11 with the boundaries of  $I_{Cmax}$ ,  $I_{CMmax}$  and  $V_{CEO}$ , all as given in the ratings. There is a  $P_{totmax}$  (1) and  $I_{SB}$  boundary (2), that both shift at higher levels of  $I_C$  when shorter pulses are used. Note that in the upper right hand corner pulse times of  $20\mu\text{s}$  are permitted leading to a square switching SOA. For overload, fault condition or power supply switch-on an extra area is added (area III). All these conditions are for  $V_{BE} \geq 0\text{ V}$ .

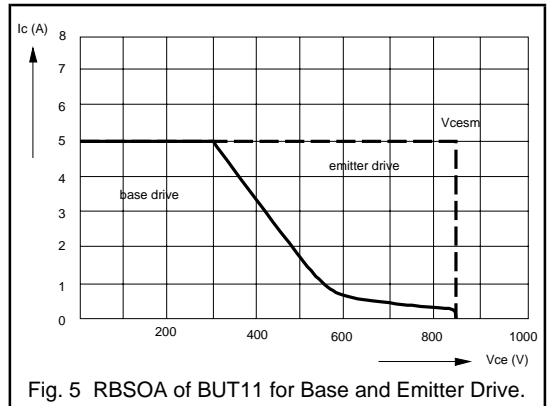


Area IV is only valid for  $V_{BE} \leq 0V$ , so this is an RBSOA extension to the SOA curve. This is not the full picture for RBSOA, area IV is only for continuous pulsed operation. For single cycle and short burst fault conditions see the separate RBSOA curve.

The RBSOA curve is valid when a negative voltage is applied to the base-emitter terminals during turn-off. This curve should be used for fault condition analysis only; continuous operation close to the limit will result in 100's W of dissipation ! Due to localised current contraction within

the chip at turn-off, damage will occur if the limit is exceeded. In nearly all cases, the damage will result in the immediate failure of the device to short circuit.

Emitter switching applications force different mechanisms for carrier recombination in the device which allow a 'square' RBSOA. A typical example is shown in Fig. 5, where for both base and emitter drive the RBSOA of the BUT11 is given.



It is striking that for emitter drive the whole  $I_C$ - $V_{CES}$  plane may be used so no snubber is necessary, however, a small snubber may prevent overshoot. The base drive RBSOA normally depends on base drive conditions, but unfortunately there is no uniform trend in this behaviour. Therefore, the RBSOA curve in the data gives the worst case behaviour of the worst case devices. Other data sheets may give RBSOA curves that at first sight look better than the Philips equivalent, but beware, these curves might hold for only a limited base drive range.

### Summary

Voltage limiting values / ratings as given in the data must never be exceeded, as they may lead to immediate device failure. Surge voltages, as sometimes given for other components, are not allowed for high voltage transistors. Current limiting values / ratings are less strict as they are time-dependent and should be used in conjunction with the FBSOA.

Static characteristics are useful for comparisons but offer little in describing the performance in an application. The dynamic characteristics may be defined for a simple test circuit but the values give a good indication of the switching performance in an application.

RBSOA is, for all switching applications, of prime importance. Philips give in their data sheets a curve for worst case devices under worst case conditions. For snubber design a value of 1 nF per 100W of throughput

power is advised as a starter value; afterwards, the  $I_C$ - $V_{CE}$  locus must be checked to see if it stays within the published RBSOA curve.

For characteristics both saturation and switching properties are given at  $I_{C\text{sat}}$ . Most figures are of limited use as they give static conditions, where in a practical situation properties are time-dependent. Switching times are given

in relatively simple circuits that may be replicated rather easily e.g. for incoming inspection.

Switching times depend strongly on drive conditions. By altering them a normal device can be turned into a super device. Beware of specmanship, this may disguise poor tolerance to variations in base drive.

## Acknowledgments

We are grateful for all the contributions from our colleagues within Philips and to the Application Laboratories in Eindhoven and Hamburg.

We would also like to thank Dr.P.H.Mellor of the University of Sheffield for contributing the application note of section 3.1.5.

The authors thank Mrs.R.Hayes for her considerable help in the preparation of this book.

The authors also thank Mr.D.F.Haslam for his assistance in the formatting and printing of the manuscripts.

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## Preface

This book was prepared by the Power Semiconductor Applications Laboratory of the Philips Semiconductors product division, Hazel Grove. The book is intended as a guide to using power semiconductors both efficiently and reliably in power conversion applications. It is made up of eight main chapters each of which contains a number of application notes aimed at making it easier to select and use power semiconductors.

**CHAPTER 1** forms an introduction to power semiconductors concentrating particularly on the two major power transistor technologies, Power MOSFETs and High Voltage Bipolar Transistors.

**CHAPTER 2** is devoted to Switched Mode Power Supplies. It begins with a basic description of the most commonly used topologies and discusses the major issues surrounding the use of power semiconductors including rectifiers. Specific design examples are given as well as a look at designing the magnetic components. The end of this chapter describes resonant power supply technology.

**CHAPTER 3** describes motion control in terms of ac, dc and stepper motor operation and control. This chapter looks only at transistor controls, phase control using thyristors and triacs is discussed separately in chapter 6.

**CHAPTER 4** looks at television and monitor applications. A description of the operation of horizontal deflection circuits is given followed by transistor selection guides for both deflection and power supply applications. Deflection and power supply circuit examples are also given based on circuits designed by the Product Concept and Application Laboratories (Eindhoven).

**CHAPTER 5** concentrates on automotive electronics looking in detail at the requirements for the electronic switches taking into consideration the harsh environment in which they must operate.

**CHAPTER 6** reviews thyristor and triac applications from the basics of device technology and operation to the simple design rules which should be followed to achieve maximum reliability. Specific examples are given in this chapter for a number of the common applications.

**CHAPTER 7** looks at the thermal considerations for power semiconductors in terms of power dissipation and junction temperature limits. Part of this chapter is devoted to worked examples showing how junction temperatures can be calculated to ensure the limits are not exceeded. Heatsink requirements and designs are also discussed in the second half of this chapter.

**CHAPTER 8** is an introduction to the use of high voltage bipolar transistors in electronic lighting ballasts. Many of the possible topologies are described.

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