National Semiconductor

March 2003

CLC730227,CLC730216
Single High Speed Op Amp Evaluation Boards (SOIC and SOT)

The CLC730227 and CLC730216 evaluation boards are designed to aid in the characterization of National Semiconductor's High Speed monolithic amplifiers.

- CLC730227 - SOIC packages
- CLC730216 - SOT packages

Use the evaluation boards as a guide for high frequency layout and as a tool to aid in device testing and characterization.

The evaluation boards accommodate general purpose amplifiers, as well as amplifiers with the following features:

- Supply current adjustment via external Resistor
- Output disable

The evaluation board schematic is shown below. Refer to the product data sheets for recommendations for component values.

BASIC OPERATION

Both boards have identical circuit configurations and are designed to accommodate both non-inverting and inverting operation. By changing RT or RIN and ROUT different input and output impedances can be matched. The SMA connectors and board traces are optimized for 50Ω operation, however other impedances can be matched as shown below.

Inverting Gain = R_F/R_G (Input Resistance = $R_T \parallel R_G$)

Non Inverting Gain = $1 + R_F/(R_G + R_T)$ (Input Resistance = R_{IN})

(R_T may be set to zero for non inverting operation)

For current feedback operational amplifiers be careful to use appropriate values of R_F. In addition the required value of Rg will limit choices for input impedance with Inverting gains.

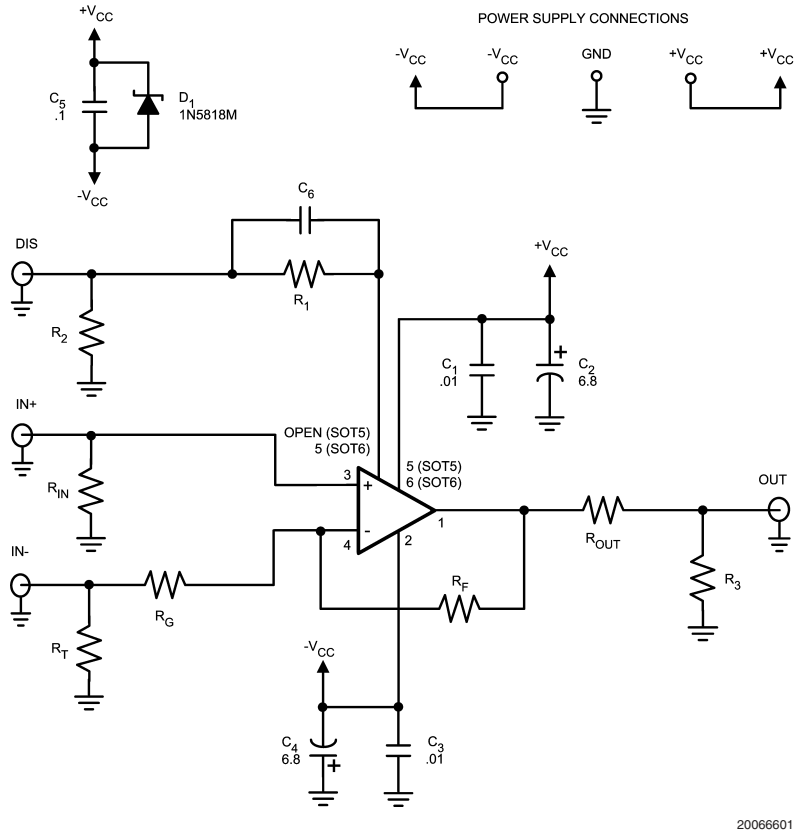

FIGURE 1. SOT Schematic

(Continued)

LAYOUT CONSIDERATIONS

Printed circuit board layout and supply bypassing play major roles in determining high frequency performance. When designing your own board use these evaluation boards as a guide and follow these steps to optimize high frequency performance:

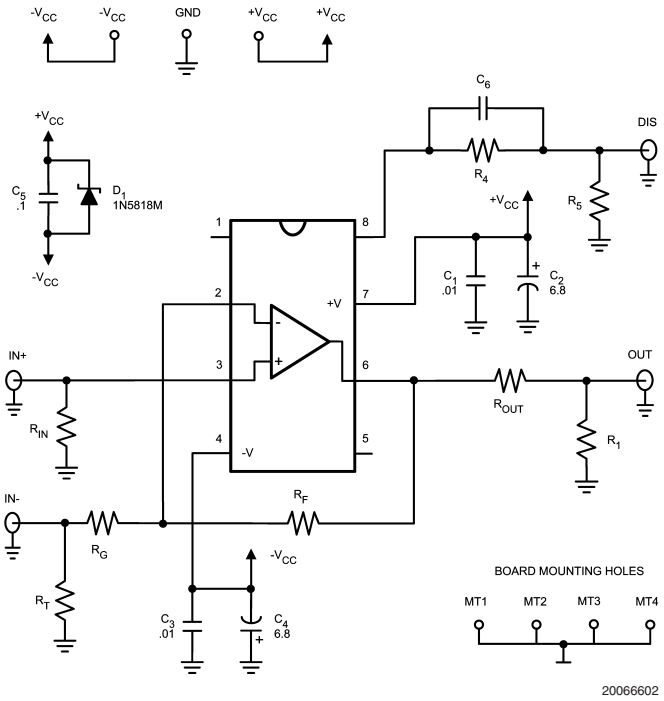

FIGURE 2. SOIC Schematic

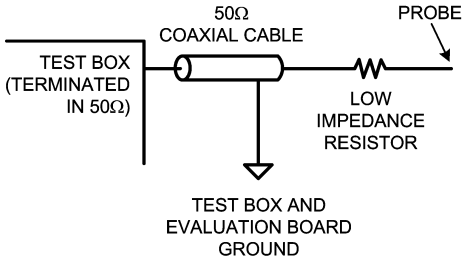

FIGURE 3. Probe Schematic

1. Use a ground plane
2. Include large (~6.8µF) capacitors on both supplies.
3. Near the device use .01µF ceramic capacitors from both supplies to ground C_1, C_3.
4. Near the device use a .1µF ceramic capacitor between the supplies C_5.
5. Remove the ground and power planes from under and around the part, especially the input and output pins.
6. Minimize all trace lengths
7. Use terminated transmission lines for long traces.
8. High-speed disable/ enable operation requires that the enable pin be treated as a signal input.

Diode D_1 is to protect the device from reverse polarity supply connections and will not be necessary for most designs.

(Continued)

Capacitor C_5 is necessary for best Harmonic Distortion performance. If C_5 is not used increase the values of C_1 and C_3 to .1µF.

R_{IN}, R_T and R_{OUT} are all impedance matching resistors. R_{IN} and R_{OUT} should be equal to the desired input/output impedance. R_T || R_G should equal the desired inverting input impedance. Note that with current feedback op amps, the optimum value of R_F and R_G is determined by the desired gain and raising R_G to obtain higher input impedance may require compromising device performance at large values of inverting gain.

The disable trace has provisions for input termination. There are also pads for series resistance and capacitance for programmable gain parts. See part datasheets for suggested values.

Sample artwork for National's Evaluation boards is included below.

The board is designed for 50Ω input and output connections into coaxial cables. For other impedances the terminating resistors can be modified to help match different impedances.

Do not use normal oscilloscope probes to test these circuits. The capacitive loading will change circuit performance drastically. Instead use low impedance resistive divider probes of 100 to 500Ω. See *Figure 3* for a sample resistive probe. The Low impedance resistor should be 50-450Ω. The ground connection should be as short as possible (~1/2"). Even with careful use of these probes results should be considered preliminary until verified with controlled impedance measurements. Even the best probes will interfere with circuit operation to some degree. Also, conductors, fingers etc. near the device will change measurement results.

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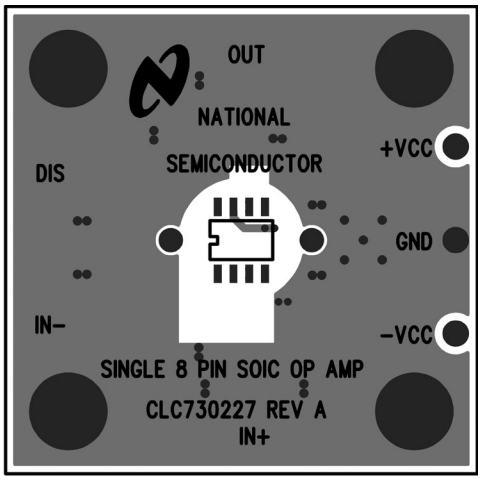

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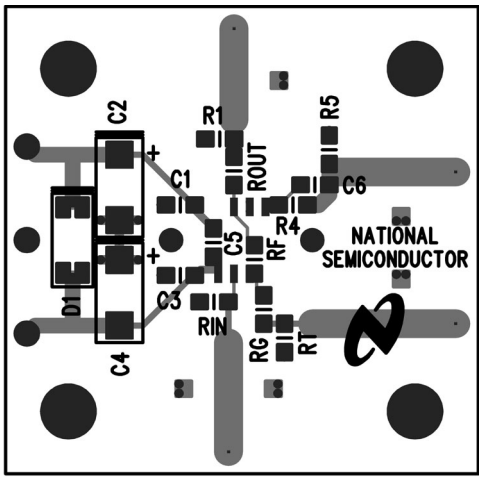

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SOIC Board Layout (Actual size = 1.5" x 1.5")

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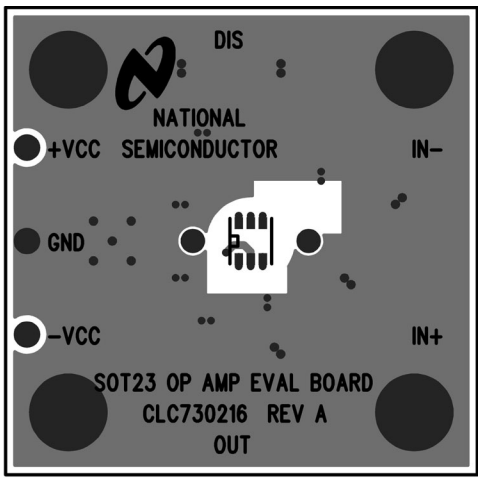

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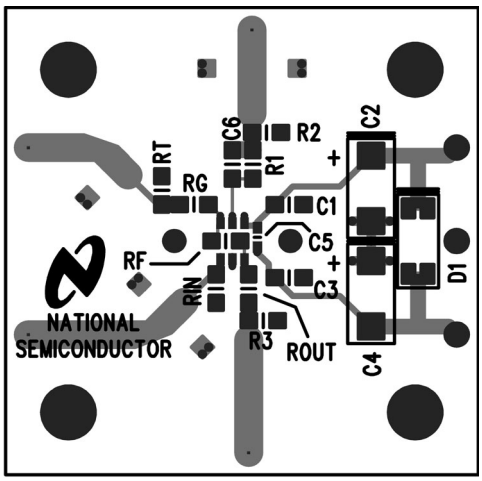

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SOT Board Layout (Actual size = 1.5" x 1.5")

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