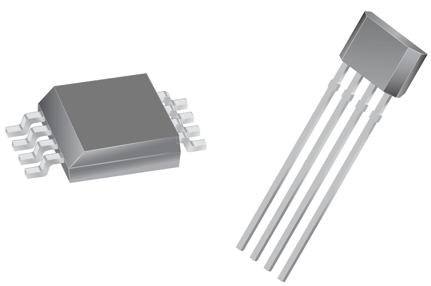
Ultra-Sensitive Dual-Channel Quadrature Hall-Effect Bipolar Switch

Features and Benefits

- Two matched Hall effect switches on a single substrate
- Sensor Hall element spacing approximately 1 mm
- Superior temperature stability
- 3.3 to 18 V operation
- Integrated ESD diode from OUTPUT and VCC pins to GND
- High-sensitivity switchpoints
- Robust structure for EMC protection
- Solid-state reliability

Package: 8 pin SOIC (suffix L), and 4 pin SIP (suffix K)



Not to scale

Description

The A3425 is a dual–output-channel, bipolar switch with each channel comprising a separate complete Hall-effect sensor circuit with dedicated Hall element and separate digital output for speed and direction signal processing capability. The independent Hall elements (E1 integrated with OUTPUTA, and E2 integrated with OUTPUTB) are photolithographically aligned to better than 1 µm. Maintaining this accurate mechanical location between the two active Hall elements eliminates the major manufacturing hurdle encountered in fine-pitch detection applications. The A3425 is a highly sensitive, temperature-stable magnetic sensing device, which is ideal for use in ring magnet-based speed and direction systems used in harsh automotive and industrial environments.

The A3425 contains two independent Hall effect switches, and has a monolithic IC that accurately locates the two Hall elements, E1 and E2, approximately 1 mm apart. The digital outputs are 90º out of phase so that the outputs are in quadrature, with the proper ring magnet design. This allows for easy processing of speed and direction signals. Extremely low-drift amplifiers guarantee symmetry between the switches to maintain signal

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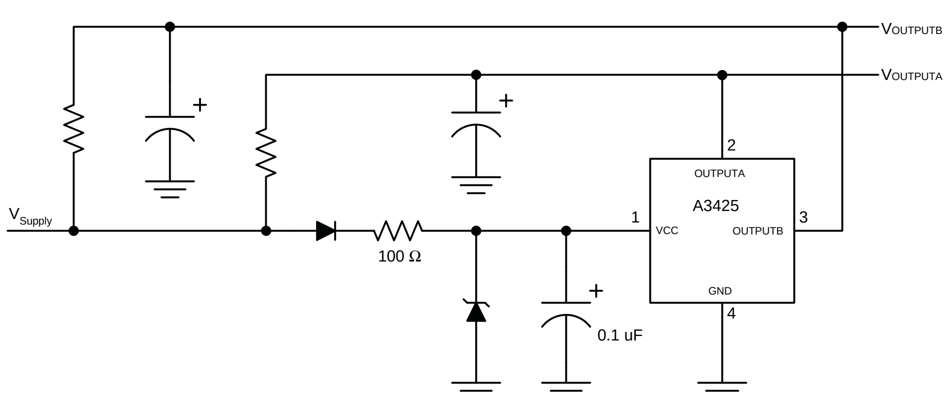
Typical Application



Using unregulated supply

Description (continued)

quadrature. The patented chopper stabilization technique cancels offsets in each channel, and provides stable operation over the operating temperature and voltage ranges. An on-chip regulator allows the use of this device over a wide operating voltage range. Post-assembly factory programming provides sensitive switchpoints that are symmetrical between the two switches.

The A3425 is available in a plastic 8-pin SOIC surface mount package (L) and a plastic 4-pin SIP (K), both in two operating temperature ranges. Each package is available in a lead (Pb) free version with 100% matte tin plated leadframe.

Selection Guide

Part Number	Packing[1]	Mounting	Ambient, T_A
A3425EK-T	Bulk, 500 pieces/bag	4-pin SIP through hole	–40ºC to 85ºC
~~A3425EL-T~~[2]	Bulk, 500 pieces/bag	8-pin SOIC surface mount	
A3425ELTR-T	13-in. reel, 3000 pieces/reel		
A3425LK-T	Bulk, 98 pieces/bag	4-pin SIP through hole	–40ºC to 150ºC
~~A3425LL-T~~[2]	Bulk, 500 pieces/bag	8-pin SOIC surface mount	
A3425LLTR-T	13-in. reel, 3000 pieces/reel		

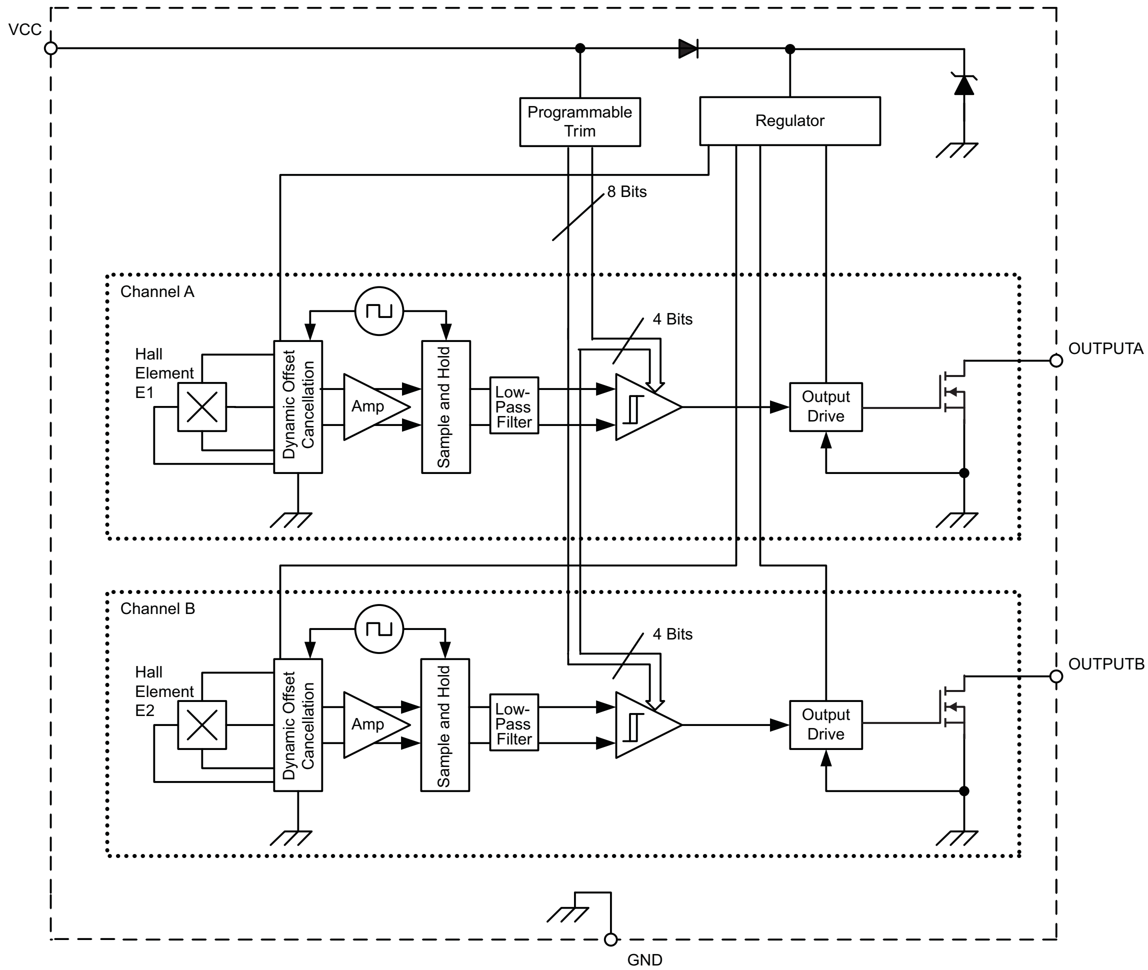
[1]Contact Allegro for additional packing options.

[2]Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 1, 2008. Deadline for receipt of LAST TIME BUY orders is May 1, 2008.

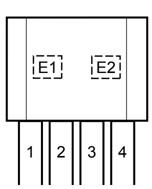
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		26.5	V
Reverse Battery Voltage	V_{RCC}		–16	V
Output Off Voltage	V_{OUTPUT}		V_{CC}	V
Output Sink Current	$I_{OUTPUT(Sink)}$		Internally Limited	–
Magnetic Flux Density	B		Unlimited	–
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

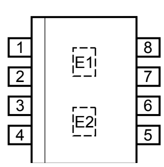
Functional Block Diagram



Package K



Package L



Terminal List Table

Pin Number		Name	Function
Package K	Package L		
1	1	VCC	Connects power supply to on-chip voltage regulator
2	2	OUTPUTA	Output from E1 via first Schmitt circuit
3	3	OUTPUTB	Output from E2 via second Schmitt circuit
4	4	GND	Terminal for ground connection
–	5-8	NC	No connection

OPERATING CHARACTERISTICS **Valid over operating temperature ranges unless otherwise noted; typical data applies to V_{CC} = 12 V, and T_A = 25ºC**

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage[1]	V_{CC}	Operating; $T_A \leq 150°C$	3.3	–	18	V
Output Leakage Current	$I_{OUTPUT(OFF)}$	Either output	–	< 1	10	μA
Output Rise Time	t_r	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	1.8	–	μs
Output Fall Time	t_f	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	1.2	–	μs
Supply Current	$I_{CC(OFF)}$	$B < B_{RP(A)}$,$B < B_{RP(B)}$	–	3.5	6.0	mA
	$I_{CC(ON)}$	$B > B_{OP(A)}$,$B > B_{OP(B)}$	–	4.0	6.0	mA
Low Output Voltage	$V_{OUTPUT(ON)}$	Both outputs; $I_{OUTPUT(SINK)}$ = 20 mA; $B > B_{OP(A)}$, $B > B_{OP(B)}$	–	160	500	mV
Output Sink Current	$I_{OUTPUT(SINK)}$		–	–	20	mA
Output Sink Current, Continuous[2]	$I_{OUTPUT(SINK)C}$	$T_J < T_{J(max)}$,V_{OUTPUT} = 12 V	–	–	70	mA
Output Sink Current, Peak[3]	$I_{OUTPUT(SINK)P}$	t < 3 seconds	–	–	220	mA
Chopping Frequency	f_C		–	340	–	kHz
TRANSIENT PROTECTION CHARACTERISTICS						
Supply Zener Voltage	V_Z	I_{CC} = 15 mA	28	33	37	V
Supply Zener Current[4]	I_Z	V_S = 28 V	–	–	9.0	mA
Reverse-Battery Current	I_{RCC}	V_{RCC} = –18 V, $T_J < T_{J(max)}$	–	2	15	mA

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OPERATING CHARACTERISTICS (continued) **Valid over operating temperature ranges unless otherwise noted; typical data applies to V_{CC} = 12 V, and T_A = 25ºC**

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max	Units
MAGNETIC CHARACTERISTICS, K Package[5]						
Operate Point: $B > B_{OP}$	$B_{OP(A)}$, $B_{OP(B)}$		–	7	35	G
Release Point: $B < B_{RP}$	$B_{RP(A)}$, $B_{RP(B)}$		–35	–7	–	G
Hysteresis: $B_{OP(A)} – B_{RP(A)}$, $B_{OP(B)} – B_{RP(B)}$	$B_{HYS(A)}$, $B_{HYS(B)}$		5	16	40	G
Symmetry: Channel A, Channel B, $B_{OP(A)} + B_{RP(A)}$, $B_{OP(B)} + B_{RP(B)}$	SYM_A, SYM_B		–40	–	40	G
Operate Symmetry: $B_{OP(A)} – B_{OP(B)}$	$SYM_{AB(OP)}$		–30	–	30	G
Release Symmetry: $B_{RP(A)} – B_{RP(B)}$	$SYM_{AB(RP)}$		–30	–	30	G
MAGNETIC CHARACTERISTICS, L Package[5]						
Operate Point: $B > B_{OP}$	$B_{OP(A)}$, $B_{OP(B)}$		–	7	30	G
Release Point: $B < B_{RP}$	$B_{RP(A)}$, $B_{RP(B)}$		–30	–7	–	G
Hysteresis: $B_{OP(A)} – B_{RP(A)}$, $B_{OP(B)} – B_{RP(B)}$	$B_{HYS(A)}$, $B_{HYS(B)}$		5	14	35	G
Symmetry: Channel A, Channel B, $B_{OP(A)} + B_{RP(A)}$, $B_{OP(B)} + B_{RP(B)}$	SYM_A, SYM_B		–35	–	35	G
Operate Symmetry: $B_{OP(A)} – B_{OP(B)}$	$SYM_{AB(OP)}$		–25	–	25	G
Release Symmetry: $B_{RP(A)} – B_{RP(B)}$	$SYM_{AB(RP)}$		–25	–	25	G

[1] When operating at maximum voltage, never exceed maximum junction temperature, $T_{J(max)}$. Refer to power derating curve charts.
[2] Device will survive the current level specified, but operation within magnetic specification cannot be guaranteed.
[3] Short circuit of the output to VCC is protected for the time duration specified.
[4] Maximum specification limit is equivalent to $I_{CC(max)}$ + 3 mA.
[5] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity).

EMC

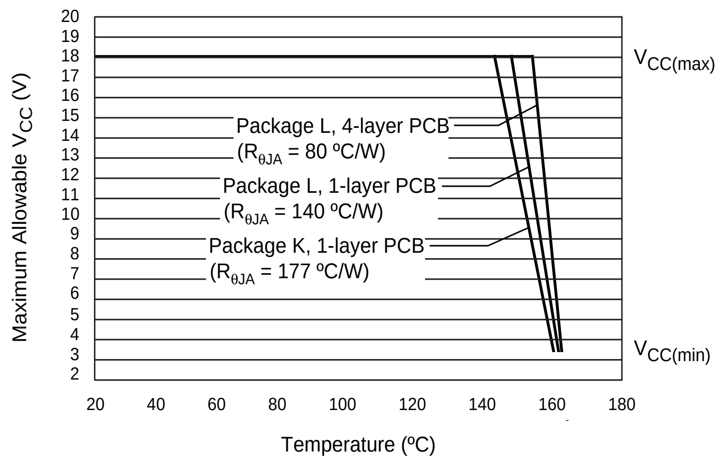
Contact Allegro MicroSystems for EMC performance.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

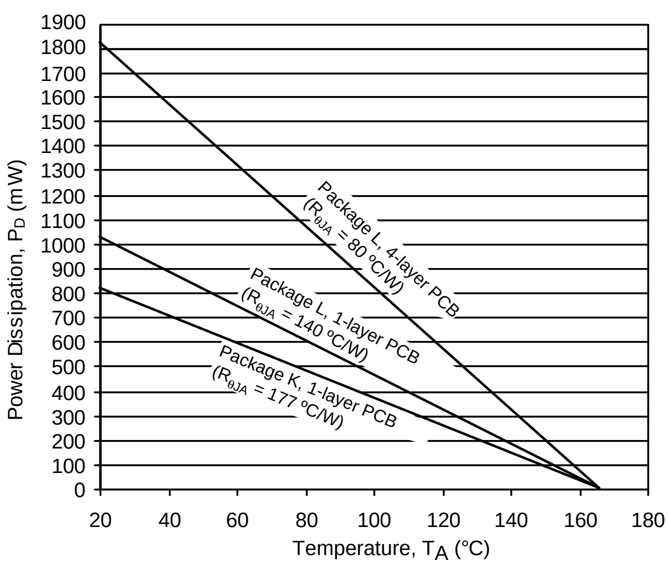
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package K, 1-layer PCB with copper limited to solder pads	177	ºC/W
		Package L-8 pin, 1-layer PCB with copper limited to solder pads	140	ºC/W
		Package L-8 pin, 4-layer PCB based on JEDEC standard	80	ºC/W

*Additional thermal data available on the Allegro Web site.

Power Derating Curve



Power Dissipation versus Temperature



Functional Description

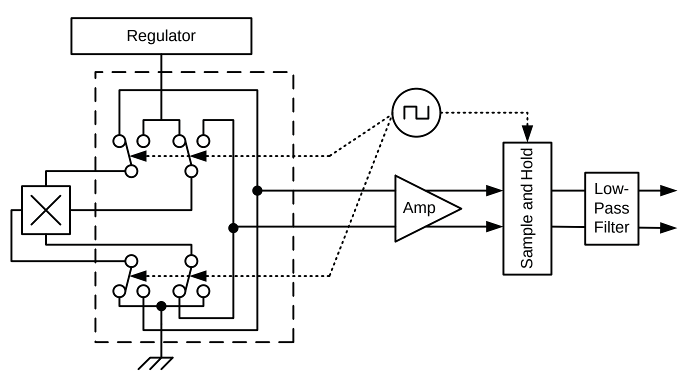
Chopper-Stabilized Technique

When using Hall effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall device. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, *dynamic quadrature offset cancellation*, removes key sources of the output drift induced by thermal and mechanical stress. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetically-induced signal to recover its original spectrum at the baseband level, while the dc offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated dc offset is suppressed.

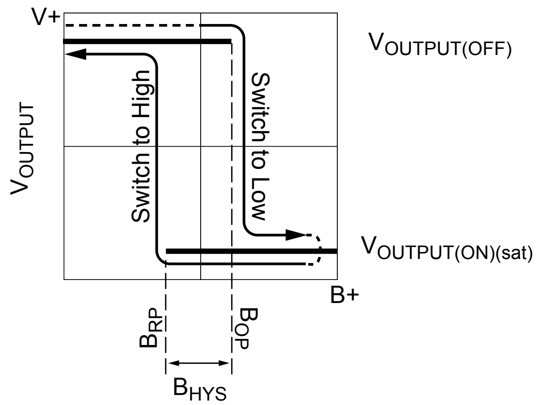
The chopper stabilization technique uses a 170 kHz high-frequency clock. The Hall element chopping occurs on each clock edge, resulting in a 340 kHz chop frequency. This high-frequency operation allows for a greater sampling rate, which produces higher accuracy and faster signal processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stress. The disadvantage to this approach is that jitter, also known as *360° repeatability*, can be induced on the output signal. The *sample-and-hold* process, used by the demodulator to store and recover the signal, can slightly degrade the signal-to-noise ratio. This is because the process generates replicas of the noise spectrum at the baseband, causing a decrease in jitter performance. However, the improvement in switchpoint performance, resulting from the reduction of the effects of thermal and mechanical stress, outweighs the degradation in the signal-to-noise ratio.

This technique produces devices that have an extremely stable quiescent Hall element output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits. This process is illustrated in the following diagram.

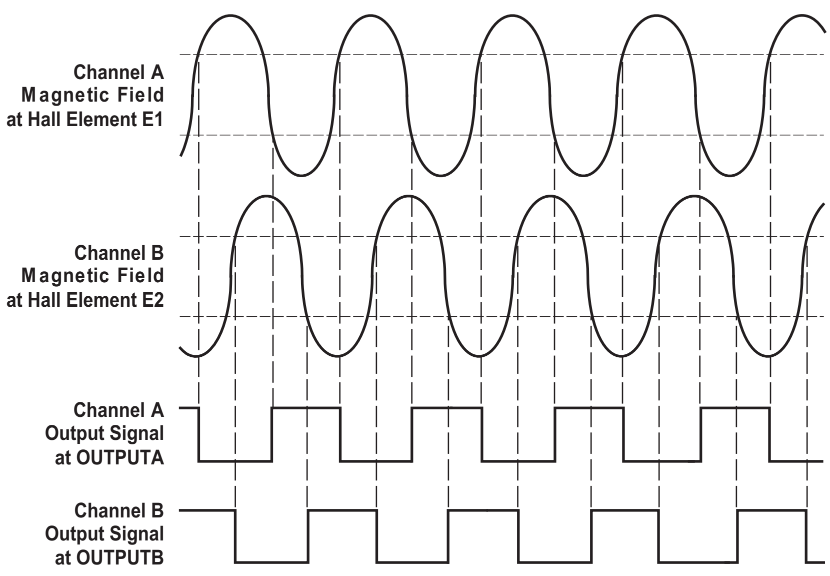


Chopper stabilization circuit (dynamic quadrature offset cancellation)

Typical Applications Operation



Output voltage in relation to sensed magnetic flux density. Output on each channel independently follows the same pattern of transition through B_{OP} followed by transition through B_{RP}.



Quadrature output signal configuration. The outputs of the two output channels have a phase difference of 90º when used with a properly designed magnet that has an optimal pole pitch of twice the Hall element spacing of 1.0 mm.

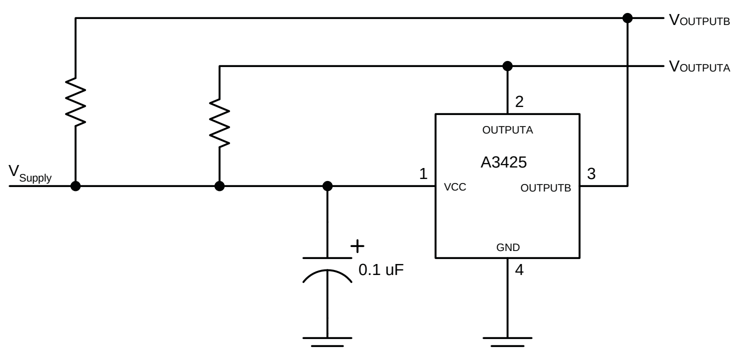
Typical Applications Circuits

This device requires minimal protection circuitry during operation with a low-voltage regulated line. The on-chip voltage regulator provides immunity to power supply variations between 3.3 and 18 V. Because the device has open-drain outputs, pull-up resistors must be included.

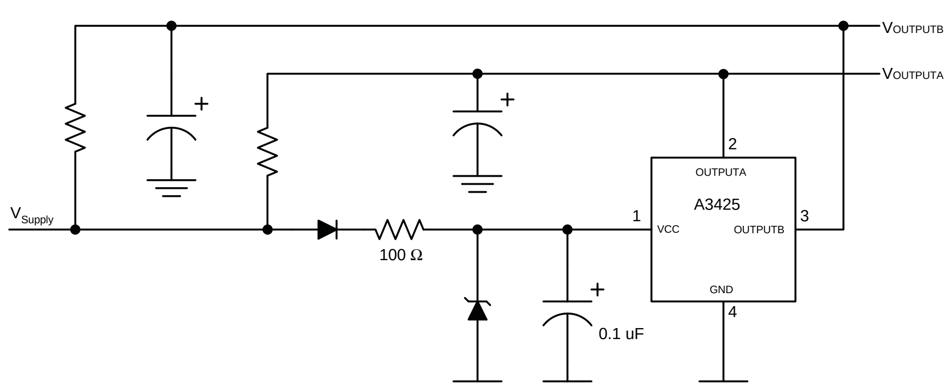
If protection against coupled and injected noise is required, then a simple low-pass filter on the supply (RC) and a filtering capacitor on each of the outputs may also be needed, as shown in the unregulated supply diagram.

For applications in which the device receives its power from unregulated sources, such as a car battery, full protection is generally required to protect the device against supply-side transients. Specifications for such transients vary for each application, so the design of the protection circuit should be optimized for each application.

For example, the circuit shown in the unregulated supply diagram includes a Zener diode that offers high voltage load-dump protection and noise filtering by means of a series resistor and capacitor. In addition, it includes a series diode that protects against high-voltage reverse battery conditions.



Regulated supply



Unregulated supply

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000
www.allegromicro.com

Typical Thermal Performance

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 12$ V, $I_{CC} = 4$ mA, and $R_{\theta JA} = 140$ °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12 \text{ V} \times 4 \text{ mA} = 48 \text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 48 \text{ mW} \times 140 \text{ °C/W} = 7°C$$

$$T_J = T_A + \Delta T = 25°C + 7°C = 32°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 150°C$, package L, using minimum-K PCB

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 140$ °C/W, $T_{J(max)} = 165°C$, $V_{CC(max)} = 18$ V, and $I_{CC(max)} = 6$ mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 140 \text{ °C/W} = 107 \text{ mW}$$

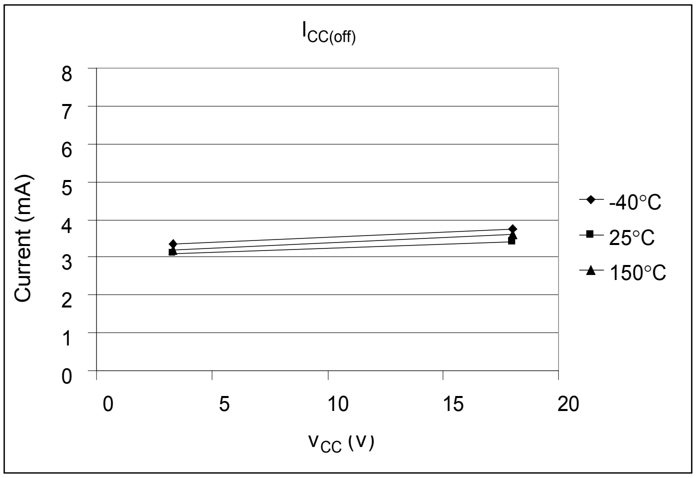
Finally, invert equation 1 with respect to voltage:

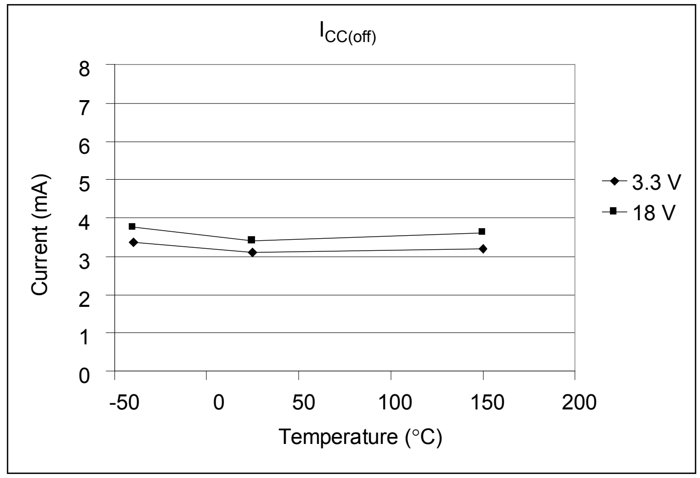
$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 107 \text{ mW} \div 6 \text{ mA} = 18 \text{ V}$$

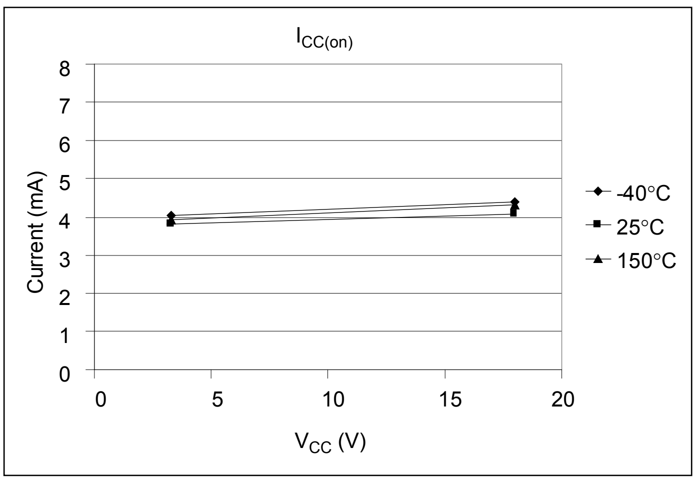
The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

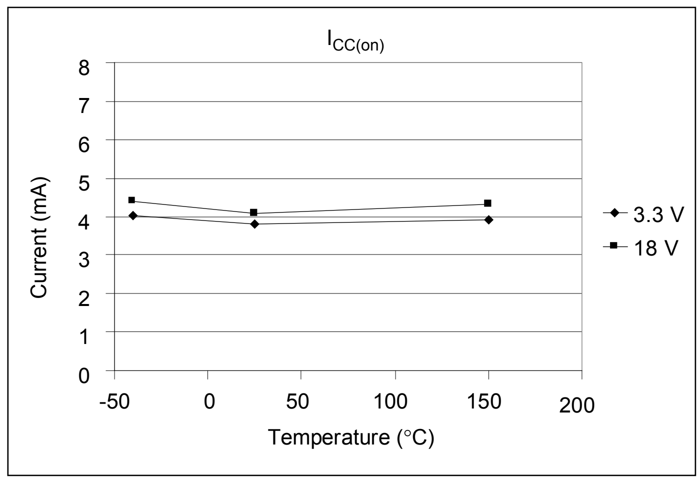
Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

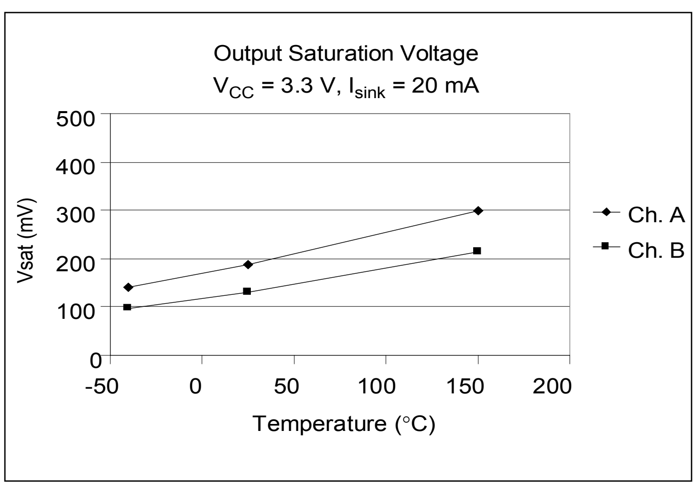
Electrical Operating Characteristics, Package L



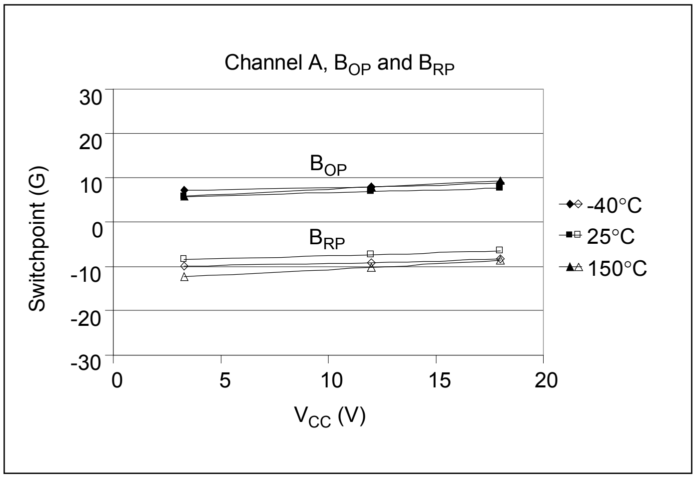


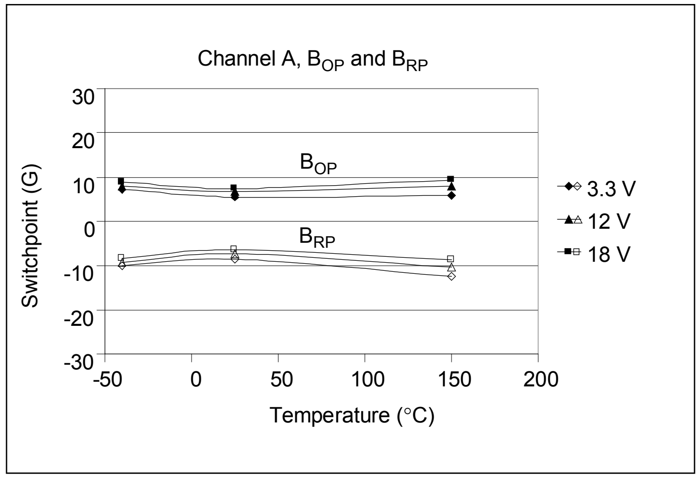


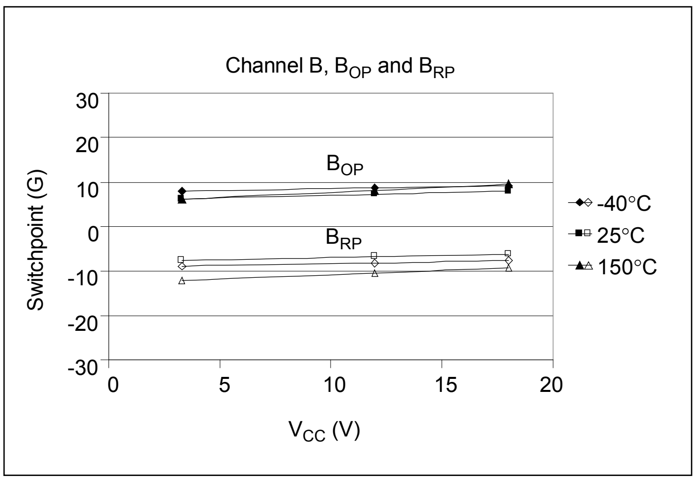


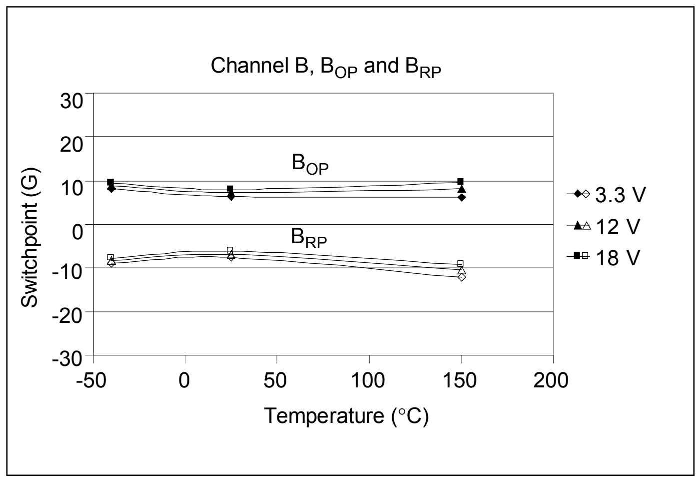


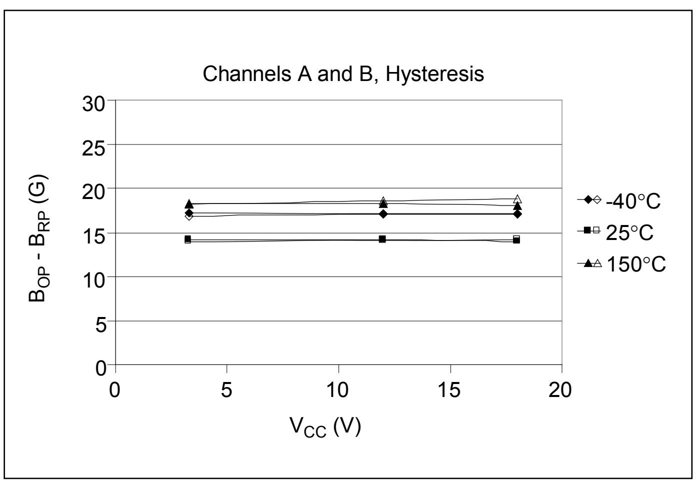
Magnetic Operating Characteristics, Package L

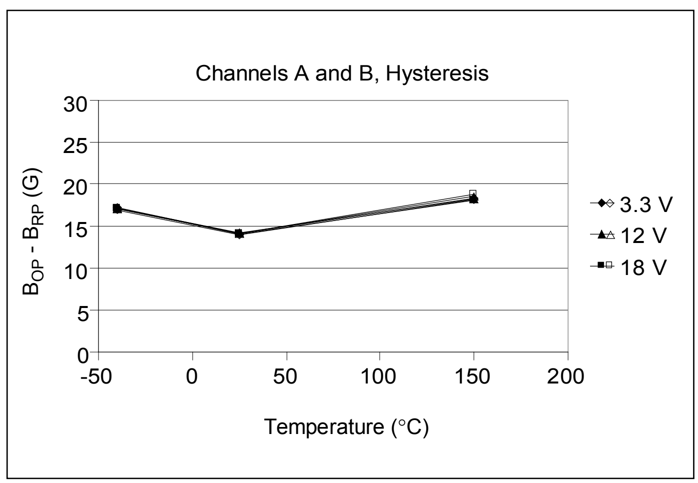






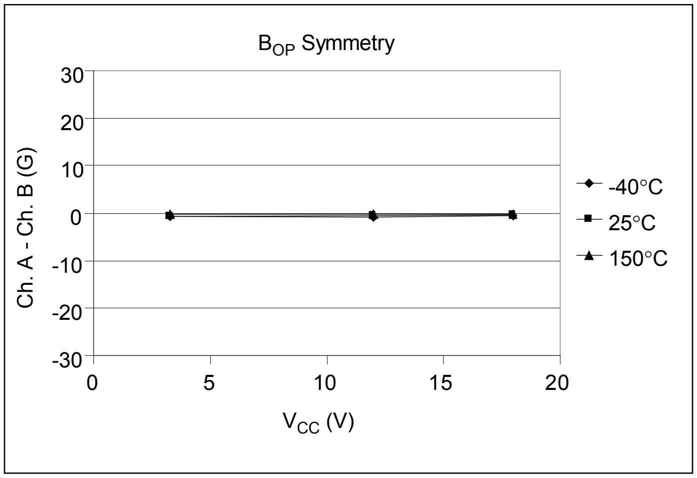


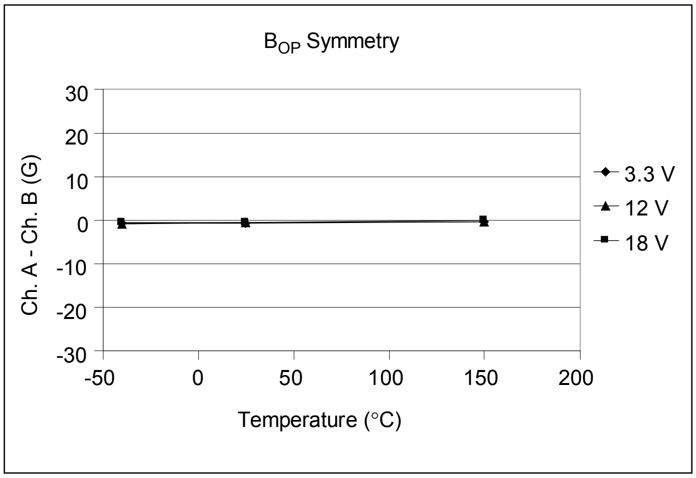


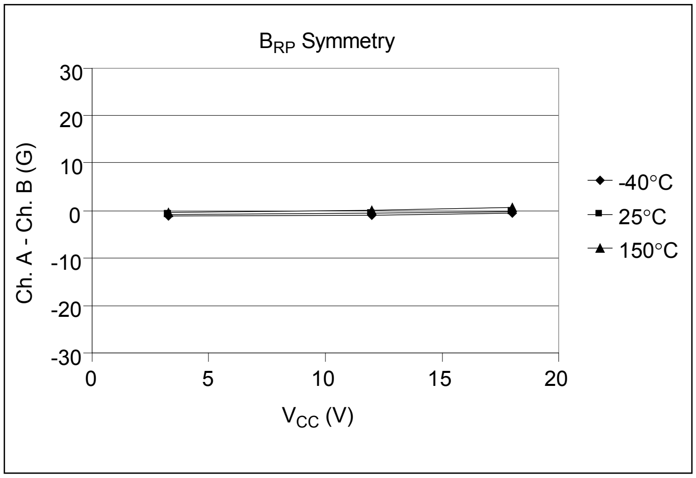


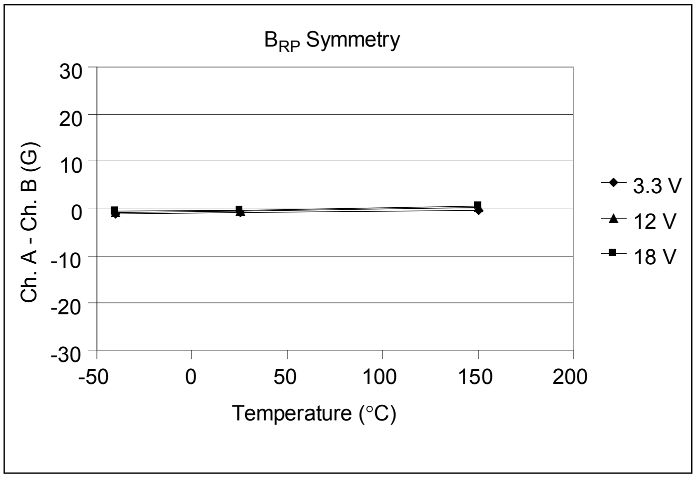
Additional magnetic characteristics on next page

Magnetic Operating Characteristics, Package L (*continued*)



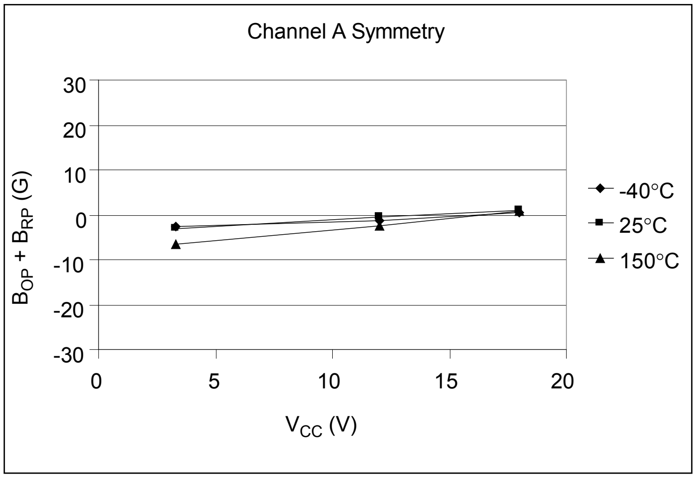


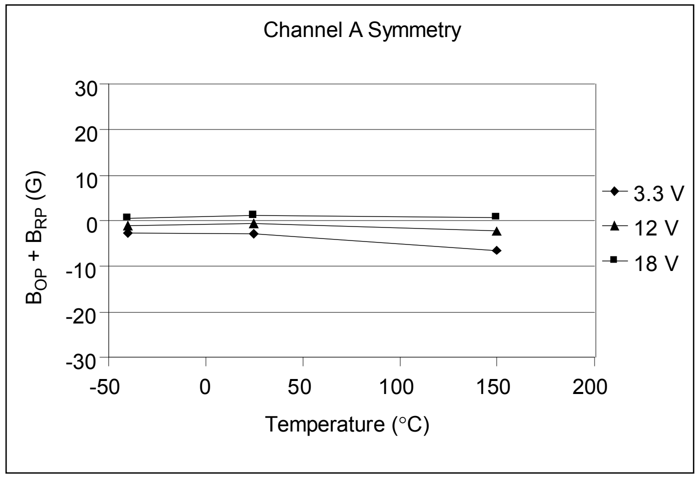


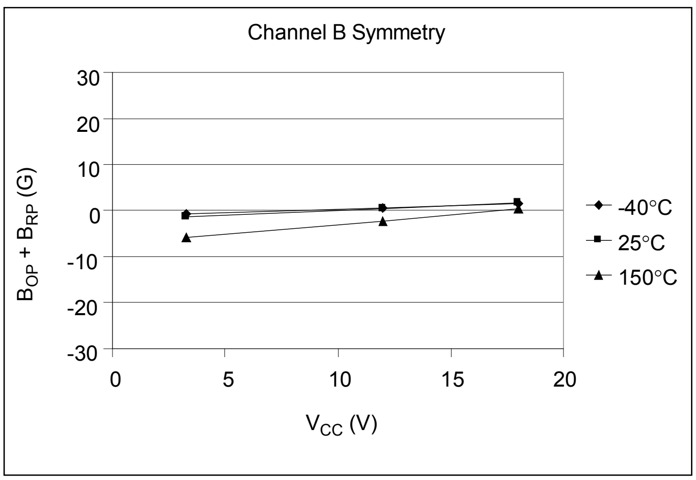


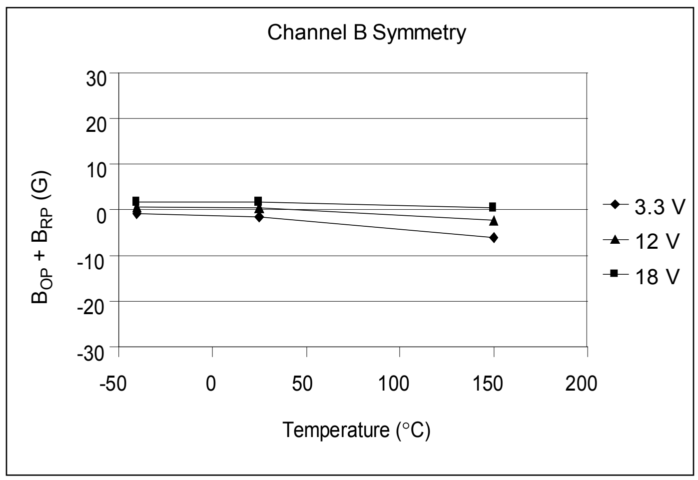
Additional magnetic characteristics on next page

Magnetic Operating Characteristics, Package L (*continued*)

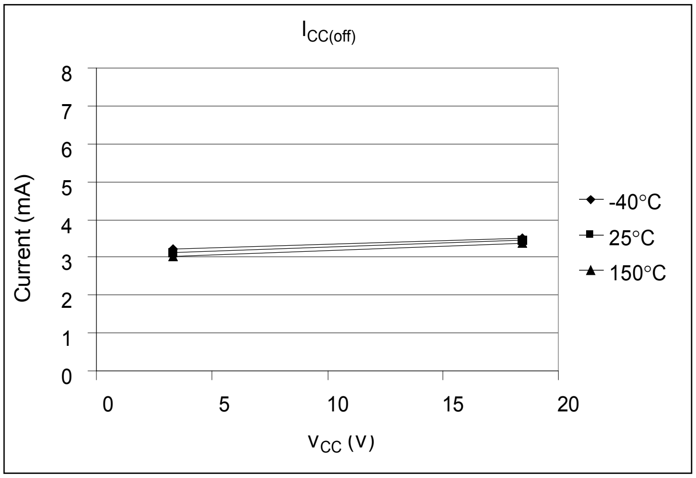


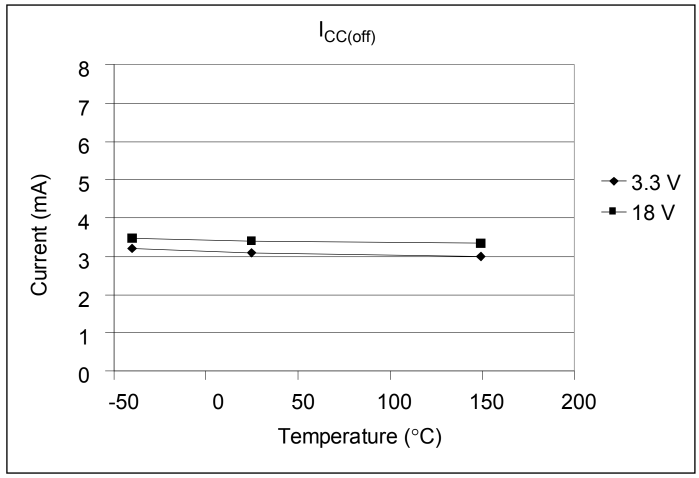


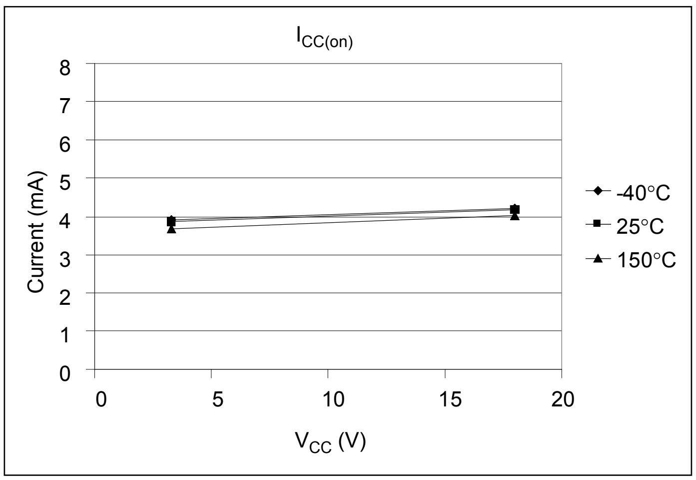


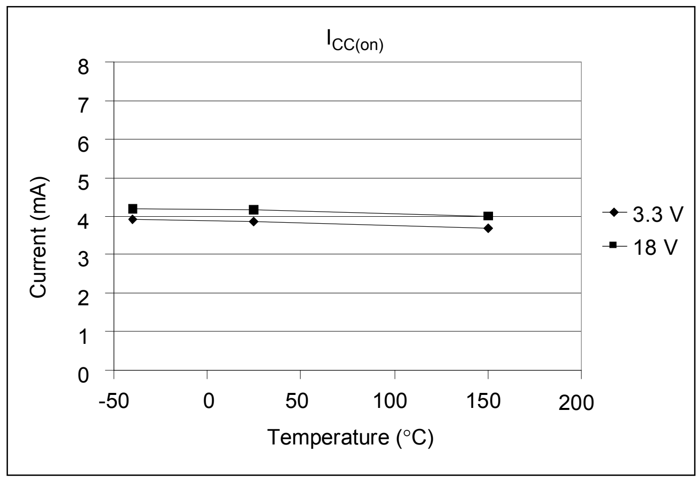


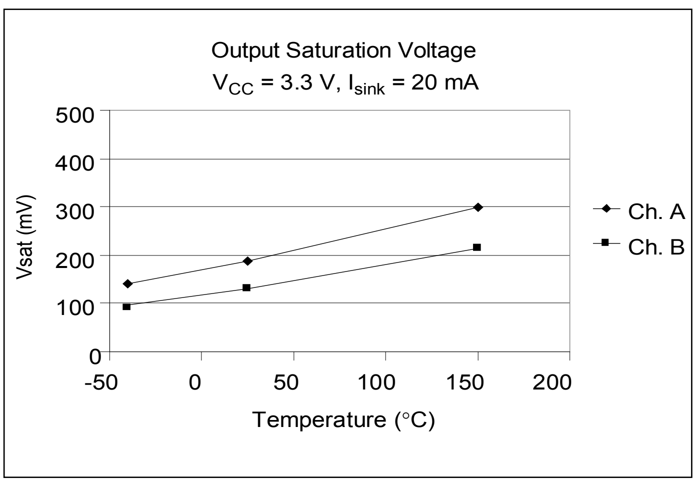
Electrical Operating Characteristics, Package K



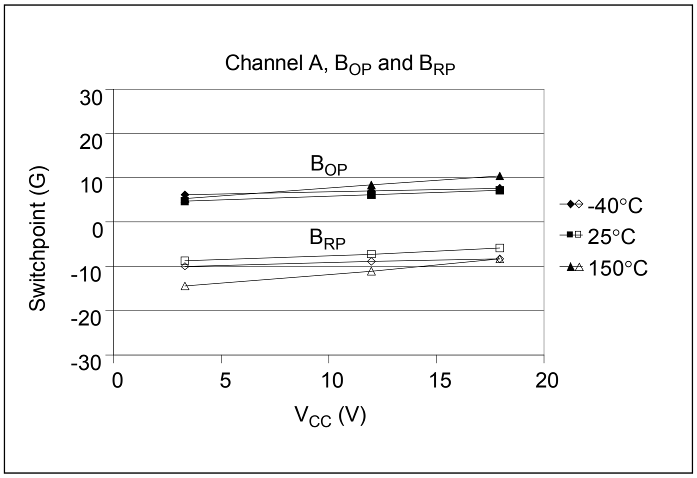


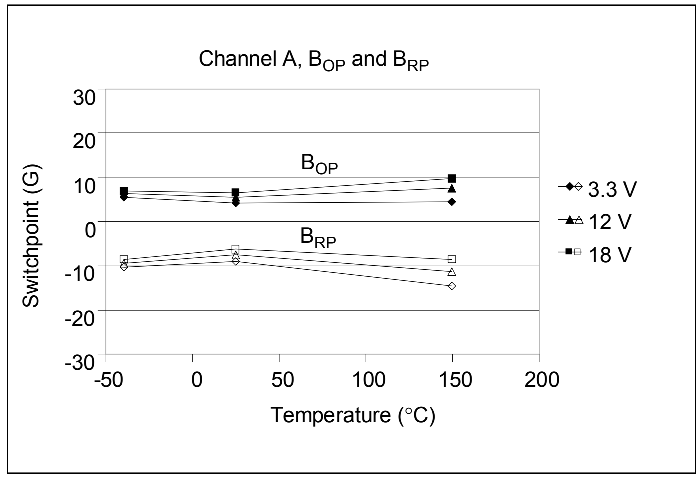


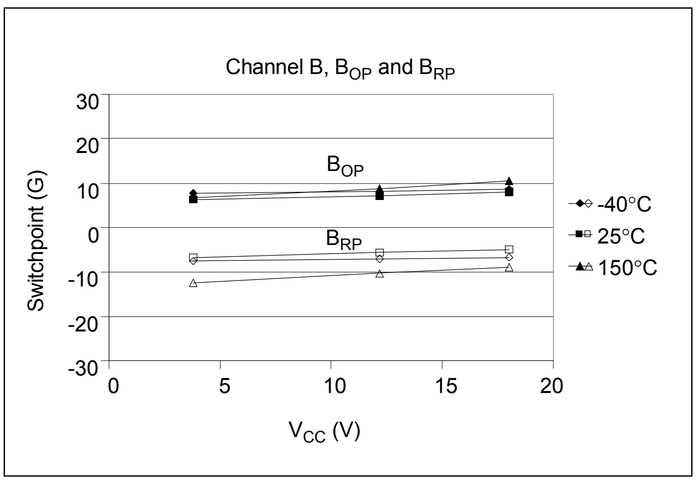


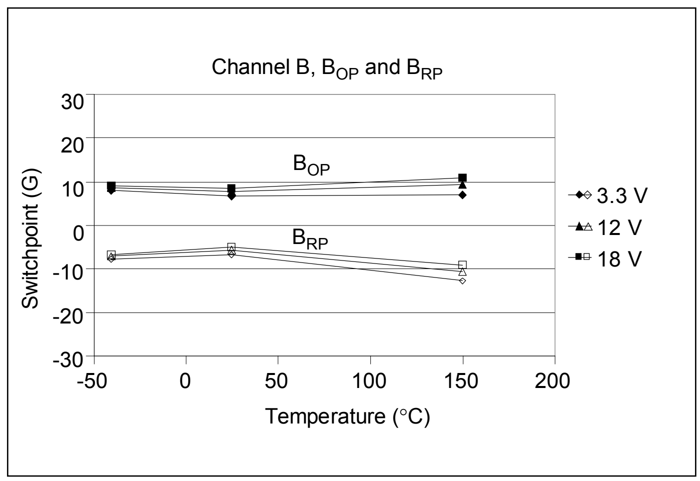


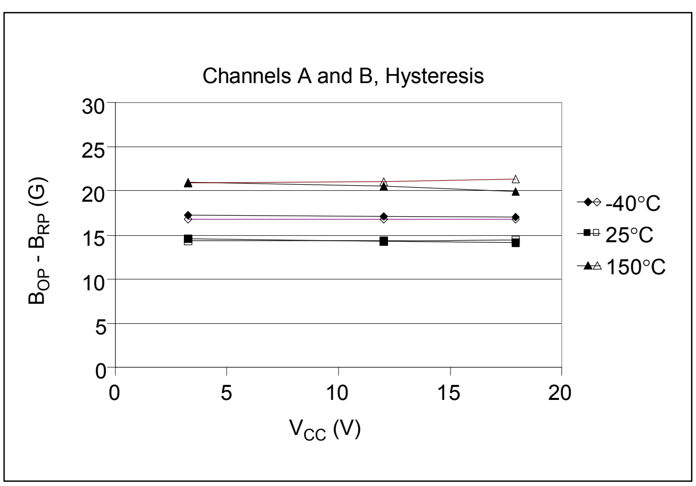
Magnetic Operating Characteristics, Package K

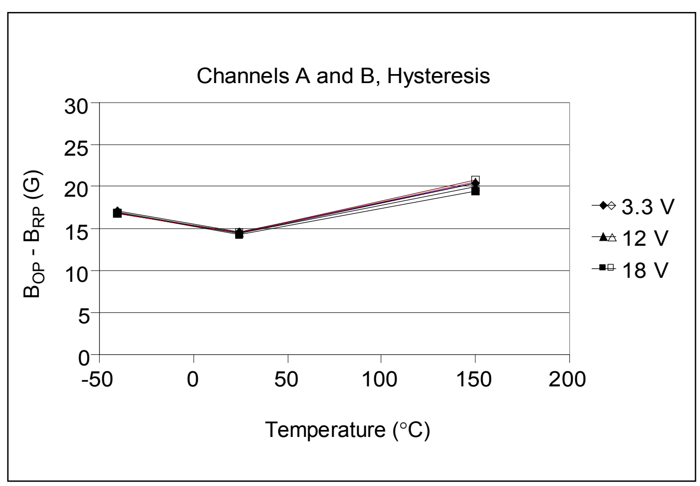






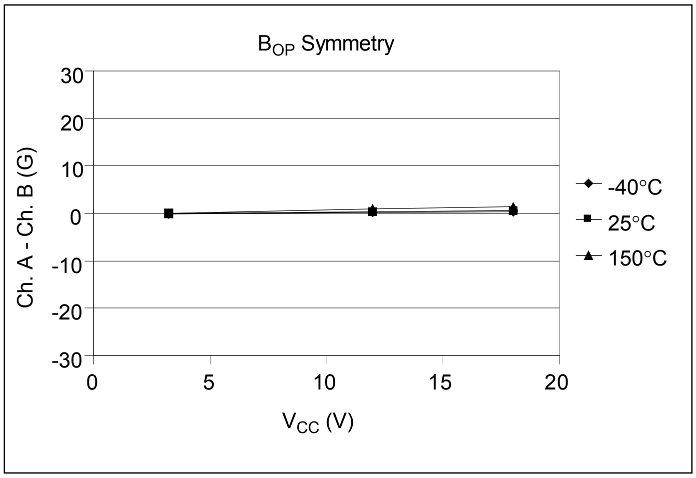


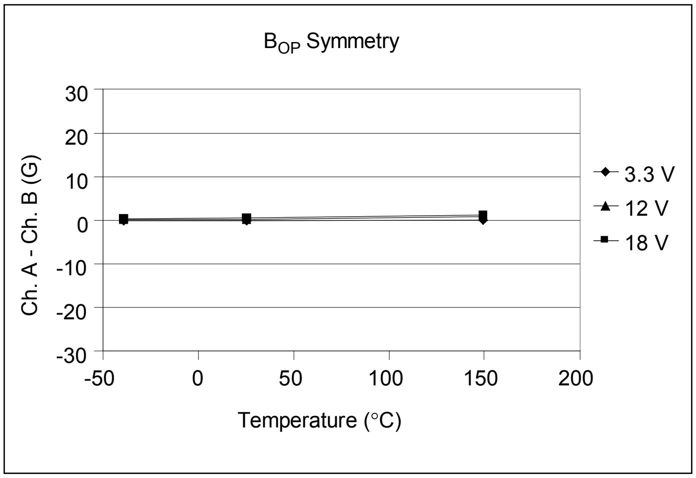


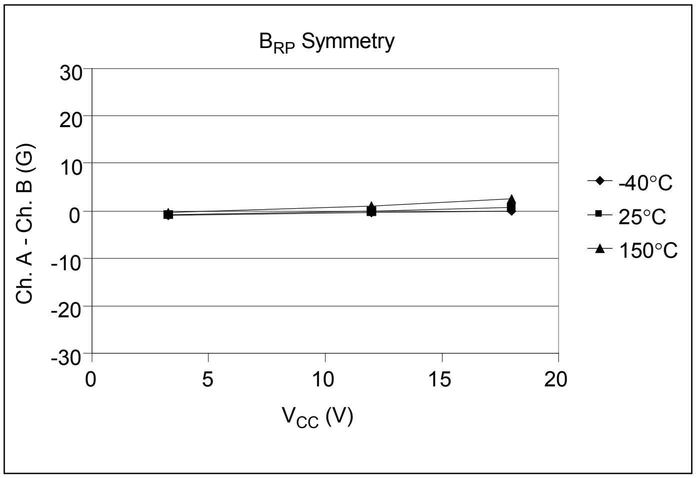


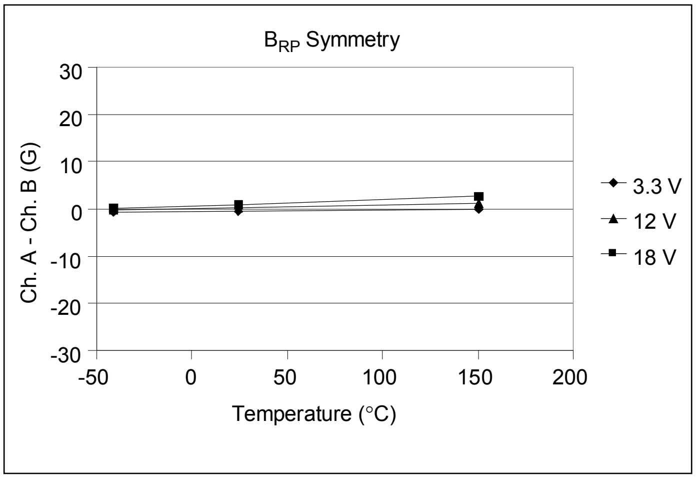
Additional magnetic characteristics on next page

Magnetic Operating Characteristics, Package K (*continued*)









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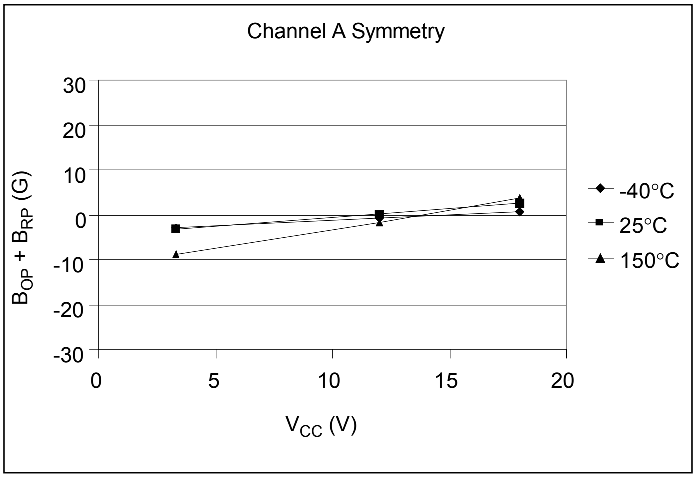
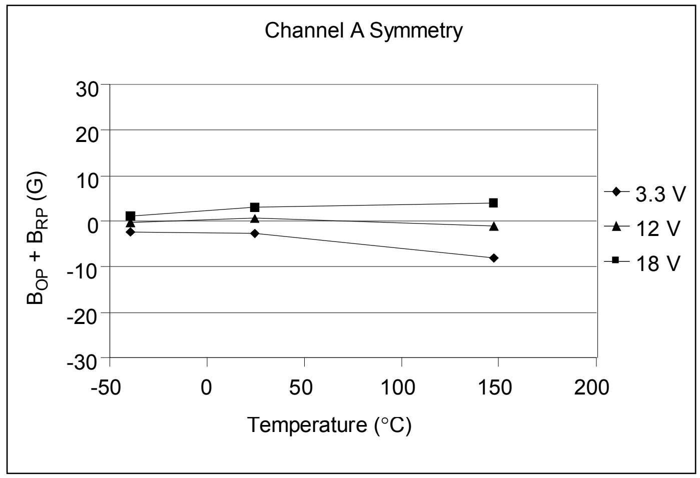
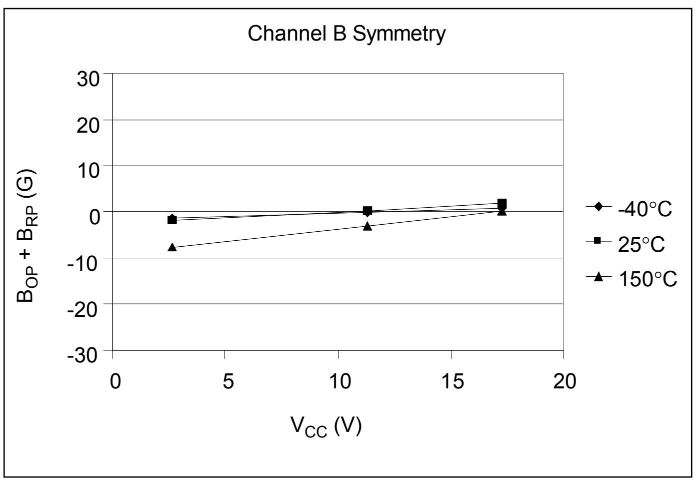
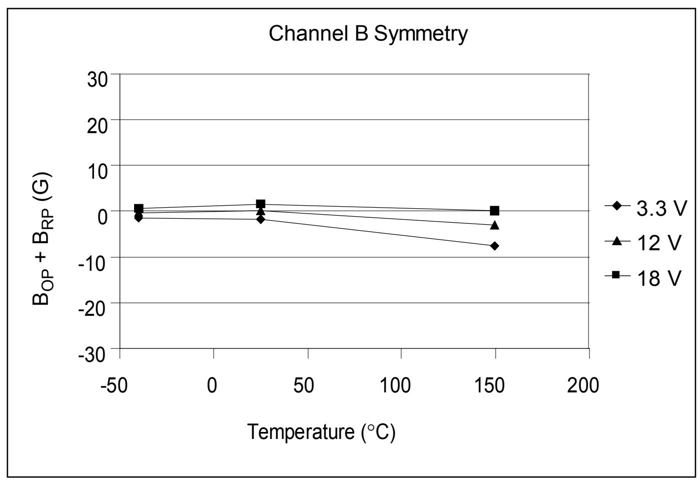
Magnetic Operating Characteristics, Package K (*continued*)

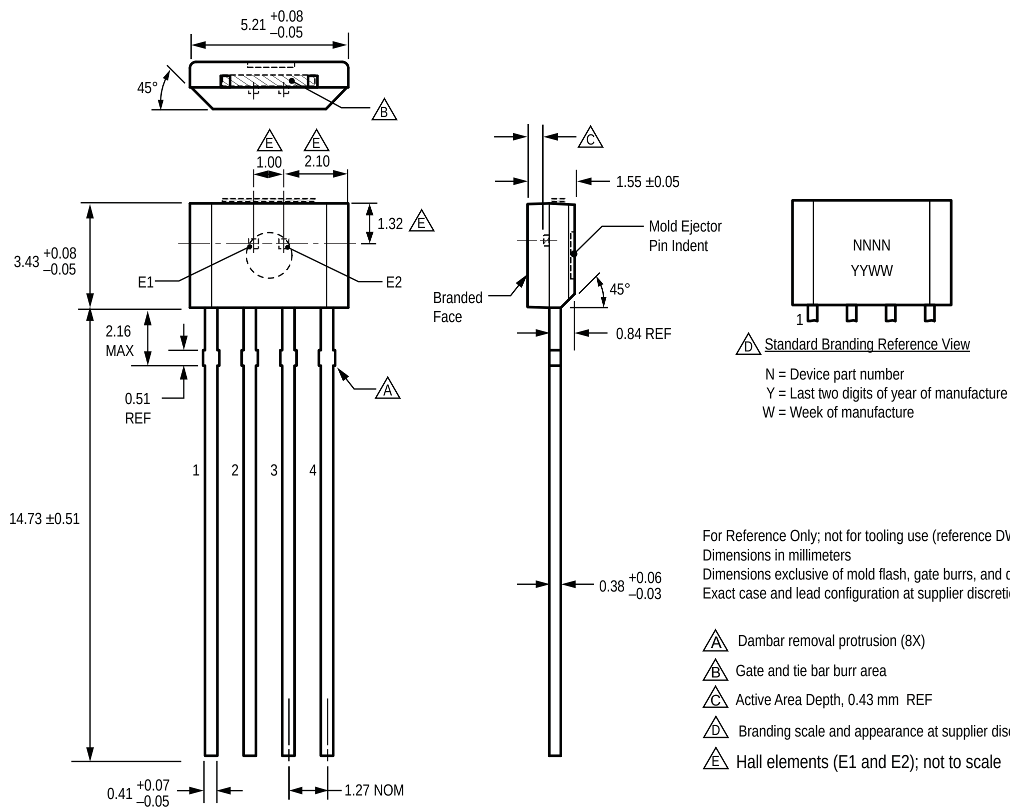








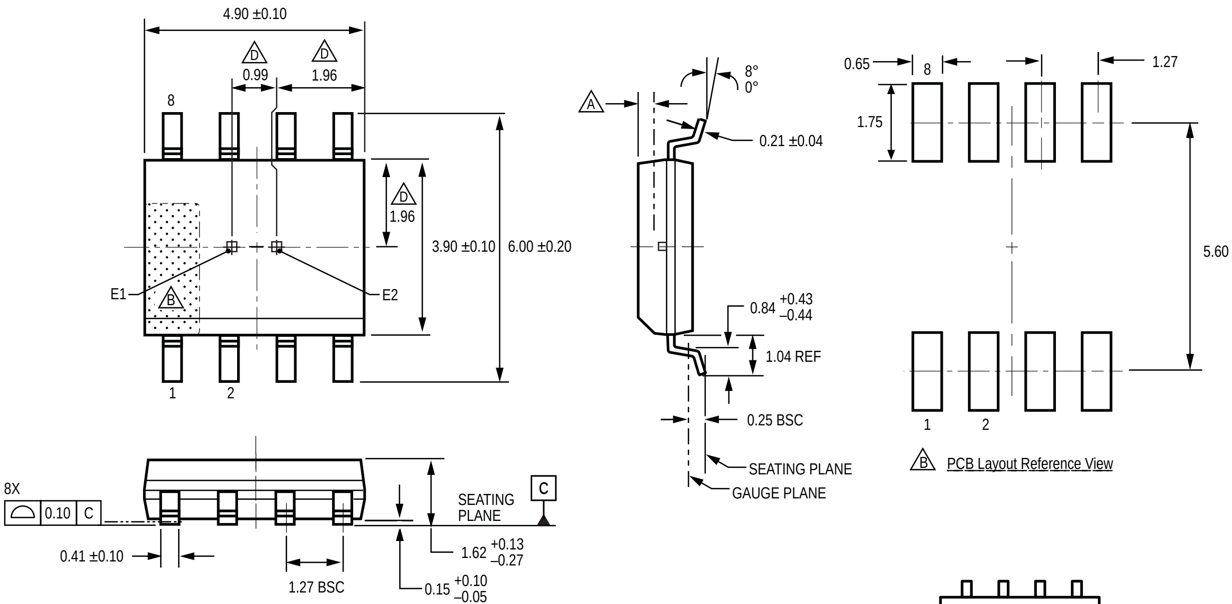
Package K, 4-pin SIP

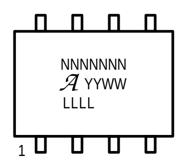


For Reference Only; not for tooling use (reference DWG-9010)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

- A: Dambar removal protrusion (8X)
- B: Gate and tie bar burr area
- C: Active Area Depth, 0.43 mm REF
- D: Branding scale and appearance at supplier discretion
- E: Hall elements (E1 and E2); not to scale

Package L, 8-pin SOIC





For Reference Only; not for tooling use (reference DWG-9204)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A: Active Area Depth, 0.40 mm REF
B: Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances
C: Branding scale and appearance at supplier discretion
D: Terminal #1 mark area

C: Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

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