

7490
276-1808

DIVIDE BY 2/5, BCD COUNTER

GENERAL DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

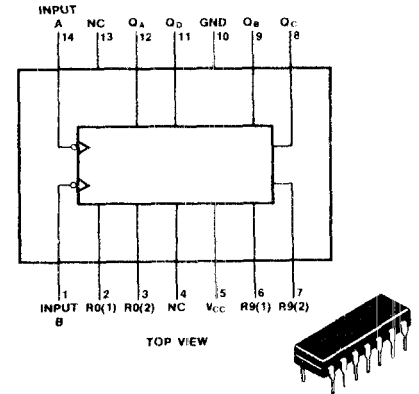
This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

To use maximum count length (decade, divide-by-twelve, or four-bit binary, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

TYPICAL RATINGS

Typical power dissipation..... 145 mW
 Count frequency..... 42 MHz
 High Level Input Voltage..... (Min) 2V
 Low Level Input Voltage..... (Max) 0.8V
 High Level Input Current..... 800µA
 Low Level Output Current..... (Max) 16 mA

PIN CONNECTION



TRUTH TABLES

RESET/COUNT TRUTH TABLE

RESET INPUTS				OUTPUT			
R0(1)	R0(2)	R9(1)	R9(2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

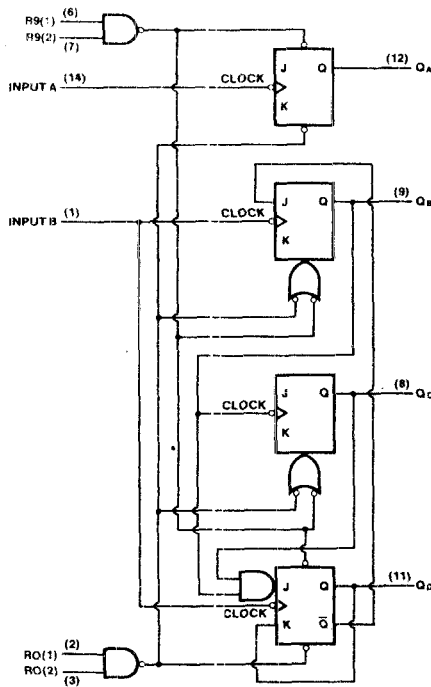
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LOGIC DIAGRAM



The J and K inputs shown without connection are for reference only and are functionally at a high level.

Notes:

- (A) Output Q_A is connected to input B for BCD count.
- (B) Output Q_D is connected to input A for bi-quinary count.