AN3161
Application note

Using the STGW35HF60WD advanced PT IGBT in parallel

Introduction

When two or more IGBTs are connected in parallel to improve the total efficiency in high output power systems, special care is required to ensure that current sharing between the devices is as equal as possible. Current sharing is mainly influenced by differences in IGBT static parameters, circuitry layout (both driving and power) and thermal imbalances. All of these elements must be considered, especially when PT (punch-through) IGBTs work in parallel, due to their negative $V_{CE(sat)}$ coefficient. In order to provide the most efficient IGBT to the market while supporting reliable and easier paralleling for higher power level applications, ST offers the STGW35HF60WD 35 A, 600 V ultra fast IGBT with $V_{CE(sat)}$ selection. This device is explained in greater detail in *Section 3: New advanced planar PT STGW35HF60WD*.

Contents

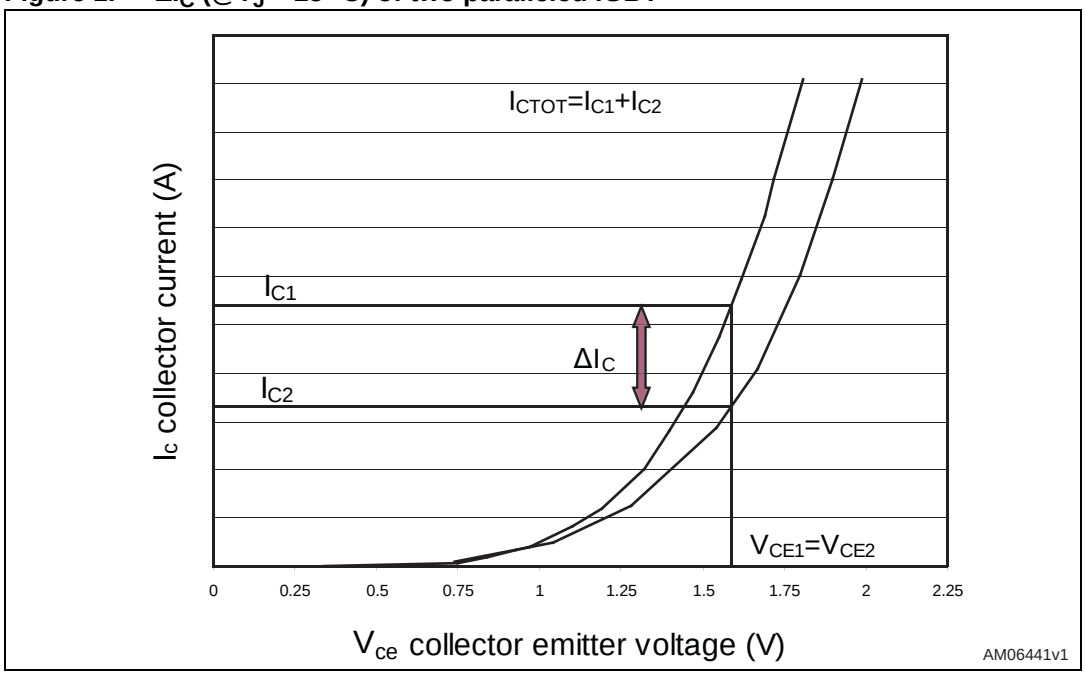
List of figures

1 Saturation voltage impact on parallel

1.1 PT, NPT and trench field stop

PT IGBTs (including those offered by STMicroelectronics) have typically negative $V_{CE(sat)}$ coefficients at current operative levels. This has a very important effect when two devices work in parallel. Due to their difference in static output characteristics, the one with the lowest static $V_{CE(sat)}$ carries more current than the other, as shown in *Figure 1*. The ΔI_C is the static current difference established at the beginning.

Figure 1. ΔI_C (@T_J = 25 °C) of two paralleled IGBT

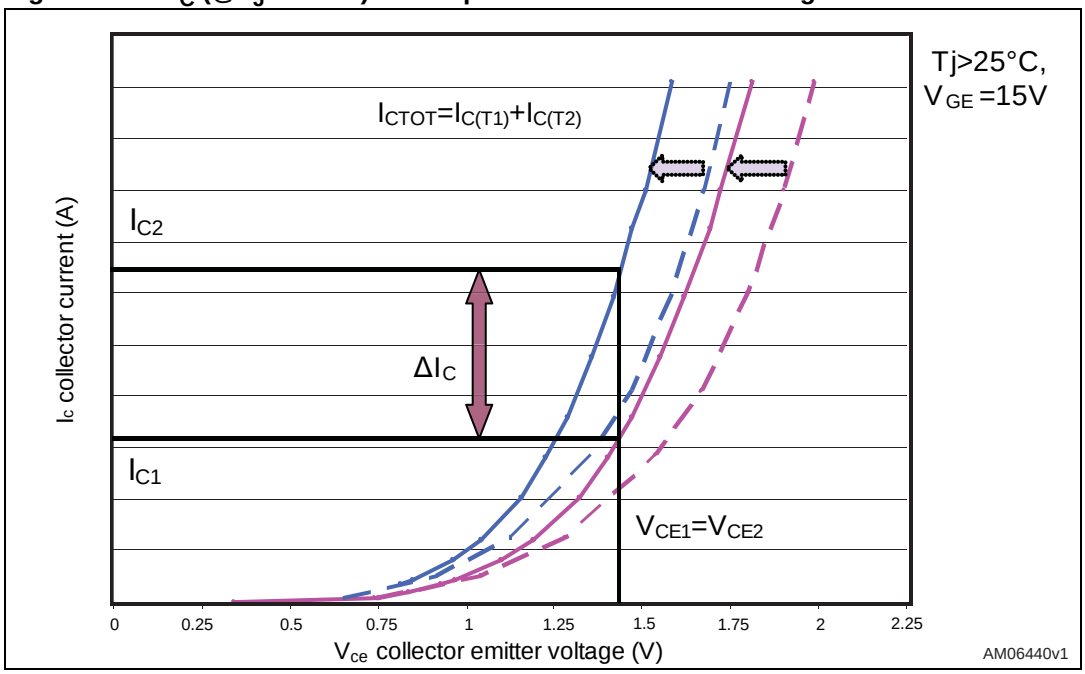


Assuming the same T_J at the beginning, the IGBT carrying higher current dissipates more power than the other, and its T_J increases. As a consequence, its $V_{CE(sat)}$ decreases and the current of the IGBT increases further. The IGBT carrying less current also decreases its static $V_{CE(sat)}$ as a consequence of the common V_{CE}, and its current must satisfy the following equation:

Equation 1

$$I_{CTOT} = I_{C1(T1)} + I_{C2(T2)}$$

Figure 2. ΔI_C (@T_J > 25 °C) of two paralleled IGBT without negative feedback



As a consequence of the negative $V_{CE(sat)}$ coefficient, a higher ΔI_C is established at high T_J (*Figure 2*). This can cause thermal instability if an accurate negative feedback is not implemented. NPT and field stop IGBTs have positive $V_{CE(sat)}$ coefficients (the latter typically starting from low current levels). When working in parallel the one carrying the higher current increases its temperature, which causes a $V_{CE(sat)}$ increase. This means that, at the same on-state voltage level, the current does not increase with temperature as in PT IGBTs; this guarantees an intrinsic balancing mechanism, preventing thermal runaway.

2 General guidelines on paralleling

2.1 Thermal system impact

In order to guarantee the satisfactory performance of paralleled devices, regardless of the IGBT technology used, it is recommended to place them on the same heatsink, very close together. If the IGBTs are sufficiently close, the one with the higher T_J will heat its neighbor, improving temperature and current sharing. PT IGBTs in particular benefit from the common heatsink, as it balances the negative $V_{CE(sat)}$ coefficient, which prevents thermal runway. If the thermal system impact is considered on paralleling, the mutual thermal resistance between the two junctions is the most important factor impacting on the dynamic ΔI_C at high temperatures. If a thin layer of silicon grease is used between the IGBT case and the heatsink, power sharing greatly improves, leading to a significant ΔI_C reduction at operating temperatures. This occurs because the silicon grease significantly decreases the thermal resistance between the relative junctions.

2.2 Layout considerations

General rules during the design phase should be adopted to minimize unavoidable asymmetries occurring under transient conditions (turn-on and turn-off). First, it is recommended to make the gate drive circuit as symmetrical as possible, and to use individual gate resistors. Individual driving stages provide two advantages:

- They avoid imbalances during the turn-on and turn-off phase. They mainly occur when the two IGBTs have different $V_{plateau}$ values and the same forced V_{GE} due to the common gate. As a consequence, one of the two IGBTs turns on before the other, and turns off later.
- They damp oscillations during the transient state, caused by the cross-capacitive coupling of the paralleled devices with the driving loop inductances. If parasitic oscillations are still present due to layout inductances, ferrite beads added to each gate wire can help to drastically reduce the oscillations.

Additionally, voltage overshoot can appear across the devices due to the di/dt and to stray inductances in the power circuit. It is suggested to make these loop inductances as short as possible in order not to exceed the absolute maximum rating of the IGBT voltage, rather than make them symmetrical. If not perfectly matched, the collector and emitter inductances can cause different current slopes during switch-off. Any IGBT technology can benefit from this layout optimization.

3 New advanced planar PT STGW35HF60WD

3.1 Notes on technology and $V_{CE(sat)}$ grouping

An advanced PT IGBT has been introduced to enhance the previous 600 V, 35 A IGBT STGW35NC60WD, tailored for high-frequency applications. From a technology point of view, two main improvements have been implemented on this IGBT:

1. The innovative double-drift process which changed the doping profile
2. The advanced planar strip layout

Both factors allow the reduction of the effective resistance in the drift (N ¯) region and significantly improve the dynamic performance, especially at high temperature. The changes performed on the horizontal and vertical structure and their effect on this IGBT are clearly shown in its datasheet: the new STGW35HF60WD shows a lower $V_{CE(sat)}$ typical value than the equivalent STGW35NC60WD, and its E_{off} max value (at I_C = 20 A, T_J = 125 °C) is guaranteed as per the datasheet. Tests performed on a significant number of STGW35HF60WD samples show that the static temperature coefficient (see *Equation 2*), changes in relation to the absolute $V_{CE(sat)}$ value, as shown in *Figure 3*.

Equation 2

$$\left[V_{CE(sat)} \cdot (T_J = 25°C) - V_{CE(sat)}(T_J = 125°C)\right] / V_{CE(sat)}(T_J = 125°C)$$

Figure 3. Static $V_{CE(sat)}$(@20 A,15 V) derating for STGW35HF60WD

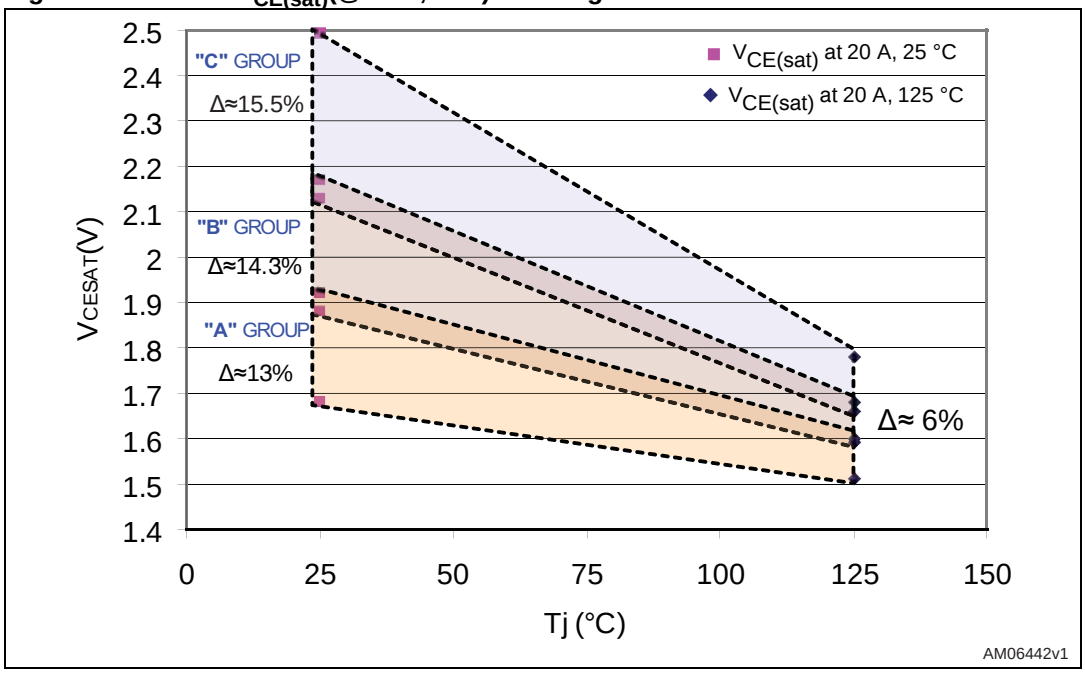


Figure 3 also explains how the total $V_{CE(sat)}$ population has been split to guarantee well-balanced and reliable paralleling. The Δ symbol beside group A, whose $V_{CE(sat)}$ values belong to the interval (1.68 V – 1.92 V [@20 A, 25 °C]), satisfies the equation:

Equation 3

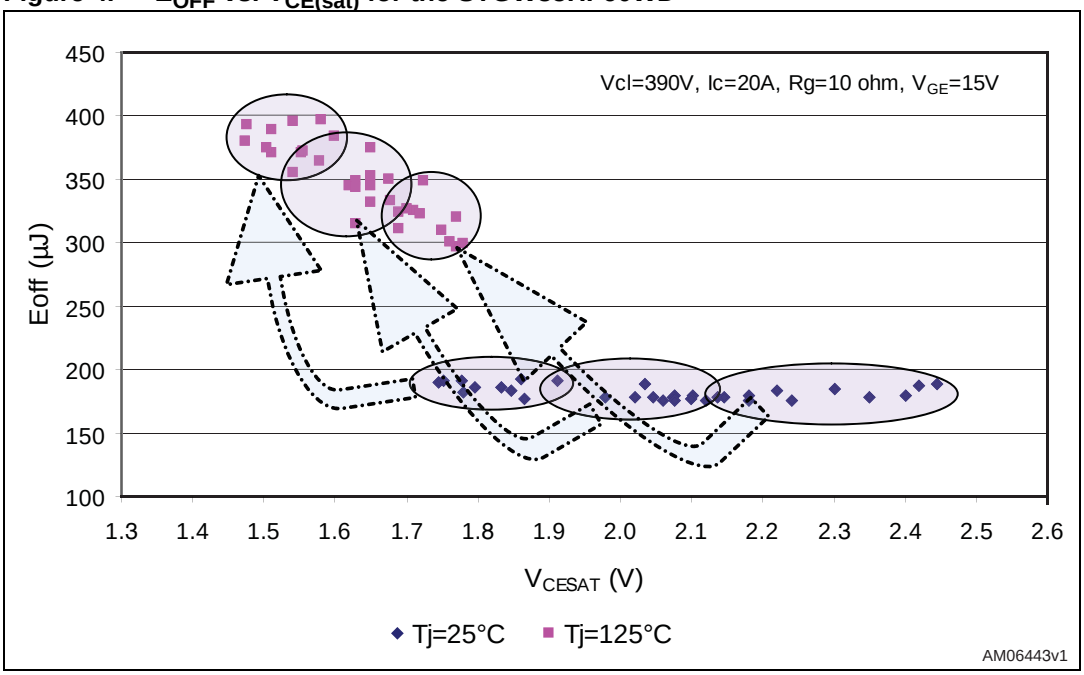
$$\Delta = (MaxValue - MinValue)/(MaxValue + MinValue)/2 = 13\%$$

The same equation can be written for groups B and C. From *Figure 3* it is clear that each group has been chosen with a specific Δ value at T_J = 25 °C. Despite the original imbalance at T_{AMB}, the Δ of each group moves towards the same value at high temperature. This balancing mechanism helps to keep a very low and stable ΔI_C when two or more IGBTs of the same group work in parallel.

3.2 E_{OFF} impact on parallel

It is well known that the E_{OFF} contribution of IGBTs on high-frequency DC-DC conversion cannot be neglected. This impact becomes significant when high T_J and high current levels are considered. The STGW35HF60WD guarantees that the E_{OFF} thermal derating can be controlled and that its value is in the range of 80% –110%. Low $V_{CE(sat)}$ samples show the worst thermal derating (~ 110%), while high $V_{CE(sat)}$ samples have the lowest thermal derating (~ 80%), which is clearly illustrated in *Figure 4*.

Figure 4. E_{OFF} vs. $V_{CE(sat)}$ for the STGW35HF60WD

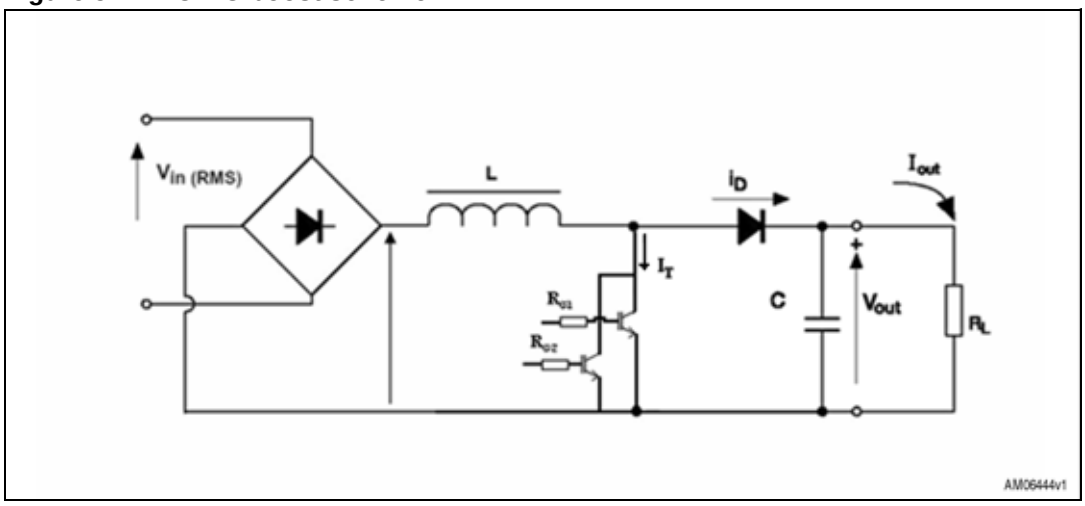


The difference in E_{OFF} derating has been considered on the $V_{CE(sat)}$ selection, and also explains why the selected groups have different widths.

4 The STGW35HF60WD on the test bench

A DC-DC boost converter (*Figure 5*) has been used as a test vehicle to evaluate two STGW35HF60WD IGBTs working in parallel.

Figure 5. DC-DC boost scheme

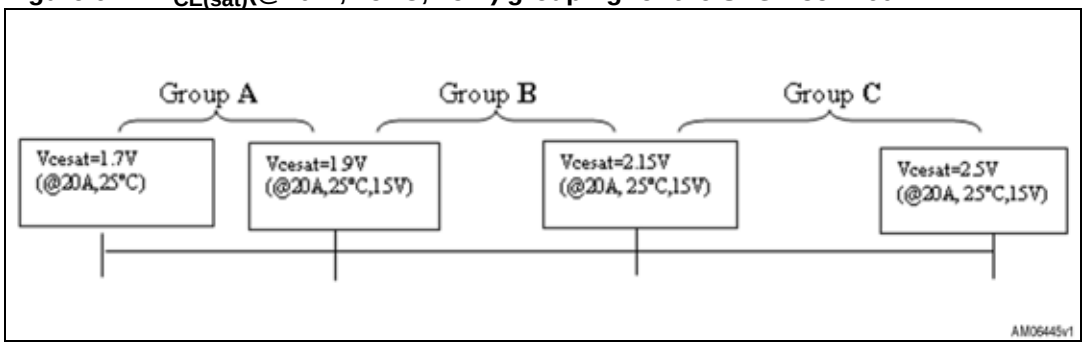


Boost specifications:

- $V_{IN(DC)}$ = 250 V
- I_{TAV} = 20 A
- V_{OUT} = 380 V
- Fsw = 30 kHz
- Duty = 0.33%
- CCM operation

A preliminary analysis has been performed to measure the dynamic ΔIC established between several couples of paralleled IGBTs. To target the best current sharing, the static $V_{CE(sat)}$(@20 A,15 V, 25 °C) has been chosen as selection criteria to split the total IGBT population (as illustrated in *Figure 6*) and three sets of tests are reported in this document.

Figure 6. $V_{CE(sat)}$(@20 A, 25 °C, 15 V) grouping for the STGW35HF60WD



Couple n.1 and n.3 tested have $\Delta V_{CE(sat)}$@20 A, 25 °C different from its relative group. For example, couple n.1, has been chosen with $\Delta V_{CE(sat)}$ = 270 mV (wider than $\Delta V_{CE(sat)}$ = 200 mV for group A) in order to guarantee a more reliable result in terms of ΔI_C. The same consideration applies for couple n.3.

- Couple n.1
  - device n.1: $V_{CE(sat)}$ = 1.75 V (@20 A, 25 °C,15 V)
  - device n.2: $V_{CE(sat)}$t = 2.02 V (@20 A, 25 °C, 15 V)

  $\Delta V_{CE(sat)}$ = 270 mV
- Couple n.2
  - device n.1: $V_{CE(sat)}$ = 1.84 V (@20 A, 25 °C,15 V)
  - device n.2: $V_{CE(sat)}$ = 2.09 V (@20 A, 25 °C, 15 V)

  $\Delta V_{CE(sat)}$ = 250 mV
- Couple n.3
  - device n.1: $V_{CE(sat)}$ = 1.94 V (@20 A, 25 °C,15 V)
  - device n.2: $V_{CE(sat)}$ = 2.34 V (@20 A, 25 °C, 15 V)

  $\Delta V_{CE(sat)}$ = 400 mV

The goal of the on-board tests was to evaluate how the dynamic ΔI_C of each group moves from board startup (T_C = 25 °C) to a steady-state condition in terms of thermal sharing (T_C = 100 °C). After board startup, the two paralleled devices share the total power, taking advantage of the common heatsink and layout optimization (as suggested in *Section 2.1* and *Section 2.2*). Thanks to the negative thermal feedback introduced by the common heatsink, the dynamic ΔI_C decreases despite of its initial value of T_C = 25 °C, and remains stable even at high T_J temperatures.

Couple n.1

Figure 7. ΔI_C at T_C = 25 °C (board startup)

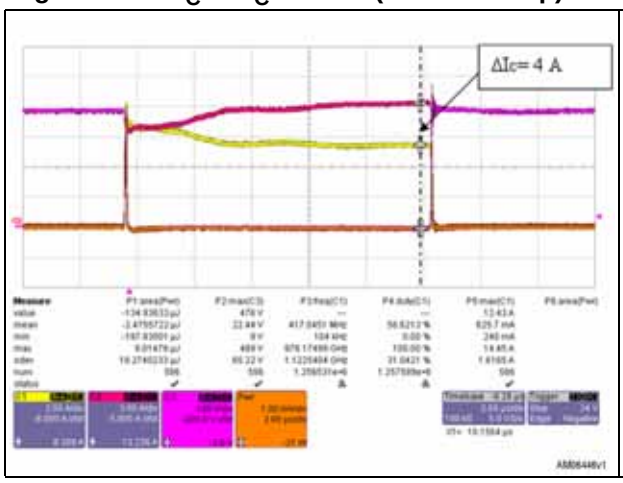
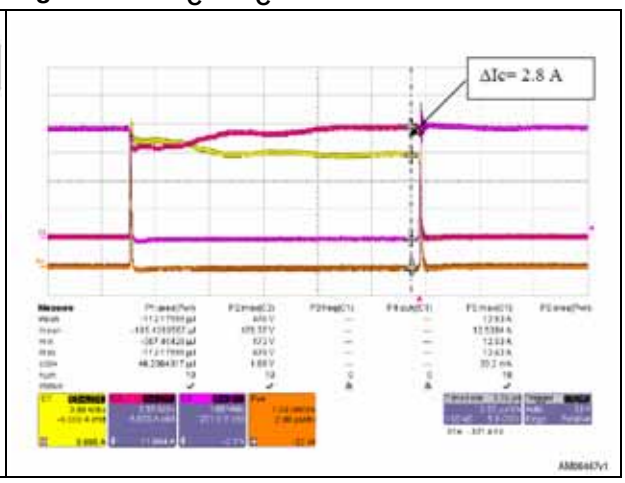


Figure 8. ΔI_C at T_C = 100 °C



Couple n.2

Figure 9. ΔI_C **at** T_C **= 25 °C (board startup)**

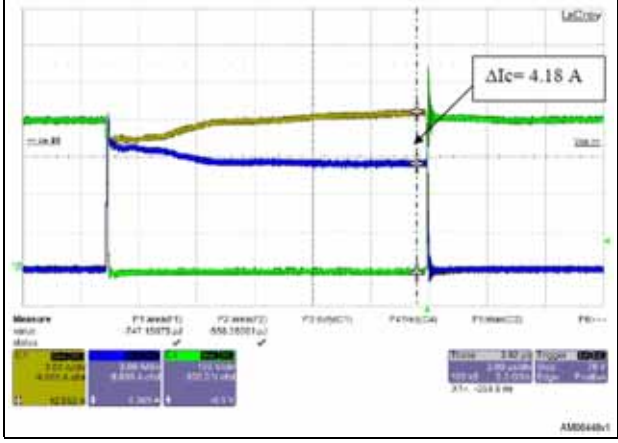
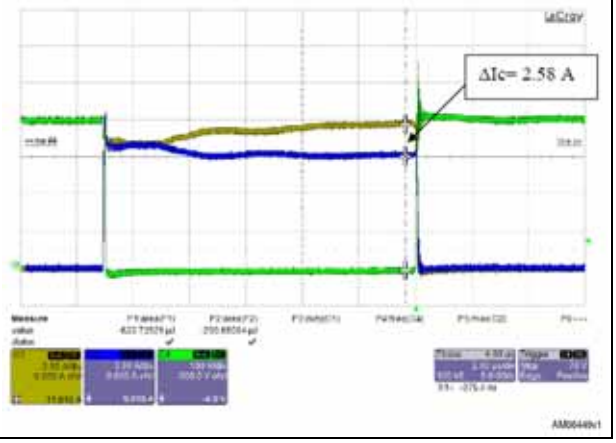


Figure 10. ΔI_C **at** T_C **= 100 °C**



Couple n.3

Figure 11. ΔI_C **at** T_C **= 25 °C (board startup)**

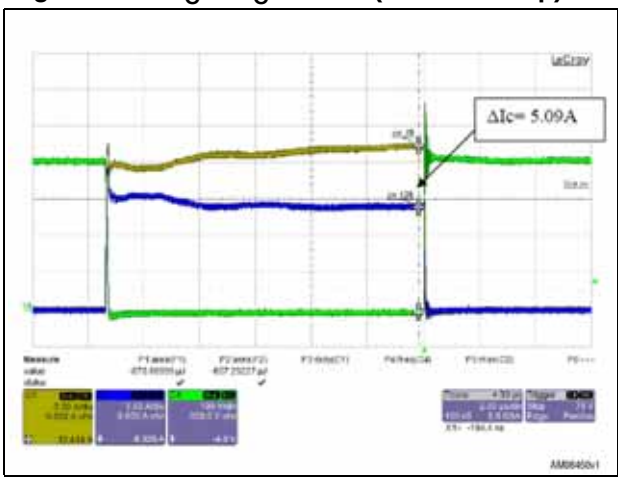


Figure 12. ΔI_C **at** T_C **= 100 °C**

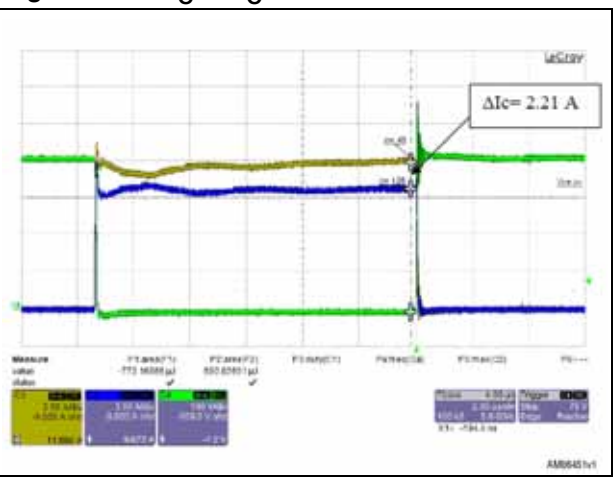


Table 1. $\Delta I_C/I_{TOT}$ **% summary**

	Couple 1 ($\Delta V_{CE(sat)}$ = 270 mV)	Couple 2 ($\Delta V_{CE(sat)}$ = 250 mV)	Couple 3 ($\Delta V_{CE(sat)}$ = 400 mV)
ΔI_C (25 °C)/I_{TOT} %	20%	21%	25.4%
ΔI_C (100 °C)/I_{TOT} %	14%	12.9%	11%

If an acceptable value of $\Delta I_C/I_{TOT}$ = 10% −14% is considered in terms of efficiency, *Table 1* shows that three $V_{CE(sat)}$ grouping allows the paralleling of the IGBTs with excellent performance results.

5 Conclusion

Several tests performed on the new advanced planar PT STGW35HF60WD show that STMicroelectronics' advanced PT technology can be paralleled with satisfactory performance in terms of thermal and current sharing. Reliable paralleling, however, requires good thermal feedback implementation and $V_{CE(sat)}$ selection of the total IGBT population. Both of these factors provide a balancing mechanism to reduce and keep stable the dynamic ΔI_C at operating conditions. Finally, the STGW35HF60WD is offered in three different $V_{CE(sat)}$ groups, as shown in *Table 2: Suggested $V_{CE(sat)}$ (@20 A, 25 °C, 15 V) selection as per datasheet* and as reported in the datasheet, for a safe parallel connection without risk of thermal runaway.

Table 2. Suggested $V_{CE(sat)}$ (@20 A, 25 °C, 15 V) selection as per datasheet (1)

Group "A"	Group "B"	Group "C"
1.68 V ─ 1.92 V	1.88 V ─ 2.17 V	2.13 V ─ 2.5 V
@20 A, 25 °C, 15 V	@20 A, 25 °C, 15 V	@20 A, 25 °C, 15 V

1. The $V_{CE(sat)}$ grouping reported above is slightly different from the one in *Figure 6*, in order to meet the testing rules.

6 Revision history

Table 3. Document revision history

Date	Revision	Changes
05-May-2010	1	Initial release.