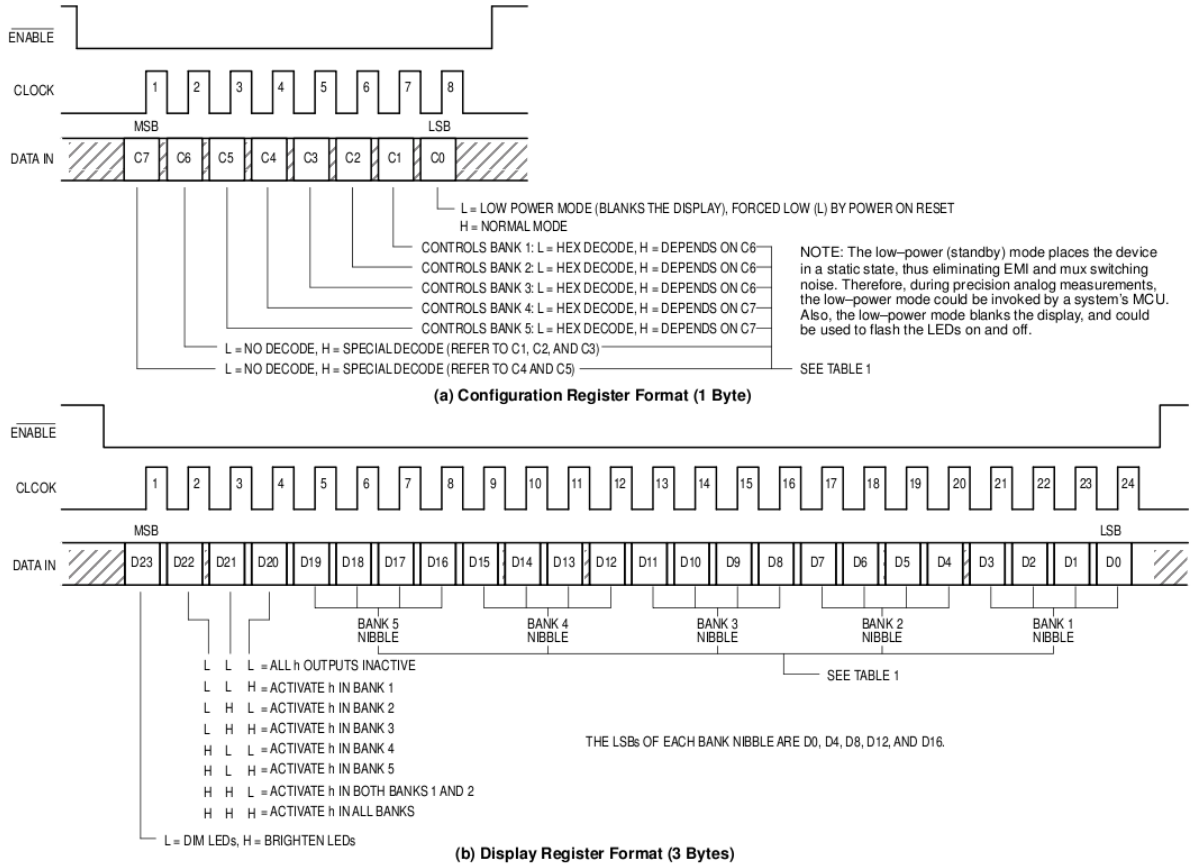

Figure 7. Timing Diagrams for Non–Cascaded Devices