Nanosecond switching using power MOSFETs

R. J. Baker
E. G. & G. Energy Measurements Inc., P. O. Box 1912, Mail Stop N-31, Las Vegas, Nevada 89125
M. D. Pocha
Lawrence Livermore National Laboratory, P. O. Box 808, Mail Stop L-156, Livermore, California 94550

(Received 22 February 1990; accepted for publication 22 April 1990)

It is shown that using the secondary breakdown effect of a bipolar transistor, often called an avalanche transistor, the large input capacitance of a power MOSFET may be charged very quickly. A power MOSFET driven by an avalanche transistor is used to generate electrical pulses of > 800 V into 50 Ω with rise times of approximately 3 ns. The output pulse amplitude can be varied by adjusting the drain-source voltage of the power MOSFET. The trigger delay of this circuit is approximately 5 ns, with jitter of < 100 ps. This circuit has been used to generate pulses at a repetition rate of greater than 1 kHz.

I. INTRODUCTION

Fast rise time (nanosecond) high-voltage (hundreds of volts) electrical pulses find many applications in instrumentation for fast transient measurements. Some typical applications are laser diode drive circuits, sweep circuits for CRT streak cameras, the gating of microchannel plates and pockels cells, and the triggering of scopes and transient recorders. We have designed a circuit that uses an avalanche transistor to turn on a Power MOSFET that produces a pulse of > 800 V into 50 Ω with a rise time of 3 ns.

The use of avalanche transistors for nanosecond pulse generation is well known.[1] Power MOSFETs are a new technology that has been primarily used for power supply design.[2] These power MOSFETs are actually made up of hundreds of smaller MOSFETs arranged in an array and integrated on one substrate.

Section II will discuss the design of pulse generator circuits using MOSFETs. The last two sections will give the experimental results and concluding remarks.

II. DESIGNING WITH POWER MOSFETS

The electrical model of a power MOSFET is shown in Fig. 1. When using the MOSFET as a switch the gate source and gate-drain capacitance must be charged and discharged. The parallel combination of these capacitances is called the input capacitance. This capacitance can be greater than 2000 pF in some cases. The ability of a gate driving circuit to charge the large input capacitance of the power MOSFETs will determine their switching speed. The gate, source, and drain lead inductances impede the transfer of charge to the input capacitance and must be considered when designing a gate driving circuit. The source and drain inductances combined with the drain-source capacitance impede the drain current when switching takes place and ultimately limit the rise time of the pulse.

It is desired that the gate driving circuit have an output impedance that is very small. Having a lower impedance driver increases the current drive capability so that a large input capacitance may be charged more rapidly. There are two approaches to achieving this small impedance. The first, and by far the most common, is to use an emitter follower or several emitter followers. This method is rather complicated, sometimes requiring as many as five stages to achieve nanosecond rise times.[3] The second method is to use an avalanche transistor to drive the input capacitance. This is the method we use.

The major concern when using an avalanche driver is not to overdrive the gate. The silicon dioxide layer can be perforated if the gate source voltage exceeds the manufactures specification and is the most common cause of failure in a Power MOSFET. This is where the lead inductances can actually help the designer by dropping part of the driver pulse voltage. A simple but effective method of protecting the gate is putting a zener diode between the gate and source.

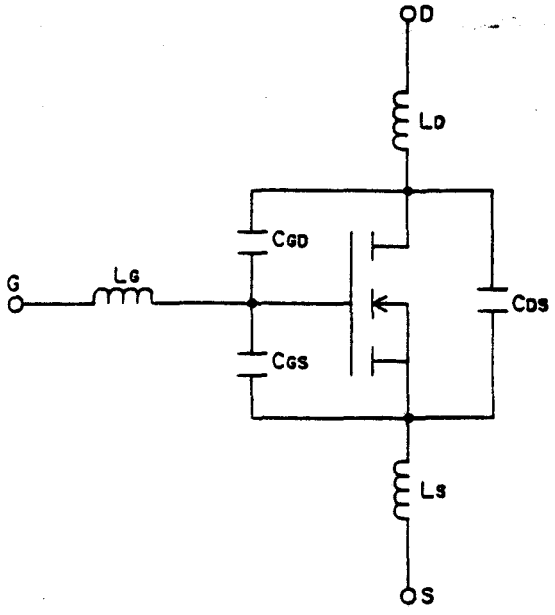

FIG. 1. Electrical model of a power MOSFET.

 0034-6748/90/082211-03$02.00

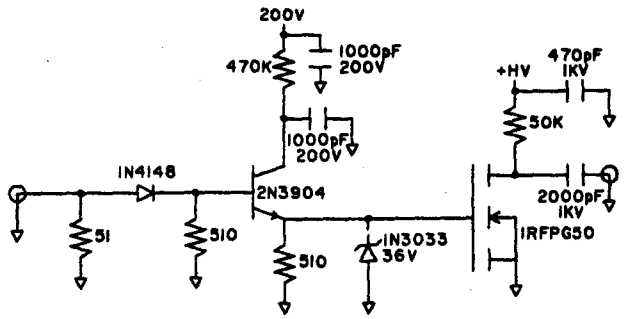

FIG. 2. Schematic diagram of MOSFET pulser.

The reference voltage of the zener is selected such that it is lower than the maximum rating of the gate-source voltage.

The schematic diagram of our pulser is shown in Fig. 2. When an input trigger is applied to the circuit the 2N3904, operating in the avalanche mode dumps the charge stored in the collector capacitor into the gate of the MOSFET and the 510-Ω load at the emitter. The charging of the input capacitance in this fashion rapidly turns the MOSFET "ON" creating the output pulse. The lower limit on the load impedance of the avalanche transistor is set by the amount of power that can be dissipated without destruction. The upper limit is determined such that the transistor never enters the active region when it is switching. The upper limit is not a concern when driving a Power MOSFET. The value of the collector capacitor must be large enough to supply the amount of charge needed to charge the input capacitance, but not so large as to overvoltage the gate. We found that 470 to 3000 pF was a good value for the collector capacitor in Fig. 2.

III. EXPERIMENTAL RESULTS

Figure 3 shows the output waveform of the pulser with 1 kV applied to the drain. The switching efficiency is greater than 80%. The inset waveform in Fig. 3 shows a 10%–90% rise time of 3 ns. Figure 4 shows different output pulse amplitudes with 800, 600, 400, and 200 V applied to the drain. Putting a zener diode between the gate and source did not affect the rise time of the output pulse. The junction capacitance of the zener diode, 1N3033 36 V, was approximately 350 pF. Adding the capacitance of the zener diode while maintaining the same rise time shows this method of driving the MOSFET is very robust. That is, rise time does not change within the normal tolerance of input capacitance from device to device.

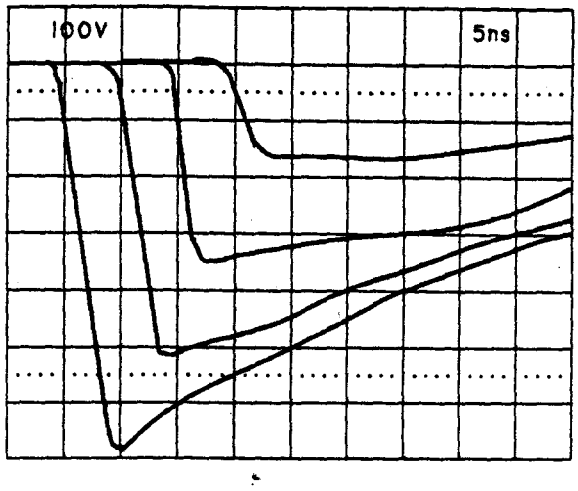

FIG. 4. Output with + HV = 800, 600, 400, and 200 V.

Figure 5 shows the voltage waveform at the gate with 1 kV at the drain. Some manufacturers specify the maximum gate source voltage of their power MOSFETs at + 20 V while others specify + 40 V. We have assumed a + 40 V maximum. Without zener diode protection in the circuit of Fig. 2, we have generated greater than 10^8 pulses. With lower power MOSFETs, we have found that due to the lower input capacitance, the gate can be destroyed if the protection zener diode is not included. We conclude that when using the avalanche driver a zener diode should be included in every case.

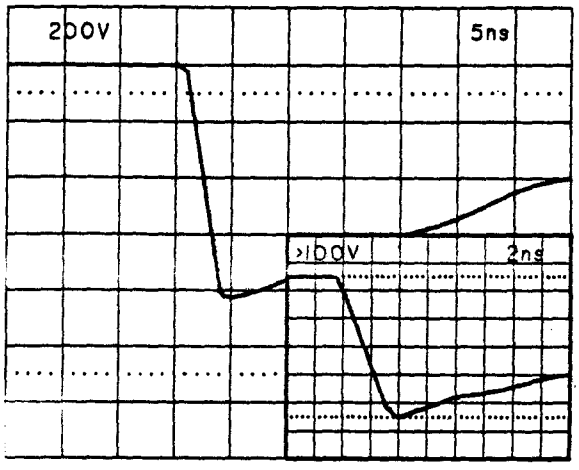

FIG. 3. Output of pulser with 1 kV applied, inset waveform shows rise time.

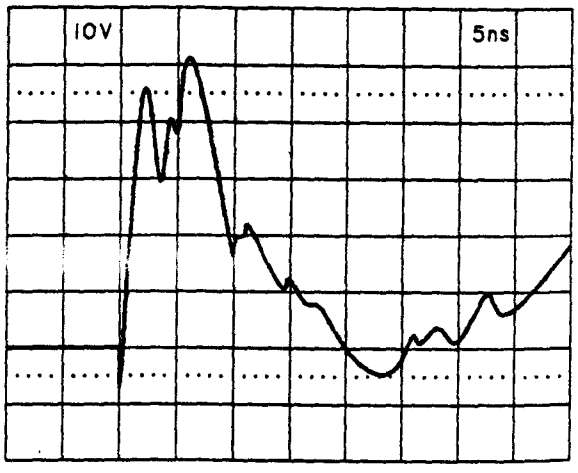

FIG. 5. Waveform at gate of MOSFET.

Using lower power MOSFETs, such as the IRF 840(500 V), we were able to attain switching efficiencies approaching 100%. Variable output pulse amplitudes may be obtained by setting the drain source voltage to the desired output pulse amplitude. Other MOSFETs manufactured by Motorola, Siliconix, and International Rectifier have also been driven using this method. The results are switching times in every case of less than or equal to 3 ns.

The maximum repetition rate of this circuit was found to be greater than 1 kHz. The limiting factors influencing the maximum repetition rate are the rate at which the collector and drain capacitance are charged and the power that can be dissipated by each transistor without damage. The measured jitter of this circuit was less than 100 ps while the turn on delay time was approximately 5 ns.

The circuit was constructed on a breadboard. The input and output connectors were SMAs. The only special technique used was to keep the lead lengths of the components as short as possible. This meant putting the components very close together.

IV. DISCUSSION

There are many advantages to generating several hundred volt, nanosecond pulses with this two transistor circuit over conventional avalanche pulsers. The output voltage can be varied over a large range simply by changing the drain bias. The output impedance of the MOSFET pulser is lower, making it easier to use with pulse forming lines. Another advantage of the low output impedance is the ability to drive lower impedance loads. Output impedance can be further reduced by the use of several MOSFETs in parallel. Connecting avalanche transistors in parallel is very difficult to implement. The MOSFET is much more rugged than the strings of avalanche transistors used to generate pulses of comparable amplitude and rise time. The MOSFET pulser is capable of generating much wider pulses than avalanche pulse generators. And finally, since there are only two transistors, the PC board fabrication is simpler.

Future work will mainly be concerned with pulse forming techniques. That is, the use of pulse forming lines for generation of rectangular pulses, stacking, and paralleling MOSFETs for higher voltage and current capabilities, respectively, and the use of pulse sharpening diodes for sharpening the leading edge of the pulse.[4]

ACKNOWLEDGMENTS

Work performed under the auspices of the United States Department of Energy by E. G. & G. Energy Measurements Inc. and the Lawrence Livermore National Laboratory under contract Nos. DE-AC08-88NV10617 and W-7405-ENG-48, respectively.

[1]W. P. Mitchell, Electronic Design 6:202-209 (1968).
[2]HEXFET- Power MOSFET Designers Manual (1987), Chap. 1.
[3]Product Catalog, Directed Energy, Inc. (1989).
[4]D. M. Benzel and M. D. Pocha, Rev. Sci. Instrum. **56**, 1456 (1985).