4.1.1 HIGH TEMPERATURE REVERSE BIAS (HTRB) HEXFET GENERATION 3, TO-220/D2PAK PACKAGE

Junction Temperature: Tj = +150°C or 175°C, as indicated
Applied Bias: Vg = Vs = 0V; Vd = 100% of maximum rated Bvdss up to 500V then 80% of maximum rated Bvdss

Device Type	Date Code	Temp (°C)	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & 80% Bvdss (note b)	Failure Rate @ 90°C & 60% UCL	FITs (note b)
IRF9630	9752	150	85	1000	0		8.0E+06	0.115	115
IRF9510L	9731	175	84	1000	0		4.1E+07	0.023	23
IRF9520	9637	175	40	1000	0		1.9E+07	0.047	47
IRF9510	9634	175	40	1000	0		1.9E+07	0.047	47
IRF9Z14	9633	175	40	1000	0		2.0E+07	0.046	46
IRF9Z34	9715	175	100	1000	0		5.0E+07	0.018	18
IRF9Z24	9636	175	50	1000	0		2.5E+07	0.037	37
IRLZ14	9703	175	300	1000	0		1.6E+08	0.006	6
IRLZ24	9646	175	15	1000	0		8.0E+06	0.114	114
IRF510	9727	150	84	1000	1	C	9.5E+06	0.212	212
IRF510	9741	150	85	1000	0		9.7E+06	0.095	95
IRF530	9629	175	40	1000	0		2.2E+07	0.042	42
IRF530	9630	175	40	1000	0		2.2E+07	0.042	42
IRF530	9638	175	40	1000	0		2.2E+07	0.042	42
IRF510	9646	175	80	1000	0		4.4E+07	0.021	21
IRF640	9748	150	85	1000	0		1.0E+07	0.089	89
IRF610	9646	150	110	1000	0		1.3E+07	0.069	69
IRF730	9702	150	195	1000	0		2.7E+07	0.034	34
IRF840	9734	150	85	1000	0		1.2E+07	0.073	73
IRF820	9722	150	85	1000	0		1.2E+07	0.073	73
IRF840	9722	150	83	1000	0		1.2E+07	0.075	75
IRF840	9732	150	170	1000	0		2.5E+07	0.037	37
IRF820S	9734	150	85	1000	0		1.2E+07	0.073	73
IRF840S	9734	150	85	1000	0		1.2E+07	0.073	73
IRF840	9732	150	85	1000	0		1.2E+07	0.073	73
IRF840	9652	150	508	1000	3	C	7.5E+07	0.056	56
IRFBC40	9646	150	20	1000	0		3.1E+06	0.292	292
IRFBE20	9741	150	85	1000	0		1.5E+07	0.060	60
TOTALS			2804		4		7.2E+08	0.007	7

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.2 POWER CYCLING
TO-220/D2PAK PACKAGE

Junction Temperature (off state): Tj = 30°C | Applied Bias (off state): Vs = Vg = 0V; V(

Junction Temperature (on state): Tj = 30°C + delta T | Applied Bias (off state): Vs = 0V; Vd = 30V to (

Power Dissipation: Pd = delta Tj + Theta jc | Cycle time:

Device Type	Date Code	Temp Change delta Tj (°C)	Qty	Test Duration (cycles)	# of fails @		
					2.5K	5K	10K
IRF9510	9634	100	50	2500	0	-	-
IRF820	9732	100	85	8572	0	0	-
IRF9620	9632	100	50	5000	0	0	-
IRF630	9652	100	90	20000	0	0	0
IRF9Z34	9704	100	96	10000	0	0	0
IRF9Z34	9715	100	100	8572	0	0	-
IRF540	9750	100	85	8572	0	0	-
IRF840	9645	100	100	10000	0	0	0
IRF840	9732	100	83	8572	0	0	-
IRF840S	9731	100	85	10000	0	0	0
IRF840S	9732	100	85	8572	0	0	-
IRF840S	9740	100	85	10000	0	0	0
IRF9Z24N	9733	100	85	8572	0	0	-
IRFZ24N	9733	100	85	8572	0	0	-
IRLZ24N	9733	100	135	8572	0	0	-
IRF5305	9734	100	85	8572	0	0	-
IRFZ44N	9721	100	82	10000	0	2	0
IRLZ44N	9733	100	50	8572	0	0	-
IRF3205	9733	100	85	8572	0	0	-
IRF3710	9645	100	99	10000	0	0	0
IRF4905	9718	100	85	8572	0	0	-
IRL3803	9644	100	20	10000	0	0	1
IRL3803	9712	100	25	10000	0	0	0
TOTALS			1830		0	2	1

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

d = 40V to 80V
50V; Vg < 12V
: 2 to 4 minutes

Fail Mode (note a)
R
C

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.3 TEMPERATURE CYCLING
TO-220 PACKAGE

Tmin = -55°C; T max = +150°C; Cycle Time (delta T = 205°C): 20 minutes; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
				250	500	1000	
IRF9Z24N	9733	85	1000	0	0	0	
IRFZ24N	9733	85	1000	0	0	0	
IRLZ24N	9733	85	1000	0	0	0	
IRF510	9646	240	1000	0	0	0	
IRF510	9727	85	1000	0	0	0	
IRF510	9741	85	1000	0	0	0	
IRF610	9646	330	1000	0	0	0	
IRF9510	9634	40	1000	0	0	0	
IRF9610	9631	40	1000	0	0	0	
IRF820	9732	84	1000	0	0	0	
IRF9520	9637	40	1000	0	0	0	
IRF9620	9632	40	1000	0	0	0	
IRFBC20	9741	85	1000	0	0	0	
IRFBC20	9747	85	1000	0	0	0	
IRFBE20	9741	85	1000	0	0	0	
IRLZ24	9646	40	1000	0	0	0	
IRFZ44N	9646	80	1000	0	0	0	
IRFZ44N	9729	170	1000	0	0	0	
IRLZ44N	9733	85	1000	0	0	0	
IRFZ46N	9750	340	1000	0	0	0	
IRFZ46N	9801	170	1000	0	0	0	
IRF540N	9646	20	1000	0	0	0	
IRF730	9702	200	1000	0	0	0	
IRF9630	9752	85	1000	0	0	0	
IRF9Z34	9704	104	1000	0	0	0	
IRF9Z34	9715	100	1000	0	0	0	
IRF3205	9733	85	1000	0	0	0	
IRF3710	9645	100	1000	0	0	0	
IRF4905	9718	680	1000	0	2	3	R
IRF840	9645	100	1000	0	0	0	
IRF840	9732	84	1000	0	0	0	
IRF840	9733	84	1000	0	0	0	
IRFBC40	9646	50	1000	0	0	0	
IRL2505	9733	85	1000	0	0	0	
IRL3803	9644	40	1000	0	0	0	
IRL3803	9712	50	1000	0	0	0	
TOTALS		4246		0	2	3	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.4 HIGH HUMIDITY, HIGH TEMP. REVERSE BIAS (H3TRB) TO-220 PACKAGE

Junction Temperature: Tj = 85°C; Relative Humidity: 85%
Applied Bias: Vg = 0V; Vd = as specified

Device Type	Date Code	Drain Voltage	Qty	Test Duration (hours)	# of fails @			Fail Mode (note a)
					168	500	1000	
IRFZ24N	9733	55	50	1000	0	0	0	
IRLZ24N	9733	55	49	1000	0	0	0	
IRF9Z14	9633	-60	48	1000	0	0	0	
IRF9510	9634	-100	35	1000	0	0	0	
IRLZ14	9703	60	290	1000	0	0	0	
IRF9530N	9643	-100	298	1000	0	0	0	
IRFIZ24G	9802	60	85	1000	0	0	0	
IRF9Z24	9636	-60	50	1000	0	0	0	
IRFBC20	9745	100	85	1000	0	0	0	
IRF6215	9649	-100	169	1000	0	0	0	
IRF6215S	9733	-100	85	1000	0	0	0	
IRF6215S	9730	-100	85	1000	0	0	0	
IRFZ44N	9733	55	50	1000	0	0	0	
IRLZ44N	9733	55	49	1000	0	0	0	
IRF6215	9706	-100	99	1000	0	0	0	
IRF9Z34	9715	-60	100	1000	0	0	0	
IRF730	9702	100	350	1000	0	0	0	
IRF840	9652	100	504	1000	0	0	0	
IRF840	9645	100	100	1000	0	0	0	
IRF540	9750	100	85	1000	0	0	0	
IRL3803	9644	30	20	1000	0	0	0	
IRL3803	9712	30	25	1000	0	0	0	
IRF3710	9645	100	100	1000	0	0	0	
IRF3205	9733	44	83	1000	0	0	0	
IRL2505	9733	55	49	1000	0	0	0	
TOTALS			2943		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.5 HIGH TEMPERATURE GATE STRESS
HEXFET GENERATION 3, TO-220/D2PAK PACKAGE

Junction Temperature: Tj = +150°C or +175°C, as specified: Applied Bias: Vs = Vd = 0V; Vg as specified

Device Type	Date Code	Temp (°C)	Gate Bias	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & Vg = 12V (6V for logic); (note d)	Failure Rate @ 90°C & Vg = 12V (FITs) (note C)
IRLZ14	9630	175	10	90	1000	0		1.68E+09	0.546
IRL540	9630	175	10	90	1000	0		1.68E+09	0.546
IRLZ14	9703	175	10	300	1000	0		5.59E+09	0.164
IRF840L	9731	150	20	85	1000	0		1.01E+10	0.090
IRF840	9652	150	20	510	1000	1	C	5.15E+09	0.394
IRF730	9702	150	20	300	1000	0		3.03E+09	0.302
IRF840	9732	150	20	85	1000	0		8.59E+08	1.065
IRF820	9732	150	20	85	1000	0		8.59E+08	1.065
IRF840	9732	150	20	170	1000	0		1.72E+09	0.533
IRF840	9733	150	20	85	1000	0		8.59E+08	1.065
IRF840	9748	150	20	85	1000	0		8.59E+08	1.065
IRF540	9750	150	20	85	1000	0		8.59E+08	1.065
IRF9610	9630	150	-20	80	1000	0		8.08E+08	1.132
IRF9630	9630	150	-20	46	1000	0		4.65E+08	1.969
IRF9Z34	9715	175	-20	100	1000	1	C	1.86E+09	1.089
TOTALS				2196		2		3.64E+10	0.085

NOTES:
b. See Appendix C of Reference 1 for an explanation of equivalent device hours for HTRB tests.
c. One FIT represents one failure in one billion (1.0E+09) hours.
d. EQUIVALENT DEV-HRS for the long term gate stress test are determined by Crook's Model (ref. 2) for an observed thermal activation energy, Ea, of 0.4 eV and an observed electric field constant of 0.108MV/cm. Extrapolation is to VG = 12 volts for an "IRF" or "IRC" device and to VG = 6 volts for an "IRL" device.

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.6 AUTOCLAVE
TO-220 PACKAGE

T= 121°C, P = 2 atmospheres, RH = 100%; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @	Fail Mode (note a)
IRF9Z24N	9733	85	96	0	
IRFZ24N	9733	85	96	0	
IRFZ24N	9803	85	96	0	
IRFZ24N	9806	85	96	0	
IRLZ24N	9803	85	96	2	L
IRLZ24N	9806	85	96	0	
IRF9610	9748	20	96	0	
IRF9610	9749	20	96	0	
IRFZ24N	9748	17	96	0	
IRLZ14	9703	300	96	0	
IRLZ24N	9748	20	96	0	
IRL3303	9738	20	96	0	
IRF530N	9749	20	96	0	
IRFBE20	9749	20	96	0	
IRFIZ24G	9802	85	96	1	L
IRFZ34N	9748	15	96	0	
IRF5305	9733	85	96	0	
IRFZ44N	9729	170	96	0	
IRFZ44N	9733	85	96	0	
IRLZ44N	9733	85	96	0	
IRFZ46N	9721	20	96	0	
IRFZ46N	9748	117	96	1	L
IRFZ46N	9748	20	96	0	
IRF540N	9748	60	96	0	
IRF630	9748	20	96	0	
IRF830	9748	18	96	0	
IRF9540N	9748	34	96	0	
IRF9540N	9749	19	96	0	
IRF9Z34	9715	100	96	0	
IRFZ46	9738	20	96	0	
IRFZ46	9748	20	96	0	
IRFZ46	9749	20	96	0	
IRF2807	9741	20	96	0	
IRF3205	9729	20	96	0	
IRF3710	9648	20	96	0	
IRF3710	9730	20	96	0	
IRF3710	9733	20	96	0	
IRF4905	9734	85	96	0	
IRF540	9750	85	96	0	
IRF640	9737	20	96	0	
IRF640	9748	20	96	0	
IRF740	9632	20	96	0	
IRF740	9731	20	96	0	
IRF840	9652	510	96	0	
IRF840	9740	20	96	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @	Fail Mode (note a)
IRFBC40	9748	20	96	0	
IRFBC40LC	9748	20	96	0	
IRFBC40LC	9749	17	96	0	
IRFZ44	9728	20	96	0	
IRFZ44	9736	20	96	0	
IRFZ44	9741	20	96	0	
IRFZ44	9745	20	96	0	
IRFZ44	9748	20	96	0	
IRL2505	9733	170	96	0	
IRL2910	9651	20	96	0	
IRL2910	9736	20	96	0	
IRL2910	9737	20	96	0	
IRL2910	9745	20	96	0	
IRL3303	9748	20	96	0	
IRL3303	9749	20	96	0	
IRL3803	9641	20	96	0	
IRL3803	9644	20	96	0	
IRL3803	9712	25	96	0	
IRLZ44	9702	19	96	0	
IRLZ44	9707	20	96	0	
IRFZ48	9714	20	96	0	
IRFZ48	9719	20	96	0	
IRFZ48	9722	20	96	0	
TOTALS		3431		4	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.7 HIGH TEMPERATURE REVERSE BIAS (HTRB) HEXFET GENERATION 5, TO-220/D2PAK PACKAGE

Junction Temperature: Tj = +150°C or 175°C, as indicated
Applied Bias: Vg = Vs = 0V; Vd = 100% of maximum rated Bvdss up to 500V then 80% of maximum rated Bvdss

Device Type	Date Code	Temp (°C)	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & 80% Bvdss (note b)	Failure Rate @ 90°C & 60% UCL	FITs (note b)
IRF6215L	9731	175	85	1000	0		4.0E+07	0.023	23
IRF6215	9649	175	340	1000	0		1.6E+08	0.006	6
IRF6215	9706	175	100	1000	0		4.7E+07	0.020	20
IRF9530N	9805	175	49	1000	0		2.4E+07	0.039	39
IRF9530N	9808	175	50	1000	0		2.4E+07	0.038	38
IRF9530N	9643	175	703	1000	0		3.4E+08	0.003	3
IRF4905	9718	175	671	1000	0		3.3E+08	0.003	3
IRL6903	9703	175	95	1000	0		4.8E+07	0.019	19
IRL3803	9712	175	25	1000	0		1.3E+07	0.070	70
IRL3803	9644	175	20	1000	0		1.1E+07	0.087	87
IRFZ46N	9801	175	170	1000	1	C	9.1E+07	0.022	22
IRFZ46N	9750	175	340	1000	0		1.8E+08	0.005	5
IRFZ46N	9741	175	200	1000	0		1.1E+08	0.009	9
IRFZ44N	9729	175	252	1000	0		1.3E+08	0.007	7
IRFZ46N	9736	175	85	500	0		2.3E+07	0.040	40
IRF3205L	9731	175	85	1000	0		4.5E+07	0.020	20
IRFZ24N	9733	175	50	1000	0		2.7E+07	0.034	34
IRL2505	9733	175	50	1000	0		2.7E+07	0.034	34
IRLZ24N	9733	175	50	1000	0		2.7E+07	0.034	34
IRLZ44N	9733	175	50	1000	0		2.7E+07	0.034	34
IRF3205	9808	175	85	1000	0		4.5E+07	0.020	20
IRFZ46N	9712	175	254	1000	1	L	1.4E+08	0.015	15
IRFZ46N	9712	175	99	1072	0		5.7E+07	0.016	16
IRFZ46N	9703	175	238	1000	0		1.3E+08	0.007	7
IRFZ46N	9705	175	100	1000	2	L	5.3E+07	0.058	58
IRFZ44N	9646	175	40	1000	0		2.1E+07	0.043	43
IRF540N	9734	175	85	1000	0		4.7E+07	0.020	20
IRF540N	9747	175	85	1024	0		4.8E+07	0.019	19
IRF540N	9732	175	85	1000	0		4.7E+07	0.020	20
IRF3710	9645	175	100	1000	0		5.5E+07	0.017	17
IRF540N	9646	175	10	1000	0		5.5E+06	0.167	167
IRF3415	9722	175	200	1000	0		1.1E+08	0.008	8
TOTALS			4851		4		2.5E+09	0.002	2

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.8 HIGH TEMPERATURE GATE STRESS
HEXFET GENERATION 5, TO-220/D2PAK PACKAGE

Junction Temperature: Tj = +150°C or +175°C, as specified: Applied Bias: Vs = Vd = 0V; Vg as specified

Device Type	Date Code	Temp (°C)	Gate Bias	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & Vg = 12V (6V for logic); (note d)	Failure Rate @ 90°C & Vg = 12V (FITs) (note C)
IRL3803	9644	175	10	20	1000	0		8.49E+08	1.078
IRL3803	9644	175	10	240	2000	0		2.04E+10	0.045
IRLZ24N	9711	175	10	99	1000	0		4.20E+09	0.218
IRLZ24N	9712	175	10	100	1000	0		4.24E+09	0.216
IRL3803	9712	175	10	25	1000	0		1.06E+09	0.862
IRL3803	9727	175	10	50	1000	0		2.12E+09	0.431
IRL3803L	9730	175	16	85	1000	0		3.61E+09	0.254
IRL3803L	9731	175	16	170	1000	0		7.21E+09	0.127
IRLZ44N	9733	175	10	50	1000	0		2.12E+09	0.431
IRL2505	9733	175	10	50	1000	0		2.12E+09	0.431
IRFZ46N	9703	175	20	240	1000	1	C	5.28E+10	0.038
IRFZ46N	9712	175	20	85	1000	0		1.87E+10	0.049
IRF3710	9731	175	20	100	1000	0		2.20E+10	0.042
IRF540N	9732	175	20	85	1000	0		1.87E+10	0.049
IRFZ44N	9733	175	20	50	1000	0		1.10E+10	0.083
IRF540N	9734	175	20	85	1000	0		1.87E+10	0.049
IRF3710	9738	175	20	20	1000	0		4.40E+09	0.208
IRFZ46N	9741	175	20	100	1000	0		2.20E+10	0.042
IRF540N	9747	175	20	85	1000	0		1.87E+10	0.049
IRFZ34N	9749	175	20	40	1000	0		8.81E+09	0.104
IRFZ46N	9749	175	20	40	1000	0		8.81E+09	0.104
IRFZ46N	9750	175	20	340	1000	0		7.48E+10	0.012
IRFZ46N	9801	175	20	170	1000	0		3.74E+10	0.024
IRFZ24N	9806	175	20	85	1000	0		1.87E+10	0.049
IRFZ44N	9807	175	20	85	1000	0		1.87E+10	0.049
IRF2807	9819	175	20	100	1000	0		2.20E+10	0.042
IRF3710	9819	175	20	200	1000	0		4.40E+10	0.021
IRFZ44N	NA	175	20	36	1000	0		7.92E+09	0.115
IRFZ46N	NA	175	20	40	1000	0		8.81E+09	0.104
IRF3710	9810	175	20	40	1000	0		8.81E+09	0.104
IRF6215	9649	175	-20	170	1000	3	C	3.74E+10	0.110
IRF9530N	9643	175	-20	300	1000	0		5.59E+09	0.164
TOTALS				3385		4		5.4E+11	0.010

NOTES:
b. See Appendix C of Reference 1 for an explanation of equivalent device hours for HTRB tests.
c. One FIT represents one failure in one billion (1.0E+09) hours.
d. EQUIVALENT DEV-HRS for the long term gate stress test are determined by Crook's Model (ref. 2) for an observed thermal activation energy, Ea, of 0.4 eV and an observed electric field constant of 0.108MV/cm. Extrapolation is to VG = 12 volts for an "IRF" or "IRC" device and to VG = 6 volts for an "IRL" device.

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.9 TEMPERATURE CYCLING
D2PAK PACKAGE

Surface mounted to test cards at 245°C peak temperature

Tmin = -55°C; T max = +150°C; Cycle Time (delta T = 205°C): 20 minutes; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
				250	500	1000	
IRF820S	9732	85	1000	0	0	0	
IRF3205S	9731	255	1000	0	0	0	
IRF840S	9721	255	1000	0	0	0	
IRF840S	9732	85	1000	0	0	0	
IRF840S	9733	85	1000	0	0	0	
IRF840S	9734	85	1000	0	0	0	
TOTALS		850		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.10 HIGH HUMIDITY, HIGH TEMP. REVERSE BIAS (H3TRB) D2PAK PACKAGE

Surface mounted to test cards at 245°C peak temperature
Junction Temperature: Tj = 85°C; Relative Humidity: 85%
Applied Bias: Vg = 0V; Vd = as specified

Device Type	Date Code	Drain Voltage	Qty	Test Duration (hours)	# of fails @ 168	500	1000	Fail Mode (note a)
IRF9510S	9723	-100	85	1000	0	0	0	
IRF840S	9721	100	169	1000	0	0	0	
IRF3205S	9731	44	169	1000	0	0	0	
TOTALS			338		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.1.11 AUTOCLAVE
D2PAK PACKAGE

Surface mounted to test cards at 245°C peak temperature

T= 121°C, P = 2 atmospheres, RH = 100%; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @	Fail Mode (note a)
IRF3205S	9731	255	96	0	
IRLZ44NS	9643	255	96	0	
IRF840S	9721	255	96	0	
TOTALS		765		0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.2.1 HIGH TEMPERATURE REVERSE BIAS (HTRB) HEXDIP PACKAGE

Junction Temperature: Tj = +150°C or 175°C, as indicated
Applied Bias: Vg = Vs = 0V; Vd = 100% of maximum rated Bvdss up to 500V then 80% of maximum rated Bvdss

Device Type	Date Code	Temp (°C)	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & 80% Bvdss (note b)	Failure Rate @ 90°C & 60% UCL	FITs (note b)
IRFD214	9751	150	85	1000	1	V	1.0E+07	0.196	196
IRFD214	9749	150	85	1000	0		1.0E+07	0.089	89
TOTALS			170		1		2.1E+07	0.098	98

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.2.2 POWER CYCLING
HEXDIP PACKAGE

Junction Temperature (off state): Tj = 30°C | Applied Bias (off state): Vs = Vg = 0V; Vd = 40V to 80V
Junction Temperature (on state): Tj = 30°C + delta T | Applied Bias (off state): Vs = 0V; Vd = 30V to 60V; Vg < 12V
Power Dissipation: Pd = delta Tj + Theta jc | Cycle time: 2 to 4 minutes

Device Type	Date Code	Temp Change delta Tj (°C)	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
					2.5K	5K	10K	
IRFD110	9627	100	60	5000	0	0	-	
IRFD9120	9623	100	64	10000	0	0	0	
TOTALS			124		0	0	0	

NOTE: THIS DATA IS TAKEN FROM QRR#54

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.2.3 TEMPERATURE CYCLING
HEXDIP PACKAGE

Tmin = -55°C; T max = +150°C; Cycle Time (delta T = 205°C): 20 minutes; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
				250	500	1000	
IRFD214	9751	85	1000	0	0	0	
IRFD214	9749	170	1000	0	0	0	
TOTALS		255		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.2.4 HIGH HUMIDITY, HIGH TEMP. REVERSE BIAS (H3TRB) HEXDIP PACKAGE

Junction Temperature: Tj = 85°C; Relative Humidity: 85%
Applied Bias: Vg = 0V; Vd = as specified

Device Type	Date Code	Drain Voltage	Qty	Test Duration (hours)	# of fails @			Fail Mode (note a)
					168	500	1000	
IRFD9014	9508	-60	50	1000	0	0	0	
IRFD9010	9605	-60	50	1000	0	0	0	
IRFD9020	9605	-60	50	1000	0	0	0	
IRFD014	9453	60	50	1000	0	0	0	
IRLD014	9503	60	50	1000	0	0	0	
IRFD1Z0	9523	100	40	1000	0	0	0	
IRFD110	9605	100	61	1000	0	0	0	
IRFD9110	9606	-100	20	1096	0	0	0	
IRFD110	9607	100	30	1000	0	0	0	
IRFD9120	9509	-100	50	1000	0	0	0	
IRFD120	9551	100	20	1000	0	0	0	
IRFD120	9605	100	50	1000	0	0	0	
IRFD9120	9605	-100	50	1096	0	0	0	
IRFD120	9525	100	40	1000	0	0	0	
IRFD210	9603	100	50	1000	0	0	0	
IRFD220	9508	100	50	1000	0	0	0	
IRFD9220	9605	-100	20	1096	0	0	0	
IRFD220	9617	100	50	1000	0	0	0	
TOTALS			781		0	0	0	

NOTE: THIS DATA IS TAKEN FROM QRR#54

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.2.5 HIGH TEMPERATURE GATE STRESS
HEXDIP PACKAGE

Junction Temperature: Tj = +150°C or +175°C, as specified: Applied Bias: Vs = Vd = 0V; Vg as specified

Device Type	Date Code	Temp (°C)	Gate Bias	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & Vg = 12V (6V for logic); (note d)	Failure Rate @ 90°C & Vg = 12V (FITs) (note C)
IRFD9120	9605	150	-20	60	1000	0		6.06E+08	1.509
IRFD9120	9509	150	-20	49	1000	0		4.95E+08	1.848
IRFD9010	9605	150	-20	10	1000	0		1.01E+08	9.056
IRFD9014	9508	150	-20	50	1000	0		5.05E+08	1.811
IRLD014	9503	150	10	50	1000	0		5.05E+08	1.811
IRLD014	9603	150	10	20	1000	0		2.02E+08	4.528
IRLD110	9603	150	10	39	1000	0		3.94E+08	2.322
IRFD014	9453	150	20	50	1000	1	V	5.05E+08	4.016
IRFD110	9605	175	20	100	1000	2	L	1.86E+09	1.653
IRFD220	9508	150	20	50	1000	0		5.05E+08	1.811
IRFD120	9525	175	20	40	1000	0		7.45E+08	1.227
IRFD120	9623	150	20	50	1000	0		5.05E+08	1.811
IRFD1Z0	9523	175	20	40	1000	0		7.45E+08	1.227
IRFD210	9623	150	20	49	1000	0		4.95E+08	1.848
TOTALS				657		3		8.17E+09	0.505

NOTE: THIS DATA IS TAKEN FROM QRR#54
NOTES:
b. See Appendix C of Reference 1 for an explanation of equivalent device hours for HTRB tests.
c. One FIT represents one failure in one billion (1.0E+09) hours.
d. EQUIVALENT DEV-HRS for the long term gate stress test are determined by Crook's Model (ref. 2) for an observed thermal activation energy, Ea, of 0.4 eV and an observed electric field constant of 0.108MV/cm. Extrapolation is to VG = 12 volts for an "IRF" or "IRC" device and to VG = 6 volts for an "IRL" device.

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.1 HIGH TEMPERATURE REVERSE BIAS (HTRB)
HEXFET GENERATION 3, D-PAK/I-PAK PACKAGE

Junction Temperature: Tj = +150°C or 175°C, as indicated

Applied Bias: Vg = Vs = 0V; Vd = 100% of maximum rated Bvdss up to 500V then 80% of maximum rated Bvdss

Device Type	Date Code	Temp (°C)	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & 80% Bvdss (note b)	Failure Rate @ 90°C & 60% UCL	FITs (note b)
IRFU9320	9722	150	255	1000	0		2.1E+07	0.044	44
IRFR9320	9720	150	85	1000	0		7.0E+06	0.131	131
IRFR9320	9724	150	170	1000	0		1.4E+07	0.065	65
IRFU9320	9713	150	100	1000	0		8.2E+06	0.111	111
IRFR9224	9712	150	250	1000	1	L	2.3E+07	0.089	89
IRFR9220	9722	150	85	1000	0		8.0E+06	0.115	115
IRFU9224	9712	150	100	1000	0		9.4E+06	0.098	98
IRFU9224	9708	150	198	1000	0		1.9E+07	0.049	49
IRFU024	9715	175	599	1024	1	L	3.3E+08	0.006	6
IRFU020	9738	175	85	1000	0		4.6E+07	0.020	20
IRFU020	9744	175	85	1000	0		4.6E+07	0.020	20
IRFR024	9703	150	84	1000	0		9.3E+06	0.098	98
IRFU024	9703	150	85	1000	0		9.4E+06	0.097	97
IRFU024	9704	150	254	1000	0		2.8E+07	0.033	33
IRFR110	9727	150	85	1000	2	V	9.7E+06	0.321	321
IRFU214	9811	150	85	1000	0		1.0E+07	0.089	89
IRFU210	9740	150	170	1000	0		2.1E+07	0.044	44
IRFU214	9740	150	85	1000	0		1.1E+07	0.086	86
IRFU420	9738	150	85	1000	0		1.2E+07	0.073	73
IRFU420	9744	150	85	1000	0		1.2E+07	0.073	73
IRFR420	9740	150	85	1000	0		1.2E+07	0.073	73
IRFR420	9722	150	255	1000	1	V	3.7E+07	0.054	54
IRFRC20	9722	150	85	1000	1	L	1.3E+07	0.152	152
IRFUC20	9745	150	85	1000	0		1.3E+07	0.069	69
IRFUC20	9704	150	100	1048	0		1.6E+07	0.056	56
TOTALS			3640		6		7.4E+08	0.010	10

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.2 POWER CYCLING
D-PAK/I-PAK PACKAGE

Junction Temperature (off state): Tj = 30°C
Applied Bias (off state): Vs = Vg = 0V; Vd
Junction Temperature (on state): Tj = 30°C + delta T
Applied Bias (off state): Vs = 0V; Vd = 30V to
Power Dissipation: Pd = delta Tj + Theta jc
Cycle time:

Device Type	Date Code	Temp Change delta Tj (°C)	Qty	Test Duration (cycles)	# of fails @		
					2.5K	5K	10K
IRFR420	9730	100	339	15000	0	0	0
IRFR9024	9744	100	80	15000	0	0	0
IRFU024	9703	100	85	10000	0	0	0
IRFU024	9704	100	255	10000	0	0	0
IRFU120	9751	100	85	15000	0	0	0
IRFU9024	9704	100	85	10000	0	0	0
IRFU9024	9707	100	85	10000	0	0	0
TOTALS			1014		0	0	0

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

d = 40V to 80V
50V; Vg < 12V
: 2 to 4 minutes

Fail Mode (note a)

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.3 TEMPERATURE CYCLING
I-PAK PACKAGE

Tmin = -55°C; T max = +150°C; Cycle Time (delta T = 205°C): 20 minutes; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
				250	500	1000	
IRFU010	9510	100	1000	0	0	0	
IRFU014	9449	100	1000	0	0	0	
IRFU014	9450	100	1000	0	0	0	
IRFU014	9451	200	1000	0	0	0	
IRFU210	9603	50	1000	0	0	0	
IRFU9110	9510	50	1000	0	0	0	
IRLU014	9537	39	1000	0	0	0	
IRFU024	9501	50	1000	0	0	0	
IRFU024	9616	40	1000	0	0	0	
IRFU224	9605	50	1000	0	0	0	
IRFU420	9449	100	1000	0	1	0	C
IRFU420	9450	200	1000	0	3	2	R
IRFU420	9451	80	1000	0	0	0	
IRFU420	9514	300	10000	1	0	1	C
IRFU420	9517	100	1000	0	0	0	
IRFU9024	9520	100	1000	0	0	0	
IRFU9024	9528	75	1000	0	0	0	
IRFU1205	9604	100	1000	0	0	0	
TOTALS		1834		1	4	3	

NOTE: THIS DATA IS TAKEN FROM QRR#54

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.4 HIGH HUMIDITY, HIGH TEMP. REVERSE BIAS (H3TRB) I-PAK PACKAGE

Junction Temperature: Tj = 85°C; Relative Humidity: 85%
Applied Bias: Vg = 0V; Vd = as specified

Device Type	Date Code	Drain Voltage	Qty	Test Duration (hours)	# of fails @			Fail Mode (note a)
					168	500	1000	
IRFU9224	9708	-100	373	1000	0	0	0	
IRFU9320	9720	-100	247	1000	0	0	0	
IRFU120	9751	100	85	1000	0	0	0	
IRFUC20	9745	100	85	1000	0	0	0	
TOTALS			790		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.5 HIGH TEMPERATURE GATE STRESS
HEXFET GENERATION 3 D-PAK/I-PAK PACKAGE

Junction Temperature: Tj = +150°C or +175°C, as specified: Applied Bias: Vs = Vd = 0V; Vg as specified

Device Type	Date Code	Temp (°C)	Gate Bias	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & Vg = 12V (6V for logic); (note d)	Failure Rate @ 90°C & Vg = 12V (FITs) (note C)
IRLR024	9722	175	10	85	1000	0		1.58E+09	0.578
IRFR024	9703	150	20	85	1000	0		8.59E+08	1.065
IRFU024	9703	150	20	84	1000	1	V	8.49E+08	2.391
IRFU024	9704	150	20	340	1000	1	V	3.44E+09	0.591
IRFR420	9722	150	20	85	1000	0		8.59E+08	1.065
IRFR420	9732	150	20	340	1000	0		3.44E+09	0.266
IRFU120	9751	175	20	85	1000	0		1.58E+09	0.578
IRFR9220	9722	150	-20	85	1000	0		8.59E+08	1.065
TOTALS				1189		2		1.35E+10	0.229

NOTES:

b. See Appendix C of Reference 1 for an explanation of equivalent device hours for HTRB tests.

c. One FIT represents one failure in one billion (1.0E+09) hours.

d. EQUIVALENT DEV-HRS for the long term gate stress test are determined by Crook's Model (ref. 2) for an observed thermal activation energy, Ea, of 0.4 eV and an observed electric field constant of 0.108MV/cm. Extrapolation is to VG = 12 volts for an "IRF" or "IRC" device and to VG = 6 volts for an "IRL" device.

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.6 AUTOCLAVE
I-PAK PACKAGE

T= 121°C, P = 2 atmospheres, RH = 100%; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @	Fail Mode (note a)
IRFU120	9751	85	96	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.7 HIGH TEMPERATURE REVERSE BIAS (HTRB) HEXFET GENERATION 5, D-PAK/I-PAK PACKAGE

Junction Temperature: Tj = +150°C or 175°C, as indicated
Applied Bias: Vg = Vs = 0V; Vd = 100% of maximum rated Bvdss up to 500V then 80% of maximum rated Bvdss

Device Type	Date Code	Temp (°C)	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & 80% Bvdss (note b)	Failure Rate @ 90°C & 60% UCL	FITs (note b)
IRFR3910	9722	175	255	1000	0		1.4E+08	0.007	7

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.8 HIGH TEMPERATURE GATE STRESS
HEXFET GENERATION 5, D-PAK/I-PAK PACKAGE

Junction Temperature: Tj = +150°C or +175°C, as specified: Applied Bias: Vs = Vd = 0V; Vg as specified

Device Type	Date Code	Temp (°C)	Gate Bias	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & Vg = 12V (6V for logic); (note d)	Failure Rate @ 90°C & Vg = 12V (FITs) (note C)
IRFR3910	9722	175	20	85	1000	1	C	1.87E+10	0.108

NOTES:
b. See Appendix C of Reference 1 for an explanation of equivalent device hours for HTRB tests.
c. One FIT represents one failure in one billion (1.0E+09) hours.
d. EQUIVALENT DEV-HRS for the long term gate stress test are determined by Crook's Model (ref. 2) for an observed thermal activation energy, Ea, of 0.4 eV and an observed electric field constant of 0.108MV/cm. Extrapolation is to VG = 12 volts for an "IRF" or "IRC" device and to VG = 6 volts for an "IRL" device.

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.9 TEMPERATURE CYCLING
D-PAK PACKAGE

Surface mounted to test cards at 245°C peak temperature

Tmin = -55°C; T max = +150°C; Cycle Time (delta T = 205°C): 20 minutes; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
				250	500	1000	
IRFR110	9727	85	1000	0	0	0	
IRFR024	9703	170	1000	0	0	0	
IRFR024	9704	340	1000	0	0	0	
IRFR3910	9722	253	1000	0	0	0	
IRFR420	9722	339	1000	0	0	0	
IRFR9024	9744	180	1000	0	0	0	
IRFR1205	9722	255	1000	0	0	0	
TOTALS		1622		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.10 HIGH HUMIDITY, HIGH TEMP. REVERSE BIAS (H3TRB) D-PAK PACKAGE

Surface mounted to test cards at 245°C peak temperature
Junction Temperature: Tj = 85°C; Relative Humidity: 85%
Applied Bias: Vg = 0V; Vd = as specified

Device Type	Date Code	Drain Voltage	Qty	Test Duration (hours)	# of fails @ 168	# of fails @ 500	# of fails @ 1000	Fail Mode (note a)
IRFR9224	9712	-100	248	1000	0	0	0	
IRFR9320	9720	-100	85	1000	0	0	0	
IRFR9320	9724	-100	170	1000	0	0	0	
IRFR024	9704	60	170	1000	0	0	0	
IRFR024	9703	60	170	1000	0	0	0	
IRFR024	9704	60	170	1000	0	0	0	
IRFR420	9722	100	255	1000	0	0	0	
IRFR9220	9722	-100	84	1000	0	0	0	
IRFRC20	9722	100	85	1000	0	0	0	
IRFR3910	9722	100	255	1000	0	0	0	
IRFR1205	9722	55	255	1000	0	0	0	
TOTALS			1947		0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.3.11 AUTOCLAVE
D-PAK PACKAGE

Surface mounted to test cards at 245°C peak temperature

T= 121°C, P = 2 atmospheres, RH = 100%; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @	Fail Mode (note a)
IRFR1205	9722	255	96	0	
IRFR024	9703	170	96	0	
IRFR024	9704	414	96	0	
IRFR3910	9722	255	96	0	
TOTALS		1094		0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.4.1 HIGH TEMPERATURE REVERSE BIAS (HTRB) HEXSENSE PACKAGE

Junction Temperature: Tj = +150°C or 175°C, as indicated
Applied Bias: Vg = Vs = 0V; Vd = 100% of maximum rated Bvdss up to 500V then 80% of maximum rated Bvdss

Device Type	Date Code	Temp (°C)	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & 80% Bvdss (note b)	Failure Rate @ 90°C & 60% UCL	FITs (note b)
IRCZ24	9521	175	40	1000	0		2.1E+07	0.043	43
IRCZ34	9513	150	48	1000	0		5.3E+06	0.172	172
IRCZ34	9628	175	40	1000	0		2.1E+07	0.043	43
IRCZ34	9523	150	40	500	0		2.2E+06	0.414	414
IRC540	9514	150	50	1000	0		5.7E+06	0.161	161
IRC540	9628	175	50	1000	0		2.7E+07	0.033	33
IRC840	9502	150	100	1000	16	L	1.5E+07	1.205	1205
TOTALS			368		16		9.8E+07	0.180	180

NOTE: THIS DATA IS TAKEN FROM QRR#54

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.4.2 POWER CYCLING
HEXSENSE PACKAGE

Junction Temperature (off state): Tj = 30°C

Applied Bias (off state): Vs = Vg = 0V; Vd = 40V to 80V

Junction Temperature (on state): Tj = 30°C + delta T

Applied Bias (off state): Vs = 0V; Vd = 30V to 60V; Vg < 12V

Power Dissipation: Pd = delta Tj + Theta jc

Cycle time: 2 to 4 minutes

Device Type	Date Code	Temp Change delta Tj (°C)	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
					2.5K	5K	10K	

No data available at this time

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.4.3 TEMPERATURE CYCLING
HEXSENSE PACKAGE

Tmin = -55°C; T max = +150°C; Cycle Time (delta T = 205°C): 20 minutes; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @			Fail Mode (note a)
				250	500	1000	
IRCZ44	9649	100	1000	0	0	0	

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.4.4 HIGH HUMIDITY, HIGH TEMP. REVERSE BIAS (H3TRB) HEXSENSE PACKAGE

Junction Temperature: Tj = 85°C; Relative Humidity: 85%
Applied Bias: Vg = 0V; Vd = as specified

Device Type	Date Code	Drain Voltage	Qty	Test Duration (hours)	# of fails @			Fail Mode (note a)
					168	500	1000	
IRCZ24	9628	60	34	1000	0	0	0	
IRCZ34	9513	60	44	1000	0	0	0	
IRCZ34	9523	60	37	1000	0	0	0	
IRCZ44	9614	60	17	1000	0	0	0	
IRCZ44	9524	60	40	1000	0	0	0	
IRC530	9601	100	17	1000	0	0	0	
IRC540	9514	100	50	1000	0	0	0	
IRC540	9549	100	16	1000	0	0	0	
IRC640	9529	100	19	1000	0	0	0	
IRC840	9502	100	50	1000	0	0	0	
TOTALS			324		0	0	0	

NOTE: THIS DATA IS TAKEN FROM QRR#54

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.4.5 HIGH TEMPERATURE GATE STRESS HEXSENSE PACKAGE

Junction Temperature: Tj = +150°C or +175°C, as specified: Applied Bias: Vs = Vd = 0V; Vg as specified

Device Type	Date Code	Temp (°C)	Gate Bias	Qty	Test Duration (hours)	# Fails	Fail Mode *	Equivalent Dev. - Hrs. @ 90°C & Vg = 12V (6V for logic); (note d)	Failure Rate @ 90°C & Vg = 12V (FITs) (note C)
IRCZ24	9521	175	20	40	1000	0		7.45E+08	1.227
IRCZ34	9525	150	20	40	500	0		2.02E+08	4.528
IRCZ34	9513	150	20	50	1000	0		5.05E+08	1.811
IRCZ44	9524	150	20	40	500	0		2.02E+08	4.528
IRCZ44	9524	150	20	40	500	0		2.02E+08	4.528
IRC540	9514	150	20	50	1000	0		5.05E+08	1.811
IRC840	9502	150	20	50	884	0		4.47E+08	2.049
TOTALS				310		0		2.81E+09	0.326

NOTE: THIS DATA IS TAKEN FROM QRR#54

NOTES:

b. See Appendix C of Reference 1 for an explanation of equivalent device hours for HTRB tests.

c. One FIT represents one failure in one billion (1.0E+09) hours.

d. EQUIVALENT DEV-HRS for the long term gate stress test are determined by Crook's Model (ref. 2) for an observed thermal activation energy, Ea, of 0.4 eV and an observed electric field constant of 0.108MV/cm. Extrapolation is to VG = 12 volts for an "IRF" or "IRC" device and to VG = 6 volts for an "IRL" device.

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift

4.4.6 AUTOCLAVE
HEXSENSE PACKAGE

T= 121°C, P = 2 atmospheres, RH = 100%; Bias: none applied

Device Type	Date Code	Qty	Test Duration (cycles)	# of fails @	Fail Mode (note a)
IRCZ34	9513	50	168	3	C
IRCZ44	9626	231	96	0	
IRC540	9514	50	168	3	L
TOTALS		331		6	

NOTE: THIS DATA IS TAKEN FROM QRR#54

*Failure Modes: C-catastrophic short; L-param. shift in drain leakage; R - param. shift in on-resistance; T - param. thermal resistance shift; V - param. threshold shift