reaching the counter. This allows the ripple-nature of the counter to stabilize (ripple through) at the correct count value. Software introduces a slight delay between closing the gate and taking the reading.

Logic level signals (nominally 0V to 5V) are input to the PIC-Gen via socket SK1 (Logic Input), switch S5 selecting their routing to gate IC7a and the counter. Signals having other voltage ranges, either above or below the 0V/5V range should not be input to socket SK1. Those having lesser swings may not trigger gate IC7a, those having swings greater than about 6V could kill it.

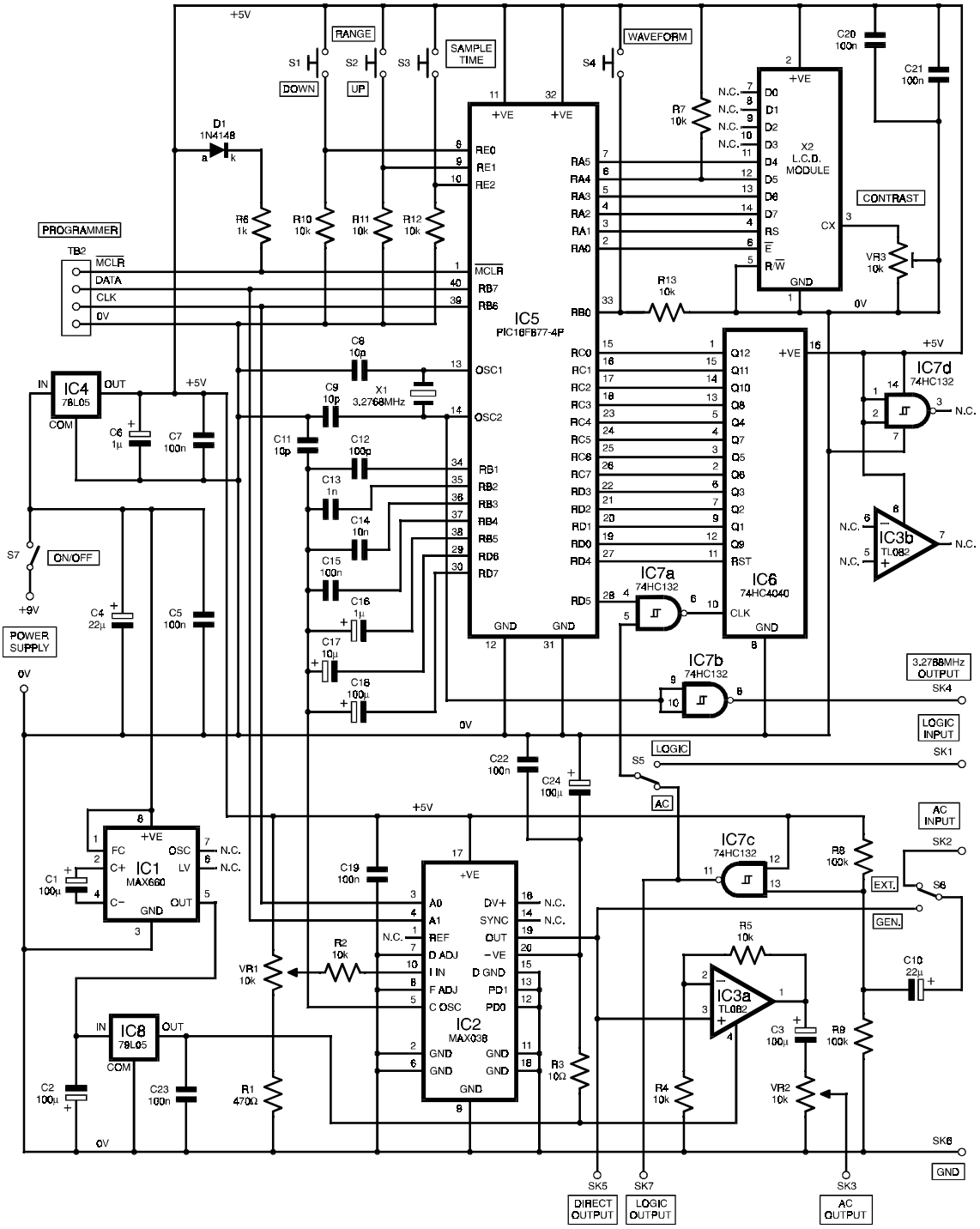

Fig.1. Full circuit diagram for the PIC-Gen Frequency generator and Counter.