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ADXL312 Quick Start User Guide

DEVICE OVERVIEW

The ADXL312 is a 3-axis low-*g* accelerometer, capable of sensing a full-scale range of up to ±12 g. Figure 1 shows the sensing axes of the device.

The ADXL312 reports positive acceleration when it is accelerated in the direction of the sensing axes shown in Figure 1. Gravity, which is a constant +1 *g* acceleration force, also factors into the overall response of the ADXL312. Figure 2 shows the output response to gravity. The user must be careful to account for gravity, as it can affect the output of one or more of the sensor axes.

The ADXL312 is supplied in a small, thin, 5 mm × 5 mm × 1.45 mm, 32-lead, plastic package. Refer to the ADXL312 data sheet for recommended printed circuit board land pattern.

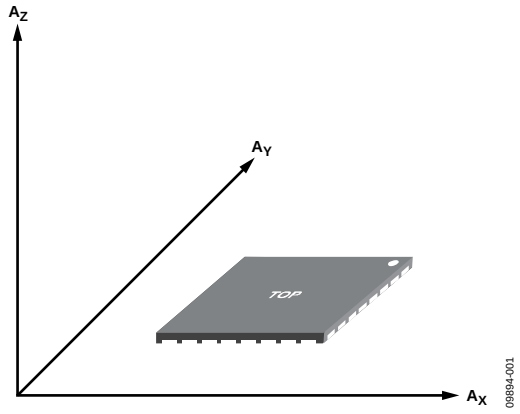

Figure 1. Sensing Axes of ADXL312

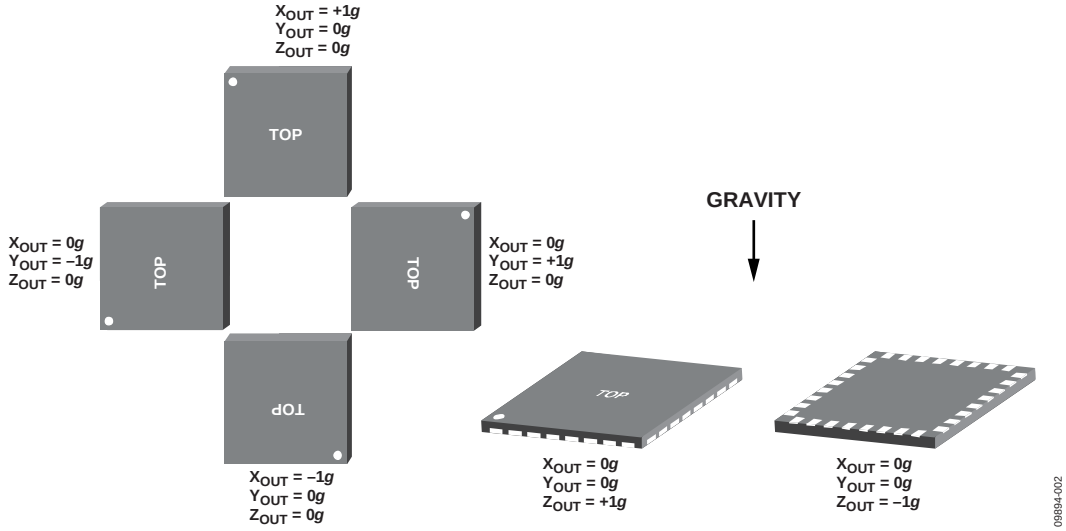

Figure 2. Output Response vs. Orientation to Gravity

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REVISION HISTORY

6/11—Revision 0: Initial Version

ELECTRICAL CONNECTION

The ADXL312 accepts commands via either the I²C or the SPI standard communication protocols. The SPI interface is compatible with either 3-wire or 4-wire configurations. Figure 3 shows the recommended electrical connections for 4-wire SPI. When using the 3-wire SPI configuration, disconnect the SDO pin.

Figure 4 shows the recommended electrical connection for I²C communications. The 7-bit I²C address for the device is 0x53, followed by the R/$\overline{W}$ bit. The user can select an alternate I²C address by connecting the SDO/ALT ADDRESS pin to the $V_{DD\ I/O}$ pin. The 7-bit I²C address for that configuration is 0x1D, followed by the R/$\overline{W}$ bit.

Refer to the ADXL312 data sheet for details on power supply decoupling.

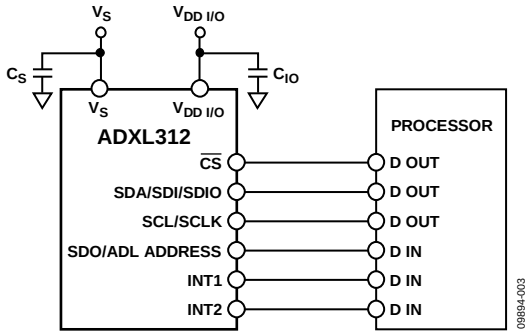

Figure 3. Recommended Connection for 4-Wire SPI Mode

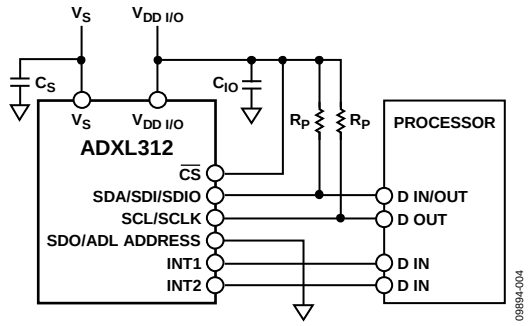

Figure 4. Recommended Connection for I²C Mode

COMMUNICATION INTERFACE

Table 1 gives the list of typical SPI configuration settings. This includes the SPI clock phase and SPI clock polarity. The ADXL312 is always configured as a slave device. For the micro controller, these settings are normally stored in the control registers. Refer to the ADXL312 data sheet for timing specifications and a command sequence.

Table 1. SPI Settings

Processor Setting	Description
Master	ADXL312 operates as slave
SPI Mode	Clock polarity (CPOL) = 1 Clock phase (CPHA) = 1
Bit Sequence	MSB first

For I²C communication, refer to the ADXL312 data sheet and *UM10204 I²C-Bus Specification and User Manual*, Rev. 03-19, June 2007, for processor settings as well as timing specifications and a command sequence.

Sometimes it is important to confirm the validity of a communication sequence before going to the next design stage. This is done by reading the DEVID register (Address 0x00). The DEVID register is read-only, and contains the value 0xE5. If the data read from DEVID is not 0xE5, it indicates that either the physical connection or command sequence is incorrect.

INITIALIZATION

Figure 5 shows the minimum initialization sequence. The ADXL312 operates in a 100 Hz ODR with a DATA_READY interrupt on the INT1 pin after this start-up sequence. When setting other interrupts or using the FIFO, it is recommended that the corresponding registers are set before the POWER_CTL and INT_ENABLE registers. Refer to the ADXL312 data sheet and the AN-1025 application note for other operation modes of ADXL312 and details about FIFO.

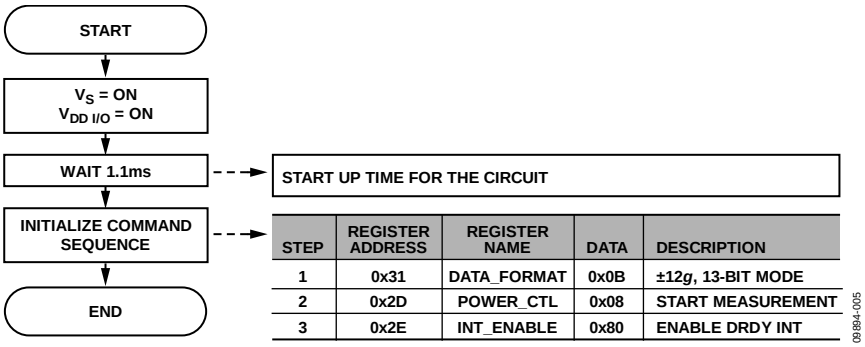

Figure 5. Minimum Initialization Sequence

READING OUTPUT DATA

The DATA_READY interrupt signal indicates that all 3-axes of acceleration data have been updated in the data registers. It is latched high when new data is ready. The interrupt behavior, latch high or latch low, can be configured through the DATA_FORMAT register. Refer to the ADXL312 data sheet for details.) Use the low-to-high transition to trigger action on an interrupt service routine. Data is read from the DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, and DATAZ1 registers. To ensure data coherency, use multibyte reads to retrieve data from the ADXL312. Figure 7 shows the read sequence example for 4-wire SPI.

DATA FORMAT

The data format of the ADXL312 is 16 bits. Once acceleration data is acquired from data registers, the user must reconstruct the data. DATAX0 is the low byte register for X-axis acceleration and DATAX1 is the high byte register. In 13-bit mode, the upper four bits are sign bits (see Figure 6). Note that other data formats are available by setting the DATA_FORMAT register. See the ADXL312 data sheet for more details.

The ADXL312 uses twos-complement data format. When in 13-bit mode, 1 LSB represents about 2.9 mg.

Table 2. ADXL312 Output Data Format

16-Bit Code (Hex)	Twos-Complement Representation (Decimal)	Acceleration (mg)
0FFF	4095	+11878
…	…	…
0002	+2	+5.8
0001	+1	+2.9
0000	0	0
FFFF	−1	−2.9
FFFE	−2	−5.8
…	…	…
F000	−4095	−11878

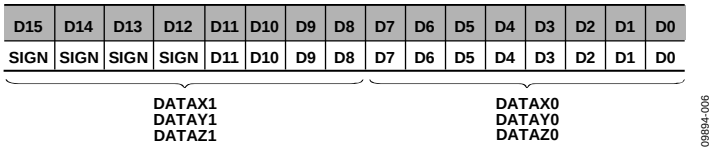

Figure 6. Data Construction

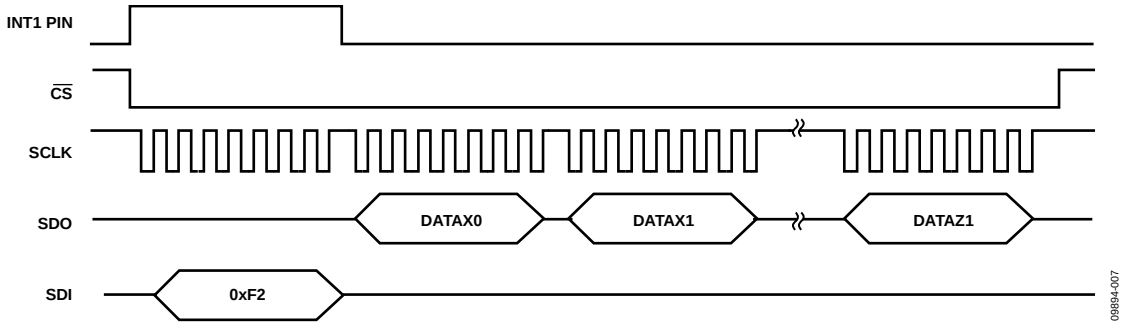

Figure 7. Data Read Timing Sequence for 4-Wire SPI Connection

USING THE SELF-TEST FEATURE

The ADXL312 provides a self-test feature that enables an electromechanical test on the device without external mechanical stimulus. Figure 8 outlines a recommended self-test sequence. For best results, place the ADXL312 in a stable environment when conducting the self-test sequence.

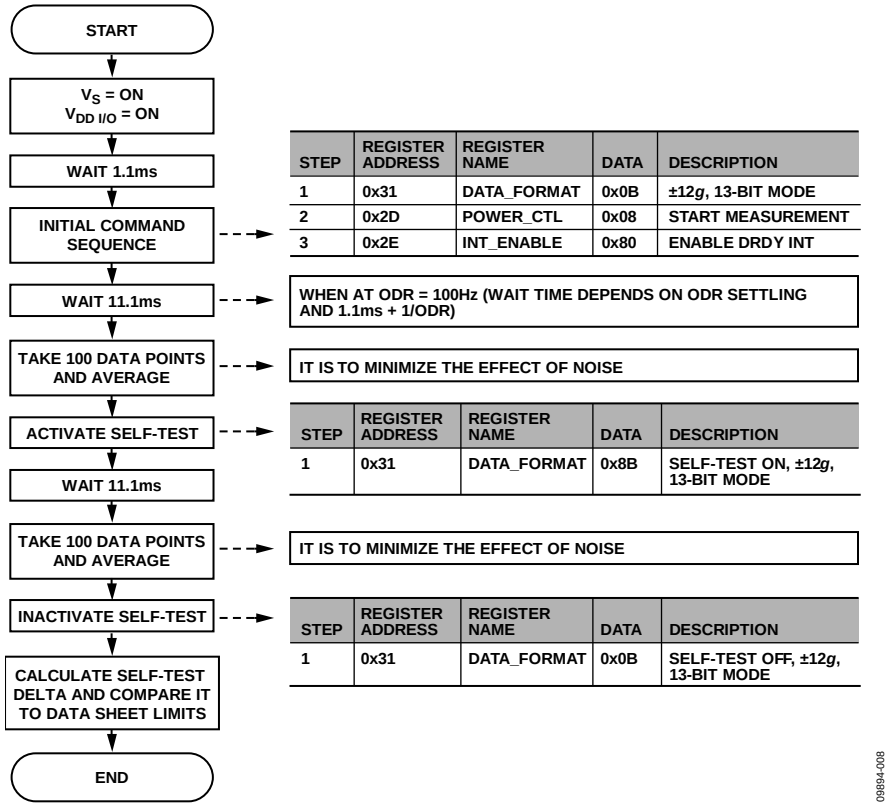

Figure 8. Self-Test Sequence

USING OFFSET REGISTERS

The ADXL312 has offset registers that facilitate offset calibration. The data format for the offset registers is 8-bit, twos compliment. The resolution of the offset registers is about 11.6 mg/LSB. If offset calibration must be finer than 11.6 mg/LSB, the calibration needs to be done at the processor. The offset register adds the value written in the register to measured acceleration. For example, if the offset is +116 mg, then write −116 mg to the offset register.

Figure 9 shows the typical offset calibration sequence.

For this routine, X/Y axes errors are zero when 0 *g* input is applied, whereas Z-axis errors are zero when 1 *g* input is applied. Greater accuracy can be achieved if it is possible to rotate the ADXL312 at calibration.

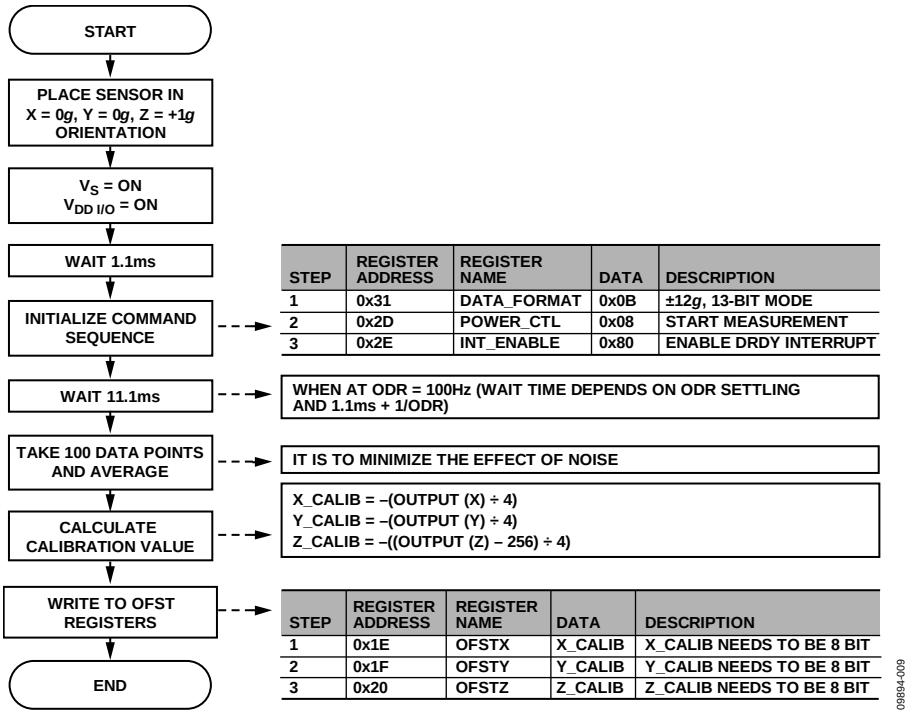

Figure 9. Offset Calibration Sequence

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