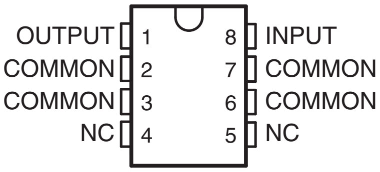
LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

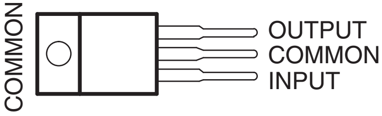
- **Very Low Dropout Voltage, Less Than 0.6 V at 150 mA**
- **Very Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751L Series**
- **60-V Load-Dump Protection**
- **Reverse Transient Protection Down to –50 V**
- **Internal Thermal-Overload Protection**
- **Overvoltage Protection**
- **Internal Overcurrent-Limiting Circuitry**
- **Less Than 500-μA Disable (TL751L Series)**

TL750L . . . D PACKAGE
(TOP VIEW)

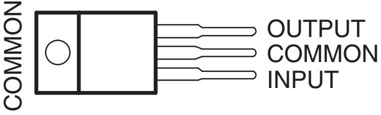


NC – No internal connection

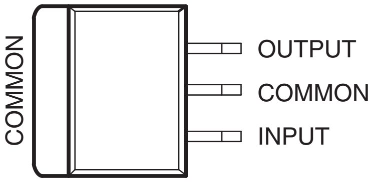
TL750L . . . KC PACKAGE
(TOP VIEW)



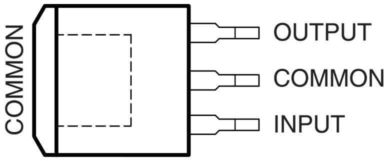
TL750L . . . KCS PACKAGE
(TOP VIEW)



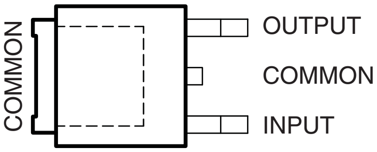
TL750L . . . KTE PACKAGE
(TOP VIEW)



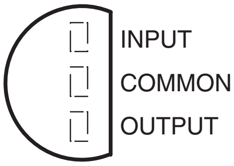
TL750L . . . KTT PACKAGE
(TOP VIEW)



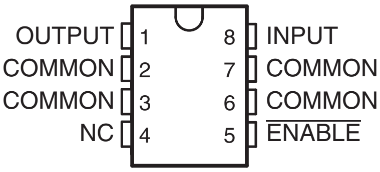
TL750L . . . KVU PACKAGE
(TOP VIEW)



TL750L . . . LP PACKAGE
(TO-92, TO-226AA)
(TOP VIEW)

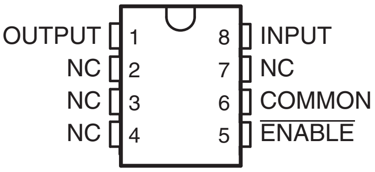


TL751L . . . D PACKAGE
(TOP VIEW)



NC – No internal connection

TL751L . . .P PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION/ORDERING INFORMATION

The TL750L and TL751L series of fixed-output voltage regulators offer 5-V, 8-V, 10-V, and 12-V options. The TL751L series also has an enable ($\overline{\text{ENABLE}}$) input. When $\overline{\text{ENABLE}}$ is high, the regulator output is placed in the high-impedance state. This gives the designer complete control over power up, power down, or emergency shutdown.

The TL750L and TL751L series are low-dropout positive-voltage regulators specifically designed for battery-powered systems. These devices incorporate overvoltage and current-limiting protection circuitry, along with internal reverse-battery protection circuitry to protect the devices and the regulated system. The series is fully protected against 60-V load-dump and reverse-battery conditions. Extremely low quiescent current during full-load conditions makes these devices ideal for standby power systems.

ORDERING INFORMATION(1)

T_J	V_O TYP AT 25°C	PACKAGE (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	5 V	PowerFLEX™ – KTE	Reel of 2000	TL750L05CKTER	TL750L05C
		SOIC – D	Tube of 75	TL750L05CD	50L05C
			Reel of 2500	TL750L05CDR	
			Tube of 75	TL751L05CD	51L05C
			Reel of 2500	TL751L05CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L05CLP	750L05C
			Reel of 2000	TL750L05CLPR	
		TO-220 – KC	Tube of 50	TL750L05CKC	TL750L05C
		TO-220 – KCS	Tube of 50	TL750L05CKCS	TL750L05C
		TO-252 – KVU	Reel of 2500	TL750L05CKVUR	750L05C
		TO-263 – KTT	Reel of 500	TL750L05CKTTR	750L05C
	8 V	SOIC – D	Tube of 75	TL750L08CD	50L08C
			Reel of 2500	TL750L08CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L08CLP	750L08C
	10 V	PDIP – P	Tube of 50	TL751L10CP	TL751L10C
		SOIC – D	Tube of 75	TL750L10CD	50L10C
			Reel of 2500	TL750L10CDR	
			Tube of 75	TL751L10CD	51L10C
			Reel of 2500	TL751L10CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L10CLP	750L10C
			Reel of 2000	TL750L10CLPR	
	12 V	SOIC – D	Tube of 75	TL750L12CD	50L12C
			Reel of 2500	TL750L12CDR	
			Tube of 75	TL751L12CD	51L12C
			Reel of 2500	TL751L12CDR	
		TO-226/TO-92 – LP	Bulk of 1000	TL750L12CLP	750L12C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE COMPONENT COUNT	
Transistors	20
JFETs	2
Diodes	5
Resistors	16

Absolute Maximum Ratings[1]

over operating junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Continuous input voltage			26	V
	Transient input voltage[2]	T_A = 25°C		60	V
	Continuous reverse input voltage			–15	V
	Transient reverse input voltage	t ≤ 100 ms		–50	V
T_J	Operating virtual junction temperature			150	°C
	Lead temperature	1,6 mm (1/16 in) for 10 s		260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The transient input voltage rating applies to the waveform shown in Figure 1.

Package Thermal Data[1]

PACKAGE	BOARD	θ_{JC}	θ_{JA}
PDIP (P)	High K, JESD 51-7	57°C/W	85°C/W
PowerFLEX™ (KTE)	High K, JESD 51-5	3°C/W	23°C/W
SOIC (D)	High K, JESD 51-7	39°C/W	97°C/W
TO-226/TO-92 (LP)	High K, JESD 51-7	55°C/W	140°C/W
TO-220 (KC)	High K, JESD 51-5	3°C/W	19°C/W
TO-220 (KCS)	High K, JESD 51-5	3°C/W	19°C/W
TO-252 (KVU)	High K, JESD 51-5	–	30.3°C/W
TO-263 (KTT)	High K, JESD 51-5	18°C/W	25.3°C/W

(1) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Recommended Operating Conditions

over recommended operating junction temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_I	Input voltage		TL75xL05	6	26	V
			TL75xL08	9	26	
			TL75xL10	11	26	
			TL75xL12	13	26	
V_{IH}	High-level $\overline{\text{ENABLE}}$ input voltage		TL75xLxx	2	15	V
V_{IL} [1]	Low-level $\overline{\text{ENABLE}}$ input voltage	T_J = 25°C	TL75xLxx	–0.3	0.8	V
		T_J = 0°C to 125°C	TL75xLxx	–0.15	0.8	
I_O	Output current		TL75xLxx	0	150	mA
T_J	Operating virtual junction temperature		TL75xLxxC	0	125	°C

(1) The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for $\overline{\text{ENABLE}}$ voltage levels and temperature only.

TL75xL05 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L05 TL751L05			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 6 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	4.8	5	5.2	V
		T_J = 0°C to 125°C	4.75		5.25	
Input regulation voltage	V_I = 9 V to 16 V			5	10	mV
	V_I = 6 V to 26 V			6	30	
Ripple rejection	V_I = 8 V to 18 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			20	50	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 6 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

---

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TL75xL08 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L08 TL751L08			UNIT
			MIN	TYP	MAX	
Output voltage	V_I = 9 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	7.68	8	8.32	V
		T_J = 0°C to 125°C	7.6		8.4	
Input regulation voltage	V_I = 10 V to 17 V			10	20	mV
	V_I = 9 V to 26 V			25	50	
Ripple rejection	V_I = 11 V to 21 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			40	80	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 9 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

---

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 10-μF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TL75xL10 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L10 TL751L10 MIN	TYP	MAX	UNIT
Output voltage	V_I = 11 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
Input regulation voltage	V_I = 12 V to 19 V			10	25	mV
	V_I = 11 V to 26 V			30	60	
Ripple rejection	V_I = 12 V to 22 V, f = 120 Hz		60	65		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	100	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		µV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 11 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

TL75xL12 Electrical Characteristics[1]

V_I = 14 V, I_O = 10 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL750L12 TL751L12 MIN	TYP	MAX	UNIT
Output voltage	V_I = 13 V to 26 V, I_O = 0 to 150 mA	T_J = 25°C	11.52	12	12.48	V
		T_J = 0°C to 125°C	11.4		12.6	
Input regulation voltage	V_I = 14 V to 19 V			15	30	mV
	V_I = 13 V to 26 V			20	40	
Ripple rejection	V_I = 13 V to 23 V, f = 120 Hz		50	55		dB
Output regulation voltage	I_O = 5 mA to 150 mA			50	120	mV
Dropout voltage	I_O = 10 mA				0.2	V
	I_O = 150 mA				0.6	
Output noise voltage	f = 10 Hz to 100 kHz			700		µV
Quiescent current	I_O = 150 mA			10	12	mA
	V_I = 13 V to 26 V, I_O = 10 mA, T_J = 0°C to 125°C			1	2	
	$\overline{\text{ENABLE}}$ ≥ 2 V				0.5	

(1) Pulse-testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-µF capacitor across the input and a 10-µF capacitor, with equivalent series resistance of less than 0.4 Ω, across the output.

PARAMETER MEASUREMENT INFORMATION

The TL750L, TL751L series are low-dropout regulators. This means that capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and its equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and temperature range. Figure 1 shows the recommended range of ESR for a given load with a 10-µF capacitor on the output.

TYPICAL CHARACTERISTICS

TL750L05
EQUIVALENT SERIES RESISTANCE
vs
LOAD CURRENT

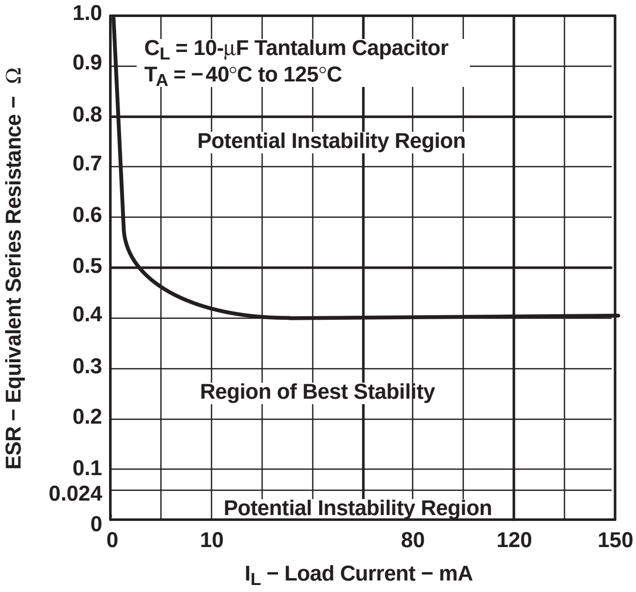


Figure 1.

TRANSIENT INPUT VOLTAGE
vs
TIME

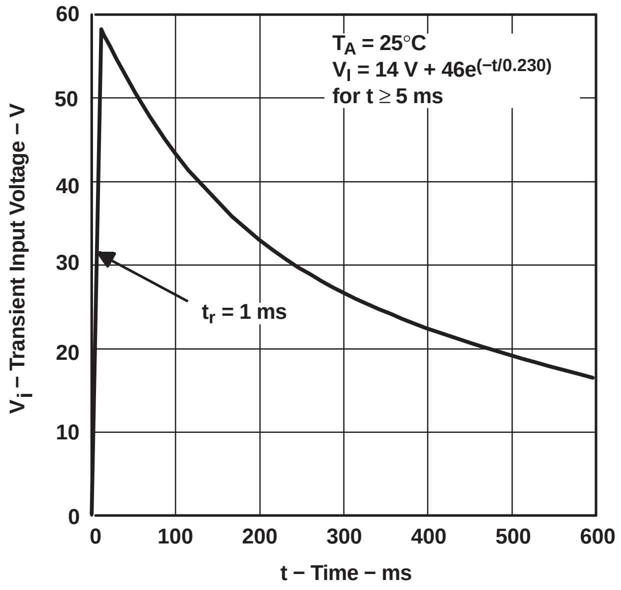


Figure 2.

TL750L05
INPUT CURRENT
vs
INPUT VOLTAGE

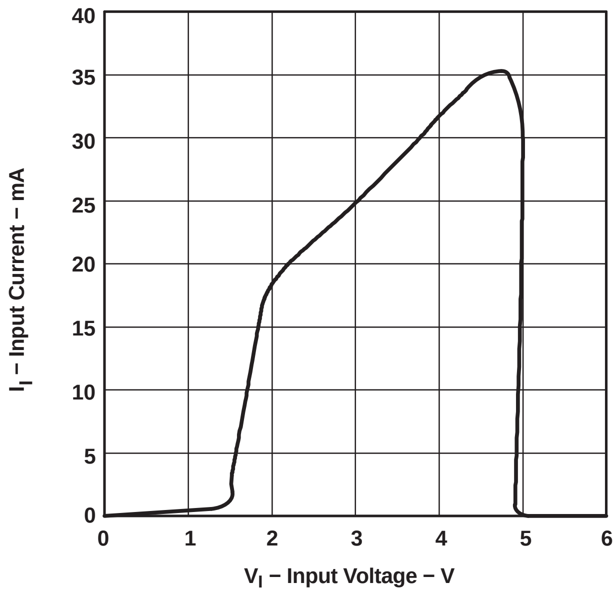


Figure 3.

TL750L12
INPUT CURRENT
vs
INPUT VOLTAGE

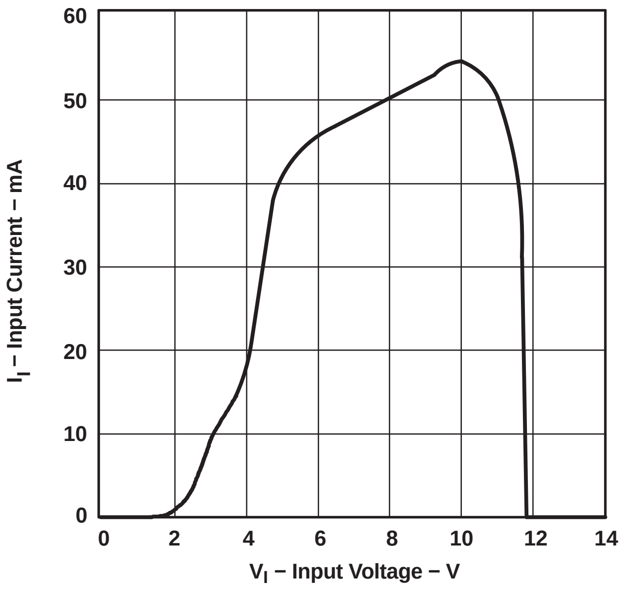


Figure 4.

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
5962-9166901Q2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
5962-9166901QPA	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL750L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L05CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L05CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L05CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L05CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L05CKCE3	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L05CKCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L05CKCSE3	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L05CKTER	OBSOLETE	PFM	KTE	3		TBD	Call TI	Call TI	
TL750L05CKTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	
TL750L05CKTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	
TL750L05CKVURG3	ACTIVE	PFM	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	
TL750L05CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L05CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L05CLPM	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	
TL750L05CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L05CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L05CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL750L05QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL750L05QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L05QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L05QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	
TL750L05QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL750L08CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL750L08CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL750L08CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL750L08CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL750L08CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL750L08CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TL750L08CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L08CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L08CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L08CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL750L08QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L08QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L08QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L08QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	
TL750L10CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L10CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L10CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L10CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L10CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TL750L10CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L10CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L10CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L10CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L10CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L10CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L10CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL750L10QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L10QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L10QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L10QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	
TL750L10QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL750L12CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L12CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L12CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L12CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L12CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L12CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL750L12CKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L12CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L12CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	
TL750L12CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL750L12QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L12QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL750L12QKC	OBSOLETE	TO-220	KC	3		TBD	Call TI	Call TI	
TL750L12QLP	OBSOLETE	TO-92	LP	3		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL750L12QP	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL751L05CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L05CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L05CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L05CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L05CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L05CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L05CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL751L05MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL751L05MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL751L05QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL751L05QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL751L05QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL751L10CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L10CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L10CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L10CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L10CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L10CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L10CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL751L10CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL751L10QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	

PACKAGE OPTION ADDENDUM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TL751L10QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL751L12CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L12CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L12CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L12CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L12CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L12CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL751L12CP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TL751L12MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL751L12MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL751L12QD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL751L12QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	
TL751L12QP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	

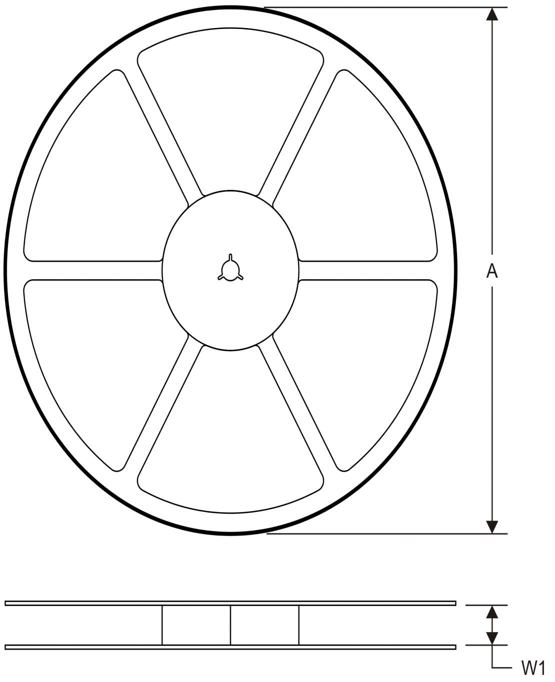
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

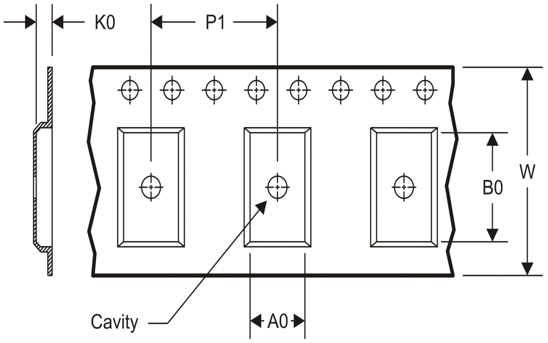
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



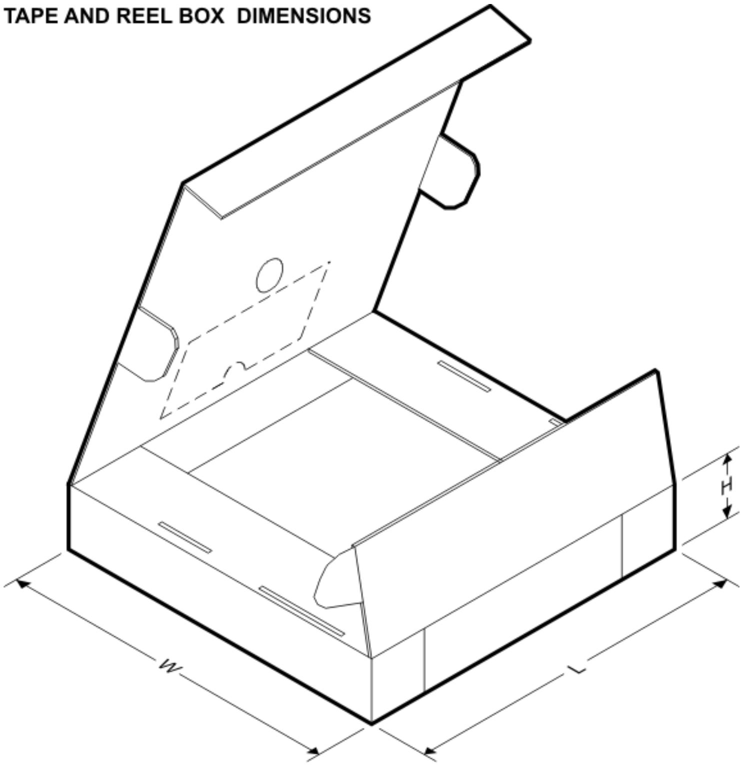
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L05CKTTR	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL750L05CKVURG3	PFM	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750L08CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L10CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL750L12CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L05CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L10CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL751L12CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

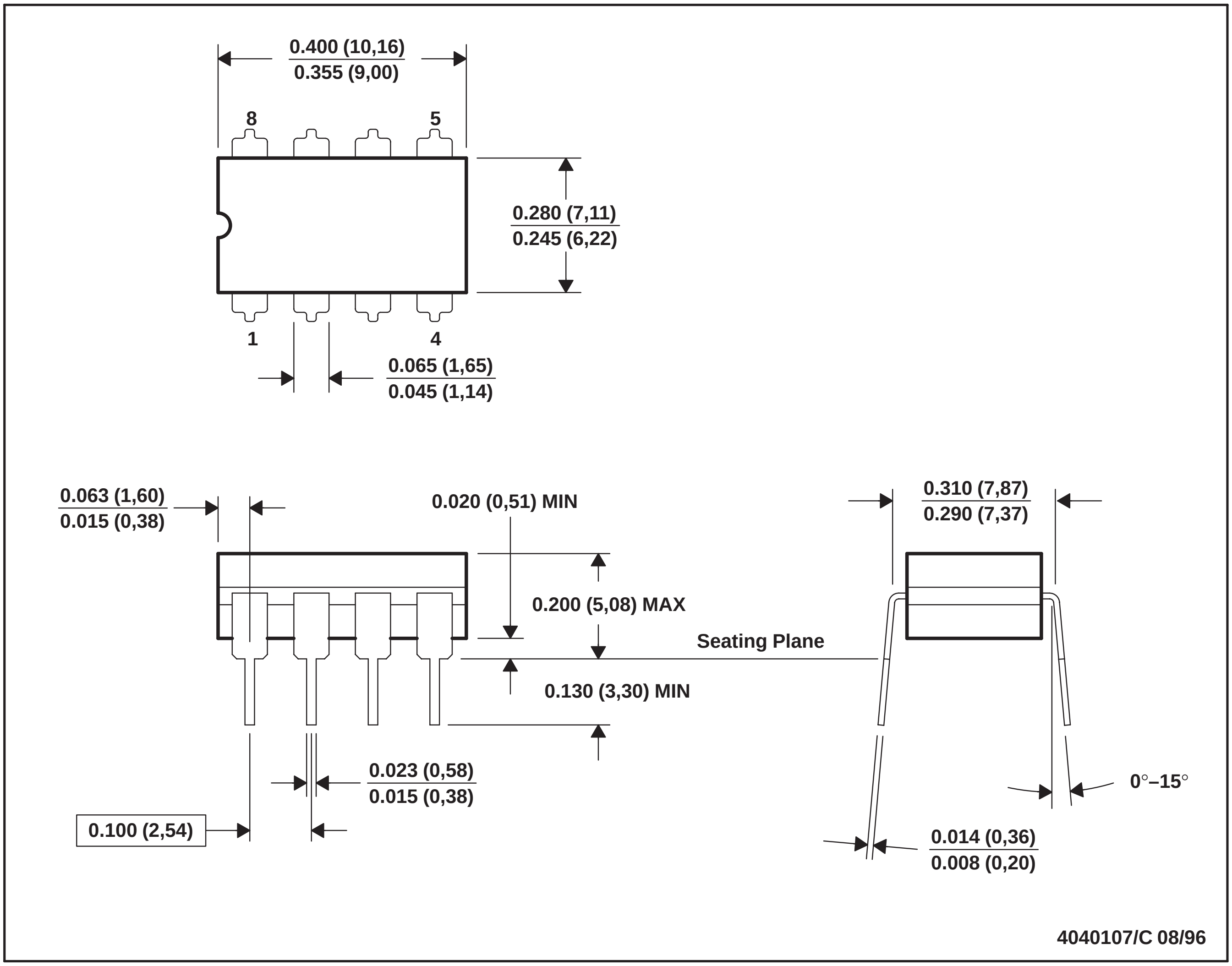
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L05CKTTR	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750L05CKVURG3	PFM	KVU	3	2500	340.0	340.0	38.0
TL750L08CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L10CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL750L12CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L05CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L10CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL751L12CDR	SOIC	D	8	2500	340.5	338.1	20.6

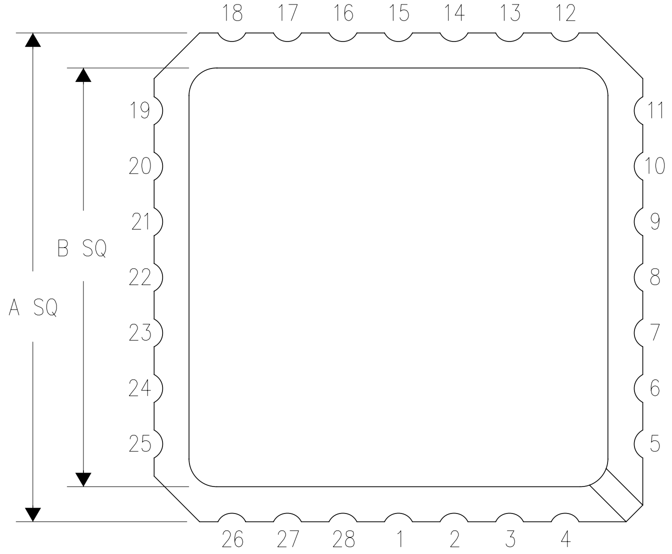
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



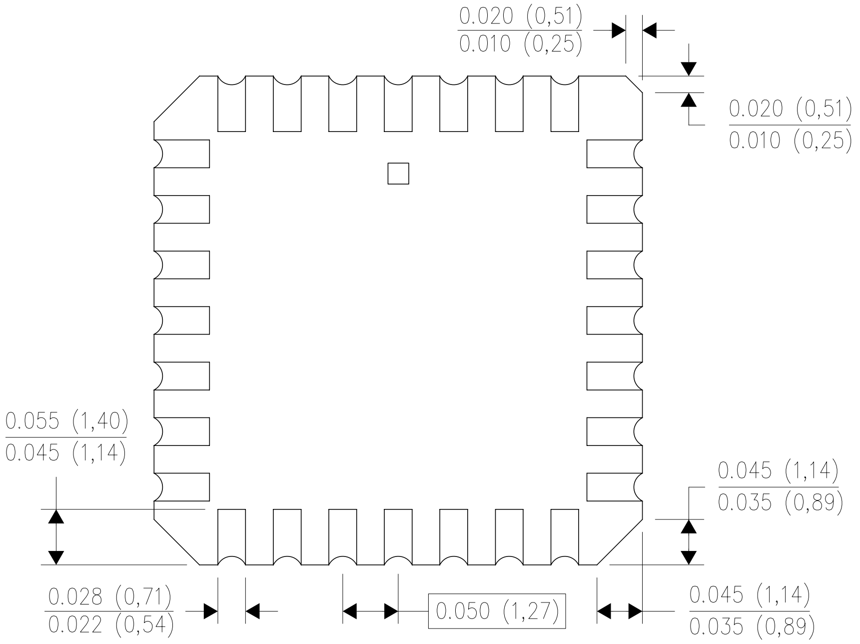
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

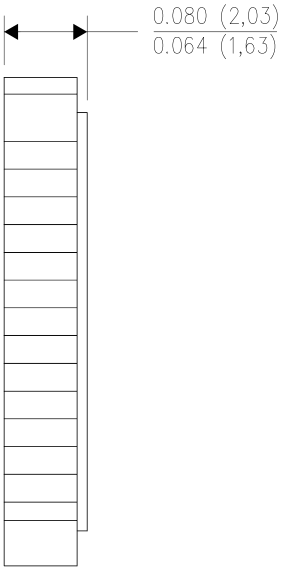
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

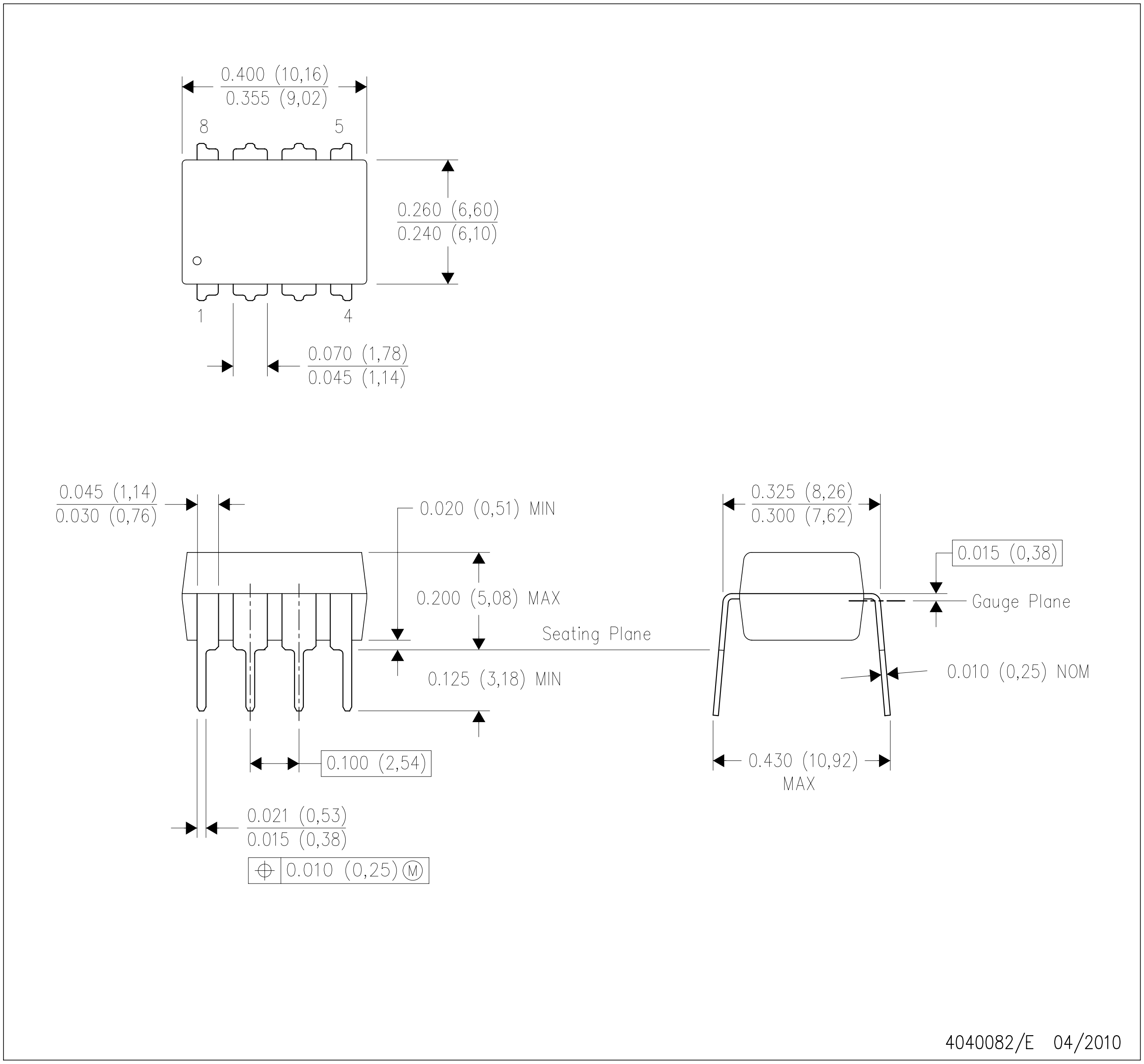




4040140/D 01/11

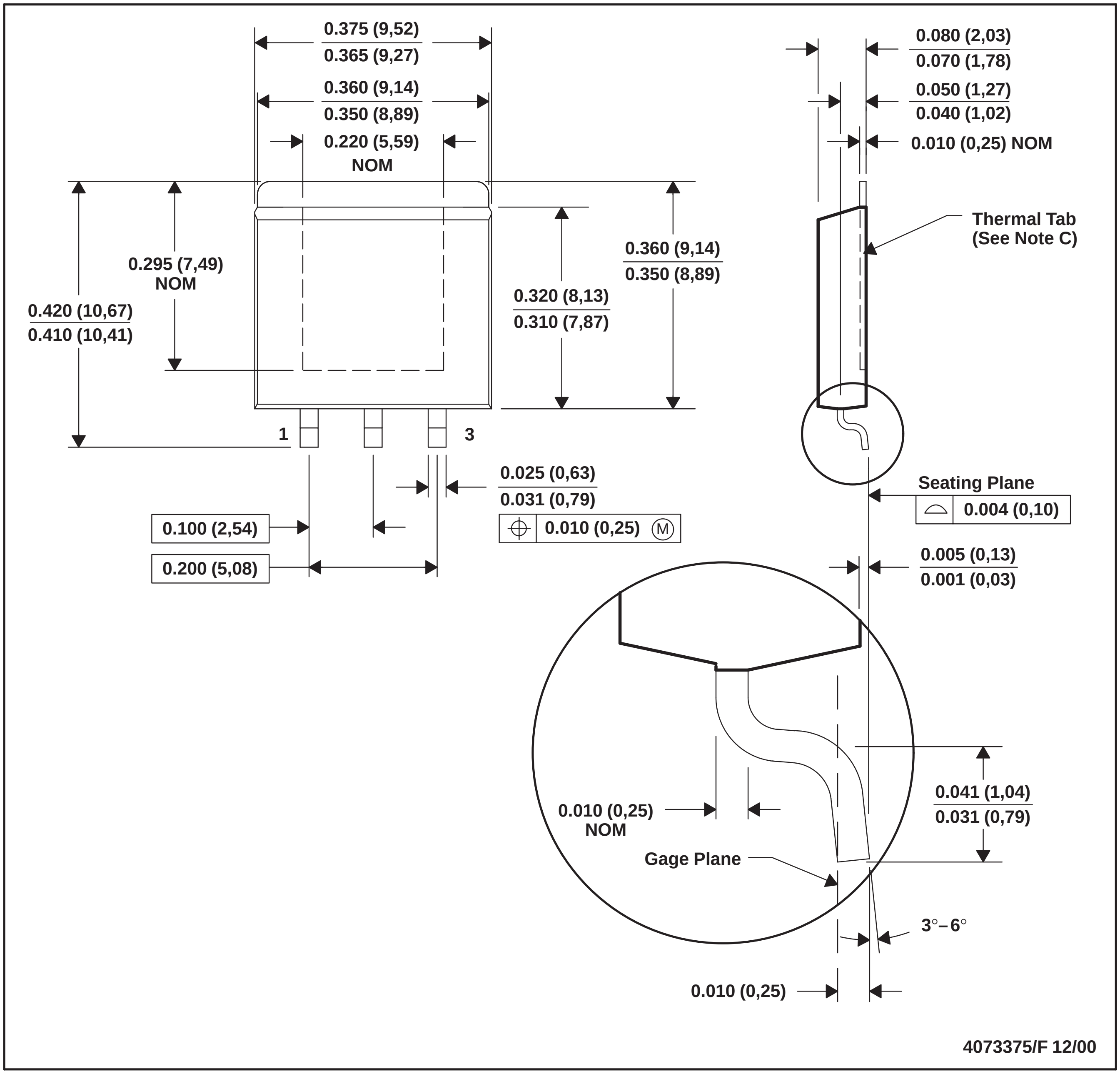
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

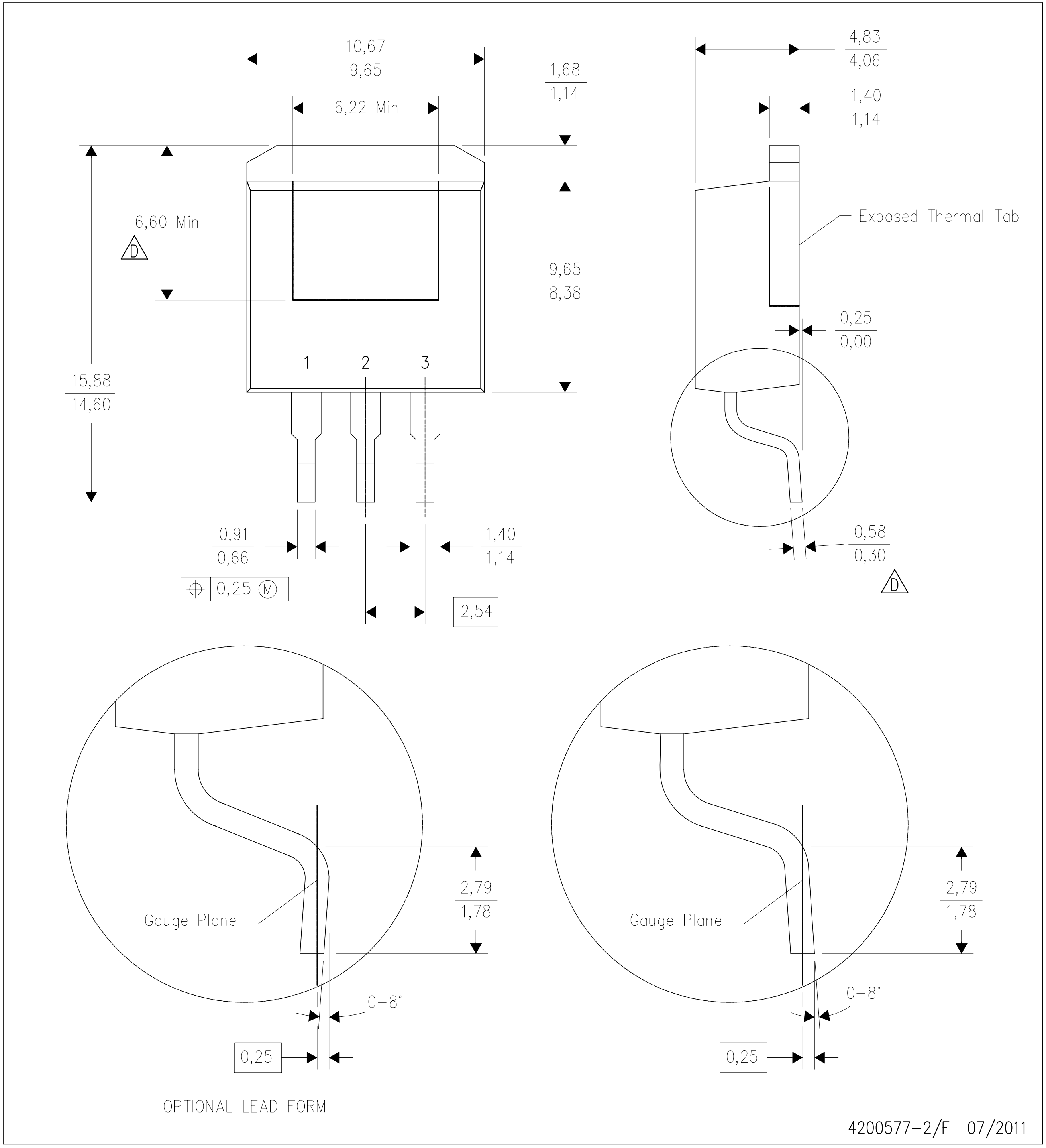
KTE (R-PSFM-G3) PowerFLEX™ PLASTIC FLANGE-MOUNT



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. The center lead is in electrical contact with the thermal tab.
- D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
- E. Falls within JEDEC MO-169

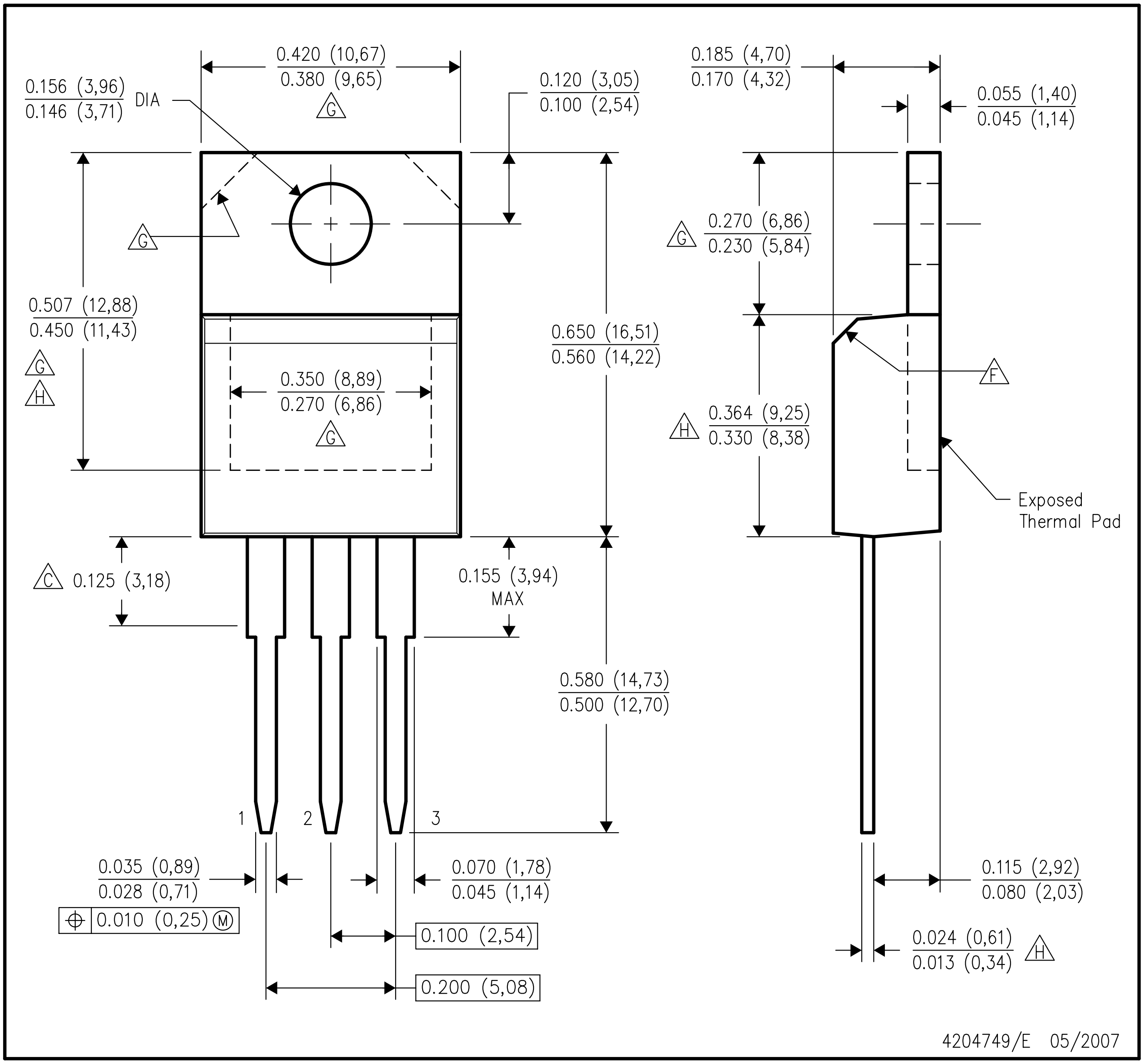
PowerFLEX is a trademark of Texas Instruments.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



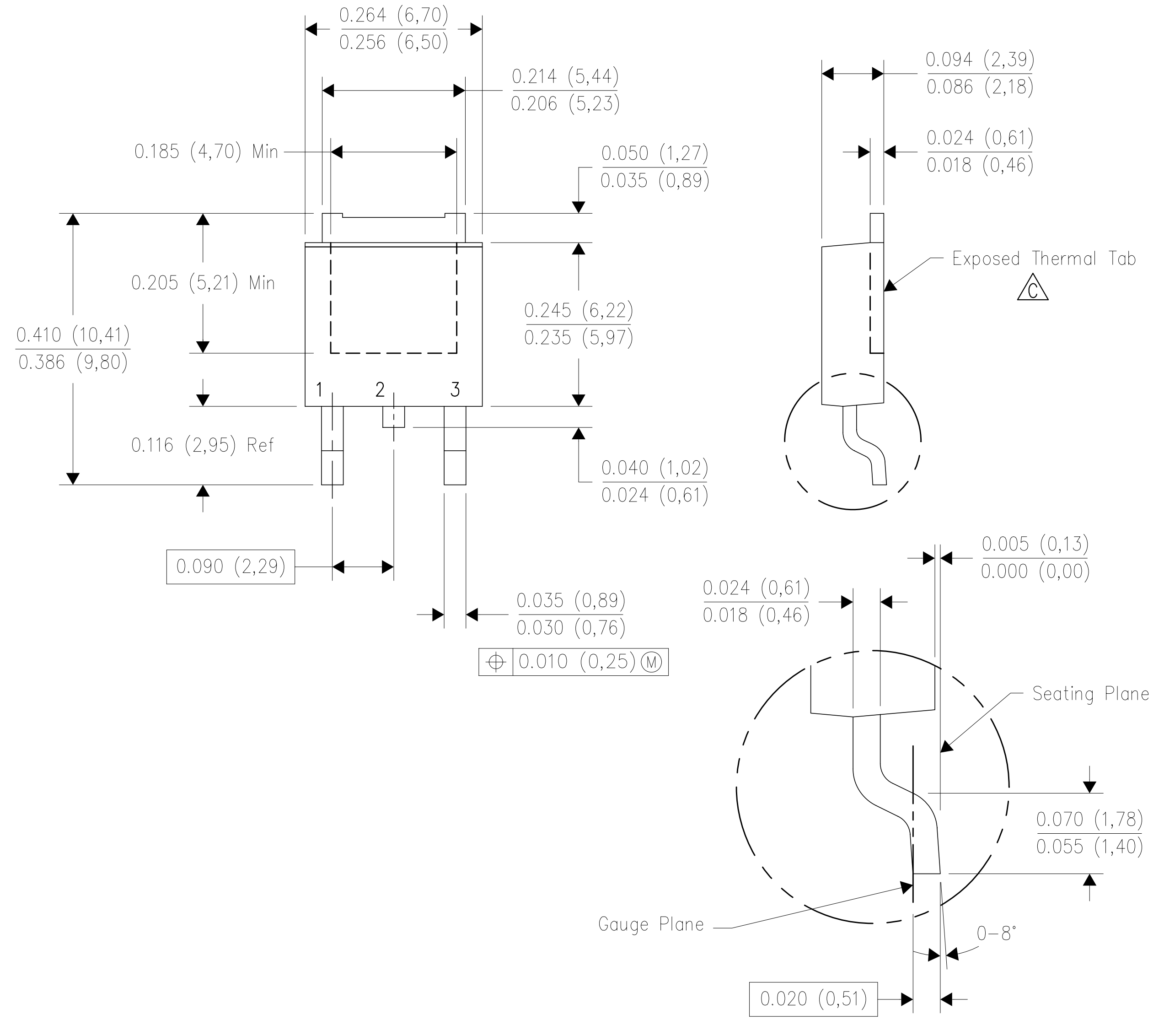
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

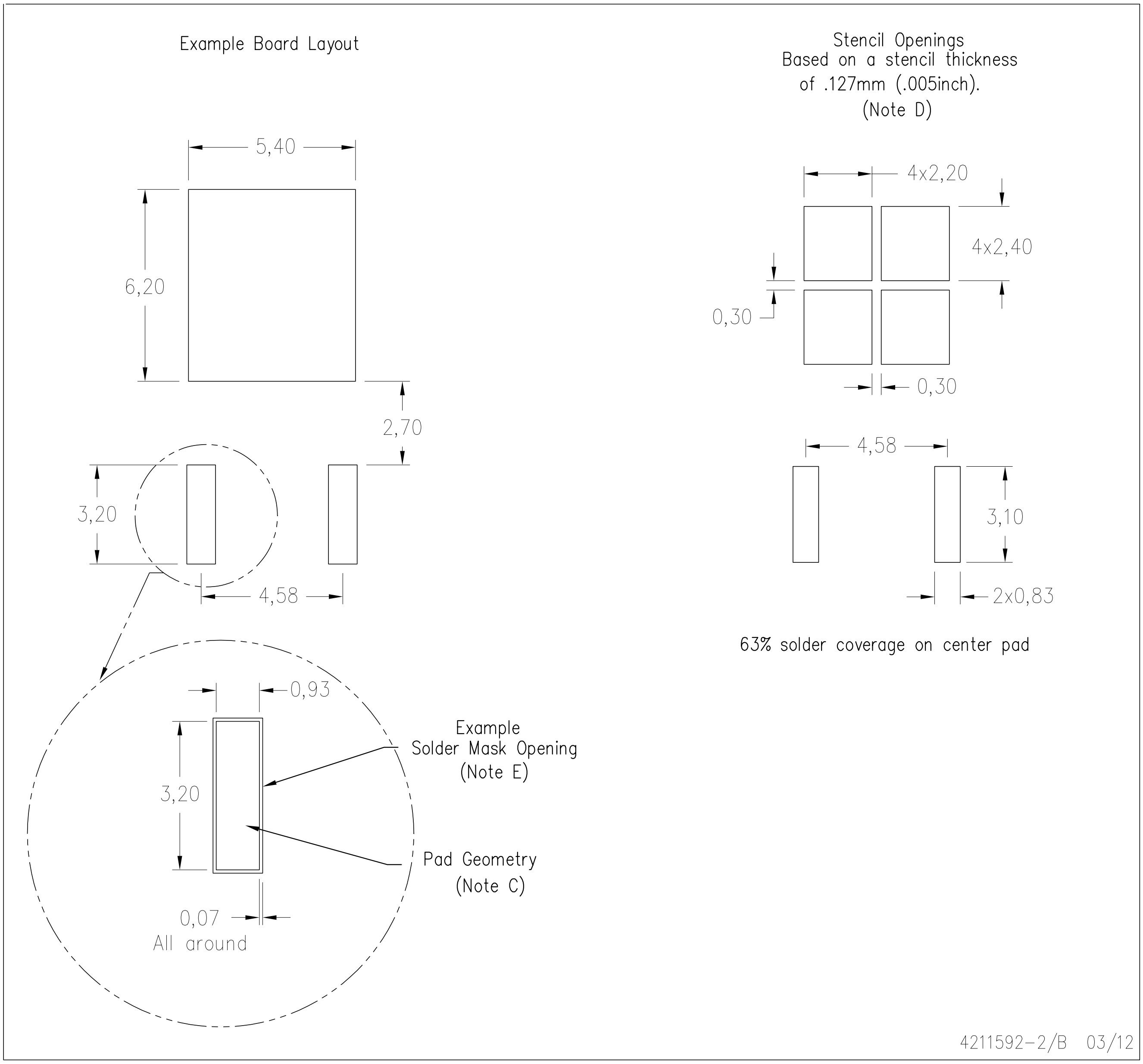
KVU (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



4205521–2/D 02/2009

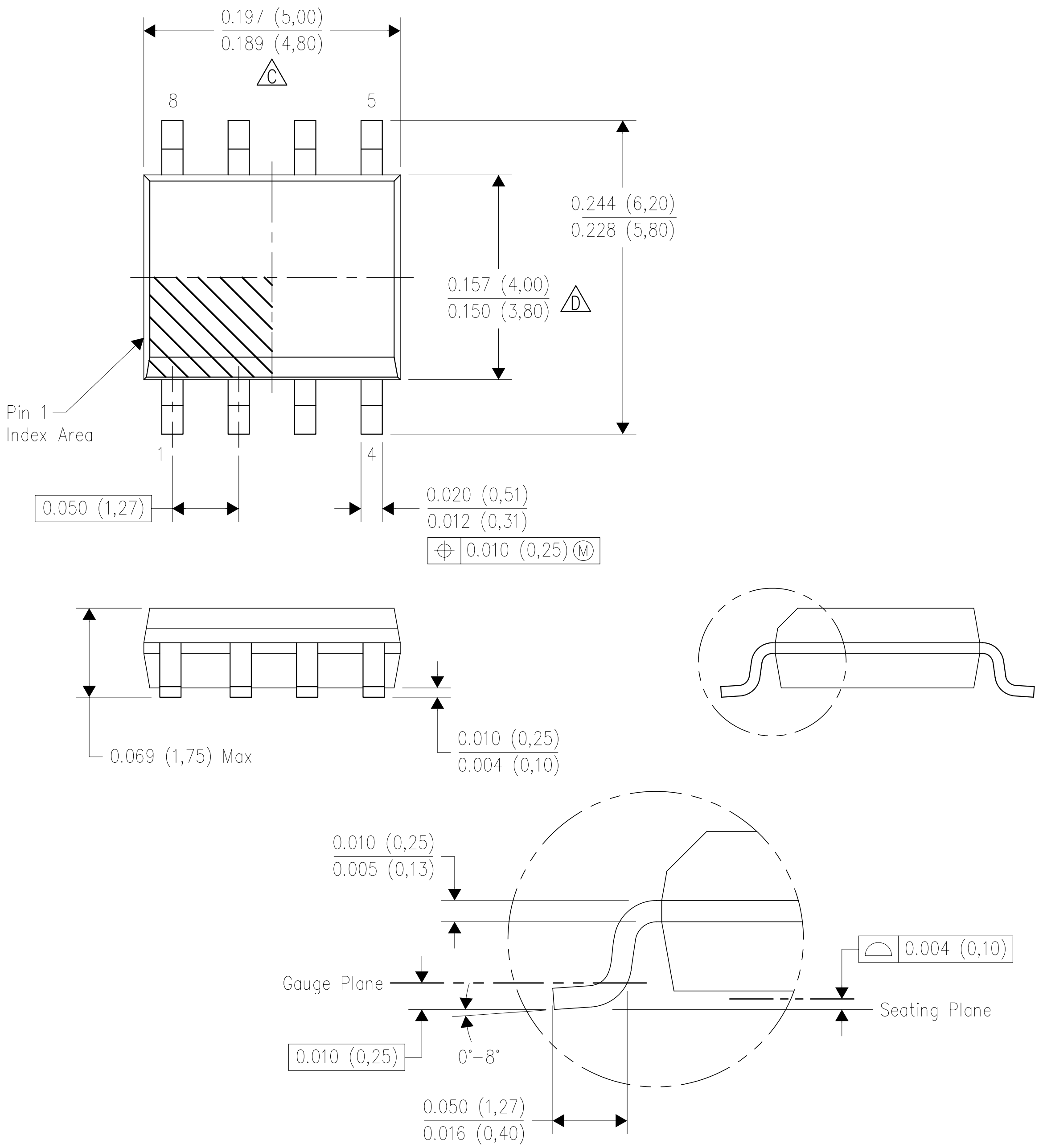
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C The center lead is in electrical contact with the exposed thermal tab.
D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
E. Falls within JEDEC TO–252 variation AA.

KVU (R-PSFM-G3) PLASTIC FLANGE MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

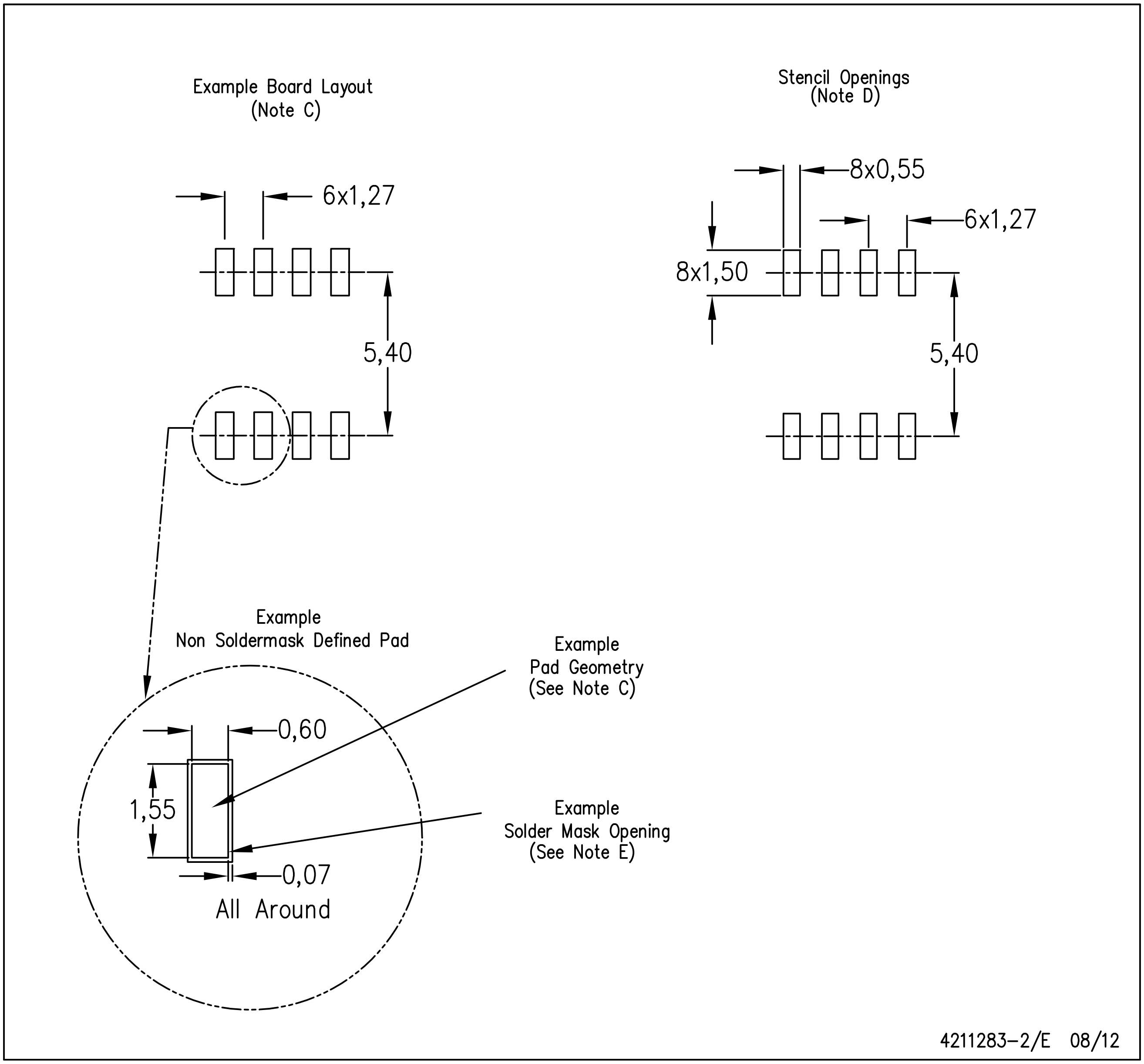
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

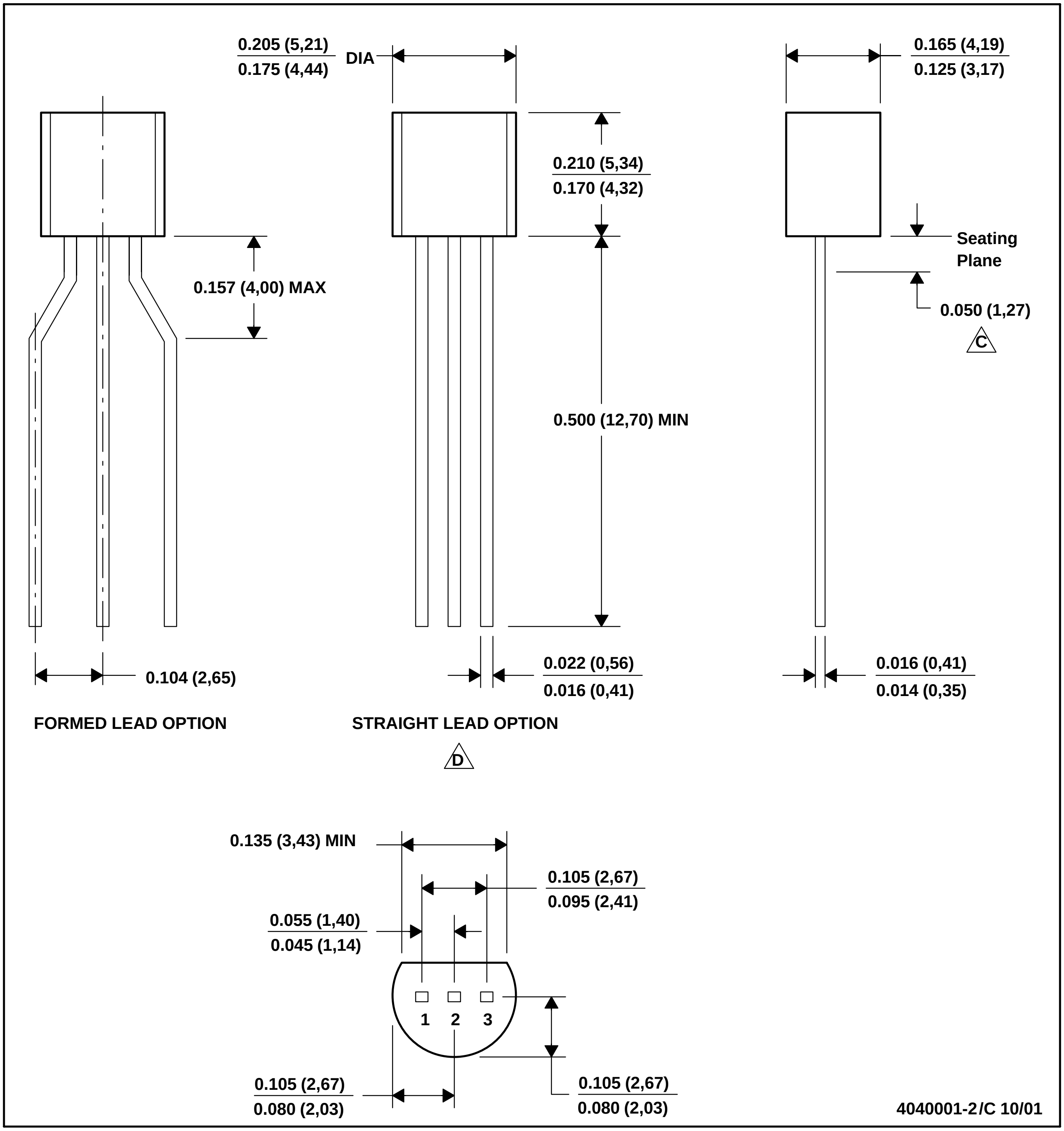
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



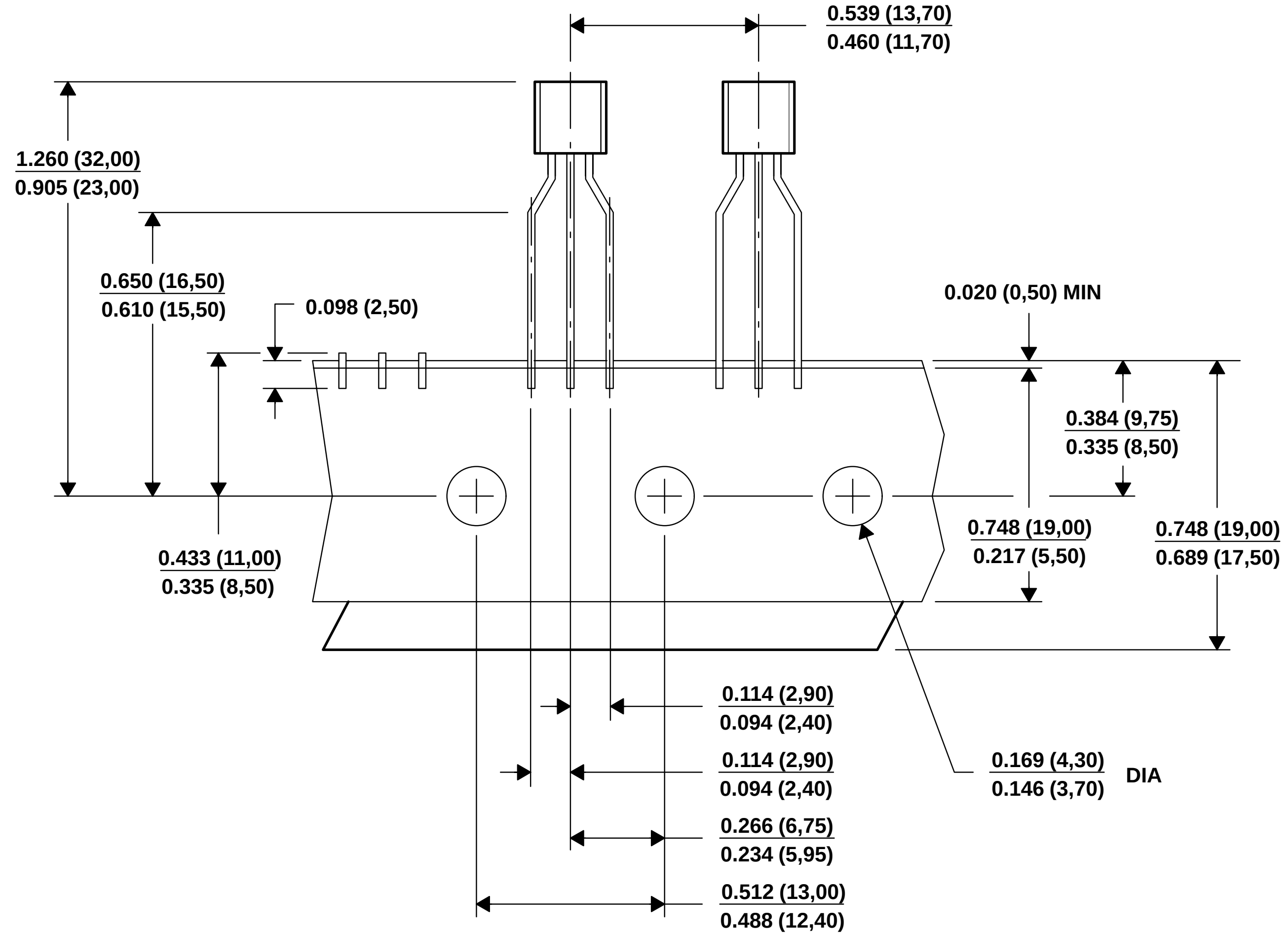
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LP (O-PBCY-W3) PLASTIC CYLINDRICAL PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area
- D. FAlls within JEDEC TO -226 Variation AA (TO-226 replaces TO-92)
- E. Shipping Method:
  - Straight lead option available in bulk pack only.
  - Formed lead option available in tape & reel or ammo pack.

LP (O-PBCY-W3) **PLASTIC CYLINDRICAL PACKAGE**

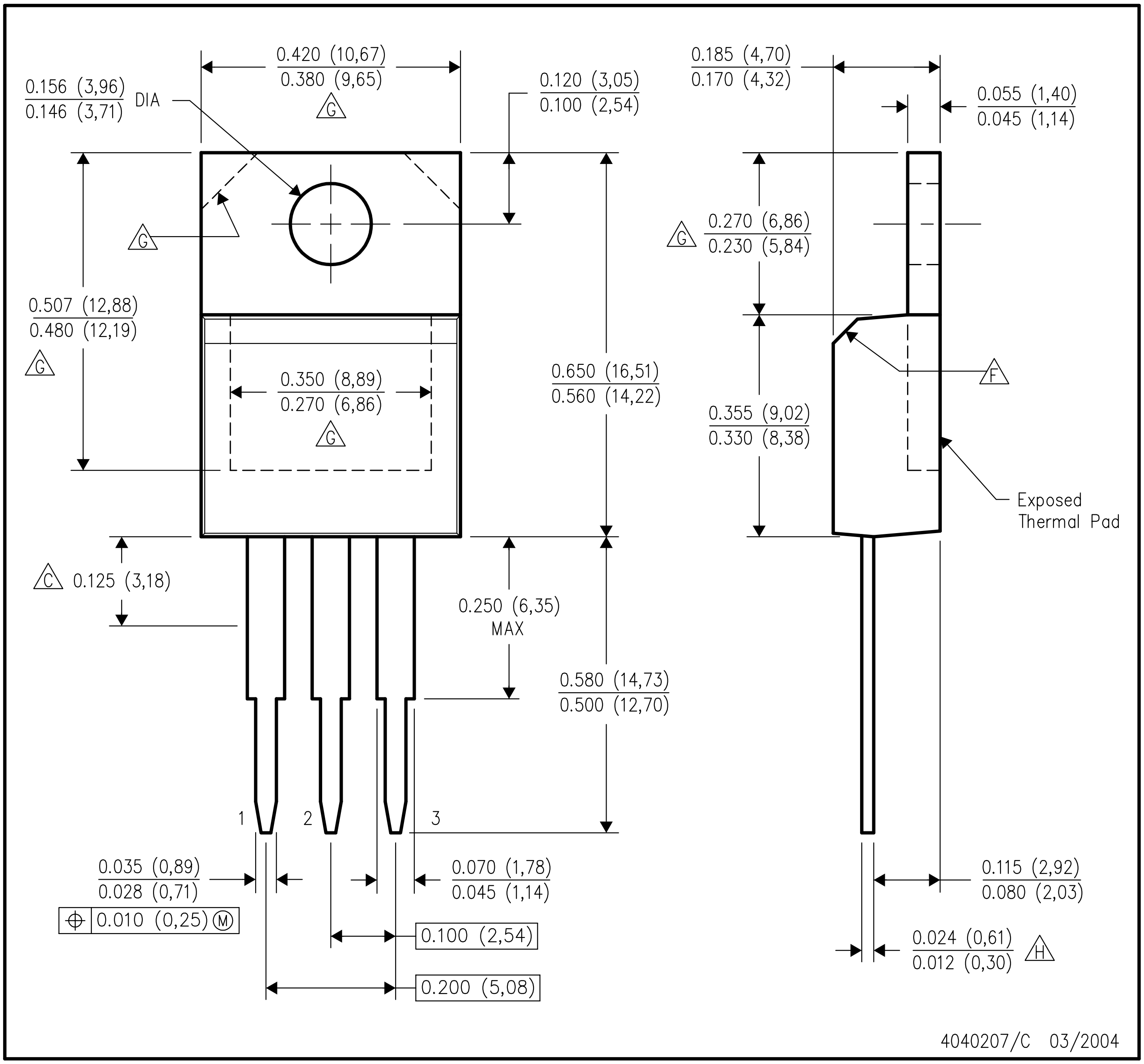


TAPE & REEL

4040001-3/C 10/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Tape and Reel information for the Format Lead Option package.

KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F The chamfer is optional.
- G Thermal pad contour optional within these dimensions.
- H Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated