Table 16. Data Conversion Time

NOMINAL DATA RATE (SPS)	EXACT DATA RATE (SPS)	FIRST DATA CONVERSION TIME AFTER FILTER RESET				SECOND AND SUBSEQUENT CONVERSION TIME AFTER FILTER RESET	
		SYNC COMMAND, MUX0 REGISTER WRITE		HARDWARE RESET, RESET COMMAND, START PIN HIGH, WAKEUP COMMAND, VBIAS, MUX1, or SYS0 REGISTER WRITE			
		(ms)(1)	NO. OF SYSTEM CLOCK CYCLES	(ms)(1)	NO. OF SYSTEM CLOCK CYCLES	(ms)	NO. OF SYSTEM CLOCK CYCLES
5	5.019	199.258	816160	200.26	820265	199.250	816128
10	10.038	99.633	408096	100.635	412201	99.625	408064
20	20.075	49.820	204064	50.822	208169	49.812	204032
40	40.151	24.92	102072	25.172	103106	24.906	102016
80	80.301	12.467	51064	12.719	52098	12.453	51008
160	160.602	6.240	25560	6.492	26594	6.226	25504
320	321.608	3.124	12796	3.25	13314	3.109	12736
640	643.216	1.569	6428	1.695	6946	1.554	6368
1000	1000	1.014	4156	1.141	4674	1	4096
2000	2000	0.514	2108	0.578	2370	0.5	2048

(1) For f_{OSC} = 4.096MHz.

Data Format

The ADS1246/7/8 output 24 bits of data in binary twos complement format. The least significant bit (LSB) has a weight of $(V_{REF}/PGA)/(2^{23} - 1)$. The positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 17 summarizes the ideal output codes for different input signals.

Table 17. Ideal Output Code vs Input Signal

INPUT SIGNAL, V_{IN} ($AIN_P - AIN_N$)	IDEAL OUTPUT CODE
≥ $+V_{REF}/PGA$	7FFFFFh
$(+V_{REF}/PGA)/(2^{23} - 1)$	000001h
0	000000h
$(-V_{REF}/PGA)/(2^{23} - 1)$	FFFFFFh
≤ $-(V_{REF}/PGA) \times (2^{23}/2^{23} - 1)$	800000h

1. Excludes effects of noise, linearity, offset, and gain errors.

Digital Interface

The ADS1246/7/8 provide a standard SPI serial communication interface plus a data ready signal ($\overline{DRDY}$). Communication is full-duplex with the exception of a few limitations in regards to the RREG command and the RDATA command. These limitations are explained in detail in the *SPI Commands* section of this data sheet. For the basic serial interface timing characteristics, see Figure 1 and Figure 2 of this datasheet.

$\overline{CS}$

The chip select pin (active low). The $\overline{CS}$ pin activates SPI communication. $\overline{CS}$ must be low before data transactions and must stay low for the entire SPI communication period. When $\overline{CS}$ is high, the DOUT/$\overline{DRDY}$ pin enters a high-impedance state. Therefore, reading and writing to the serial interface are ignored and the serial interface is reset. $\overline{DRDY}$ pin operation is independent of $\overline{CS}$.

Taking $\overline{CS}$ high deactivates only the SPI communication with the device. Data conversion continues and the $\overline{DRDY}$ signal can be monitored to check if a new conversion result is ready. A master device monitoring the $\overline{DRDY}$ signal can select the appropriate slave device by pulling the $\overline{CS}$ pin low.

The ADS1246/7/8 implement a timeout function for all listed commands in the event that data is corrupted and chip select is permanently tied low. However, it is important in systems where chip select is tied low permanently that register writes always be fully completed in 8 bit increments. The SCLK line should also be kept clean and situations should be avoided where noise on the SCLK line could cause the device to interpret the transient as a false SCLK. In systems where such events are likely to occur, it is recommended that chip select be used to frame communications to the device.

DATA FORMAT

The ADS1255/6 output 24 bits of data in Binary Two's Complement format. The LSB has a weight of $2V_{REF}/(PGA(2^{23} - 1))$. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 16 summarizes the ideal output codes for different input signals.

Table 16. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} ($AIN_P - AIN_N$)	IDEAL OUTPUT CODE(1)
$\geq \frac{+ 2V_{REF}}{PGA}$	7FFFFFh
$\frac{+ 2V_{REF}}{PGA(2^{23} - 1)}$	000001h
0	000000h
$\frac{- 2V_{REF}}{PGA(2^{23} - 1)}$	FFFFFFh
$\leq \frac{- 2V_{REF}}{PGA}\left(\frac{2^{23}}{2^{23} - 1}\right)$	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

GENERAL-PURPOSE DIGITAL I/O (D0-D3)

The ADS1256 has 4 pins dedicated for digital I/O and the ADS1255 has 2 digital I/O pins. All of the digital I/O pins are individually configurable as either inputs or outputs through the IO register. The DIR bits of the IO register define whether each pin is an input or output, and the DIO bits control the status of the pins. Reading back the DIO register shows the state of the digital I/O pins, whether they are configured as inputs or outputs by the DIR bits. When digital I/O pins are configured as inputs, the DIO register is used to read the state of these pins. When configured as outputs, DIO sets the output value. On the ADS1255, the digital I/O pins D2 and D3 do not exist and the settings of the IO register bits that control operation of D2 and D3 have no effect on that device.

During Standby and Power-Down modes, the GPIO remain active. If configured as outputs, they continue to drive the pins. If configured as inputs, they must be driven (not left floating) to prevent excess power dissipation.

The digital I/O pins are set as inputs after power-up or a reset, except for D0/CLKOUT, which is enabled as a clock output. If the digital I/O pins are not used, either leave them as inputs tied to ground or configure them as outputs. This prevents excess power dissipation.

CLOCK OUTPUT (D0/CLKOUT)

The clock output pin can be used to clock another device, such as a microcontroller. This clock can be configured to operate at frequencies of f_{CLKIN}, $f_{CLKIN}/2$, or $f_{CLKIN}/4$ using CLK1 and CLK0 in the ADCON register. Note that enabling the output clock and driving an external load will increase the digital power dissipation. Standby mode does not affect the clock output status. That is, if Standby is enabled, the clock output will continue to run during Standby mode. If the clock output function is not needed, it should be disabled by writing to the ADCON register after power-up or reset.

CLOCK GENERATION

The master clock source for the ADS1255/6 can be provided using an external crystal or clock generator. When the clock is generated using a crystal, external capacitors must be provided to ensure start-up and a stable clock frequency, as shown in Figure 22. Any crystal should work with the ADS1255/6. Table 17 lists two crystals that have been verified to work. Long leads should be minimized with the crystal placed close to the ADS1255/6 pins. For information on ceramic resonators, see application note SBAA104, *Using Ceramic Resonators with the ADS1255/6*, available for download at www.ti.com.

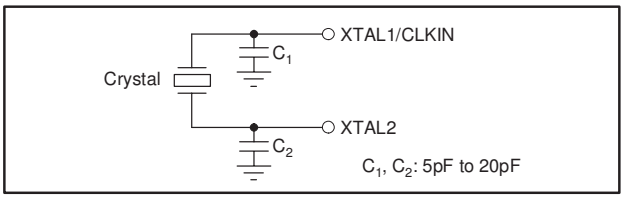

Figure 22. Crystal Connection

Table 17. Sample Crystals

MANUFACTURER	FREQUENCY	PART NUMBER
Citizen	7.68MHz	CIA/53383
ECS	8.0MHz	ECS-80-5-4

When using a crystal, neither the XTAL1/CLKIN nor XTAL2 pins can be used to drive any other logic. If other devices need a clock source, the D0/CLKOUT pin is available for this function. When using an external clock generator, supply the clock signal to XTAL1/CLKIN and