GLOBALLY MODULATED SELF-OSCILLATING AMPLIFIER WITH IMPROVED LINEARITY

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An exact oscillation criterion applicable to all binary self-oscillating structures and accounting for modulation index is derived. An exact expression for the averaged DC transfer from the comparator input to the output is derived, permitting precise prediction of the linearity of the modulation process. A 400W amplifier optimised according to these insights was built and results are presented.

INTRODUCTION

Self-oscillating amplifiers are commonly classified into two categories: hysteresis-controlled (HC) oscillation and phase-shift controlled (PSC) oscillation. Yet it has been amply shown that both categories are not fundamentally different [1]. They are only so classified based on the analytical method that works best to predict their behaviour. The classic 360º phase shift criterion used to determine the idle switching frequency of PSC amplifiers is known to be inexact and incapable of predicting the modulation dependent switching frequency. The piece-wise linear time-domain approach used to understand HC amplifiers (such as used, for example, in [2]) does predict the exact oscillation frequency in function of modulation index but becomes inexact as soon as the loop pole is not at DC or when loop order >1.

1 DEFINITIONS

F	Unless otherwise noted, switching frequency, either actual or prospective.
S	Laplacian operator; $2i\pi f$.
H	Duty cycle
$H(s)$	Complete loop function from comparator out to the comparator input, including delays.
V_{mod}	Instantaneous output voltage of the loop function
V_{DCIN}	Average DC component of voltage across comparator inputs.
V_0	Reference voltage on the inverting comparator input.
V_{SQ}	Square wave voltage. In the open loop model, an external source. In the closed loop model, the comparator output.
T	time
HC	Hysteresis controlled
PSC	Phase-shift controlled

2 SELF-OSCILLATION

A self-oscillating amplifier is essentially a square wave oscillator constructed as a comparator with a linear function wrapped around it.

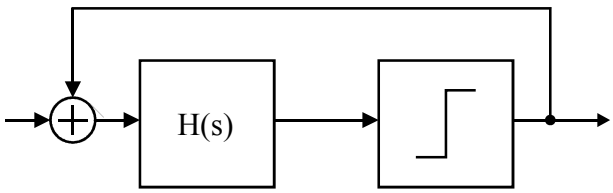

Figure 1: Generic self-oscillating circuit

H may or may not include the output filter. If the number of zeros (n_z) equals the number of poles (n_p) and at least one of those zeros is in the right half-plane the circuit is classified as hysteresis controlled. If n_p-$n_z \geq 2$ and all are in the left half-plane, the circuit is classified as phase-shift controlled. In accordance with this model whole classes of loop functions remain unexplored and unclassified. This already suggests that the division of self-oscillating circuits into HC and PSC is a false dichotomy and not fundamental at all. For the purpose of this analysis the location of the summing node is immaterial.

3 CLASSIC PHASE-SHIFT CRITERION

PSC amplifiers are usually said to oscillate at the frequency where the total loop phase is 360º.

$$\arg\left(H\left(2i\cdot\pi\cdot f\right)\right)=0 \qquad (1)$$

In spite of its ubiquity this analysis is fallacious. It is half of the Barkhausen criterion for sine wave oscillators. The other half states that the magnitude of loop gain be unity at the oscillation frequency. A class

D amplifier is a square wave oscillator and the gain of a binary quantizer is undefined.

Still, equation (1) predicts idle oscillation frequency within a few per cent when *H* has at least two poles more than it has zeros.

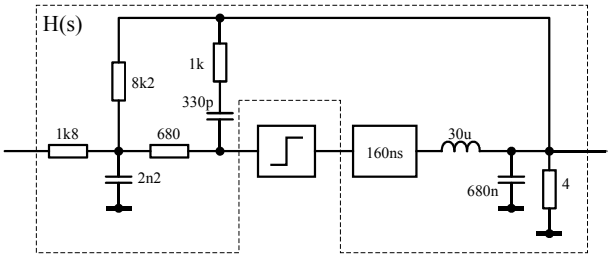

Figure 2: Example PSC circuit

Figure 2 shows a commonly used globally modulated self-oscillating circuit. *H(s)* includes propagation delay of the comparator and the power stage, the loaded output filter and the control network (input is terminated with a low impedance). According to the phase shift criterion this circuit should oscillate at 494 kHz.

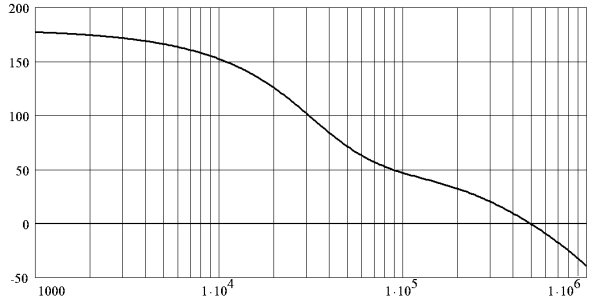

Figure 3: Phase plot of figure 2

As will be seen later the actual idle switching frequency turns out to be 466 kHz. At idle the discrepancy is mild but the phase criterion does not predict what happens to *f* when the amplifier is modulated.

The discrepancy does become extreme when the phase shift criterion is used to predict the oscillation frequency of a HC amplifier.

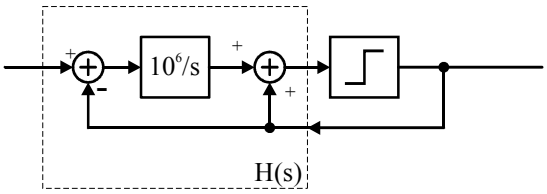

Figure 4: Example HC amplifier

The amplifier of Figure 4 has $H(s)=1-10^6/s$, and must clearly oscillate at 250 kHz. Yet, at that frequency, phase shift is 32.5º. In fact, there is no solution to the phase shift criterion:

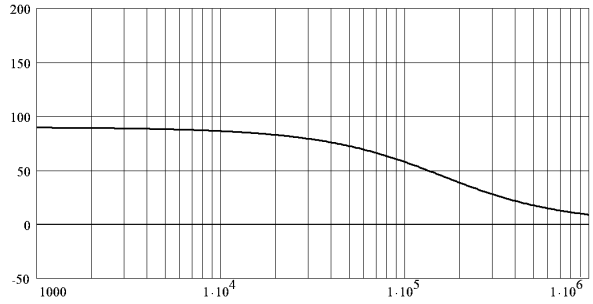

Figure 5: Phase plot of figure 4

Phase shift asymptotically approaches 0 but never quite gets there. The classical criterion would have this circuit oscillate at an infinitely high frequency.

4 EXACT OSCILLATION CRITERION

An exact oscillation criterion should presume a square wave output and account for the variation of the oscillation frequency as a function of duty cycle.

4.1 Open-loop model

In a self-oscillating amplifier, frequency *f* and duty cycle *h* are dependent. A given combination of duty cycle and frequency is an oscillation condition if there exists a voltage V_0 that, when compared against the output of the loop function driven by a square wave of said frequency and duty cycle, produces another identical square wave:

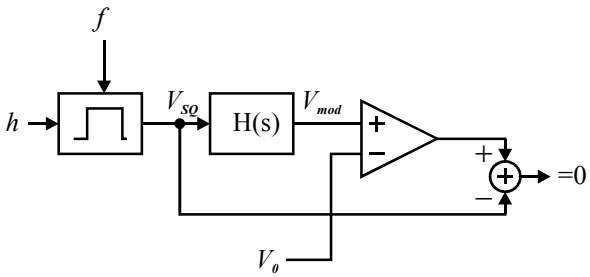

Figure 6: Conceptual open-loop oscillation condition test

According to this model, finding *f* for a given *h* would mean varying *f* and *h* until the output of the comparator matches that of the square wave source. Varying V_0 is an unnecessary complexity though. For one, V_0 is an artefact of the open loop model. In reality the loop simply settles on a given duty cycle in response to an input voltage applied somewhere in the loop, whereas here we are doing the reverse: setting the duty cycle and working out the operating condition to go with that. We may also say that the oscillation condition is met if the instantaneous value of V_{mod} at the rising edge is the same as the instantaneous value of V_{mod} at the falling edge. That voltage will be V_0.

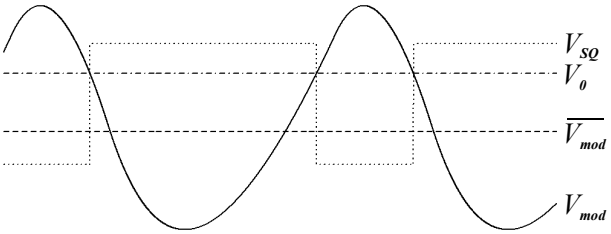

Figure 7: Signals of figure 6 with *H(s)* that of figure 2 with oscillation condition fulfilled (*h*=0.3).

4.2 Analysis

Determining whether the oscillation condition is met entails calculating the instantaneous value of V_{mod} at the rising and falling edges and subtracting them. A square wave of frequency *f* and duty cycle *h* can be written as:

$$V_{SQ}(t)=\mathrm{Re}\left(2\cdot h-1+\frac{4}{\pi}\cdot\sum_{n=0}^{\infty}\frac{1-e^{-2i\cdot\pi\cdot n\cdot h}}{2i\cdot n}\cdot e^{2i\cdot\pi\cdot f\cdot n\cdot t}\right) \quad (2)$$

The real part of this function is a square wave switching between -1 and 1 with the first rising edge at t=0 and the first falling edge at $t=h/f$. The input voltage of the comparator is obtained by multiplying each frequency term by the loop function at the same frequency:

$$V_{mod}(t) = \mathrm{Re}\left((2\cdot h-1)\cdot H(0)+\frac{4}{\pi}\cdot\sum_{n=0}^{\infty}\frac{1-e^{-2i\cdot\pi\cdot n\cdot h}}{2i\cdot n}\cdot H(2i\cdot\pi\cdot f\cdot n)\cdot e^{2i\cdot\pi\cdot f\cdot n\cdot t}\right) \quad (3)$$

The oscillation condition is fulfilled when:

$$V_{mod}(0)=V_{mod}\left(\frac{h}{f}\right) \quad (4)$$

i.e.

$$V_{mod}(0)-V_{mod}\left(\frac{h}{f}\right)=0 \quad (5)$$

Substituting (3) in (5), canceling DC terms and constant factors we get:

$$\mathrm{Re}\left(\sum_{n=1}^{\infty}\frac{\left(1-e^{-2i\cdot\pi\cdot n\cdot h}\right)\cdot\left(1-e^{2i\cdot\pi\cdot n\cdot h}\right)}{2i\cdot n}\cdot H(2i\cdot\pi\cdot f\cdot n)\right)=0 \quad (6)$$

Which, for practical reasons that will become clear later, we may want to rewrite as:

$$\arg\left(\sum_{n=1}^{\infty}\frac{\left(1-e^{-2i\cdot\pi\cdot n\cdot h}\right)\cdot\left(1-e^{2i\cdot\pi\cdot n\cdot h}\right)}{2\cdot n}\cdot H(2i\cdot\pi\cdot f\cdot n)\right)=0 \quad (7)$$

The criterion of (6) or (7) will correctly predict the switching frequency of any loop where H either has at least one more pole than it has zeros or has some delay in it. It will fail when *H* has no delay and when the number of zeros equals the number of poles as it tries to sample V_{mod} right in the middle of a discontinuity.
In order to respond to the output of *H* just before the edges of V_{SQ}, the following limit form may be used:

$$\arg\left(\lim_{t\to 0^-}\sum_{n=1}^{\infty}\frac{\left(1-e^{-2i\cdot\pi\cdot n\cdot h}\right)\cdot\left(1-e^{2i\cdot\pi\cdot n\cdot h}\right)}{2\cdot n}\cdot H(2i\cdot\pi\cdot f\cdot n)\cdot e^{i\cdot f\cdot t}\right)=0 \quad (8)$$

This is the exact oscillation criterion for self-oscillating class D amplifiers. Regrettably, like the classical criterion, this equation can only be solved numerically.

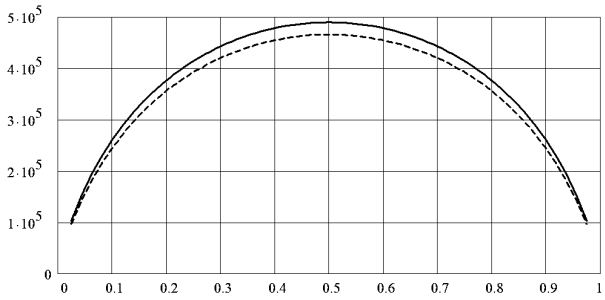

Figure 8: Switching frequency of figure 2 as a function of duty cycle with 4Ω (dashed) and 3Ω (solid) load.

4.3 Relationship with the classical criterion

Substituting *h*=0.5 (idle) in (8) and truncating the summation after the first term reduces the exact criterion to the classical criterion. The exact criterion may be said to be a version of the classical criterion with all harmonics added in.

4.4 Exact criterion as loop phase

Considering that, it may be instructive to plot the criterion in the same way that a phase plot is made.
The "square wave phase plot" of the circuit of Figure 2 is this:

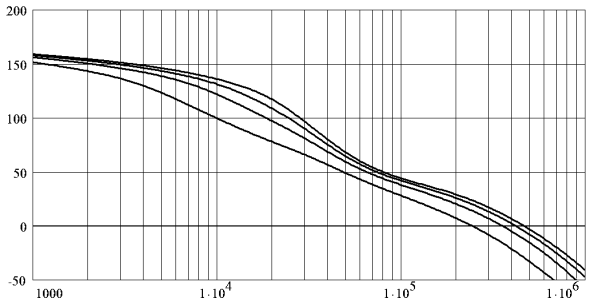

Figure 9: Phase plot of figure 2 according to the exact criterion for *h*=0.5, 0.3, 0.2 and 0.1

The idle switching frequency is now correctly predicted as 466 kHz, and so are the switching frequencies for other duty cycles.

Likewise, correct operating conditions are obtained for the hysteresis controlled circuit:

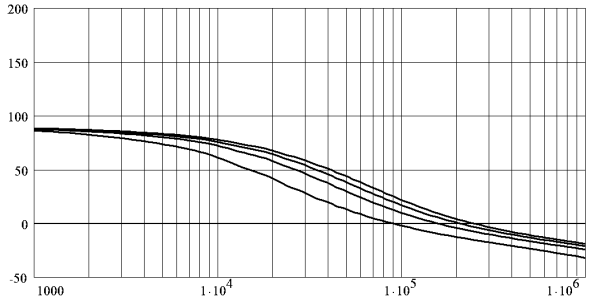

Figure 10: Phase plot of figure 4 according to the exact criterion for h=0.5, 0.3, 0.2 and 0.1

The idle plot neatly crosses zero at 250 kHz, corresponding to the exact switching frequency also found by time domain analysis.

5 DC TRANSFER ANALYSIS

Having obtained a means for characterizing the relationship between duty cycle and oscillation frequency, we can proceed to compute the small signal gain of the comparator.

5.1 DC modulator input voltage

Referring back to Figure 7 one notes that there is an offset between V_0 and $\overline{V_{mod}}$. This offset is the effective DC input to the modulator.

$$V_{DCIN} = V_0 - V_{mod} \tag{9}$$

From (3):

$$\overline{V_{mod}} = (2 \cdot h - 1) \cdot H(0) \tag{10}$$

V_0 is the modulator input at the switching instant, e.g. t=0.

$$V_0 = V_{mod}(0) \tag{11}$$

From (3), (9) and (11):

$$V_{DCIN} = \mathrm{Re}\left(\frac{4}{\pi} \cdot \sum_{n=0}^{\infty} \frac{e^{-2i \cdot \pi \cdot n \cdot h} - 1}{2i \cdot n} \cdot H(2i \cdot \pi \cdot f \cdot n) \right) \tag{12}$$

Together with equation (8), (12) gives us all we need to compute the DC transfer from modulator output (duty cycle) to input. Doing this for the circuit of Figure 2 at two different loads illustrates the load-dependent linearity of self-oscillating circuits with partial or full post-filter feedback.

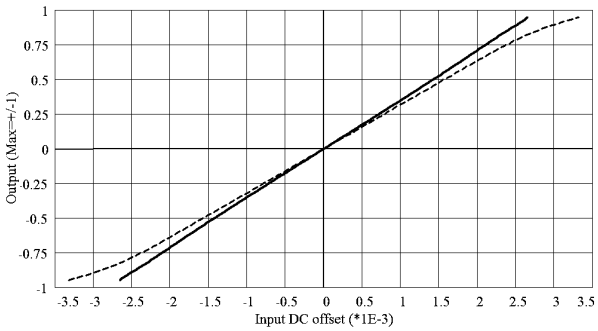

Figure 11: DC transfer of the circuit of figure 2 with 4Ω (dashed) and 3Ω (solid) load.

5.2 Modulator Gain

The derivative of the DC transfer curve is the DC gain of the modulator.

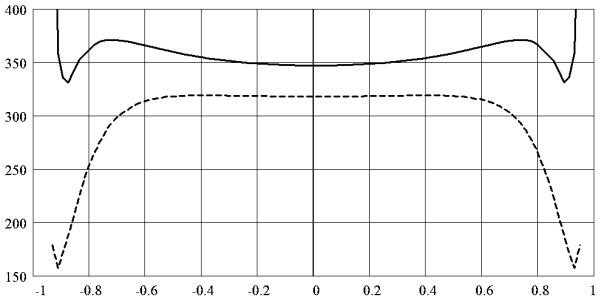

Figure 12: Small-signal gain of figure 2 as a function of output with 4Ω (dashed) and 3Ω (solid) load.

5.3 Loop gain

Loop gain becomes *H(s)* multiplied by the modulator gain found above. The slope-based estimate used in previous research [3] is fallacious because it presumes that the residual is an independent carrier. In reality the residual changes in response to the modulation itself. Actual loop gain of a typical PSC circuit turns out to be about 2dB higher than the slope based estimate.

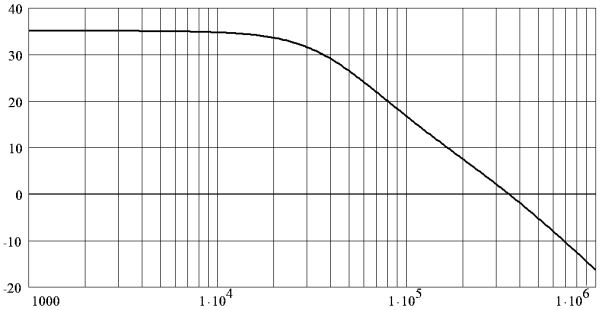

Figure 13: Loop gain of the circuit of figure 2.

Note that although this plot is quite correct at low frequencies, aliasing of the loop function is, for the time

being, ignored, and subject to further analysis. See [5] for an analysis of the case h=0.5.

6 EXPERIMENTS

The foregoing analysis showed that modulator linearity is fully predictable on the basis of the loop transfer function alone. A first prototype amplifier was constructed with no particular attention paid to modulator linearity. Later, a second prototype was built according to the insights of this study.

6.1 Design Requirements

The main requirement was a small signal bandwidth > 100 kHz and low distortion in the audio range. To prevent slew limiting, power bandwidth was set to around 70 kHz and idle switching frequency to 650 kHz.

6.2 First prototype

The loop function consists of the propagation delay, the output filter, an active complex pole pair, one passive real pole, a complex pair of zeros and one real zero.

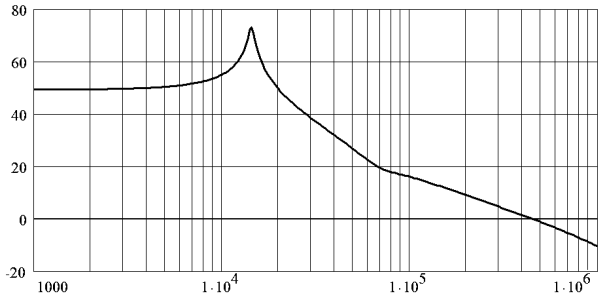

Figure 14: Loop gain of first prototype amp.

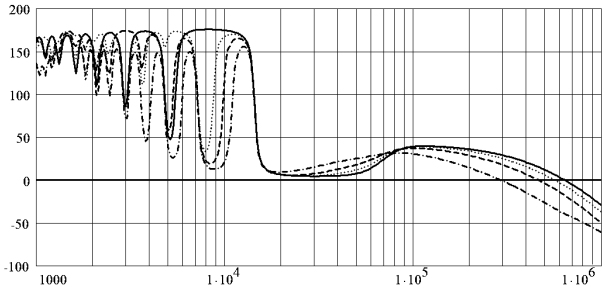

Figure 15: Square wave phase plot corresponding to figure 14 for h=0.5, 0.3, 0.2 and 0.1

Since the oscillation criterium includes harmonics of the switching frequency, we find the sharp phase step at the active pole echoed at sub-harmonic frequencies. Some systems might actually have solutions at sub-harmonics of high-Q poles. In practice this does not mean that the system can oscillate stably at such frequencies. The same high Q pole would resonate and force extra transitions, a possibility ignored by formula (4). The system would settle at the solution corresponding to the pole itself.

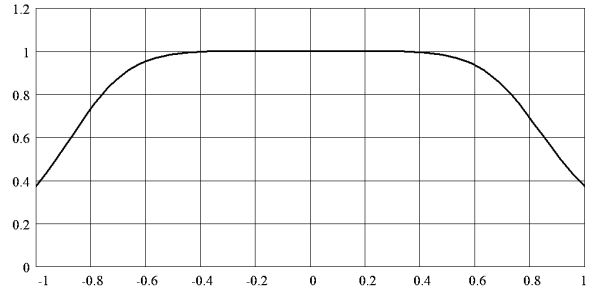

Figure 16: Plot of gain vs. V_{DCIN} (both normalized) of first amplifier prototype

As the loop gain predicts, distortion at low power levels is quite good. As the gain plot predicts, modulator distortion becomes significant starting from about a quarter of maximum power.

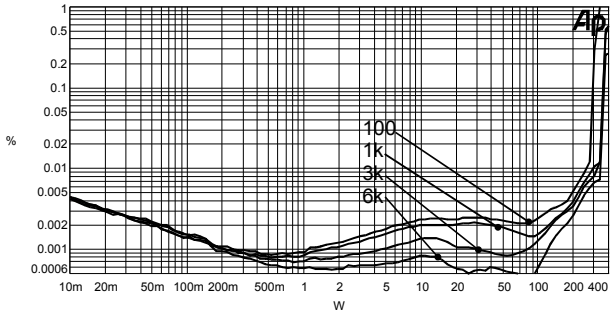

Figure 17: THD+N of first amplifier prototype.

Note that the plots are not mislabelled. The distortion at higher frequencies is indeed lower than at low frequencies owing to the spike in loop gain around 15 kHz.

6.3 Second prototype

Compared to the first prototype another real pole has been added and the propagation delay reduced to compensate.

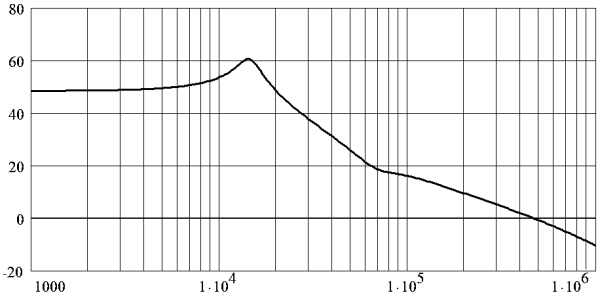

Figure 18: Loop gain of second prototype amp

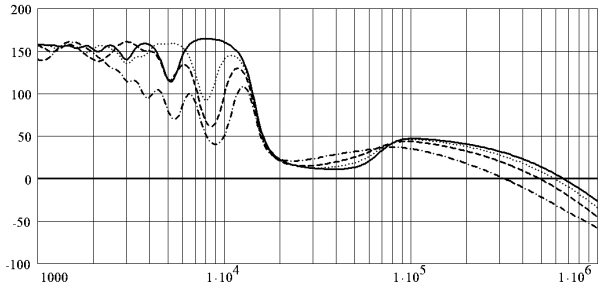

Figure 19: Loop phase of second prototype amp

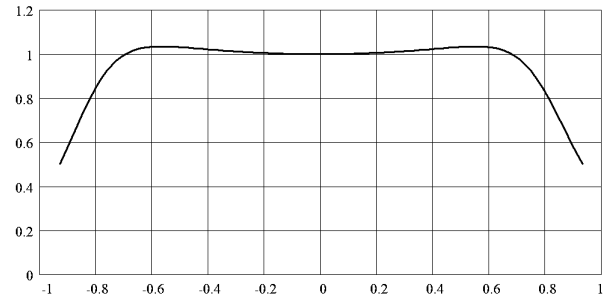

Figure 20: Gain vs. input of second amplifier prototype

This circuit should make it well past half power before distortion increases appreciably, as attested in the THD plot. All THD plots are measured with a 20kHz measurement band-width.

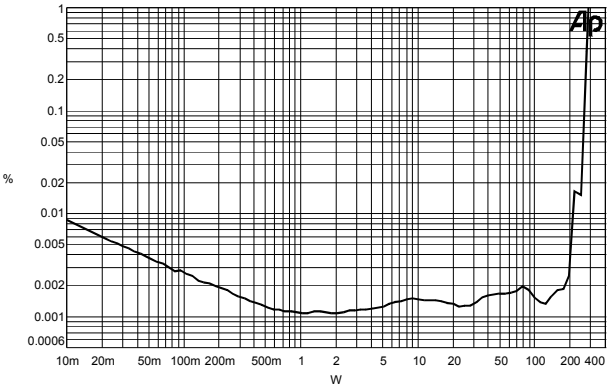

Figure 21: THD plot of second prototype (1 kHz)

The THD versus frequency plot of this amplifier is quite instructive. Although it was not the objective of this study, this measurement indicates that DC nonlinearity of the modulator is the only significant contributor to distortion. The distortion profile mirrors loop gain. There is no apparent rise in distortion as frequency goes up.

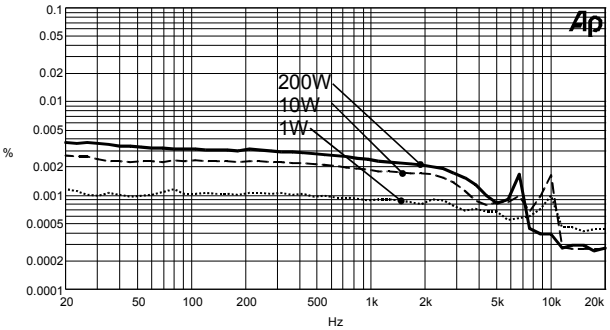

Figure 22: THD vs. frequency

The same observation is borne out by the HF IMD measurement.

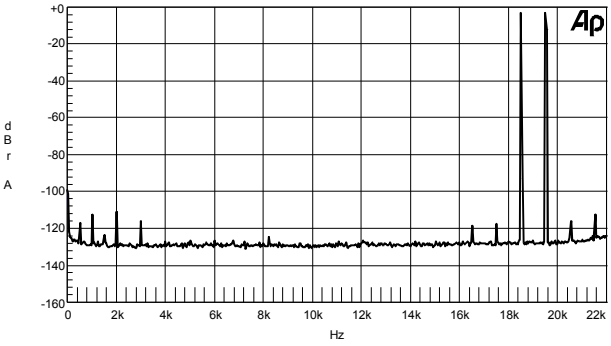

Figure 23: HF IMD test at 50W/4ohm

For the sake of completeness, a frequency response and output impedance graph are included below.

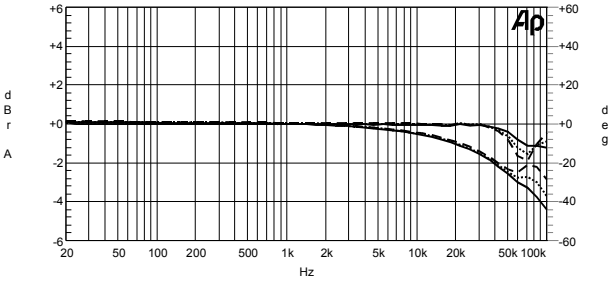

Figure 24: Frequency and phase response into 4Ω, 8Ω and open circuit

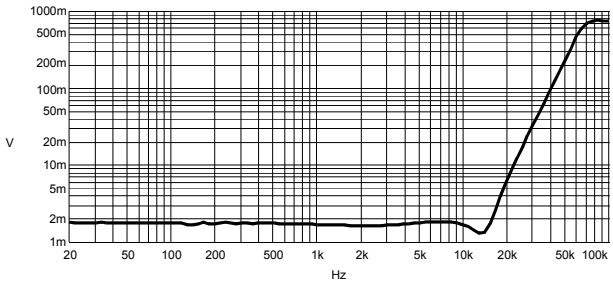

Figure 25: Output impedance

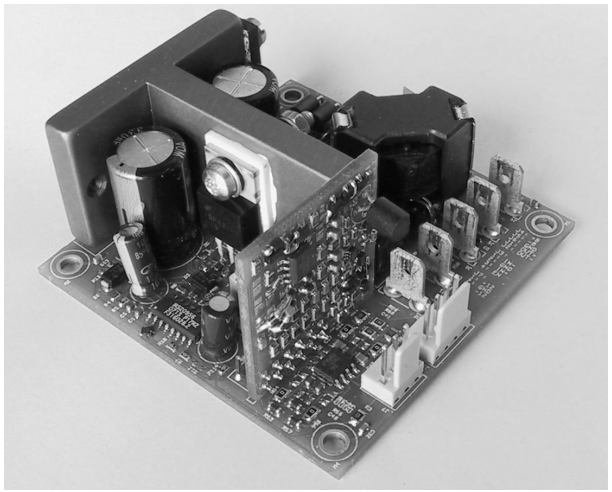

Figure 26: First prototype

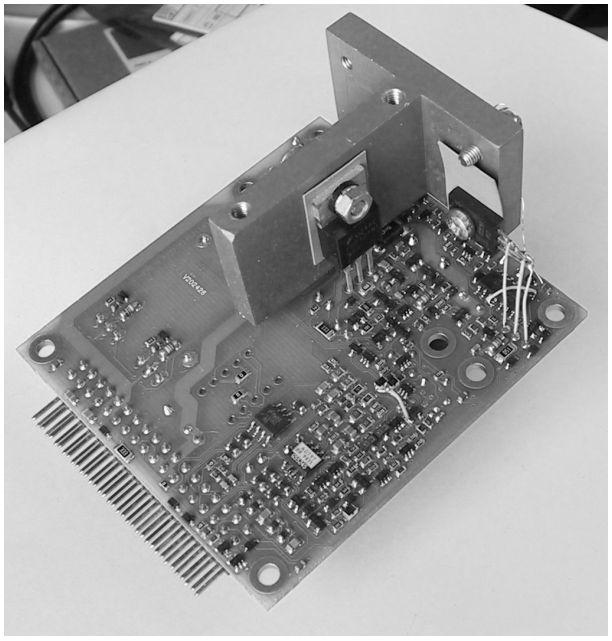

Figure 27: Second prototype

7 DIRECTIONS FOR FUTURE WORK

The practical results, especially at higher input frequencies, would suggest that modulation distortion mechanisms other than the static non-linear voltage transfer of the PWM process do not contribute significantly, in apparent contrast with fixed-frequency modulation [4]. Further work is needed to understand under what conditions this is true. Also, as said earlier, the current work still represents loop gain as *H(s)* multiplied by modulator gain. This cannot be accurate: the modulation process is a sampling process which affects the effective loop function. This too needs to be better characterised for self-oscillating loops and other instances of doubly sampled PWM. For h=0.5 this has already been elaborated elsewhere [5].

8 CONCLUSIONS

An efficient, universally applicable mathematical method was developed for predicting the steady-state operating conditions of a self-oscillating class D amplifier. From a practical perspective this fills most of the gap between simple linearised models and actual hardware performance.

9 IP NOTICE

The prototypes made for this study include design features that were not discussed further for reasons of IP protection. These are the techniques used to reduce load sensitivity, to control overload recovery and to restrict operation to a single wanted solution of the oscillation criterium.

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