FA5332P(M)

Bipolar IC
For Power Factor Correction

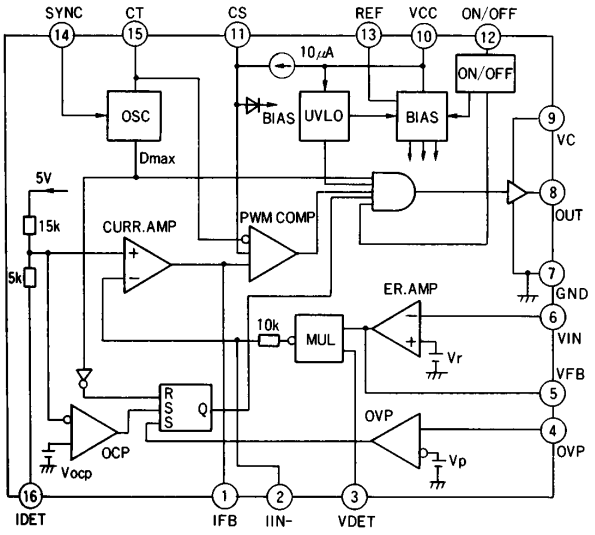
■ Description

FA5332P(M) is a control IC for a power factor correction system. This IC uses the average current control system to ensure stable operation. With this system, a power factor of 99% or better can be achieved.

■ Features

- Drive circuit for connecting a power MOS-FET(Io=±1.5A)
- Pulse-by-pulse overcurrent and overvoltage limiting function
- Output ON/OFF control function by external signals
- External synchronizing signal terminal for synchronous operation with other circuits
- Undervoltage malfunction prevention function
- Low standby current (90μA typical) for simple start-up circuit
- 16-pin package (DIP/SOP)
- ±2% accuracy reference voltage for setting DC output and overvoltage protection
- Good regulation of PFC output voltage from no-load to full-load

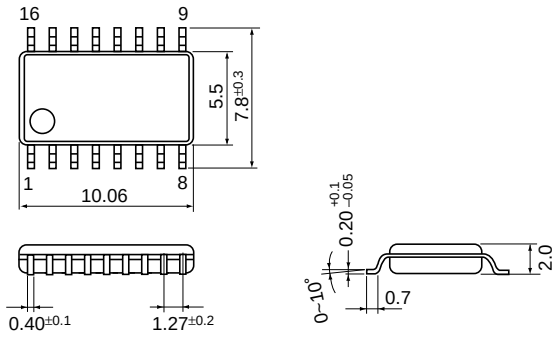
■ Block diagram



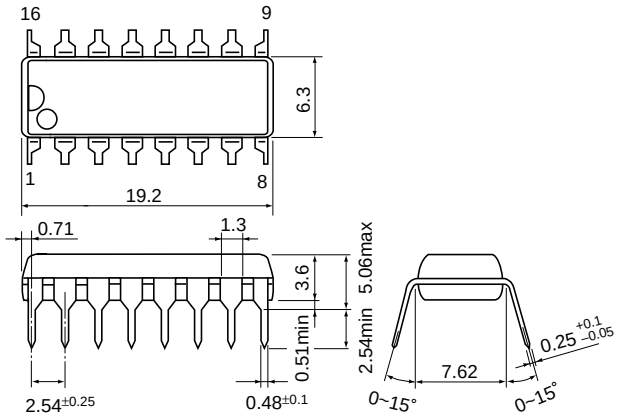
Pin No.	Pin symbol	Description
1	IFB	Current error amplifier output
2	IIN–	Inverting input to current error amplifier
3	VDET	Multiplier input
4	OVP	Overvoltage protection input
5	VFB	Voltage error amplifier output
6	VIN–	Inverting input to voltage error amplifier
7	GND	Ground
8	OUT	Output
9	VC	Power supply to output circuit
10	VCC	Power supply
11	CS	Soft-start
12	ON/OFF	Output ON/OFF control input
13	REF	Reference voltage
14	SYNC	Oscillator synchronization input
15	CT	Oscillator timing capacitor and resistor
16	IDET	Non-inverting input to current error amplifier

■ Dimensions, mm

● SOP-16



● DIP-16



■ Absolute maximum ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}, V_C	30	V
Output current	I_O	±1.5	A
Input voltage	V_{SYNC}, $V_{ON/OFF}$, V_{VIN-} V_{VDET}, V_{OVP}	–0.3 to +5.3	V
	V_{IDET}	–10.0 to +5.3	V
Total power dissipation (Ta=25°C)	P_d	850 (DIP-16) *1	mW
		650 (SOP-16) *2	
Operating temperature	Topr	–30 to +85	°C
Storage temperature	Tstg	–40 to +150	°C

Notes:
*1 Derating factor Ta > 25°C: 6.8mW/°C (on PC board)
*2 Derating factor Ta > 25°C: 5.2mW/°C (on PC board)

■ Recommended operating conditions

Item	Symbol	Min.	Max.	Unit
Supply voltage	V_{CC}, V_C	10	28	V
IDET terminal input voltage	V_{IDET}	–1.0	0	V
VDET terminal input voltage	V_{VDET}	0	2.4	V
VDET terminal peak input voltage	V_{PVDET}	0.65	2.4	V
Oscillator timing capacitance	C_T	330	1000	pF
Oscillator timing resistance	R_T	10	75	kΩ
Oscillation frequency	f_{OSC}	15	150	kHz
Noise filter resistance connected to IDET terminal	R_n	0	27	Ω

■ Electrical characteristics (Ta=25°C, C_T=470pF, R_T=22kΩ, V_{CC}=V_C=18V)

Oscillator section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC}	C_T=470pF R_T=22kΩ	68	75	82	kHz
Frequency variation 1 (due to supply voltage change)	f_{dV}	V_{CC}=10 to 30V		1	3	%
Frequency variation 1 (due to temperature change)	f_{dT}	Ta=–30 to +85°C		5	8	%
Output peak voltage	V_{OSC}			3.55		V
Synchronizing input peak voltage	V_{SYNC}	SYNC terminal voltage	1.5			V

Voltage error amplifier section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Reference voltage	Vr		1.519	1.550	1.581	V
Input bias current	I_{BE}		–500	–50		nA
Open-loop voltage gain	A_{VE}		80			dB
Output voltage	V_{OE+}	No load	3.5	3.8		V
	V_{OE-}			50	200	mV
Output source current	I_{OE+}	V_{OE}=0V		–900		µA

Current error amplifier section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input threshold voltage	$V_{TH\ IDET}$	V_{VDET}=0V V_{VFB}=Vr, Rn=30Ω	0	30	60	mV
Input bias current	I_{BC}	V_{IDET}=0V	–350	–250	–150	μA
Open-loop voltage gain	A_{VC}		80			dB
Output voltage	V_{OC+}	No load	3.5	3.8		V
	$V_{OC–}$			50	200	mV
Output source curent	I_{OC+}	V_{IFB}=0V		–900	μA	

Reference voltage section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Output voltage	V_{REF}		4.8	5.0	5.2	V
Voltage variation 1 (by supply voltage variation)	V_{RDV}	V_{CC}=10 to 30V			25	mV
Voltage variation 2 (by load change)	V_{RDT}	I_{OR}=0.1 to 2mA		2	5	mV

Multiplier section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
VDET terminal input voltage	V_{MVDET}		0		2.4	V
VFB terminal input voltage	V_{MVFB}		1.5		3.5	V
Output current	I_M	$V_{IIN–}$=0V		–65		μA
Output voltage coefficient	K			–1.0		–

Pulse width modulation circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Maximum duty cycle	D_{MAX}		89	92	95	%

Output circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Output voltage	V_{OL}	I_O=100mA		1.3	1.8	V
	V_{OH}	I_O=–100mA V_{CC}=18V	15.5	16.5		V
Rise time	tr	No load		300		ns
Fall time	tr	No load		200		ns

Soft-start circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input threshold voltage	V_{THCSO}	Duty cycle=0%		0.1		V
	V_{THCSM}	Duty cycle=D_{MAX}		3.55		V
Charge current	I_{CHG}	CS terminal=0V		–10		μA

Overvoltage protection circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input threshold voltage	V_{THOVP}	OVP terminal voltage	1.617	1.650	1.683	V
Input threshold voltage/reference voltage(V_{THOVP}/ Vr)	α		1.044	1.065	1.086	–
Delay time	T_{PDOVP}			200		ns

Overcurrent limiting circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Input threshold voltage	V_{THOCP} voltage	I_{DET} terminal	–1.20	–1.10	–1.00	V
Delay time	T_{PDOCP}			200		ns

Output ON/OFF circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Threshold voltage	$V_{THONOFF}$	Ta=–30°C	3.7		4.3	V
		Ta=+25°C	2.8		3.4	V
		Ta=+85°C	1.5		2.8	V
Input current at ON	I_{THON}	ON/OFF terminal voltage=$V_{THONOFF}$		10	40	µA

Undervoltage lockout circuit section

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
OFF to ON threshold voltage	V_{THUON}		14.6	15.3	16.0	V
ON to OFF threshold voltage	I_{THUOFF}		7.6	8.3	9.0	V
Voltage hysteresis	V_{UHYS}			7.0		V

Overall device

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Standby current	I_{CCST}	V_{CC}=14V		90	140	µA
Operating-state supply current	I_{CCOP}			10	15	mA
OFF-state supply current	I_{CCOFF}	Pin 12=0V		1.1	1.8	mA

■ Description of each circuit

1. Oscillator section

This section outputs sawtooth waves oscillating between 0.15 and 3.55V using the capacitor charge and discharge characteristics. Figure 1 shows how to connect the required external components to this circuit. The oscillation frequency is determined by the C_T and R_T values. The relationship between the C_T and R_T values is shown in characteristic curves. Pin 14 (SYNC) is a synchronizing input terminal whose threshold voltage is about 1V. As Fig. 1 shows, input rectangular synchronizing signal waves to pin 14 through an RC circuit. Set the free-running frequency about 10% lower than the synchronizing signal frequency. Connect a clamp diode (D1) to prevent an unwanted current inside the IC.

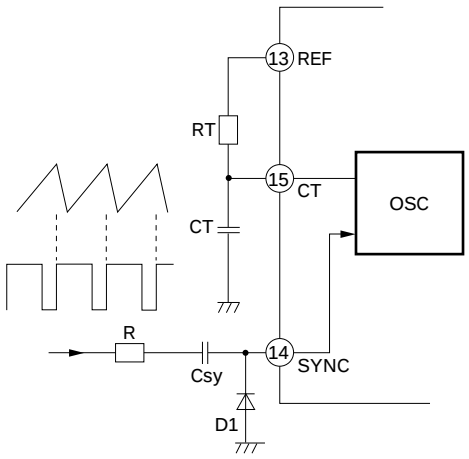


Fig. 1 Oscillator

2. Voltage error amplifier and overvoltage limiting circuit

The voltage error amplifier forms a voltage feedback loop to keep the output voltage stable. The positive input terminal of this amplifier is connected to the reference voltage (Vr). Fig. 2 shows how to connect the required external components to this circuit.
The output voltage (Vo) is as follows:

$$Vo = \frac{R1 + R2}{R1} \bullet Vr \quad \text{..... (1)}$$

Vr=1.55V(typ.)

Connect a resistor and a capacitor in parallel across error amplifier output pin 5 and error amplifier negative input pin 6 to set the voltage gain (Av).
The Av value is as follows:

$$Av = \frac{R4}{R3\ (\ 1 + j\omega\ C1 \bullet R4\ )} \quad \text{..... (2)}$$

Error amplifier cutoff frequency (fc) is as follows:

$$fc = \frac{1}{2\pi\ C1 \bullet R4} \quad \text{..... (3)}$$

If 100 or 120Hz ripples appear at the error amplifier output, the active filter does not operate stably. To ensure stable operation, set the fc value to about 1Hz.

An overvoltage detection comparator (C1) is built in to limit the voltage if the output voltage exceeds the design value. The reference input voltage (Vp) is as follows:

$$Vp = \alpha \bullet Vr \quad \text{..... (4)}$$

α =1.065

The connections shown in Fig. 2 limit the output voltage to α times the design value.

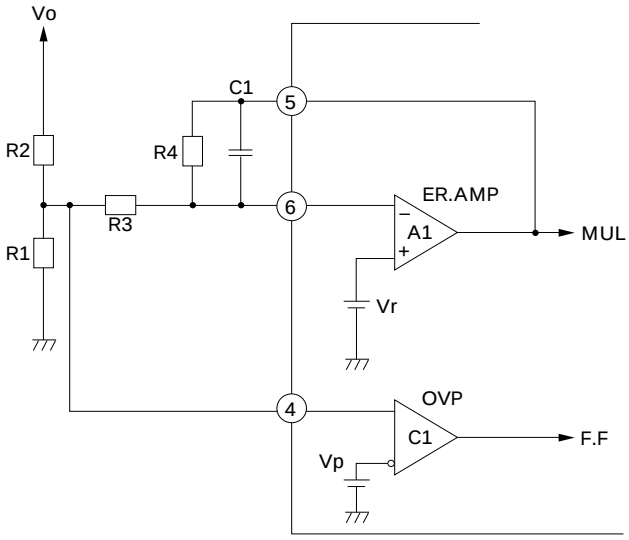


Fig. 2 Voltage error amplifier and overvoltage limiting circuit

3. Current error amplifier and overcurrent limiting circuit

The current error amplifier forms a current loop to change the input circuit current into sinusoidal waves. As Fig. 3 shows, the multiplier output is connected to pin 2 (IIN –) through a resistor (RA) to input the reference current signal. Pin 16 (IDET) is a current input terminal. Design the circuit so that the voltage at pin 16 will be within the range from 0 (GND potential) to –1.0V. Connect a phase correction resistor and capacitors across pin 1 (amplifier output) and pin 2. See Fig. 4 for the expected gain characteristics of the circuit shown in Fig. 3.

Here,

$$Z = \frac{1}{2\pi R5 \cdot C3} \quad \text{.....(5)}$$

$$p = \frac{1}{2\pi R5 \cdot C} \quad \text{.....(6)}$$

$$C = \frac{C2 \cdot C3}{C2 + C3}$$

The voltage gain (G1) between Z and P of the circuit (gain between pins 16 and 1) is given as follows:

$$G1 = 20 \cdot \log_{10} \{ 0.75 (\frac{R5}{RA} + 1) \} \quad \text{.....(7)}$$

Ensure an adequate phase margin by selecting C1 and C2 so that the p/z ratio is about 10. The current error amplifier output is used as an input to the comparator for PWM.

The overcurrent detection comparator (C2) limits an overcurrent. The threshold voltage for overcurrent detection at pin 16 is –1.10V. Connect noise filters Rn and Cn to prevent the voltage at pin 16 from fluctuating due to noise, causing the comparator to malfunction. For Rn, select a resistor of up to 27Ω. (See P66, 4. No-load operation)

4. Comparator for PWM

Figure 5 shows the comparator for PWM. When the oscillator output (Va) is smaller than the current error amplifier output (Vc), the comparator output is high and the output ON signal is generated at pin 8. Pin 11 (CS) is a terminal for soft start. This terminal charges capacitor C4 with the internal constant current (10μA) for a soft start. Priority is given to Vb and Vc whichever is lower.

5. Multiplier

The multiplier generates a reference current signal. Input a fully rectified sinusoidal signal voltage into pin 3 (VDET). Design the circuit to keep the peak voltage at pin 3 within a range from 0.65V to 2.4V. The multiplier output voltage (Vm) is roughly given as follows (see Fig. 6):

Vm = 1.25 – (Ve –1.55) • Vs ..... (8)

As Fig. 3 shows Vm is internally connected to pin 2 (IIN–) of the current error amplifier A2 through a 10kΩ resistor. (See the characteristic curve, page 67 for the input and output characteristics of the multiplier.)

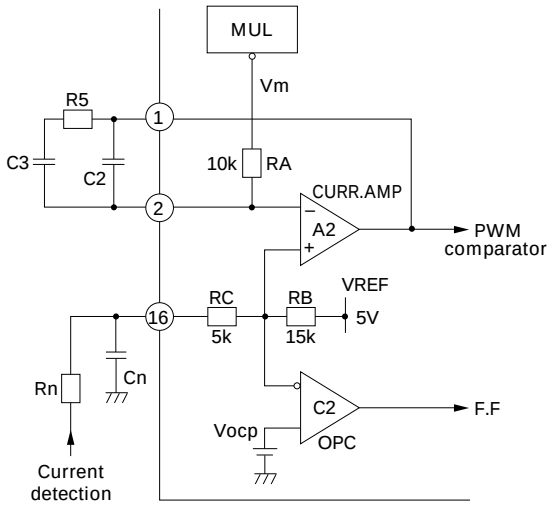


Fig. 3 Current error amplifier and overcurrent limiting circuit

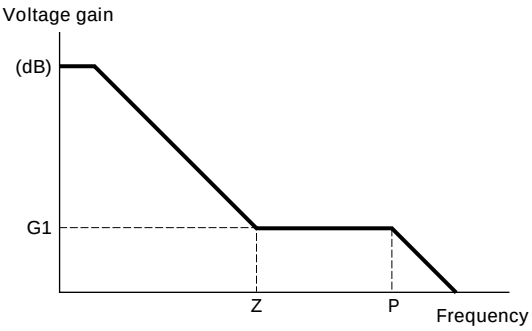


Fig. 4 Voltage gain-frequency

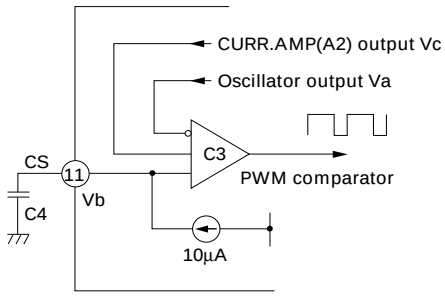


Fig. 5 PWM comparator

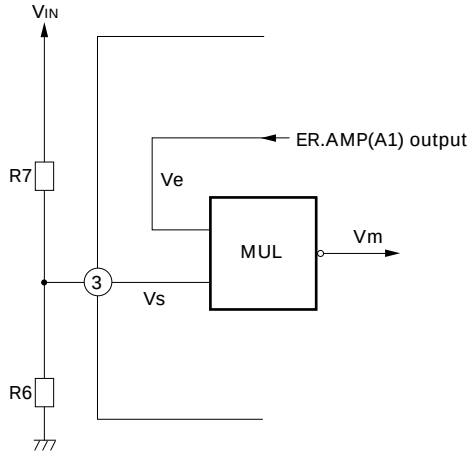


Fig. 6 Multiplier

6. ON/OFF control input circuit

Figure 7 shows the ON/OFF control input circuit. If pin 12 is set to the high level (enable), this IC outputs pulses from the OUT pin. If pin 12 is set to the low level (disable), the internal bias power (reference voltage) goes off and the IC current consumption becomes about 1/10 that of its ON state. The output level of pin 11 (CS for soft start) also goes low.

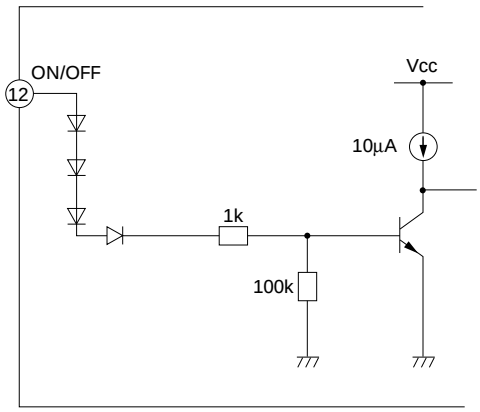


Fig. 7 ON/OFF control input circuit

7. Output circuit

As Fig. 8 shows, pin 9 is configured as the high power terminal (VC), independent of the IC power terminal (VCC). This pin allows an independent drive resistance when the power MOSFET is ON and OFF. If the drive resistances in the ON and OFF states are Rg (on) and Rg (off), the following formulas can be used to determine the total gate resistance Rg:

Rg (on) = Rg1 + Rg2 ..... (9)

Rg (off) = Rg2 ..... (10)

In the standby state, the output level of pin 8 is held low. If the potential at the drain terminal of the power MOSFET fluctuates, the gate-drain capacitance may drive the IC output voltage at pin 8 to below 0. Once the voltage at pin 8 reaches –0.6V, an unwanted current flows in the IC and a large abnormal current flows in the output circuit when the output transistor is turned on. To prevent this, connect a Schottky diode across the gate and source of the power MOSFET.

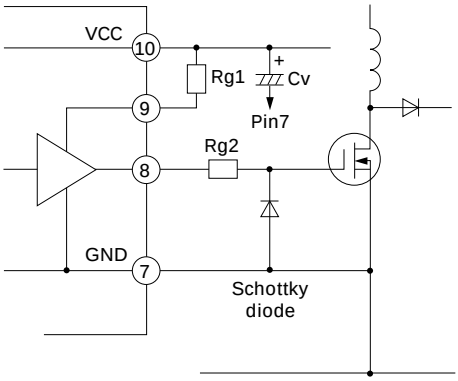


Fig. 8 Output circuit

■ Design advice

1. Start circuit

Figure 9 shows a sample start circuit. Since the IC current while the Vcc pin voltage rises from 0V to V_{THON} is as small as 90μA (typ.), the power loss in resistor R_A is small. If an additional winding is prepared in the voltage step-up inductor (L), power to the control circuit can be supplied from this circuit. However, the voltage must be stabilized by a regulator circuit (REG) to prevent an excess rise of the IC supply voltage (Vcc). Use fast or ultra-fast rectifier diodes for the rectifier circuit (DB1) of the winding for high-frequency operation.

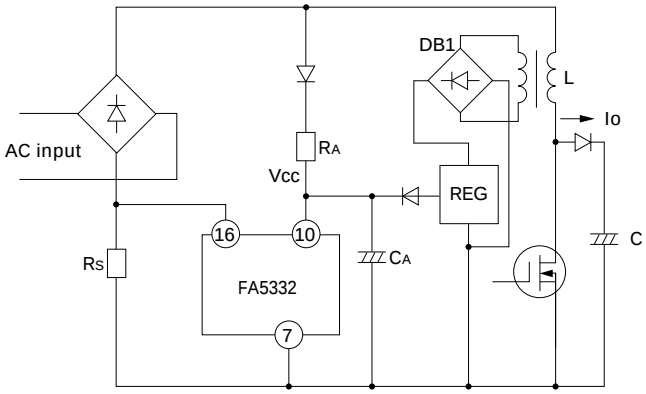


Fig. 9 Start circuit

2. Current sensing resistor

The current sensing resistor (Rs) detects the current in the inductor. Rs is used to make the input current sinusoidal. The current in the inductor produces a negative voltage across Rs. The voltage is input to IC pin 16 (IDET). Determine the value of Rs so that the peak voltage of the IDET pin is –1V.

$$Rs = \frac{Vin}{\sqrt{2} \bullet Pin} \quad \text{..... (11)}$$

Vin: Minimum AC input voltage (effective value) [V]
Pin: Maximum input power [W]

Since the threshold voltage of the overcurrent limiting circuit (pin 16) is –1.10V, the peak input current limit (ip) is determined by:

$$ip = \frac{1.10}{Rs} \quad \text{..... (12)}$$

3. Voltage step-up type converter

Figure 9 shows the basic circuit of a voltage step-up type converter which is used as a power factor correction.

(a) Output voltage

For stable operation, set the output voltage to be 10V or more over the peak value of the maximum input voltage. When using this IC for an active filter, set the output voltage (Vo) as follows:

$$Vo \geq \sqrt{2} \bullet Vin + 10V \quad \text{..... (13)}$$

Vin: Maximum AC input voltage [V]
(effective value of sinusoidal wave)

(b) Voltage step-up inductor

When using a voltage step-up converter in continuous current mode, the ratio of inductor current ripple to the input peak current is set to about 20%. Determine the inductance as follows:

$$L \geq \frac{Vin^2 \, (Vo - \sqrt{2} \bullet Vin)}{\gamma \bullet fs \bullet Pin \bullet Vo} \quad \text{..... (14)}$$

Vin: Minimum AC input voltage (effective value) [V]
γ : Ratio of inductor current ripple (peak to peak value) to the input peak current (about 0.2)
fs: Switching frequency [Hz]
Pin: Converter's maximum input power [W]

As the characteristic curves on page 67 show, the peak voltage at pin 3 should be at least 0.65V, even when the AC input voltage is minimal. Considering this, determine R6 and R7 shown in Fig. 6.

Example:

When Vin is 85V and Pin is 300W, the formulas of (11) and (12) can be calculated as:

$$Rs = \frac{85}{\sqrt{2} \bullet 300} = 0.2 \, [\Omega]$$

$$ip = \frac{1.10}{0.2} = 5.5 \, [A]$$

And,

$$\sqrt{2} \bullet 85 \bullet \frac{R6}{R6 + R7} = 0.65 \, [V]$$

If R6 is set to 2.7kΩ to satisfy these formulas, R7 becomes 480kΩ.

Example:

When Vin is 85V, Vo is 385V, and γ is 0.2, the formula of (14) can be calculated as:

$$L \geq \frac{2.48 \times 10^4}{fs \bullet Pin} \, [H] \quad \text{..... (15)}$$

(c) Smoothing capacitor

When a voltage step-up converter is used in a power factor correction circuit, the input current waveform is regulated to be in-phase with the input voltage waveform. Therefore, ripple noise of twice the input line frequency appears at the output. The output voltage (υ_o) is represented as:

$$\upsilon_o = Vo - \frac{Io}{2 \bullet \omega_o \bullet C} \bullet \sin 2\omega_o t \quad \text{..... (16)}$$

Vo: Average output voltage
Io: Output current
ω_o: 2π fo (fo: Input power frequency, 50 or 60Hz)
C: Smoothing capacitor value

Therefore, the peak-to-peak value of the output ripple voltage Vrp is given by:

$$Vrp = \frac{Io}{\omega_o C} \quad \text{..... (17)}$$

Using formula (17), determine the necessary C value.

4. No-load operation

In the circuit shown in Fig.10, the following condition should be meet to prevent from overvoltage and audible noise during no-load or light-load operation.

$R_n \leq 27\Omega$
and, R_X: don't connect.

- You can connect R_5 which is series with capacitor C_3.
- If you connect R_{OFST}, dead time of AC input current will extend.
- It is better not to connect R_X. But in some application, it is effective for stable operation to connect R_X which reduce DC gain of current error amplifier.
  If R_X is connected, connect R_{OFST} as the following condition.

$2.5 < (R_{OFST}/R_X) < 2.9$ (including tolerance of the resistor)

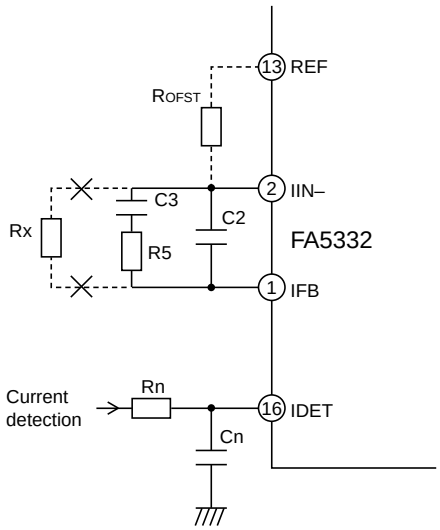


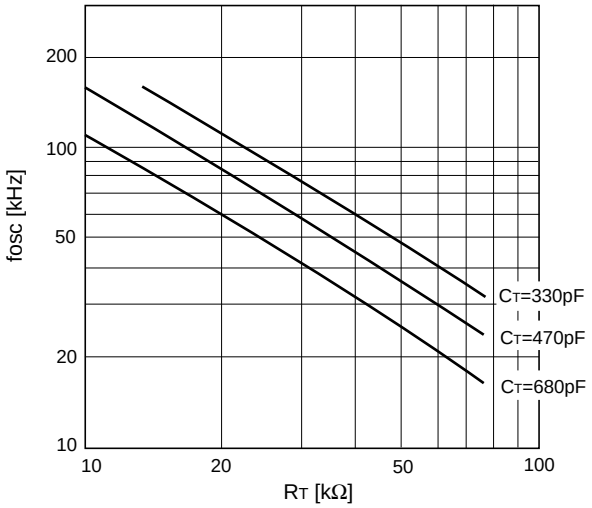
Fig.10

5. How to prevent from intermittent switching of low frequency

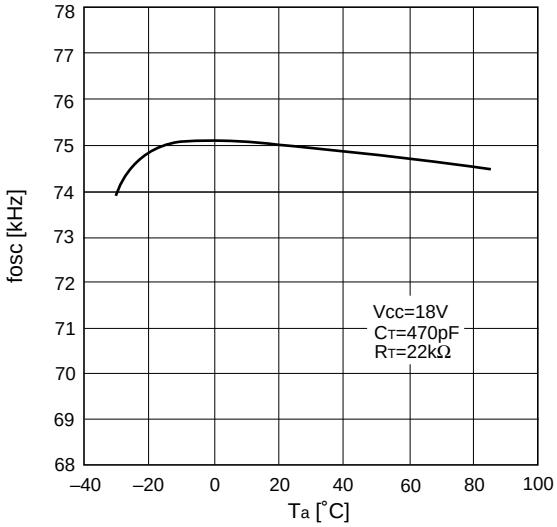
An intermittent switching, which frequency is lower than 10Hz, occurs in some applications.
In this case, it is possible to prevent from this intermittent switching to reduce feedback gain by decreasing the resistance of R4. (See Fig. 2)
You must check the effect thoroughly because this intermittent switching depends on load, temperature and input condition.

■ Characteristic curves (Ta = 25°C)

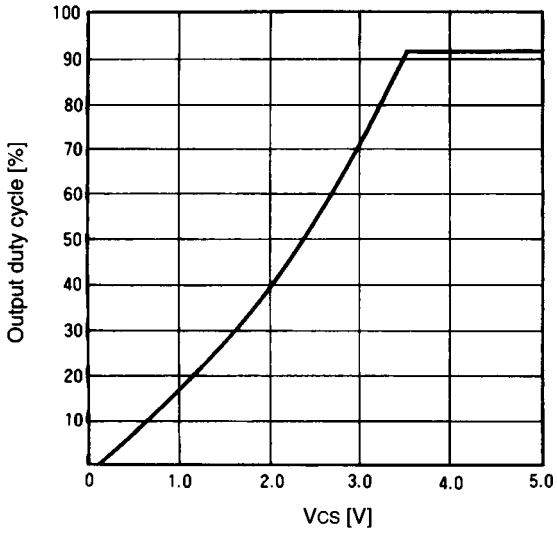
Oscillation frequency (fosc) vs. timing resistor resistance (R_T)



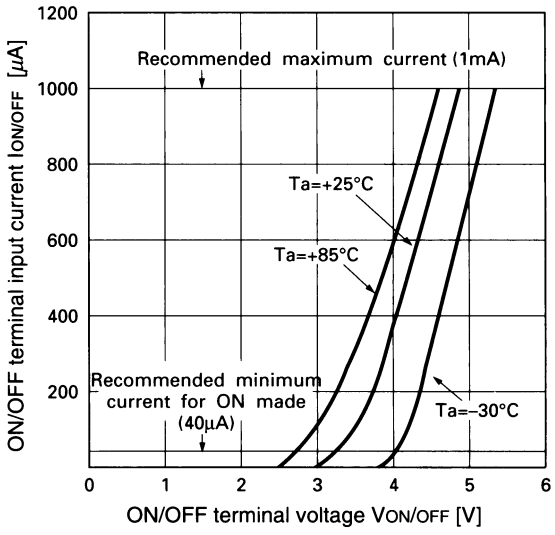
Oscillation frequency (fosc) vs. ambient temperature (Ta)



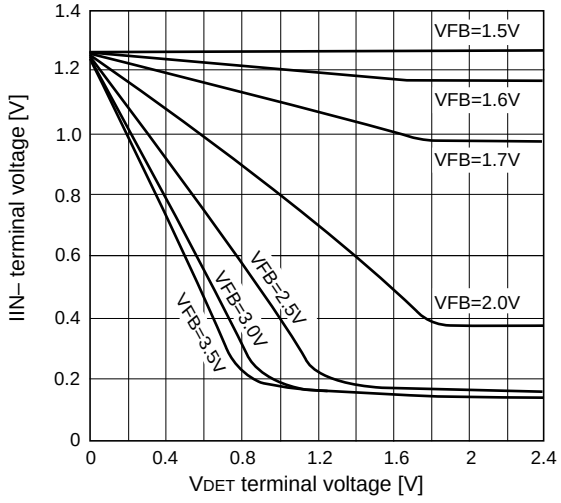
Output duty cycle vs. CS terminal voltage (V_{CS})



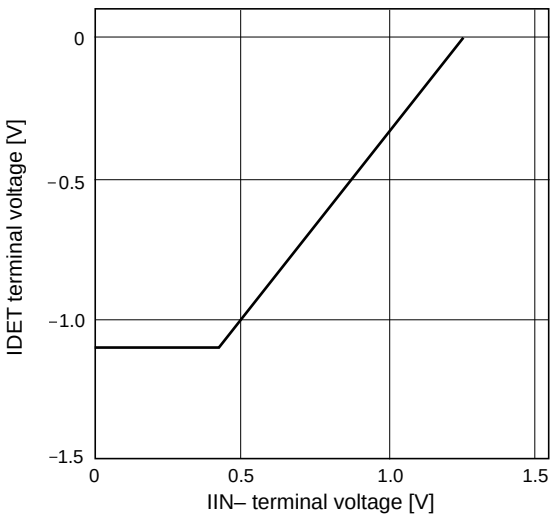
ON/OFF control terminal current vs. ON/OFF control terminal voltage



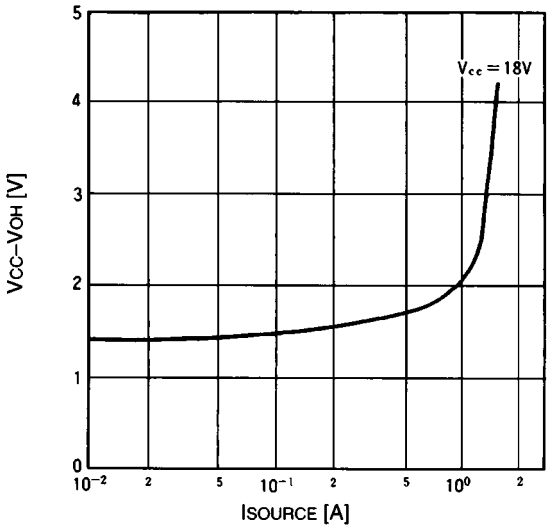
IIN– terminal voltage vs. VDET terminal voltage
Multiplier I/O



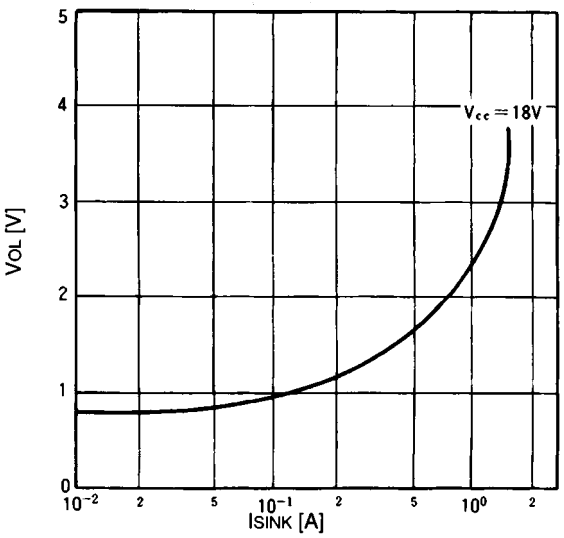
IDET terminal voltage vs. IIN– terminal voltage
Normal operation



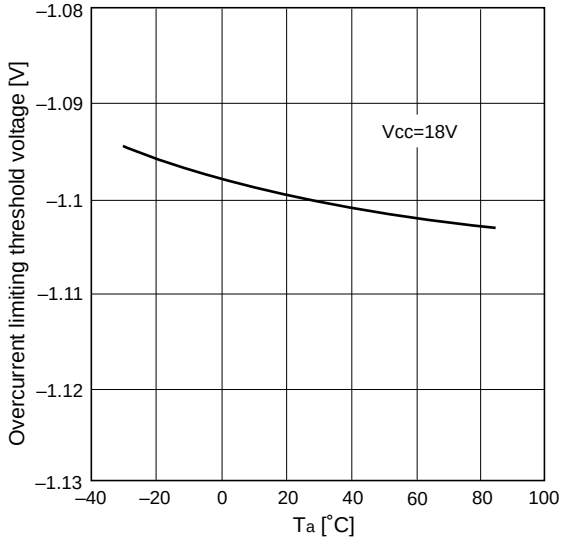
H-level output voltage (V_{OH}) vs. output source current (I_{SOURCE})



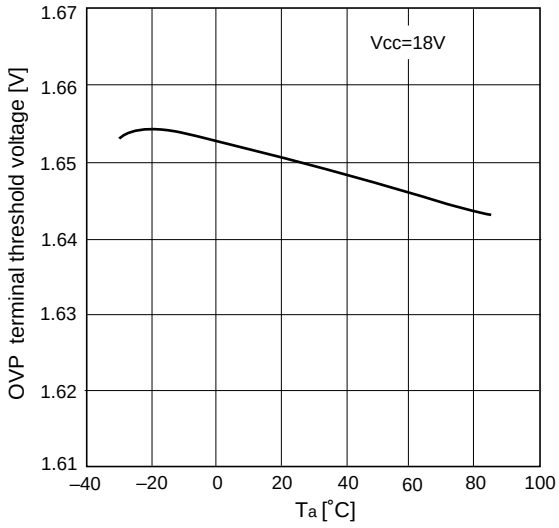
L-level output voltage(V_{OL}) vs. output sink current (I_{SINK})



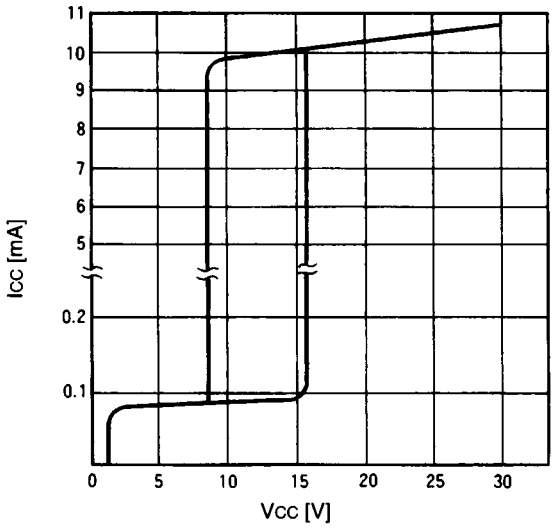
Overcurrent limiting threshold voltage vs. ambient temperature (Ta)



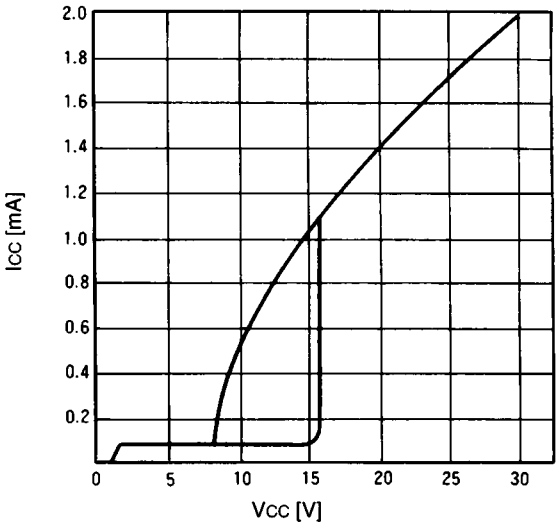
OVP terminal threshold voltage vs. ambient temperature (Ta)



Supply current (I_{CC}) vs. supply voltage (V_{CC})
Normal operation

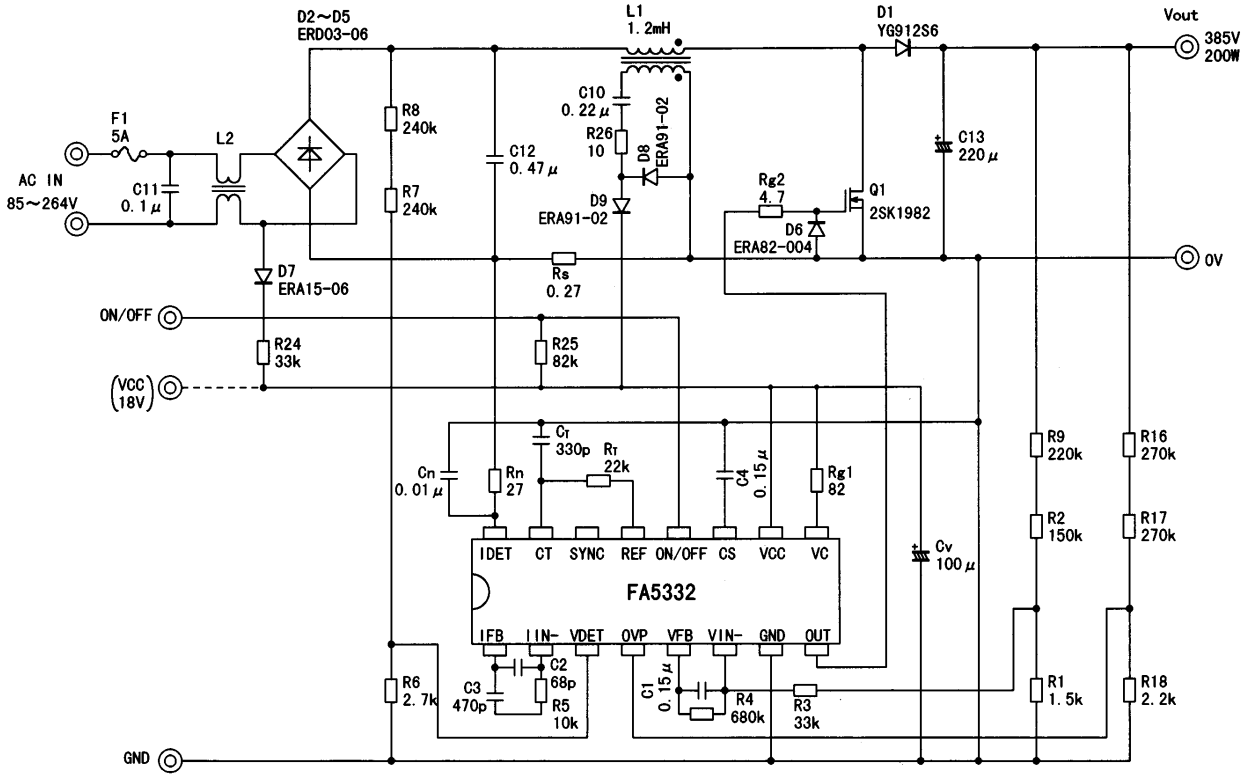


Supply current (I_{CC}) vs. supply voltage (V_{CC})
OFF mode



■ Application circuit

● Example of application circuit



Parts tolerances characteristics are not defined in the circuit design sample shown above. When designing an actual circuit for a product, you must determine parts tolerances and characteristics for safe and economical operation.