

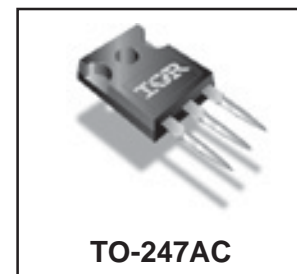
**Applications**

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

$V_{DSS}$	$R_{DS(on)}$ typ.	$I_D$
<b>500V</b>	<b>0.135Ω</b>	<b>32A</b>

**Benefits**

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low  $R_{DS(on)}$



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	32	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	20	
$I_{DM}$	Pulsed Drain Current ①	130	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	460	W
	Linear Derating Factor	3.7	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case )	300	
	Mounting torque, 6-32 or M3 screw		

**Avalanche Characteristics**

Symbol	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	450	mJ
$I_{AR}$	Avalanche Current①	—	32	A
$E_{AR}$	Repetitive Avalanche Energy①	—	46	mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case④	—	0.26	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient④	—	40	

# IRFP32N50K

International  
IR Rectifier

## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	500	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.54	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA④
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	0.135	0.16	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 32A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	50	μA	V <sub>DS</sub> = 500V, V <sub>GS</sub> = 0V
		—	—	250	μA	V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 30V
	Gate-to-Source Reverse Leakage	—	—	-100	nA	V <sub>GS</sub> = -30V

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

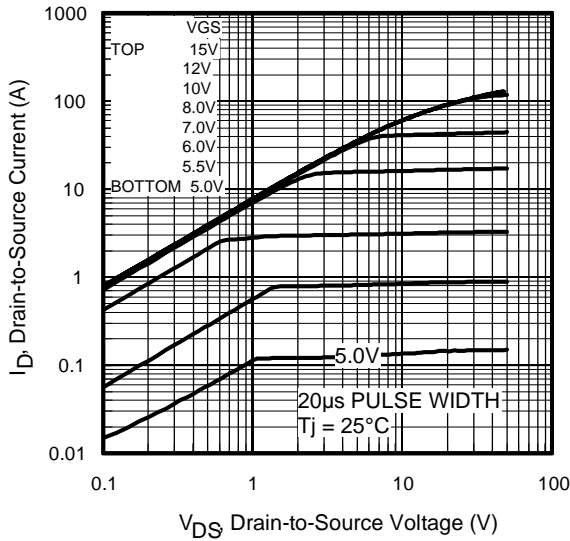
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	14	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 32A
Q <sub>g</sub>	Total Gate Charge	—	—	190	nC	I <sub>D</sub> = 32A V <sub>DS</sub> = 400V V <sub>GS</sub> = 10V ④
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	59		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	84		
t <sub>d(on)</sub>	Turn-On Delay Time	—	28	—	ns	V <sub>DD</sub> = 250V I <sub>D</sub> = 32A R <sub>G</sub> = 4.3Ω V <sub>GS</sub> = 10V ④
t <sub>r</sub>	Rise Time	—	120	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	48	—		
t <sub>f</sub>	Fall Time	—	54	—		
C <sub>iss</sub>	Input Capacitance	—	5280	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance	—	550	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	45	—		
C <sub>oss</sub>	Output Capacitance	—	5630	—		
C <sub>oss</sub>	Output Capacitance	—	155	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	265	—		

## Diode Characteristics

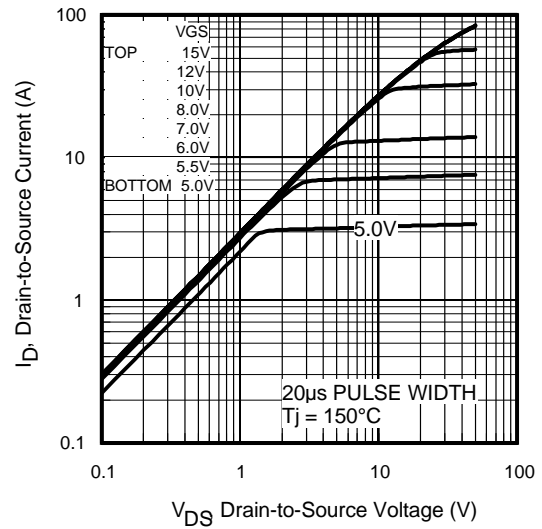
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	32	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	130		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 32A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	530	800	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 32A
Q <sub>rr</sub>	Reverse Recovery Charge	—	9.0	13.5	μC	di/dt = 100A/μs ④
I <sub>RRM</sub>	Reverse Recovery Current	—	30	—	A	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Notes:

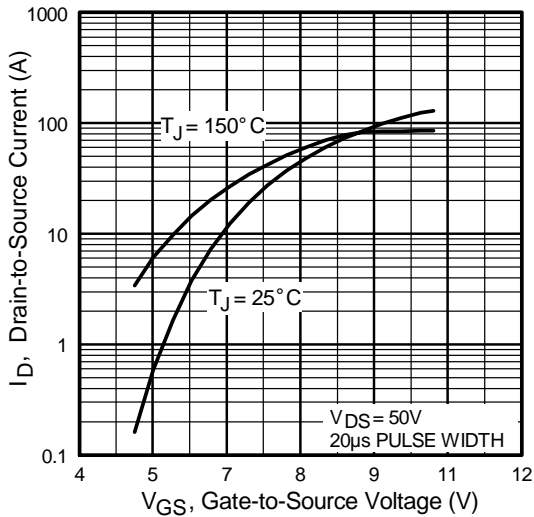
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting T<sub>J</sub> = 25°C, L = 0.87mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 32A,
- ③ I<sub>SD</sub> ≤ 32A, di/dt ≤ 296A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DS</sub>.
- ⑥ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C



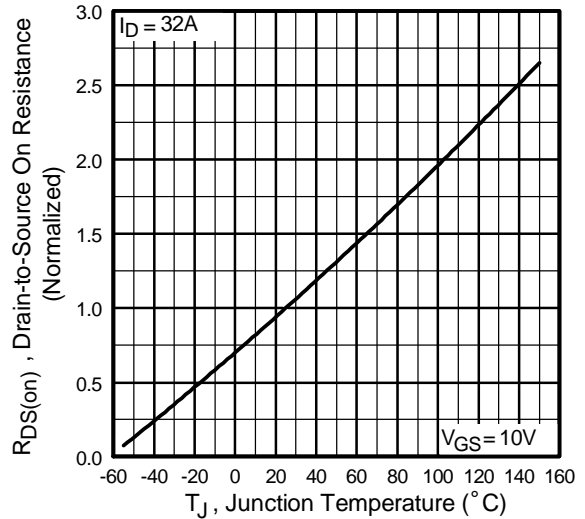
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

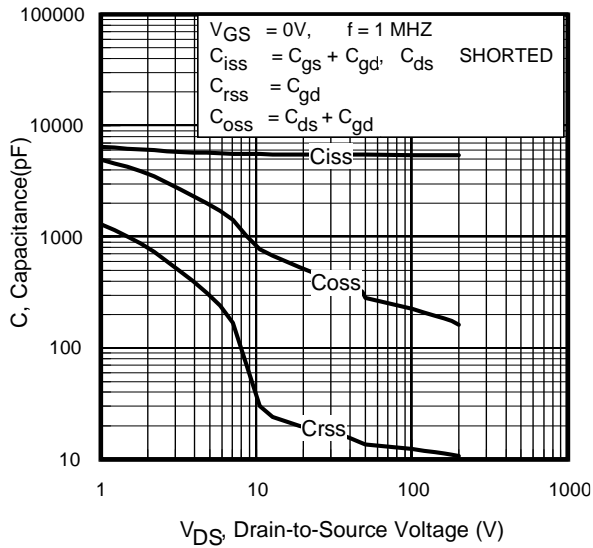


**Fig 3.** Typical Transfer Characteristics

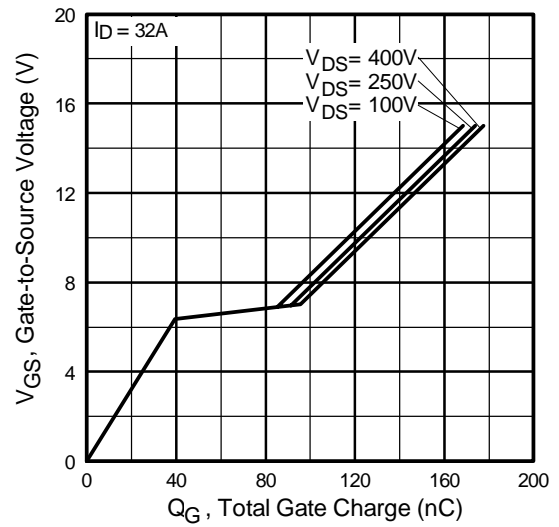


**Fig 4.** Normalized On-Resistance Vs. Temperature

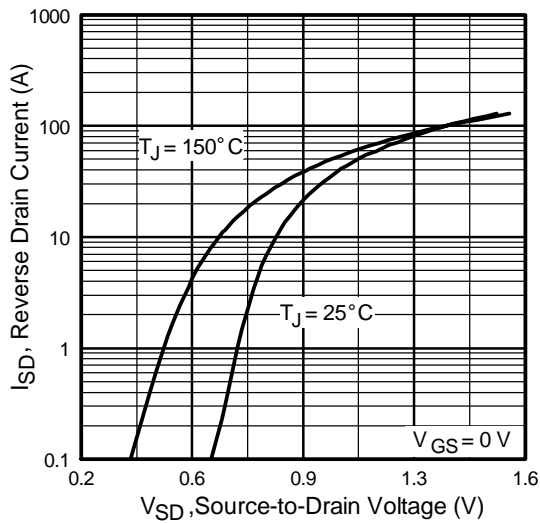
# IRFP32N50K



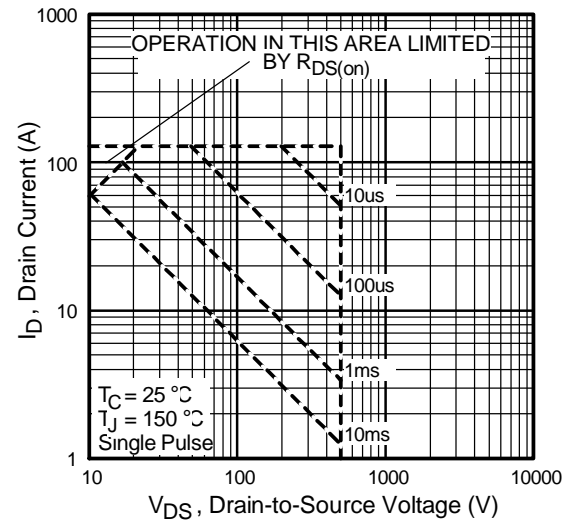
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



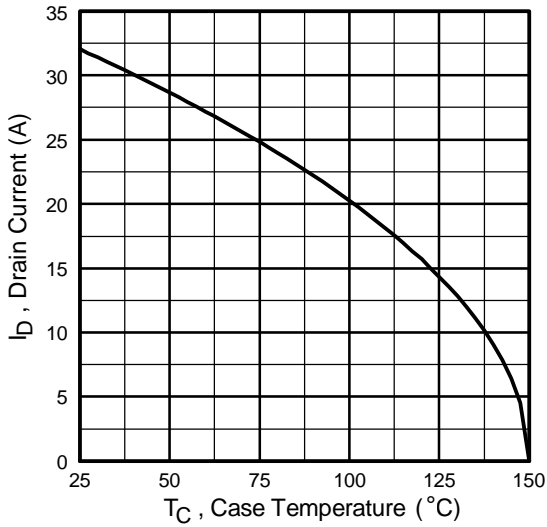
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



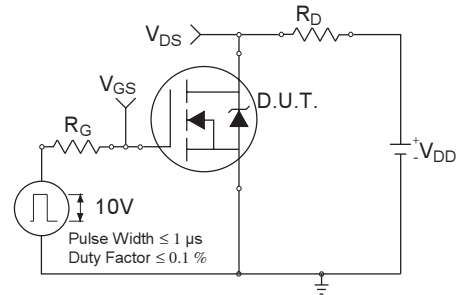
**Fig 7.** Typical Source-Drain Diode Forward Voltage



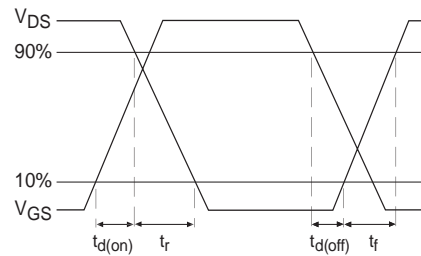
**Fig 8.** Maximum Safe Operating Area



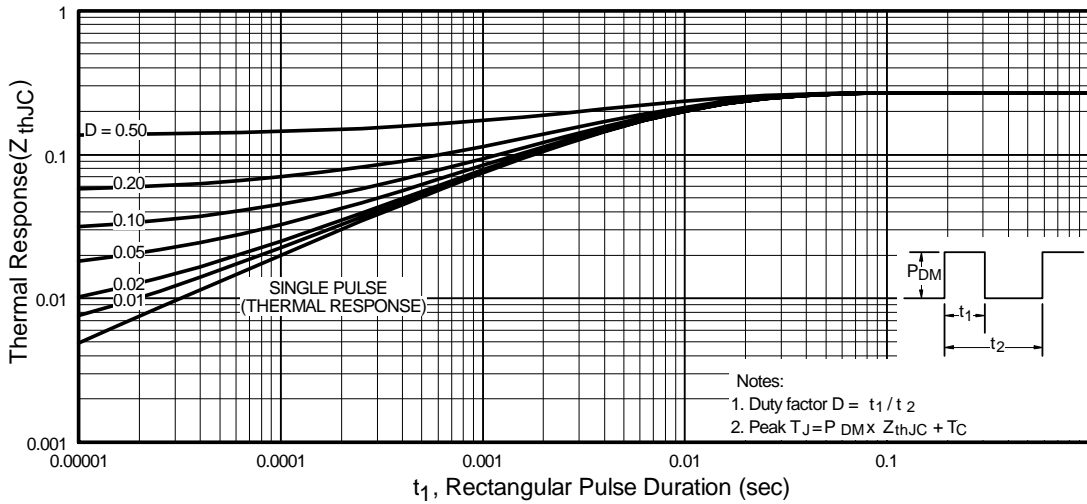
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

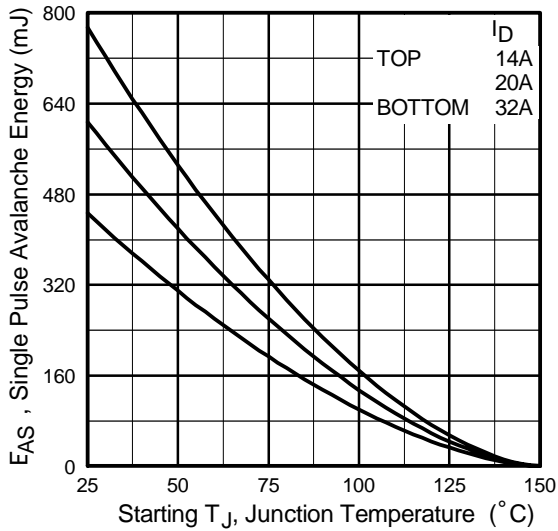


**Fig 10b.** Switching Time Waveforms

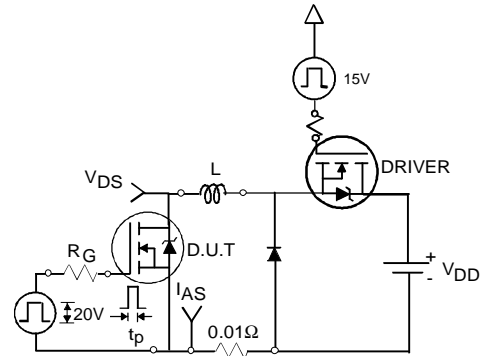


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

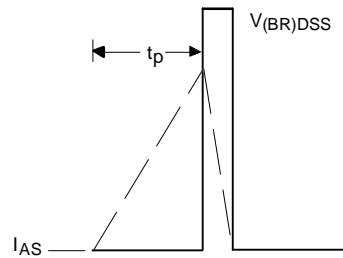
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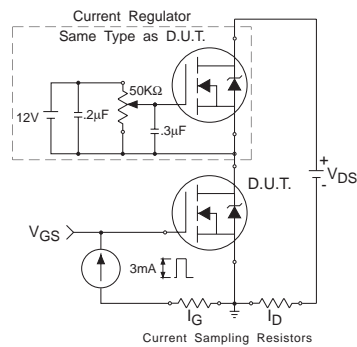
**Fig 12a.** Maximum Avalanche Energy Vs. Drain Current



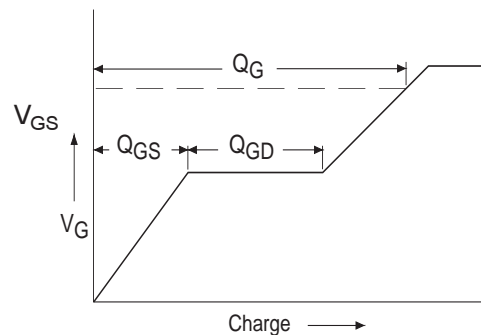
**Fig 12c.** Unclamped Inductive Test Circuit



**Fig 12d.** Unclamped Inductive Waveforms

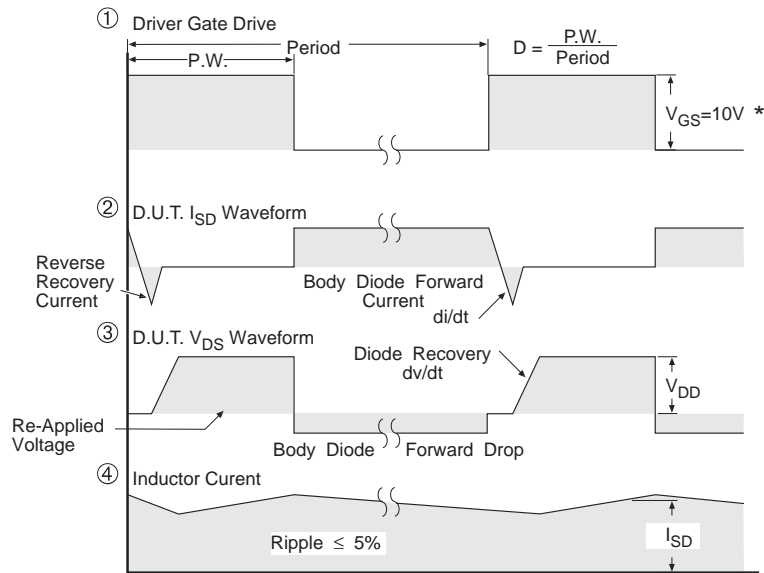
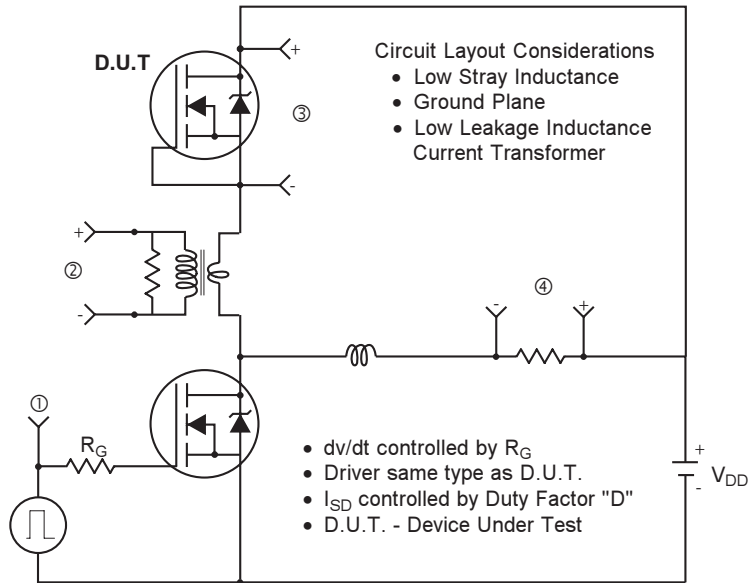


**Fig 13a.** Gate Charge Test Circuit



**Fig 13b.** Basic Gate Charge Waveform

## Peak Diode Recovery dv/dt Test Circuit



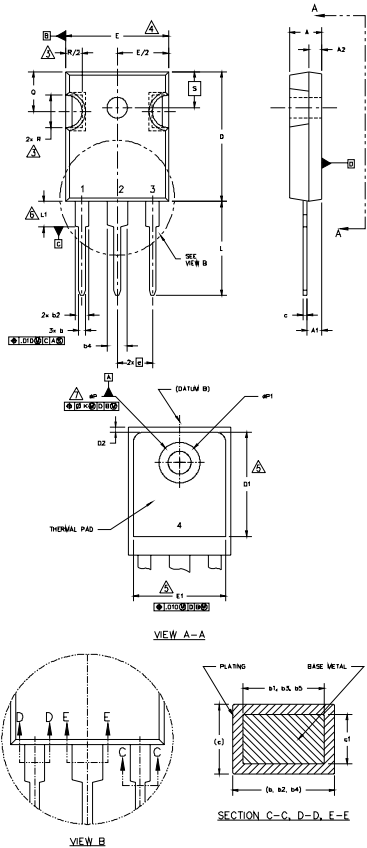
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRFP32N50K

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TO-247AC Package Outline Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91]

B. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION C.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.37	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.034	0.38	0.86	
c1	.015	.030	0.38	0.76	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.030	0.51	0.76	
E	.602	.625	15.29	15.87	4
E1	.540	-	15.72	-	
e	.215 BSC		5.46 BSC		
ek	.010		2.54		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
N	3		7.62 BSC		
$\phi P$	.140	.144	3.56	3.66	
$\phi P1$	-	.275	-	6.98	
Q	.209	.224	5.31	5.69	
R	.178	.216	4.52	5.49	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

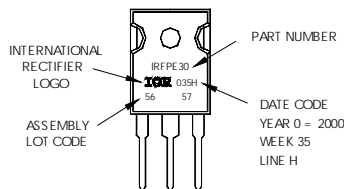
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30  
WITH ASSEMBLY  
LOT CODE 5657  
ASSEMBLED ON WW35, 2000  
IN THE ASSEMBLY LINE "H"  
Note: "P" in assembly line  
position indicates "Lead-Free"



This product has been designed and qualified for the industrial market.  
Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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TAC Fax: (310) 252-7903

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