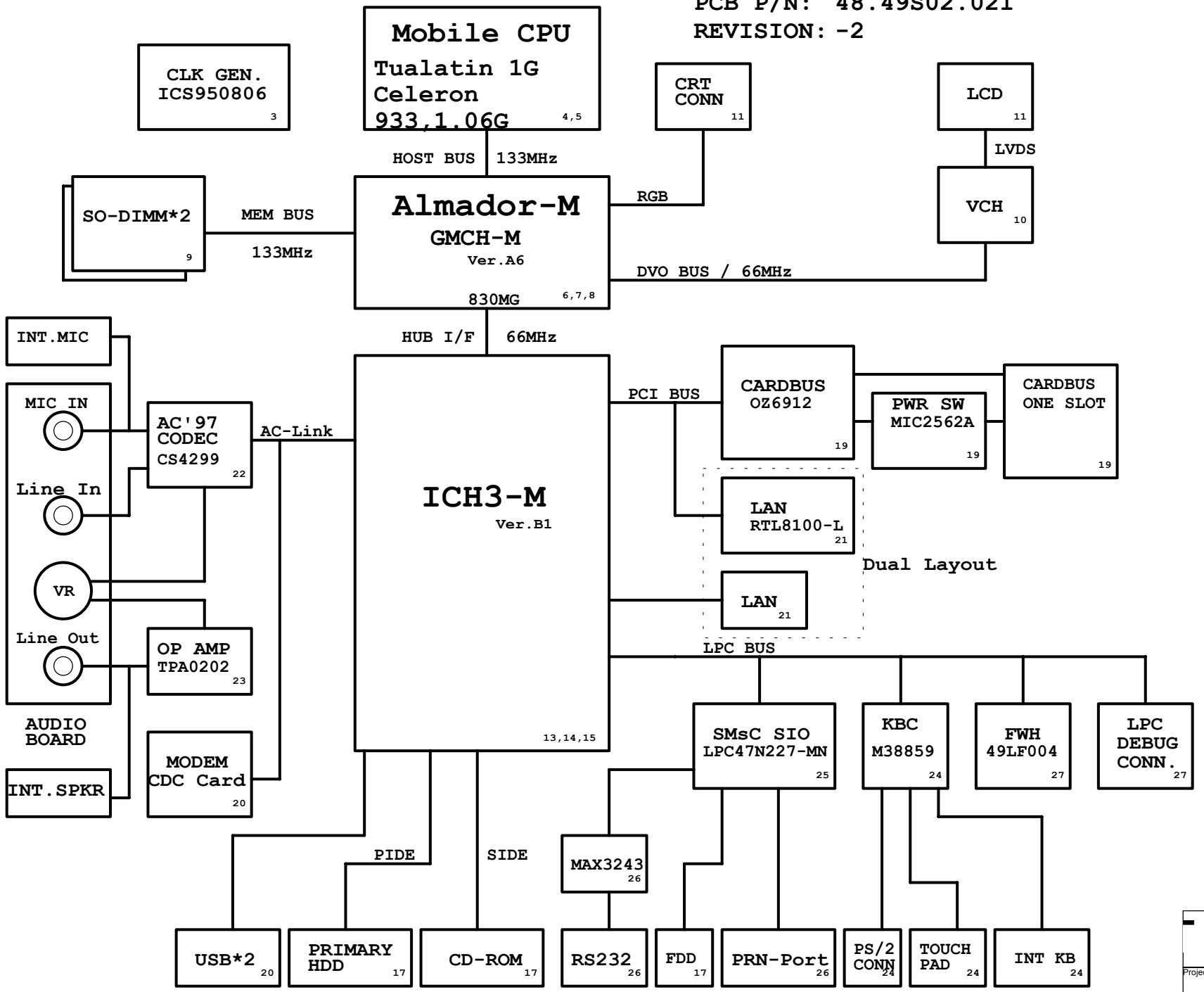
Falcon 3M

Project code: 91.49S01.001
PCB P/N: 48.49S02.021
REVISION: -2



PCB LAYER
L1: Signal 1
L2: GND
L3: Signal 2
L4: VCC
L5: Signal 3
L6: GND
L7: Signal 4
L8: Signal 5

DC/DC&CHARGER
Switching Power
MAX1632/OZT05J02

INPUTS	OUTPUTS
DCBATOUT	5VS_S5 3V_S5 1D8V_S5 3D3V_S5AC 1D8V_S5AC 5V_S3 3D3V_S3 5V_S0 3D3V_S0 12V_S0
AD+	BT+

PAGE:30/33,34

CPU DC/DC
Switching Power
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 VCCT_S0

PAGE:28,29

OTHER DC/DC
MAX1793/MAX1792

INPUTS	OUTPUTS
3D3V_S0	1D8V_S0
3D3V_S0	1D5V_S0

PAGE:29

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Project: Block Diagram

Size	Document Number	Rev
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REVISION HISTORY

SB 10/18/01

P6 BC340(0.01u) CHANGE TO SIZE 0402

P8 BC304(68P) CHANGE TO 33P(SIZE 0402) AND ADD BC590(33P SIZE 0402)

P10 RN6 CHANGE TO 4.7K OHM

P11 LCD CONNECTOR CHANGE TO 40PIN(20.F0312.040)

P12 CHANGE R61 0 OHM TO R47

P13 U64 AND BC493 DUMMY

P14 LAN_RST# ADD A DUMMY RESISTANCE PULL-UP TO 3D3V_S5

P15 TC18 CHNAGE TO 10U(BC589)

P17 CN16 ROTATE 180 DEGREE

P20 ADD BC590(0.1U) ON USBPWR0 FOR EMI
R29,R30,R31,R32 CHANGE TO L27,L28,L29,L30(BLM11B750S) FOR EMI

P21 L1,L2 CHANGE TO BLM18HG102SN1 FOR EMI
BC60 MOUNT 1000P AND XFR_TDC PULL-UP 3D3V_S0

P22 U72 CHANGE TO CS4200-XQ AND MODIFY SCH. FOR IT
ADD A DUMMY RESISTANCE CONNECT AUD_GND AND GND FOR EMI

P23 MODIFY EXT_MIC_IN
HP_IN# PULL-UP TO OP5VA_S0 AND U74 PIN NC
L27 CHANGE TO 0 OHM

P24 LAUNCH KEY CONNECT TO KBC P6-[3..6]

P28 ADD L31(FBMJ3216HS800T),BC597(0.1U) AND R173 CHANGE 4.7 OHM FOR EMI
MODIFY CPU_CORE FOR CELERON933
TC11,TC12 EXCHANGE COMPONENT

P29 ADD R564 4.7 OHM FOR EMI

P32 CN7 CHANGE TO 22.10037.341
BC105 CHANGE TO CONNECT TO AD_JK FOR EMI

P33 L13 CHANGE TO O OHM

P34 R500,R501 CHANGE TO 2.2K OHM
Q49 CHANGE TO TP0610 AND IT'S PIN1 CONNECT TO 5V_S5

P35 ADD 2 GND PAD K16,K17

SB 10/23/01

P18 U47 CHANGE TO G768C AND RB2 MOUNT 4.7K OHM

-1 11/27/01

P8 R333 CONNECT TO 3D3V_S0 AND ADD A DUMMY RESISTANCE CONNECT TO 3D3V_S3
BC230 CHANGE TO 0.01U

P10 CHANGE ALL SCD1U10V2MX TO SCD1U16V

P11 U26 CHANGE TO TPS2013AD AND CN12 CHANGE TO SYN-CONN40A-1

P12 CN9 PIN2 ADD INT_MIC_IN
PIN7 AND PIN8 ADD TWO DUMMY RESISTANCES CONNECT TO ICH_SDA AND ICH_SCL
ADD TWO SCD1U AND ONE 1000P ON 3D3V_S5

P13 SMLINK0 AND SMLINK1 PULL-UP TO 3D3V_S5
ICH_SCL AND ICH_SDA ADD A DUMMY RESISTANCE PULL-UP TO 3D3V_S0
ADD TWO 0 OHM ON CC_SMI# AND CC_STPCLK#

P14 U64 DUMMY AND R561 MOUNT 10K OHM
ADD 0 OHM ON PM_STPCPU#

P20 C39 MOUNT 22P

P21 L6,L7,L8,L9 CHANGE TO 0 OHM

P23 ADD INT_MIC_IN AND MIC PRE_AMP(DUMMY FIRST)

P28 MODIFY CPU VCORE FOR TUALATIN 1G

P32 ADD TWO SCD1U ON BT+ FOR EMI
R441 DUMMY

P34 U63 CHANGE TO LP2951ACM
BC95 CHANGE TO 0.47U

P35 U45 PIN5 AND PIN6 CONNECT TO GND

-2 12/07/01

P.M. Change CPU SPEC from BGA Package to Micro-FCPGA Package

P4 U31A CHANGE TO BGA47G-SKT2-U
U31B CHANGE TO BGA47G-SKT2-U

P5 U31C CHANGE TO BGA47G-SKT2-U
U31D CHANGE TO BGA47G-SKT2-U

P13 R404 CHANGE TO DUMMY, R576 CHANGE TO 0 OHM, R577 CHANGE TO DUMMY

P17 R327 CHANGE TO 0 OHM, R330 CHANGE TO DUMMY
INTEL ICH-3M CHANGE NEW VERSION

P18 R291 CHANGE TO D36, U50 PIN1 CHANGE TO 3D3V_S0

P24 RN11 PIN1,2,3,4 CHANGE TO 3D3V_S3

P28 DEL CPU_CORE, DEL G7 G8 G9 G10 G11, DEL TC7 TC 14

P30 DEL M1632_5V_1 3D3V_S5AC_1, DEL G1 G2 G3 G4 G5 G6

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Project: Falcon 3M Rev_History

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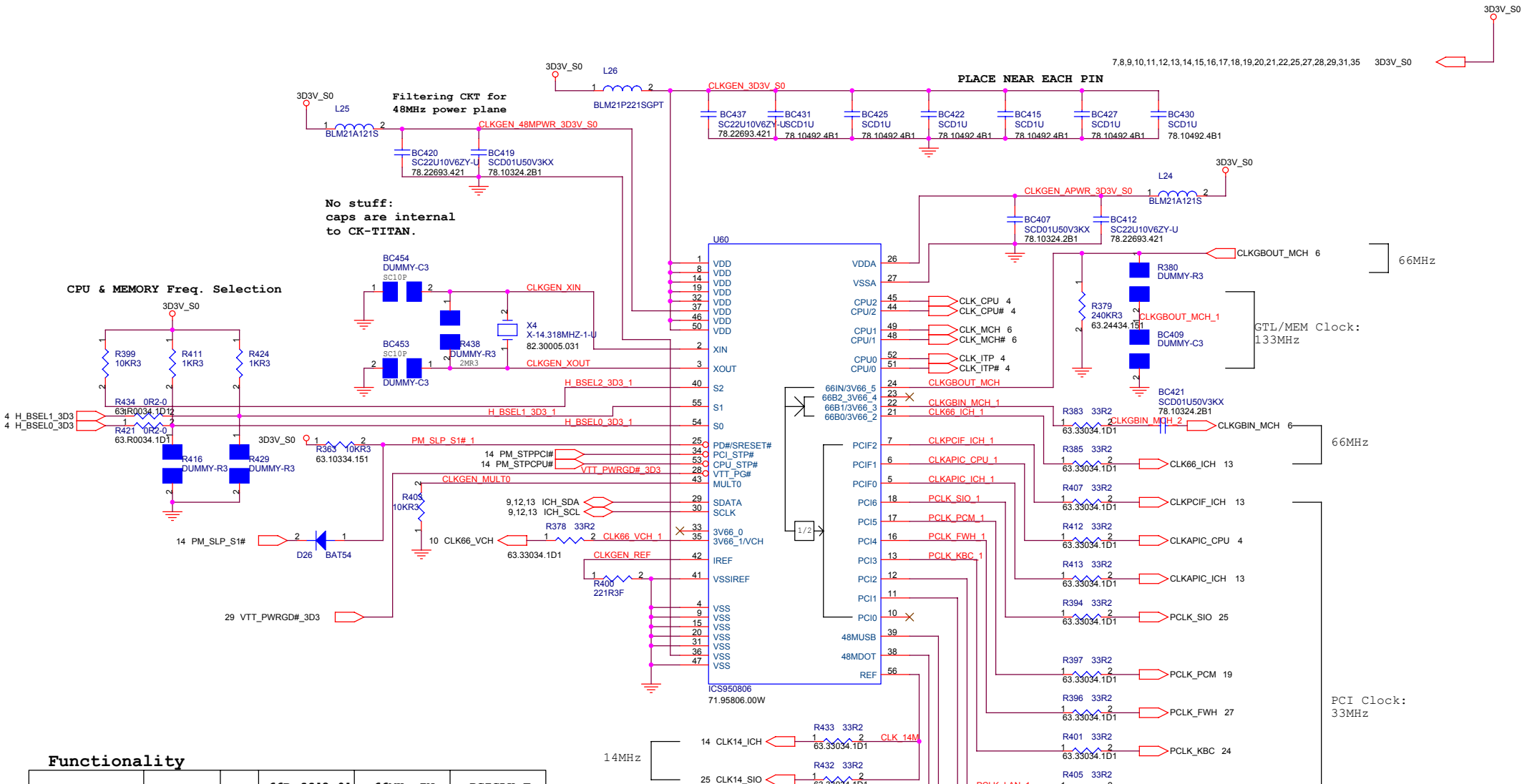

Functionality

BIT			CPUCLK	3V66	66Buff[2:0]	66MHz_IN	PCICLK_F	
					3V66[4:2]	3V66_5	PCICLK	
FS2	FS1	FS1	MHz	MHz	MHz	MHz	MHz	
0	0	0	66.66	66.66	66.66	33.33	33.33	
0	0	1	100.00	66.66	66.66	33.33	33.33	
0	1	0	200.00	66.66	66.66	33.33	33.33	
0	1	1	133.33	66.66	66.66	33.33	33.33	
1	0	0	66.66	66.66	66MHz_IN	Input	66MHz_IN/2	
1	0	1	100.00	66.66	66MHz_IN	Input	66MHz_IN/2	
1	1	0	200.00	66.66	66MHz_IN	Input	66MHz_IN/2	
1	1	1	133.33	66.66	66MHz_IN	Input	66MHz_IN/2	Defualt

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Project: CLOCK GENERATOR

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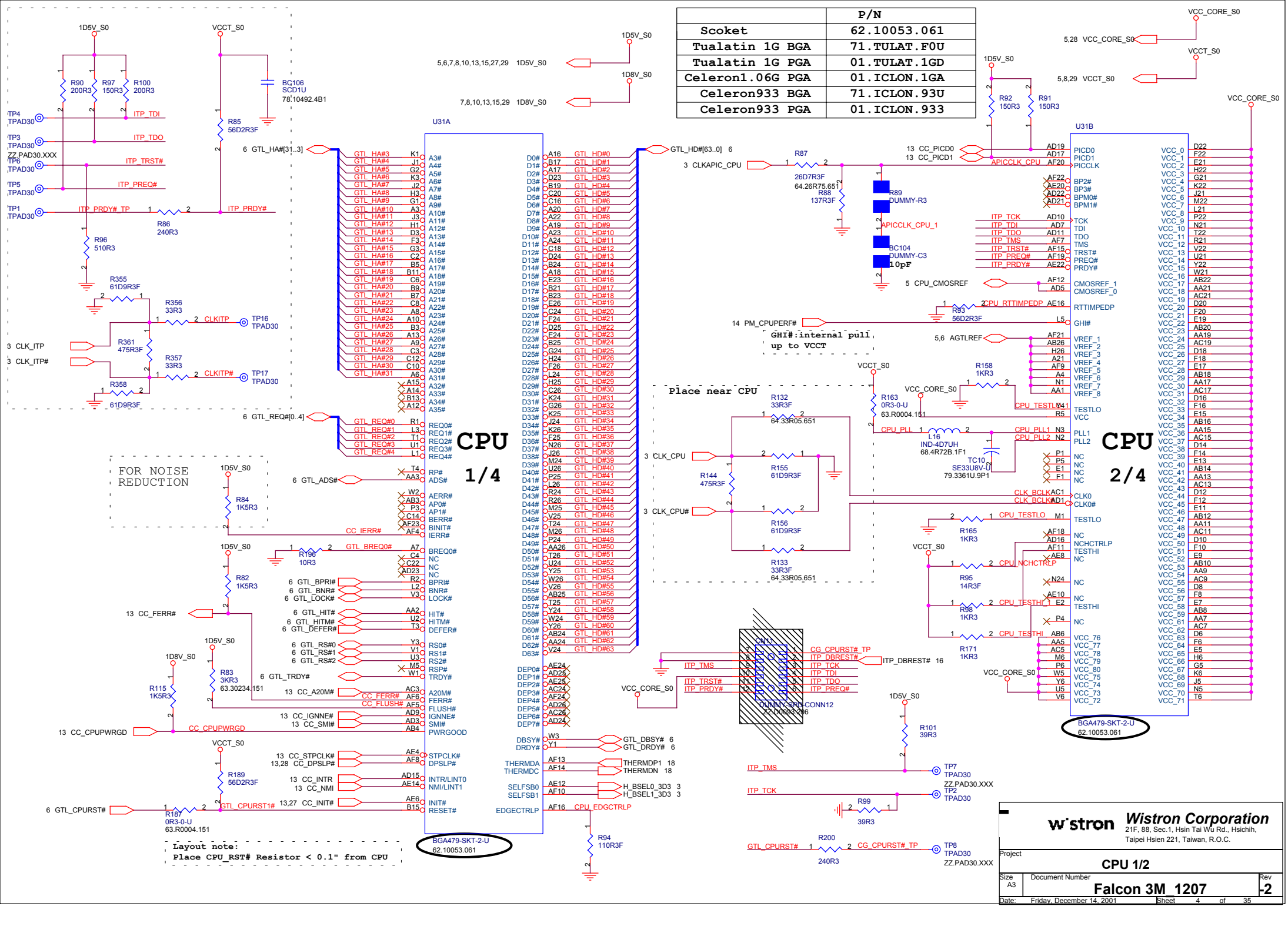
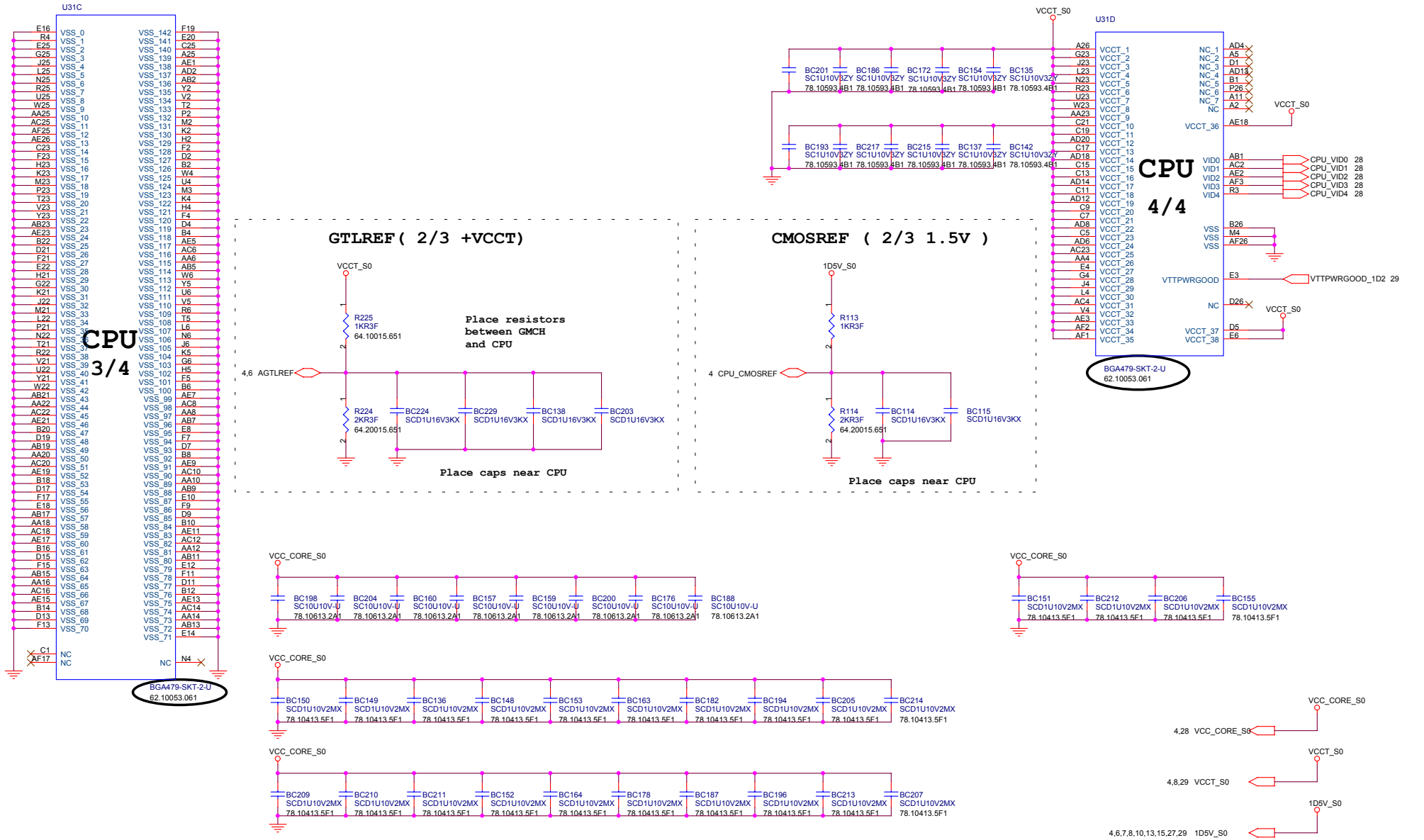
	P/N
Scoket	62.10053.061
Tualatin 1G BGA	71.TULAT.F0U
Tualatin 1G PGA	01.TULAT.1GD
Celeron1.06G PGA	01.ICLON.1GA
Celeron933 BGA	71.ICLON.93U
Celeron933 PGA	01.ICLON.933





Decouping Recommendation

				Falcon 3M	Kodiak Ver. 0.5
VCC_CORE	Underneath balls on solder side	0.47uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	10uF / 6.3V * 12
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 8	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 6	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

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Project: CPU 2/2 CONFIGURATION

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Date: Friday, December 14, 2001 | Sheet 5 of 35

Have some pin difference between A2 and A3 stepping

AGP_REF used as DVO_REF for DVO device

Must place on top side

Put these Damping resistor close GMCH

SM_OCLK Trace Length = 0.15 inch

Must place on top side

Place near GMCH

GMCH-MG Ver:A6
P/N:71.0GMCH.X0U

SM_RCOMP = 1/2 PCB impedance
DVO_RCOMP = PCB impedance
HUB_RCOMP = PCB impedance
AGP_RCOMP = PCB impedance
Almador checklist

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Project: GMCH (1/3)
Size: A3
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AGP_PAR	Pull-up 8.2K to 1.5VRUN	AGP device attached
	Pull-down 2.2K to GND	DVO device attached

Strapping Option for SW detection of AGP or DVO device

DVOA_D5 Int. P/D	0 = DESKTOP 1 = MOBILE	Pull-up 2.2K to V1.5S
DVOA_D6 Int. P/D	0 = Dual ended term. 1 = Single ended term.	Pull-up 2.2K to V1.5S
DVOA_D0 Int. P/U	0 = 200MHz 1 = 133MHz	Pull-down 2.2K to GND
DVOA_D1 Int. P/U	0 : IOQD = 1 1 : IOQD = 8	Pull-down 2.2K to GND
DVOA_D7 Int. P/D	0 : Normal mode 1 : Invoking the XOR Chain test mode	
DVOA_D8 Int. P/D	0 : Normal mode 1 : Tri-stating all GMCH outputs when ICH3-M is in XOR Chain mode.	

Per Intel GMCH EDS Rev0.7 12/22/2K

DVO_INTR#	Pull-up 100K to 1.5VRUN	Pull-up/down required if DVOA not implemented.
DVO_FIELD	Pull-down 100K to GND	
DVO_CLKIN	Pull-up 100K to 1.5VRUN	
DDC1CLK DDC1DAT	Pull-up 2.2K to +5VRUN	Non-5V tolerant, Q-Switch required for 5V support
DDC2CLK DDC2DAT	Pull-up 10K to +5VRUN	
I2CCLK I2CDATA	Pull-up 10K to +3VRUN	

U46D

U46C

GRAPH-U1
71.0GMCH.F0U

CRT

DVI

AGP,GPIO,SDVO,I2C,SMBUS MEMORY

GMCH Internal Swap

4.7K RDDP1.0 P.72

Be close to pin RDDP 1.0

9/13 per Intel

DVO port of GMCH is +1.5V Power plane

DVO port of VCH is +1.8V Power plane

Pull-up required for ext. AGP GFX and int. DVO GFX

Connect pin AE20, G24(VSSA_DPLL[0,1]) to the respective decoupling caps of pin AC20, F25(VCCA_DPLL[0,1])

4,5,6,8,10,13,15,27,29 1D5V_S0

4,8,10,13,15,29 1D8V_S0

3,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,25,27,28,29,31,35 3D3V_S0

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Project: GMCH (2/3)

Size: A3 | Document Number: Falcon 3M_1207 | Rev: -2

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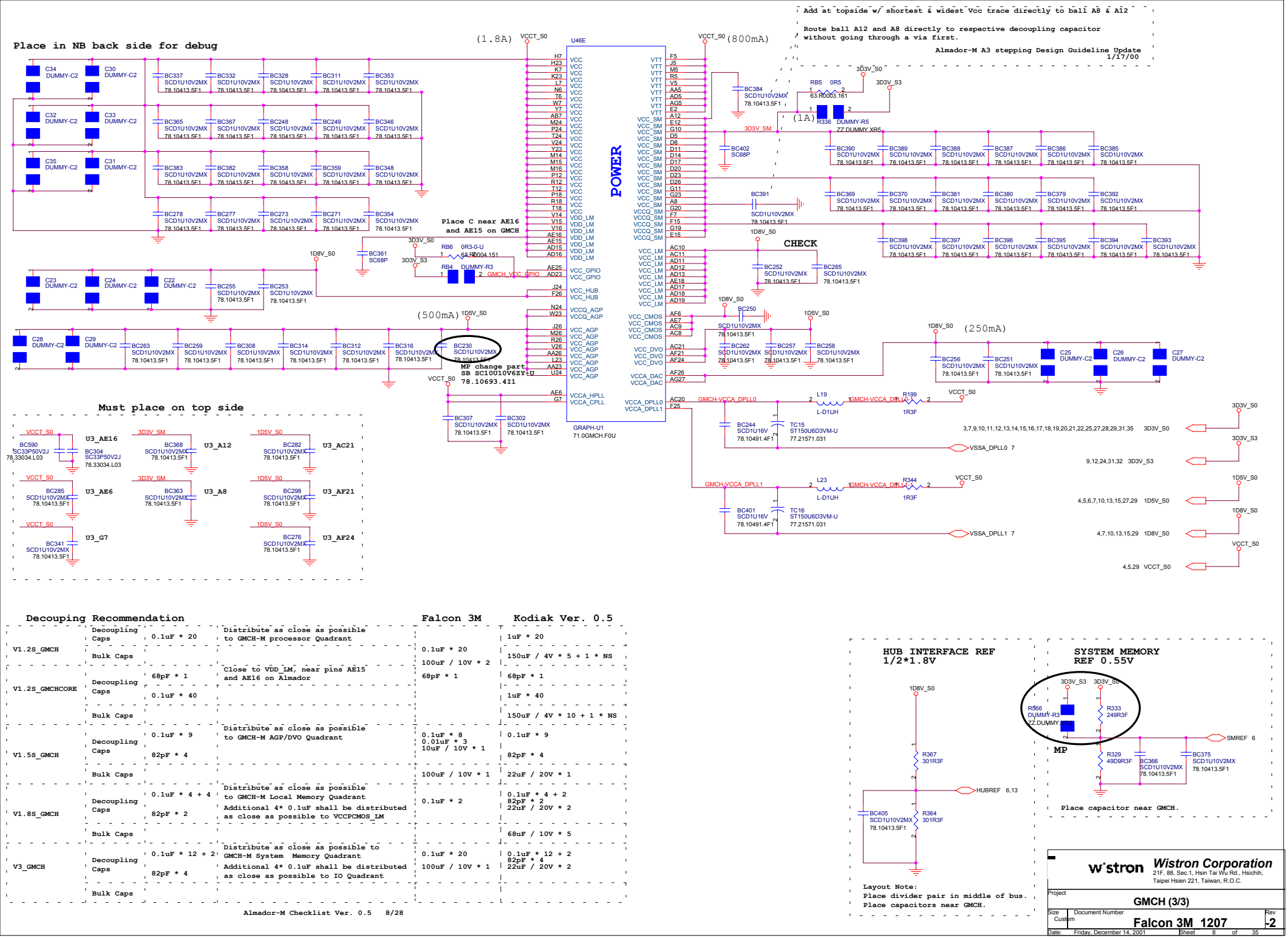

Decouping Recommendation

				Falcon 3M	Kodiak Ver. 0.5
V1.2S_GMCH	Decoupling Caps	0.1uF * 20	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20	1uF * 20
	Bulk Caps			100uF / 10V * 2	150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1 0.1uF * 40	Close to VDD_LM, near pins AE15 and AE16 on Almador	68pF * 1	68pF * 1 1uF * 40
	Bulk Caps				150uF / 4V * 10 + 1 * NS
V1.5S_GMCH	Decoupling Caps	0.1uF * 9 82pF * 4	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 8 0.01uF * 3 10uF / 10V * 1	0.1uF * 9 82pF * 4
	Bulk Caps			100uF / 10V * 1	22uF / 20V * 1
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 4 82pF * 2	Distribute as close as possible to GMCH-M Local Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to VCCPCMOS_LM	0.1uF * 2	0.1uF * 4 + 2 82pF * 2 22uF / 20V * 2
	Bulk Caps				68uF / 10V * 5
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2 82pF * 4	Distribute as close as possible to GMCH-M System Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant	0.1uF * 20 100uF / 10V * 1	0.1uF * 12 + 2 82pF * 4 22uF / 20V * 2
	Bulk Caps				

Almador-M Checklist Ver. 0.5 8/28

HUB INTERFACE REF 1/2*1.8V

Layout Note:
Place divider pair in middle of bus.
Place capacitors near GMCH.

SYSTEM MEMORY REF 0.55V

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Project: GMCH (3/3)
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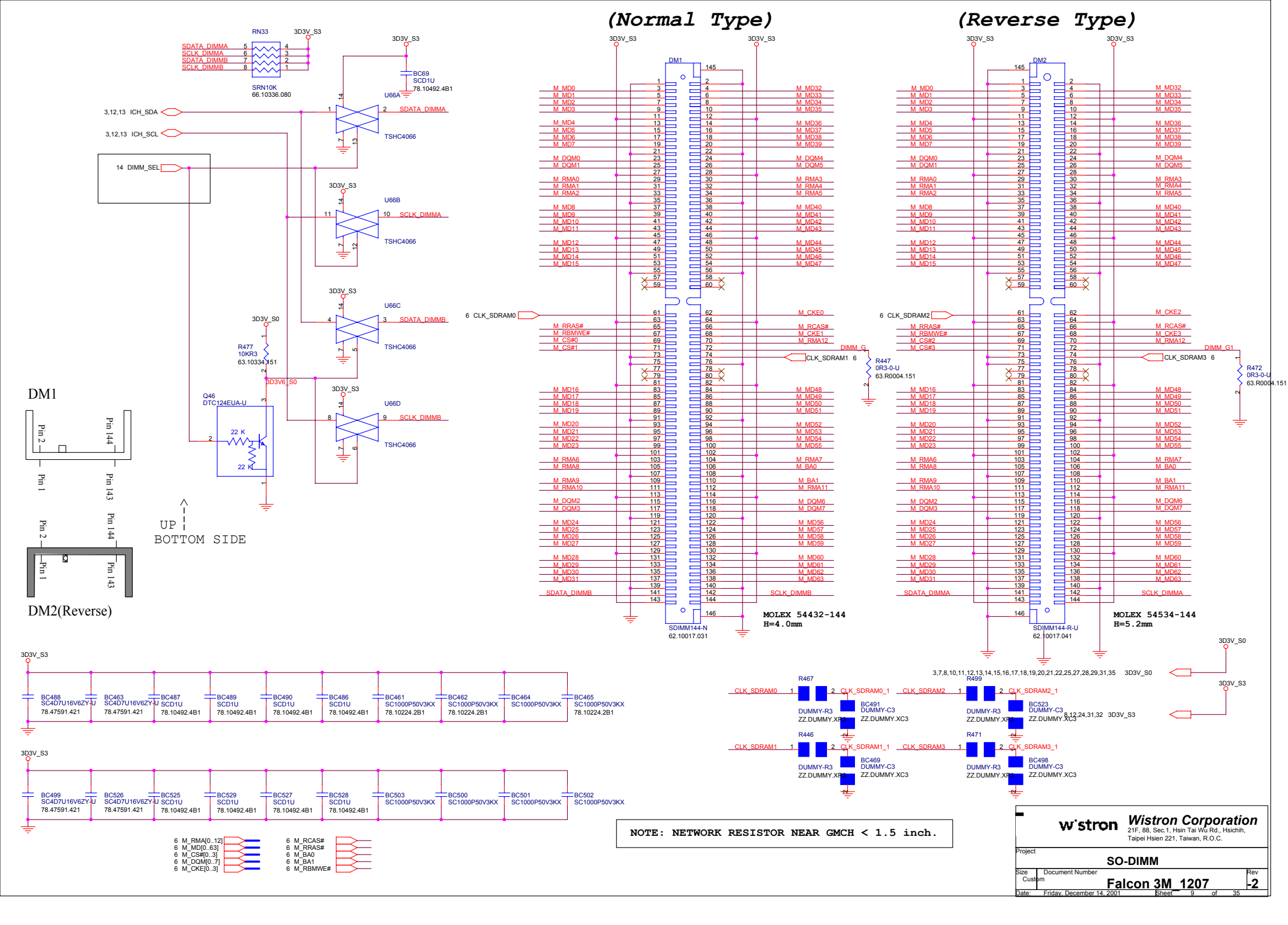
(Normal Type)
(Reverse Type)
RN33
SRN10K
66.10336.080
SDATA_DIMMA
SCLK_DIMMA
SDATA_DIMMB
SCLK_DIMMB
3D3V_S3
3D3V_S0
BC69
SCD1U
78.10492.4B1
U66A
U66B
U66C
U66D
TSHC4066
3,12,13 ICH_SDA
3,12,13 ICH_SCL
14 DIMM_SEL
R477
10KR3
63.10334.151
3D3V6_S0
Q46
DTC124EUA-U
22 K
DM1
DM2
Pin 2
Pin 144
Pin 1
Pin 143
UP
BOTTOM SIDE
DM1(Normal)
DM2(Reverse)
6 CLK_SDRAM0
CLK_SDRAM1 6
CLK_SDRAM2 6
CLK_SDRAM3 6
DIMM_G
R447
0R3-0-U
63.R0004.151
R472
63.R0004.151
M_MD0
M_MD1
M_MD2
M_MD3
M_MD4
M_MD5
M_MD6
M_MD7
M_DQM0
M_DQM1
M_RMA0
M_RMA1
M_RMA2
M_MD8
M_MD9
M_MD10
M_MD11
M_MD12
M_MD13
M_MD14
M_MD15
M_RRAS#
M_RBMWE#
M_CS#0
M_CS#1
M_CS#2
M_CS#3
M_MD16
M_MD17
M_MD18
M_MD19
M_MD20
M_MD21
M_MD22
M_MD23
M_RMA6
M_RMA8
M_RMA9
M_RMA10
M_DQM2
M_DQM3
M_MD24
M_MD25
M_MD26
M_MD27
M_MD28
M_MD29
M_MD30
M_MD31
SDATA_DIMMB
SDATA_DIMMA
M_MD32
M_MD33
M_MD34
M_MD35
M_MD36
M_MD37
M_MD38
M_MD39
M_DQM4
M_DQM5
M_RMA3
M_RMA4
M_RMA5
M_MD40
M_MD41
M_MD42
M_MD43
M_MD44
M_MD45
M_MD46
M_MD47
M_CKE0
M_CKE2
M_RCAS#
M_CKE1
M_CKE3
M_RMA12
M_MD48
M_MD49
M_MD50
M_MD51
M_MD52
M_MD53
M_MD54
M_MD55
M_RMA7
M_BA0
M_BA1
M_RMA11
M_DQM6
M_DQM7
M_MD56
M_MD57
M_MD58
M_MD59
M_MD60
M_MD61
M_MD62
M_MD63
SCLK_DIMMB
SCLK_DIMMA
SDIMM144-N
62.10017.031
SDIMM144-R-U
62.10017.041
MOLEX 54432-144
H=4.0mm
MOLEX 54534-144
H=5.2mm
3,7,8,10,11,12,13,14,15,16,17,18,19,20,21,22,25,27,28,29,31,35 3D3V_S0
8,12,24,31,32 3D3V_S3
R467
R446
R499
R471
CLK_SDRAM0
CLK_SDRAM1
CLK_SDRAM2
CLK_SDRAM3
CLK_SDRAM0_1
CLK_SDRAM1_1
CLK_SDRAM2_1
CLK_SDRAM3_1
DUMMY-R3
ZZ.DUMMY.XR3
BC491
BC469
BC523
BC498
DUMMY-C3
ZZ.DUMMY.XC3
BC488 SC4D7U16V6ZY-U 78.47591.421
BC463 SC4D7U16V6ZY-U 78.47591.421
BC487 SCD1U 78.10492.4B1
BC489 SCD1U 78.10492.4B1
BC490 SCD1U 78.10492.4B1
BC486 SCD1U 78.10492.4B1
BC461 SC1000P50V3KX 78.10224.2B1
BC462 SC1000P50V3KX 78.10224.2B1
BC464 SC1000P50V3KX
BC465 SC1000P50V3KX 78.10224.2B1
BC499 SC4D7U16V6ZY-U 78.47591.421
BC526 SC4D7U16V6ZY-U 78.47591.421
BC525 SCD1U 78.10492.4B1
BC529 SCD1U 78.10492.4B1
BC527 SCD1U 78.10492.4B1
BC528 SCD1U 78.10492.4B1
BC503 SC1000P50V3KX
BC500 SC1000P50V3KX
BC501 SC1000P50V3KX
BC502 SC1000P50V3KX
6 M_RMA[0..12]
6 M_MD[0..63]
6 M_CS#[0..3]
6 M_DQM[0..7]
6 M_CKE[0..3]
6 M_RCAS#
6 M_RRAS#
6 M_BA0
6 M_BA1
6 M_RBMWE#
NOTE: NETWORK RESISTOR NEAR GMCH < 1.5 inch.
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Project
SO-DIMM
Size
Custom
Document Number
Falcon 3M_1207
Rev
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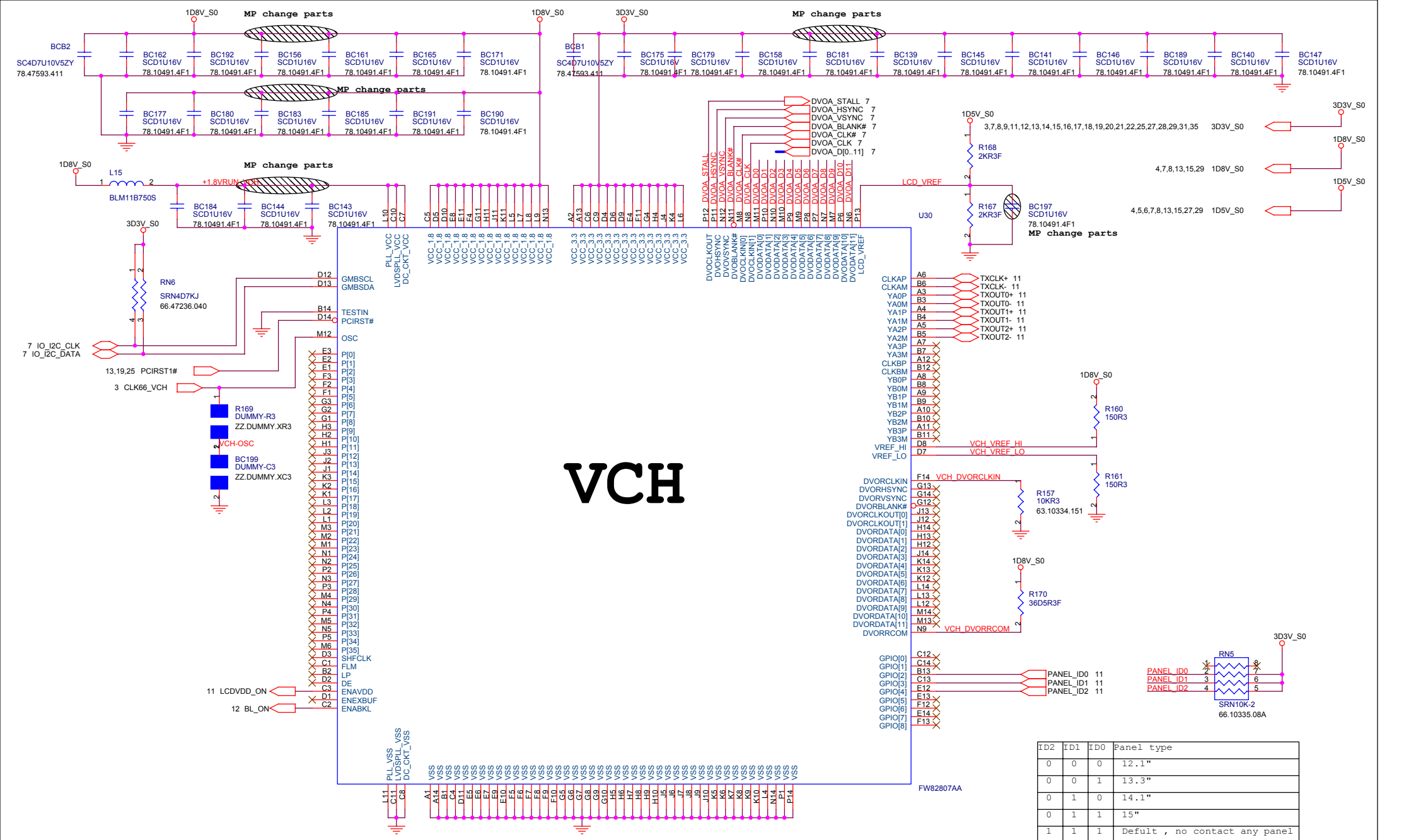

ID2	ID1	ID0	Panel type
0	0	0	12.1"
0	0	1	13.3"
0	1	0	14.1"
0	1	1	15"
1	1	1	Defult , no contact any panel

Strapping Options

GPIO[5:2]	10 - 4.7K Ohm	Can be used for panel ID select. Default state is GPI w/ int. weak pull down.
GPIO6	10 - 4.7K Ohm	For normal VCH operation pin has to be read as low. Default state is GPI w/ int. weak pull down.
GPIO[8:7]	10 - 4.7K Ohm	Used for GMBus base address select. Default state is GPI w/ int. weak pull down.

Almador check ver.0.5

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Project: VCH

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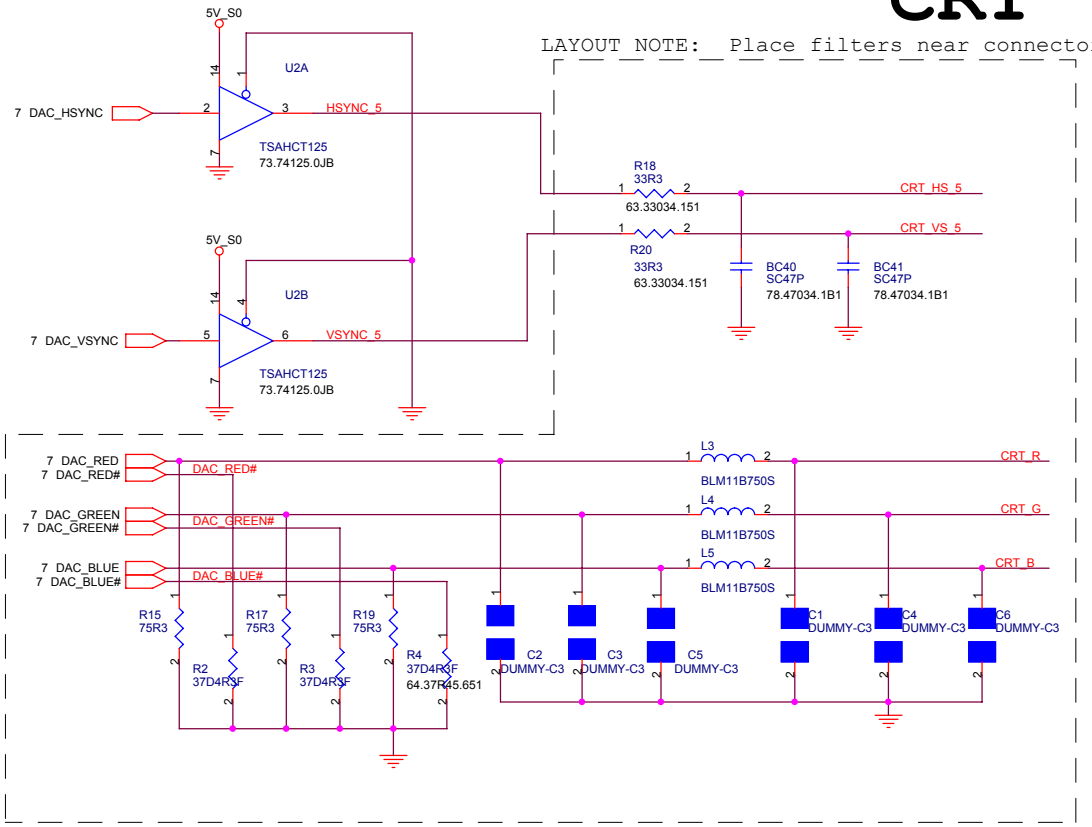
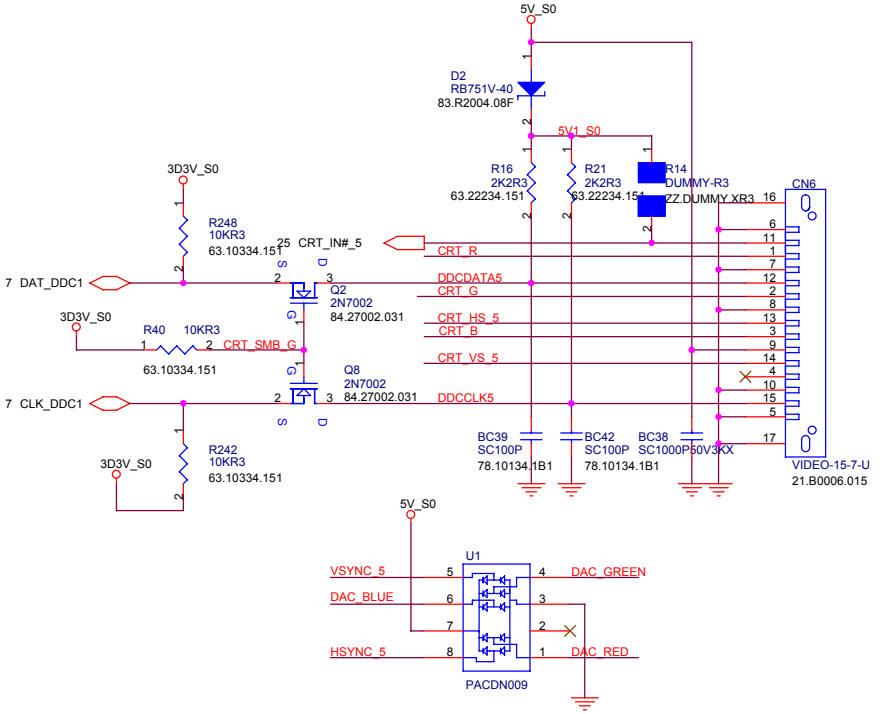
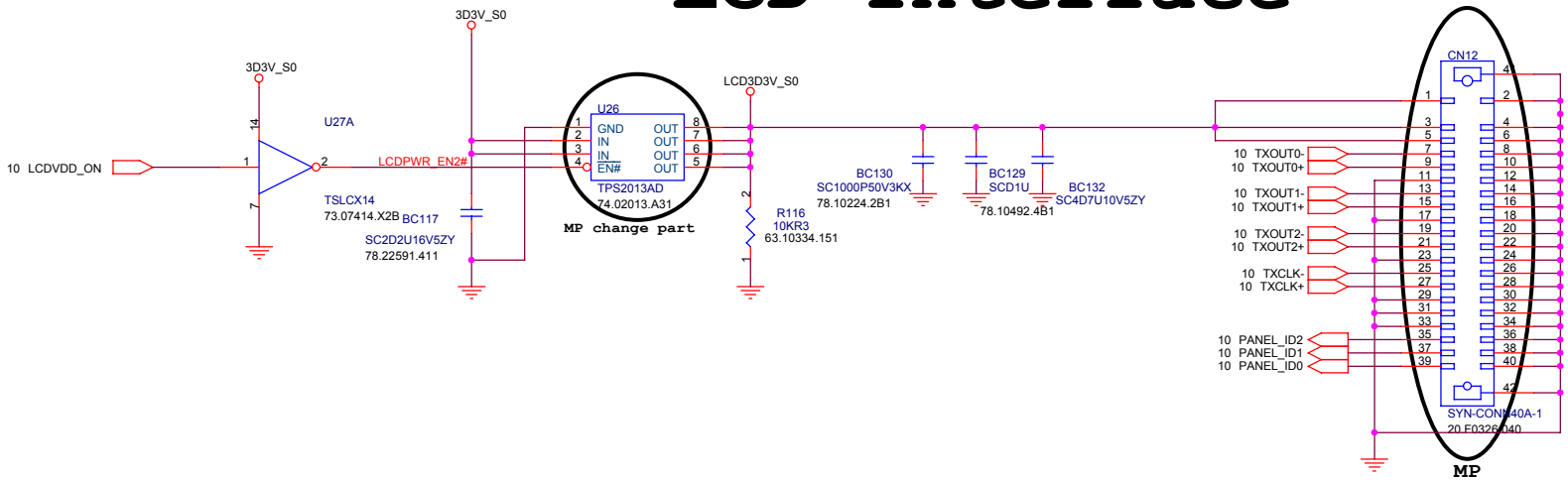
CRT

LAYOUT NOTE: Place filters near connector.





LCD Interface



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Project	CRT& LVDS	
Size A3	Document Number Falcon 3M_1207	Rev -2
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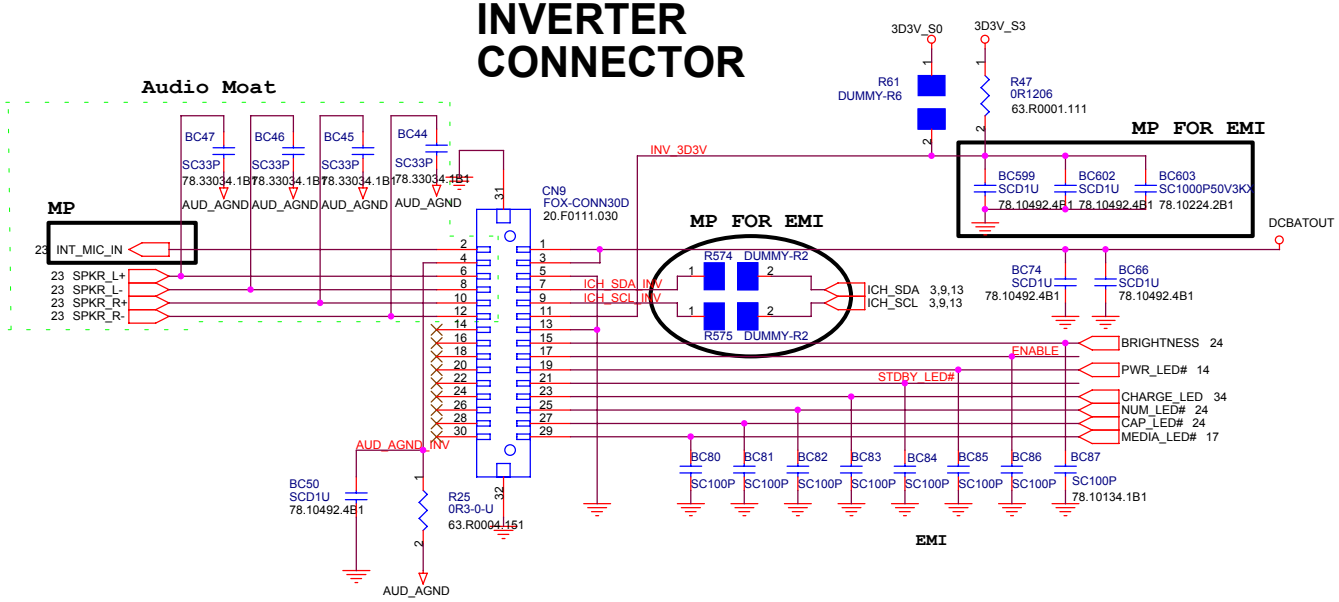
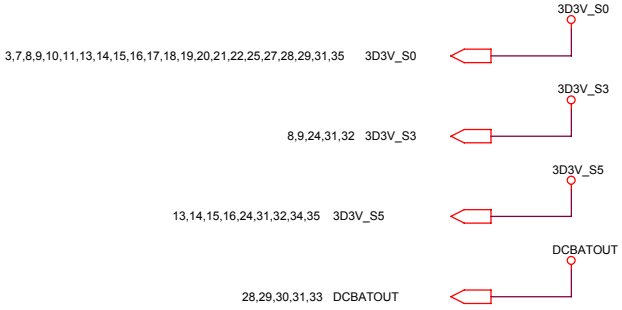
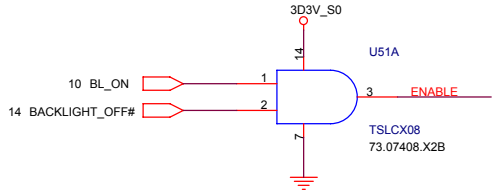
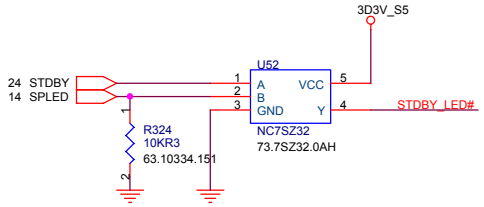
INVERTER CONNECTOR



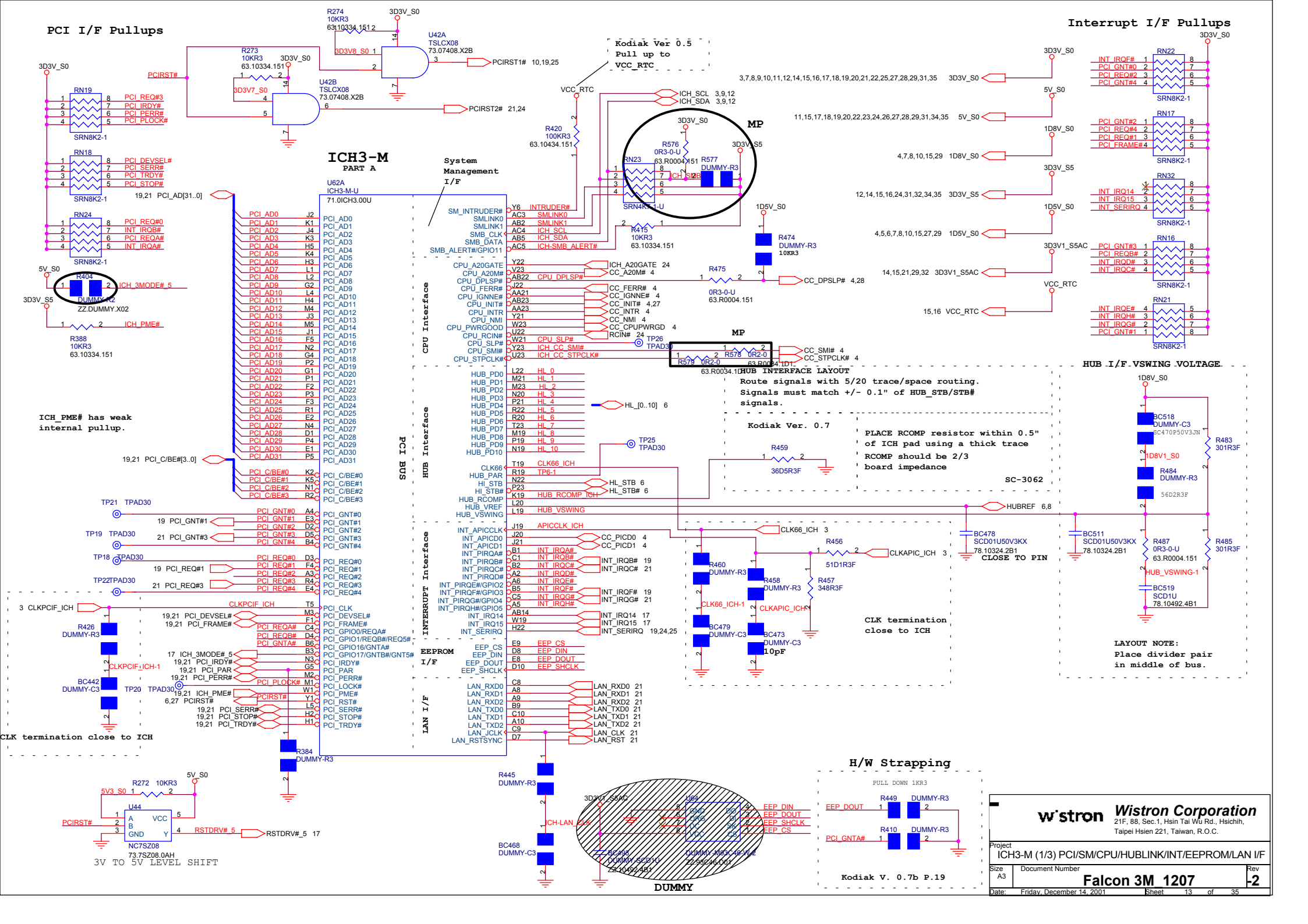


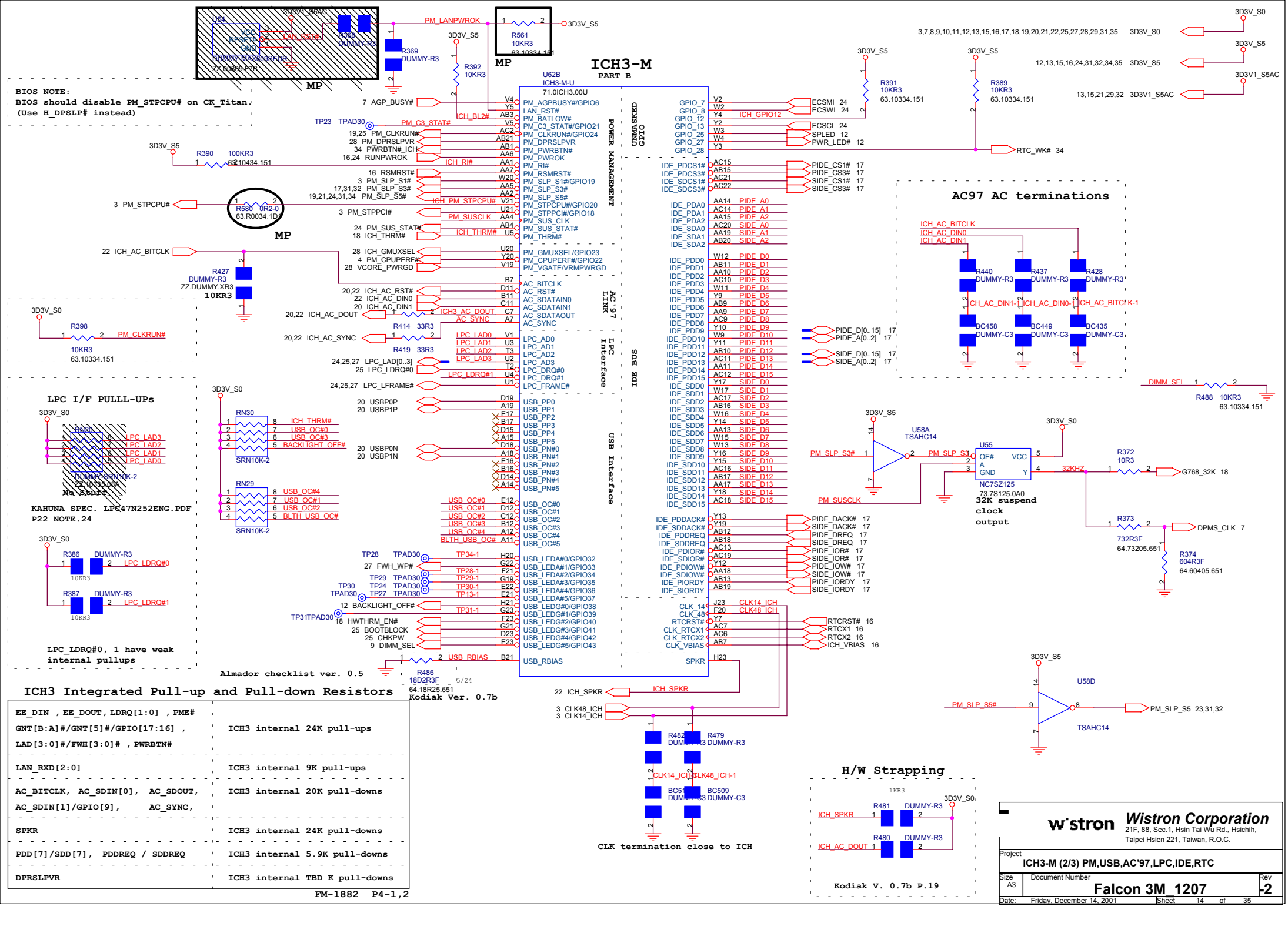


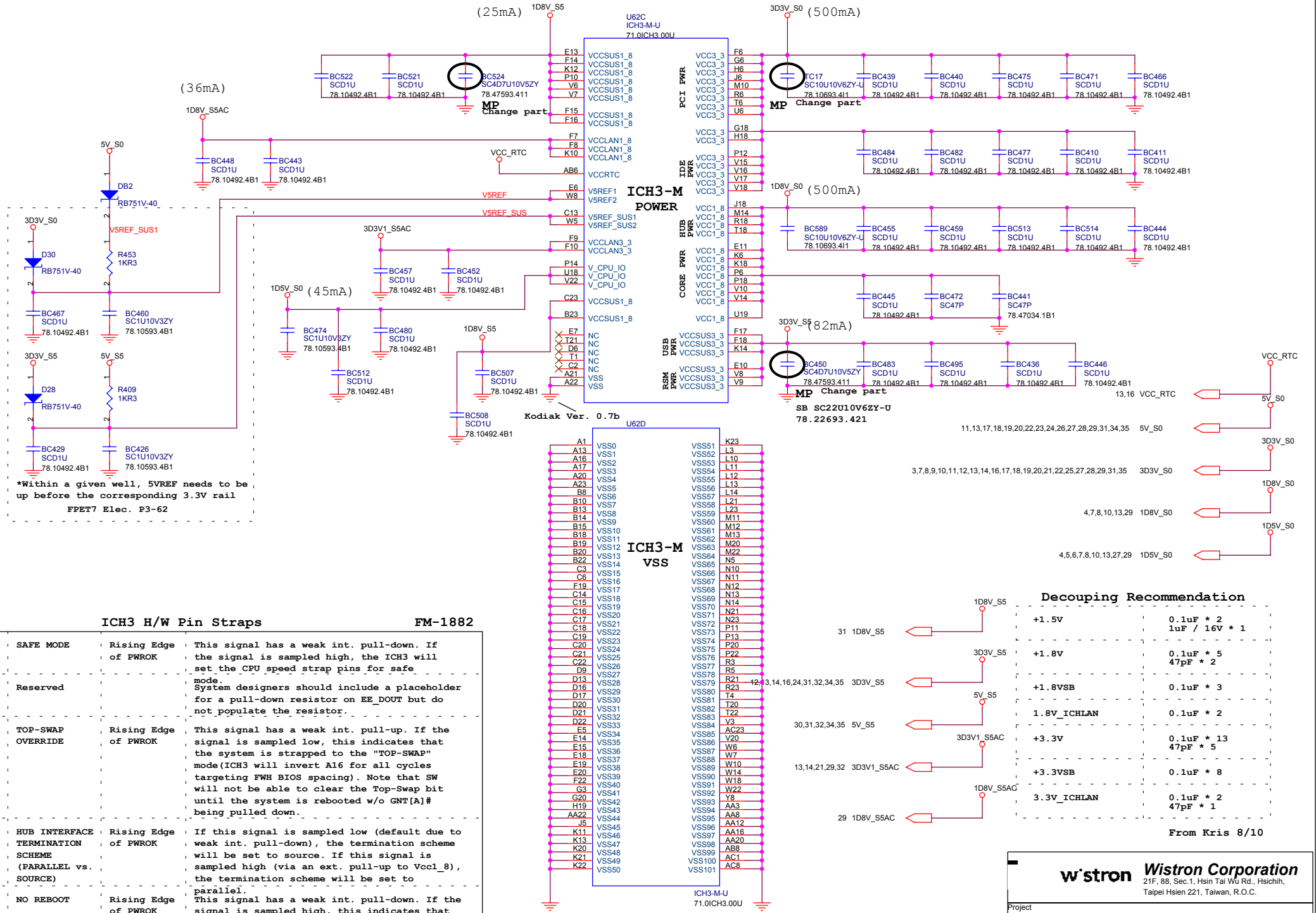


Power Plane	S5	S5	S5	S0	S5	S3	S5	S5		
Control Signal	PM_SLP_S5#	PM_SLP_S3#	PM_SLP_S1#	EMAIL_LED	STDBY	SPLED	STDBY_LED		Standby_LED	E_mail_LED
POWER ON DFAULT	H	H	H	X	H	H	L		OFF	None
S0	H	H	H	X	H	H	L		OFF	None
S1	H	H	L	X	L	L	L		ON	None
Enter/Leave S3	H	H	L	X	L	L	L		ON	None
S3	H	L	L	X	L	L	L		ON	None
Enter/Leave S4	H	L	L	X	L	Flash	FLASH		Flash	None
S4/S5	H	L	L	X	H	FLASH	L		OFF	None

wistron	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Project	**Inverter**	
Size A3	Document Number **Falcon 3M_1207**	Rev -2
Date: Friday, December 14, 2001	Sheet 12 of 35	


PCI I/F Pullups
Interrupt I/F Pullups
ICH3-M
PART A
System Management I/F
Kodiak Ver 0.5 Pull up to VCC_RTC
MP
CPU Interface
HUB Interface
PCI BUS
INTERRUPT Interface
EEPROM I/F
LAN I/F
HUB INTERFACE LAYOUT
Route signals with 5/20 trace/space routing.
Signals must match +/- 0.1" of HUB_STB/STB# signals.
Kodiak Ver. 0.7
PLACE RCOMP resistor within 0.5" of ICH pad using a thick trace
RCOMP should be 2/3 board impedance
SC-3062
HUB_I/F_VSWING_VOLTAGE
ICH_PME# has weak internal pullup.
CLK termination close to ICH
CLOSE TO PIN
LAYOUT NOTE: Place divider pair in middle of bus.
H/W Strapping
3V TO 5V LEVEL SHIFT
DUMMY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Project
ICH3-M (1/3) PCI/SM/CPU/HUBLINK/INT/EEPROM/LAN I/F
Size A3
Document Number
Falcon 3M_1207
Rev -2
Date: Friday, December 14, 2001
Sheet 13 of 35


BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan
(Use H_DPSLP# instead)
ICH3-M
PART B
U62B
ICH3-M-U
71.0ICH3.00U
POWER MANAGEMENT
UNMASKED GPIO
AC'97 LINK
LPC Interface
IDE BUS
USB Interface
AC97 AC terminations
LPC I/F PULLL-UPs
KAHUNA SPEC. LPC47N252ENG.PDF
P22 NOTE.24
LPC_LDRQ#0, 1 have weak
internal pullups
Almador checklist ver. 0.5
ICH3 Integrated Pull-up and Pull-down Resistors
EE_DIN , EE_DOUT, LDRQ[1:0] , PME#
GNT[B:A]#/GNT[5]#/GPIO[17:16] ,
LAD[3:0]#/FWH[3:0]# , PWRBTN#
ICH3 internal 24K pull-ups
LAN_RXD[2:0]
ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT,
AC_SDIN[1]/GPIO[9], AC_SYNC,
ICH3 internal 20K pull-downs
SPKR
ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ
ICH3 internal 5.9K pull-downs
DPRSLPVR
ICH3 internal TBD K pull-downs
FM-1882 P4-1,2
Kodiak Ver. 0.7b
CLK termination close to ICH
H/W Strapping
Kodiak V. 0.7b P.19
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Project
ICH3-M (2/3) PM,USB,AC'97,LPC,IDE,RTC
Size A3
Document Number
Falcon 3M_1207
Rev -2
Date: Friday, December 14, 2001
Sheet 14 of 35



Decouping Recommendation

+1.5V	0.1uF * 2 1uF / 16V * 1
+1.8V	0.1uF * 5 47pF * 2
+1.8VSB	0.1uF * 3
1.8V_ICHLAN	0.1uF * 2
+3.3V	0.1uF * 13 47pF * 5
+3.3VSB	0.1uF * 8
3.3V_ICHLAN	0.1uF * 2 47pF * 1

From Kris 8/10

ICH3 H/W Pin Straps FM-1882

AC_SDOUT	SAFE MODE	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A]#	TOP-SWAP OVERRIDE	Rising Edge of PWROK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode(ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWROK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot " mode (ICH3 will disable the TXO Timer system reboot feature).

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Project: ICH3-M (3/3) PCI/SM/CPU/HUBLINK/INT/EEPROM/LAN I/F

Size: A3 | Document Number: Falcon 3M_1207 | Rev: -2

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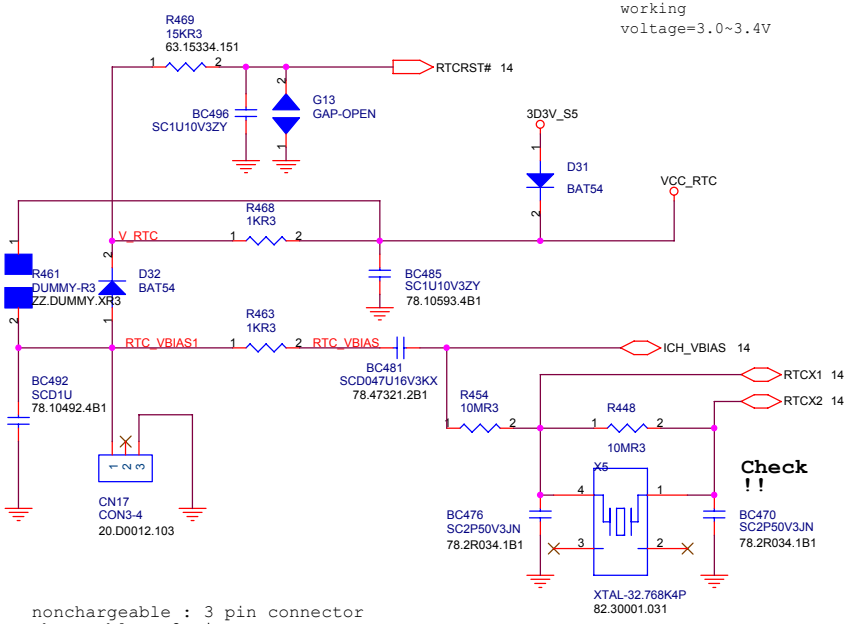
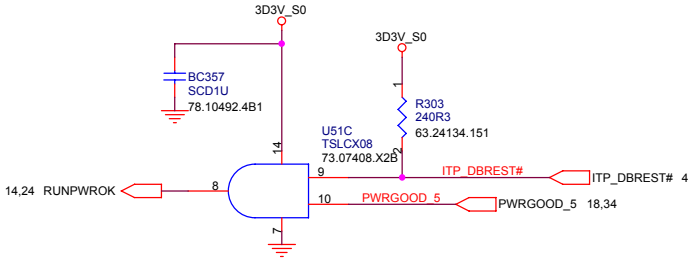
RTC

RTC BATTERY:210mAH
P/N ??.20023.121
working
voltage=3.0~3.4V

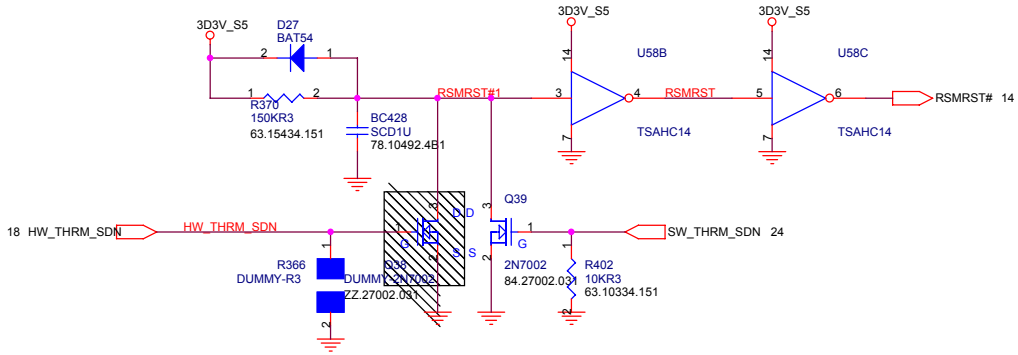


nonchargeable : 3 pin connector
chargeable : 2 pin connector

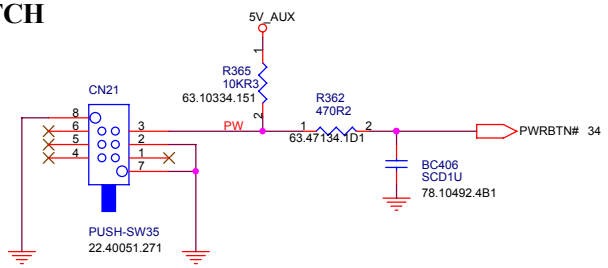
PWRGOOD Sequence

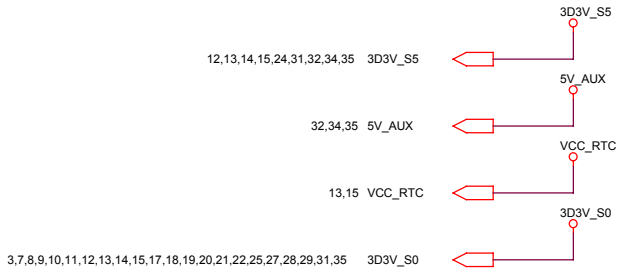


ICH3 Resume Well Reset



POWER SWITCH





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Taipei Hsien 221, Taiwan, R.O.C.

Project	RTC/Power Sequence	
Size A3	Document Number Falcon 3M_1207	Rev -2
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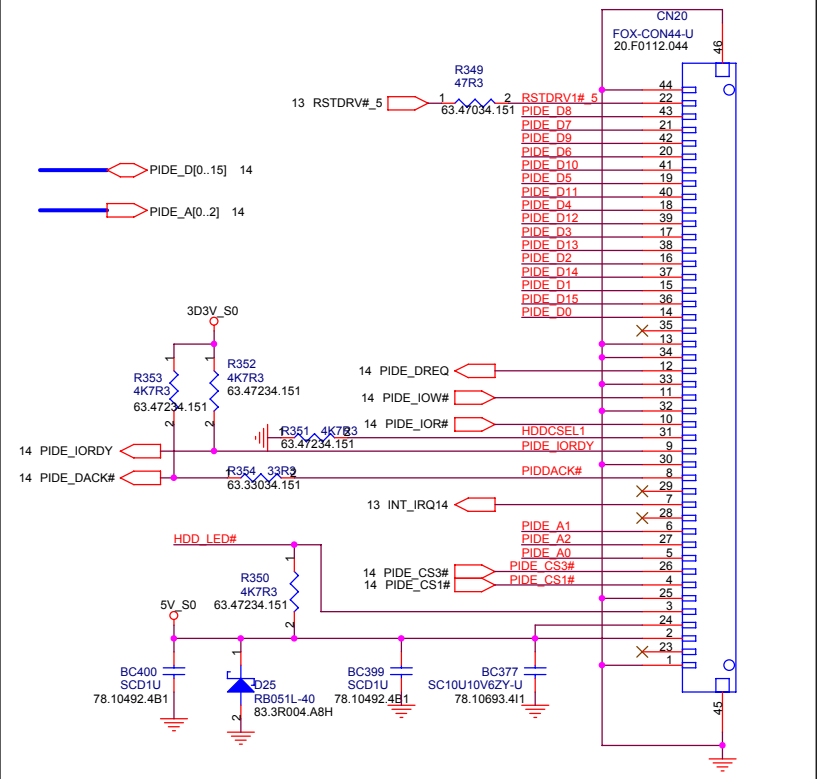
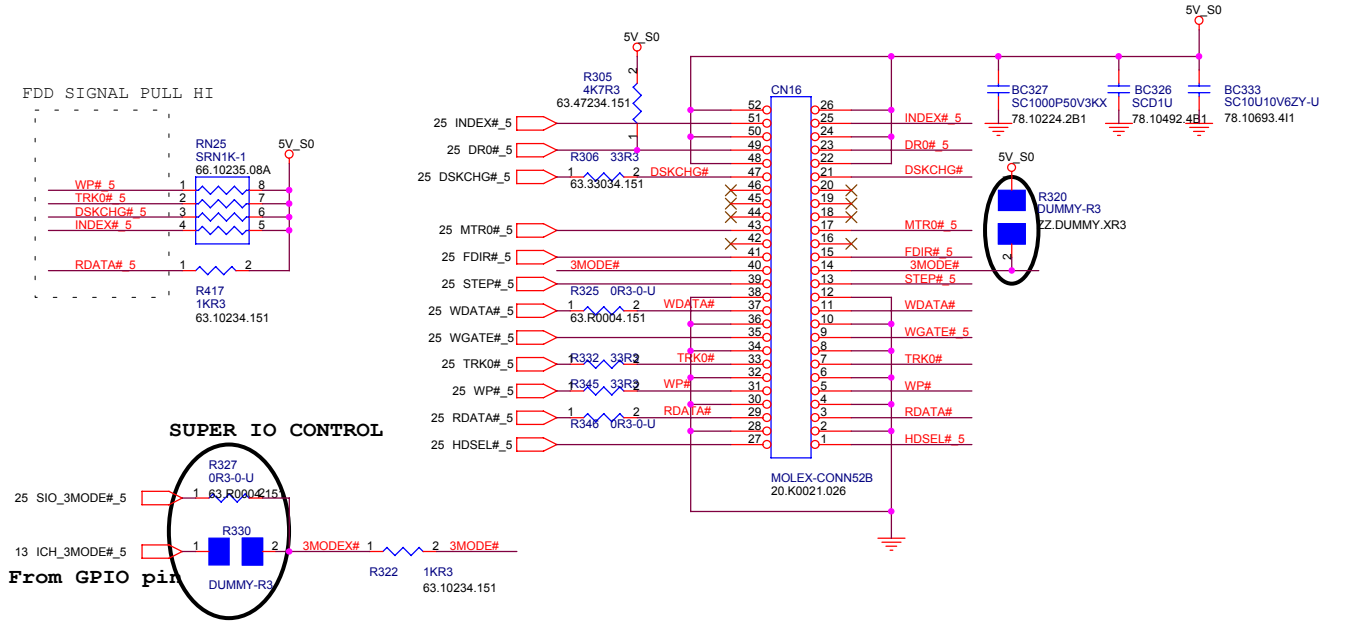
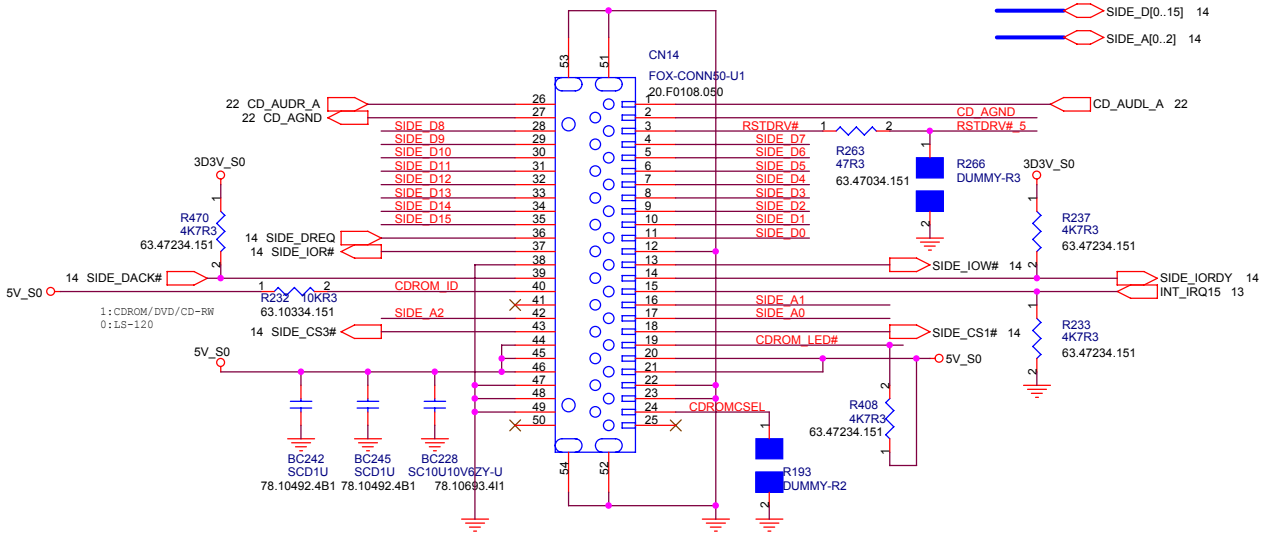
HDD Connector

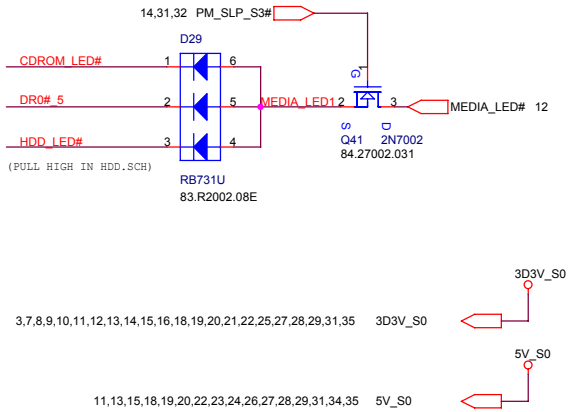


FDD Connector



CD-ROM Connector





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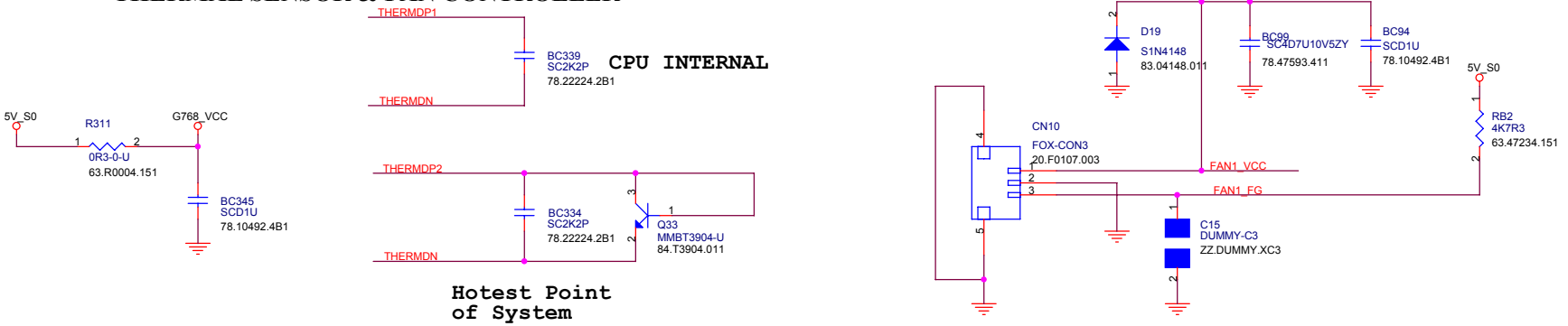
Taipei Hsien 221, Taiwan, R.O.C.

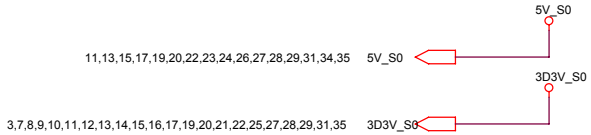
Project: HDD_CD-ROM_FDD

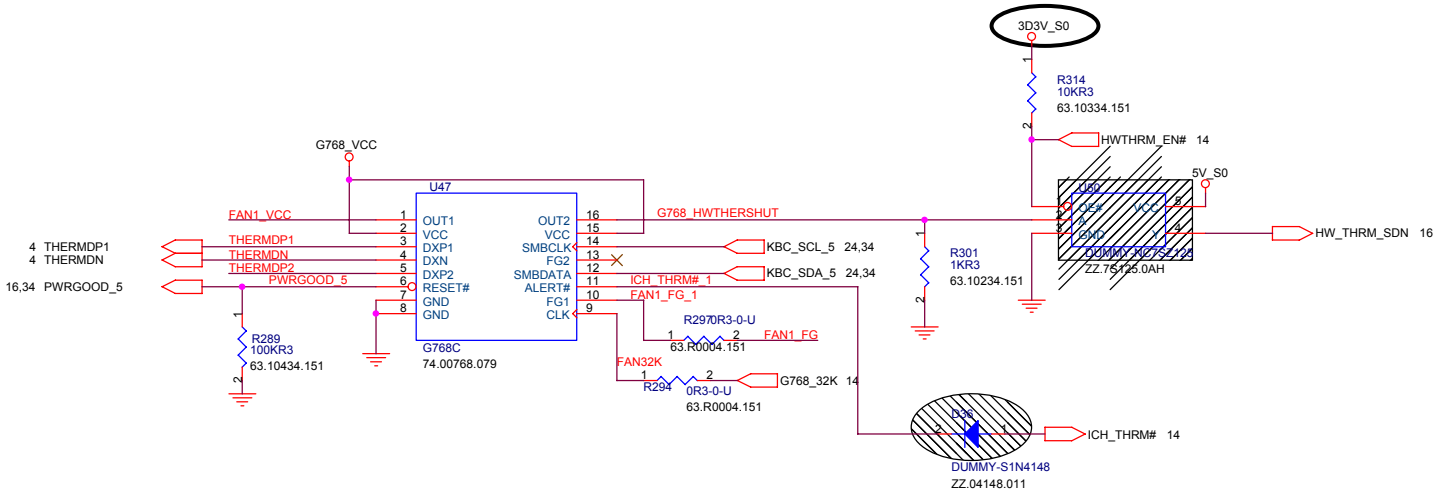
Size: A3 | Document Number: Falcon 3M_1207 | Rev: -2

Date: Friday, December 14, 2001 | Sheet 17 of 35

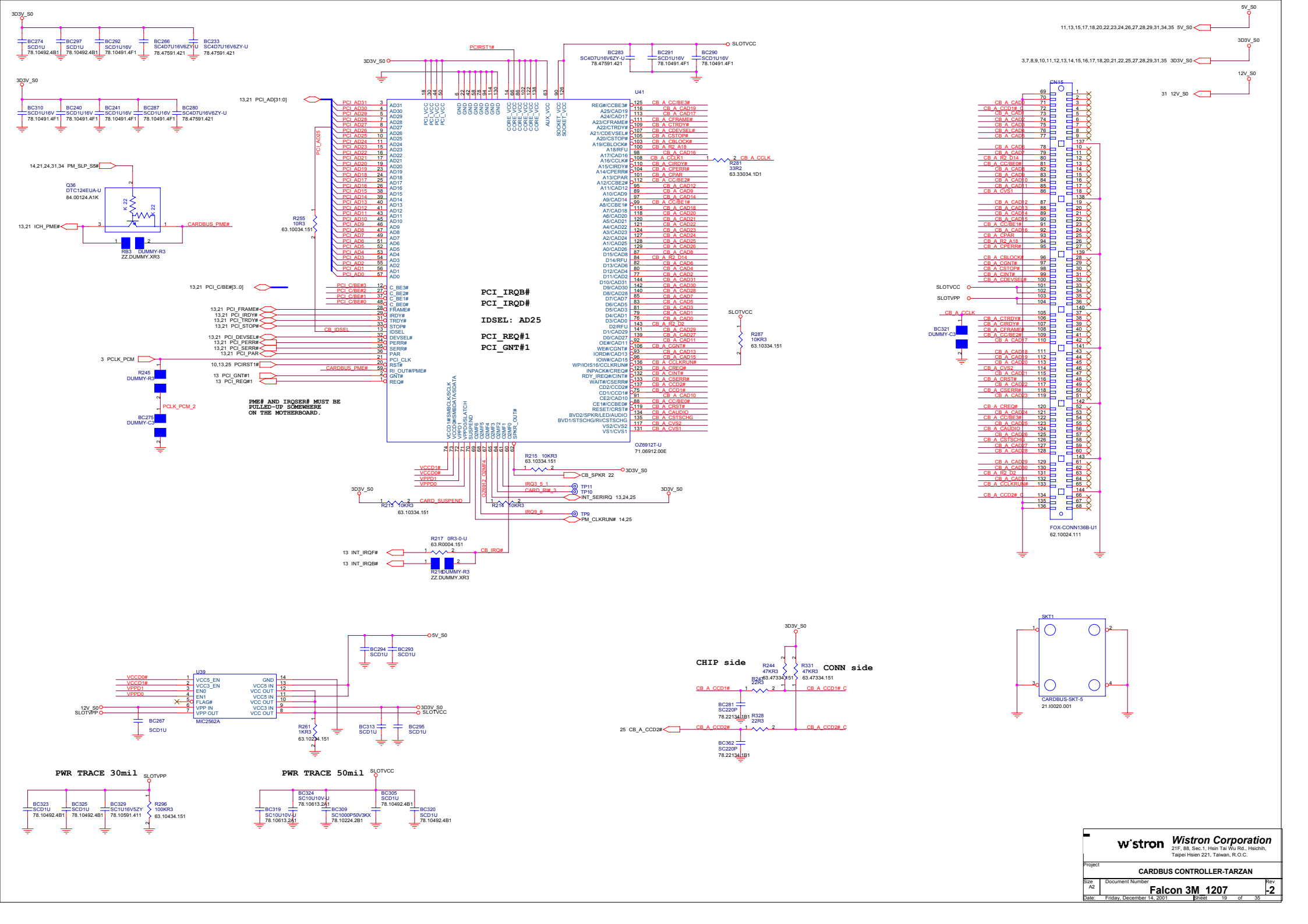
THERMAL SENSOR & FAN CONTROLLER







Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Project: Thermal Sensor		
Size: A3	Document Number: Falcon 3M_1207	Rev: -2
Date: Friday, December 14, 2001	Sheet 18 of 35	


PCI_IRQB#
PCI_IRQD#
IDSEL: AD25
PCI_REQ#1
PCI_GNT#1
PME# AND IRQSER# MUST BE PULLED-UP SOMEWHERE ON THE MOTHERBOARD.
CHIP side
CONN side
PWR TRACE 30mil
PWR TRACE 50mil
U41
OZ6912T-U
71.06912.00E
U39
MIC2562A
CN15
FOX-CONN136B-U1
62.10024.111
SKT1
CARDBUS-SKT-5
21.I0020.001
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Project
CARDBUS CONTROLLER-TARZAN
Size A2
Document Number
Falcon 3M_1207
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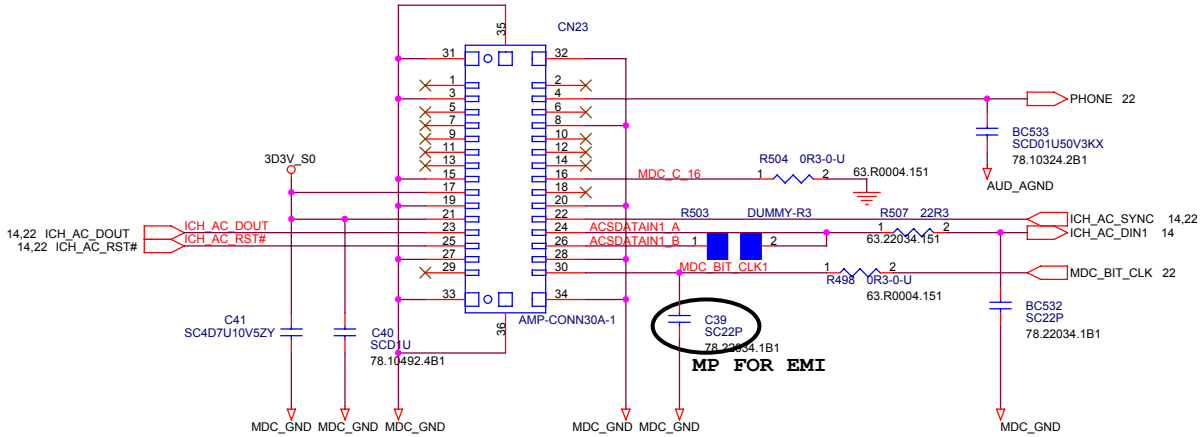
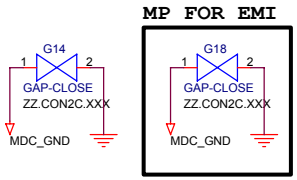
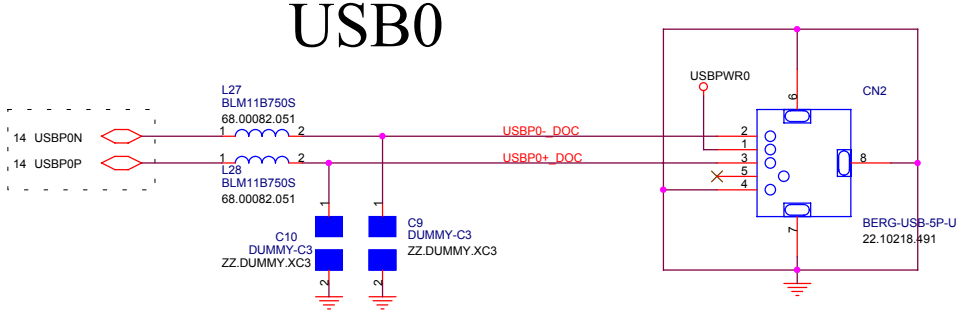
Date: Friday, December 14, 2001
Sheet 19 of 35

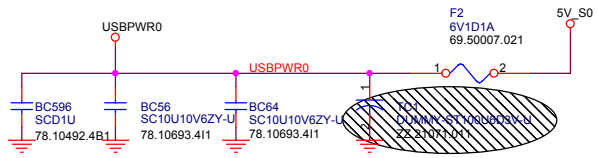
MODEM BOARD CONNECTOR



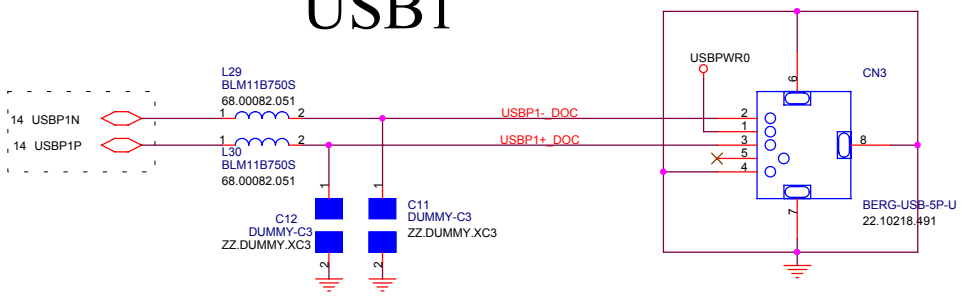


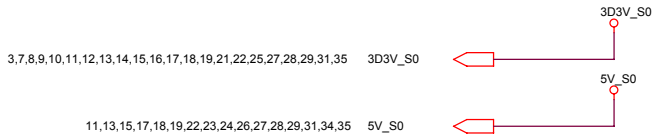
USB0





USB1





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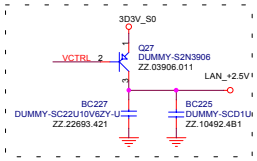
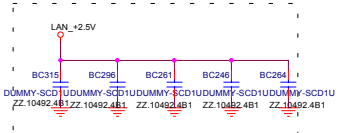
Taipei Hsien 221, Taiwan, R.O.C.

Project	MODEM / USB	
Size A3	Document Number Falcon 3M_1207	Rev -2
Date: Friday, December 14, 2001	Sheet 20 of 35	

REALTEK LAN SOLUTION



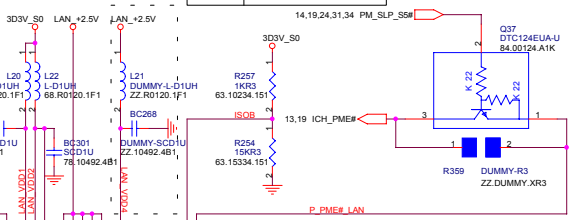
The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.

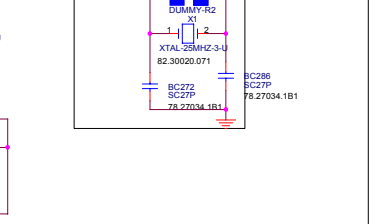


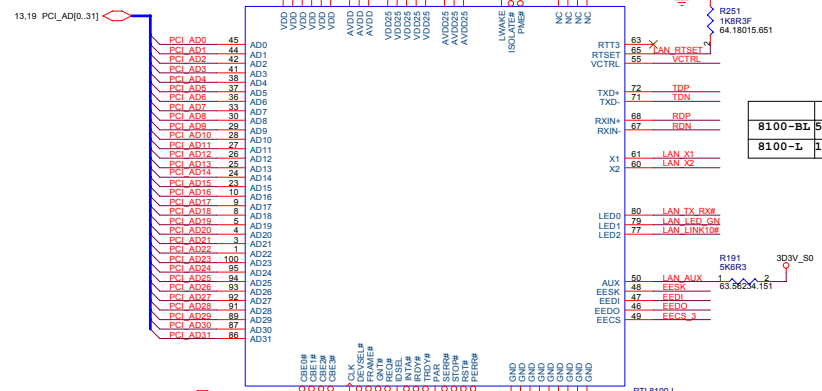
The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.

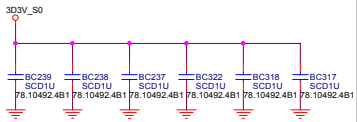
LWAKE	PCI 2.1
PME#	PCI 2.2 (ACPI)

100ohm @100MHz

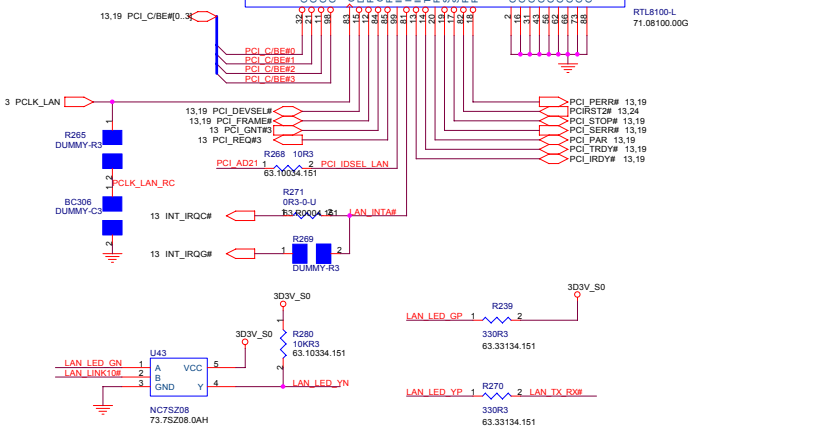






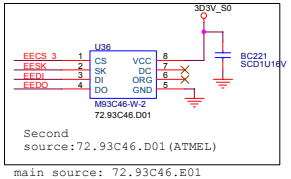


	R251	BC60	R556
8100-BL	5.9K ohm	No STUFF	No STUFF
8100-L	1.8K ohm	1000P	0 ohm



LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX
LED1	LINK100	LINK10/100	LINK10/100	LINK100
LED2	LINK10	FULL	RX	LINK10

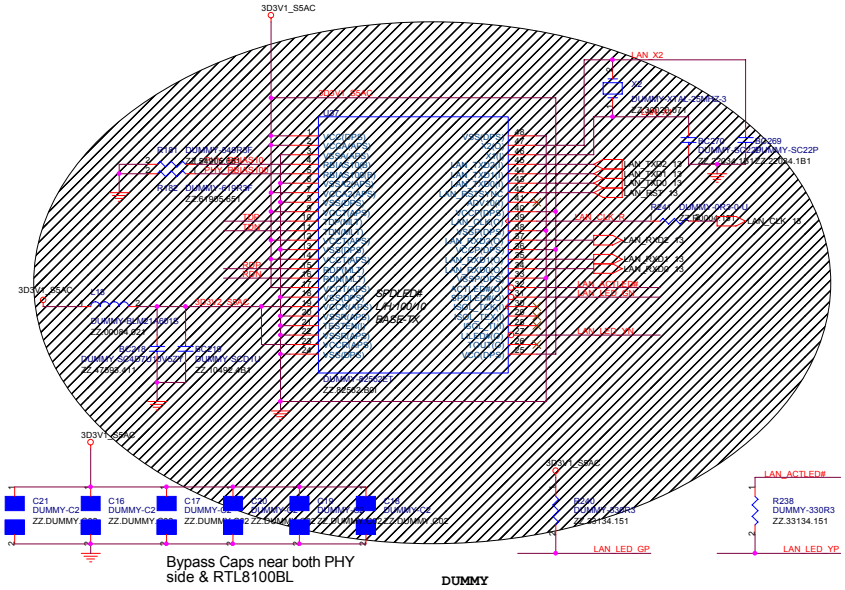
Green LED:Speed 100: ON/Speed 10:OFF
Yellow LED:Link : ON, TX/RX: Flash(10Hz)



Second source:72.93C46.D01(ATMEL)

main source: 72.93C46.E01

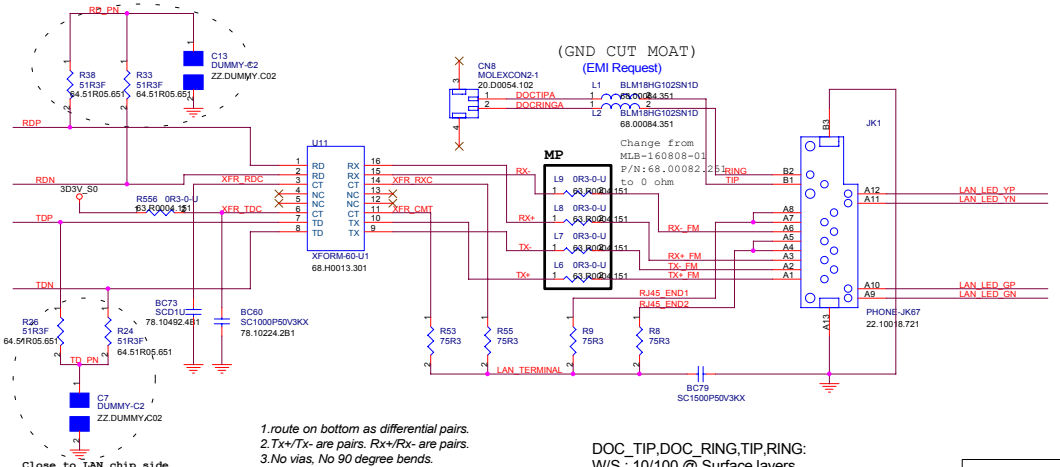
INTEL LAN SOUTION



Bypass Caps near both PHY side & RTL8100BL

DUMMY

Use 50 ohm trace
R559 R560 R561 R562 close to 82562



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

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Project: LAN RTL-8100-L & RJ45/11

Size: A2 | Document Number: Falcon 3M_1207 | Rev: -2

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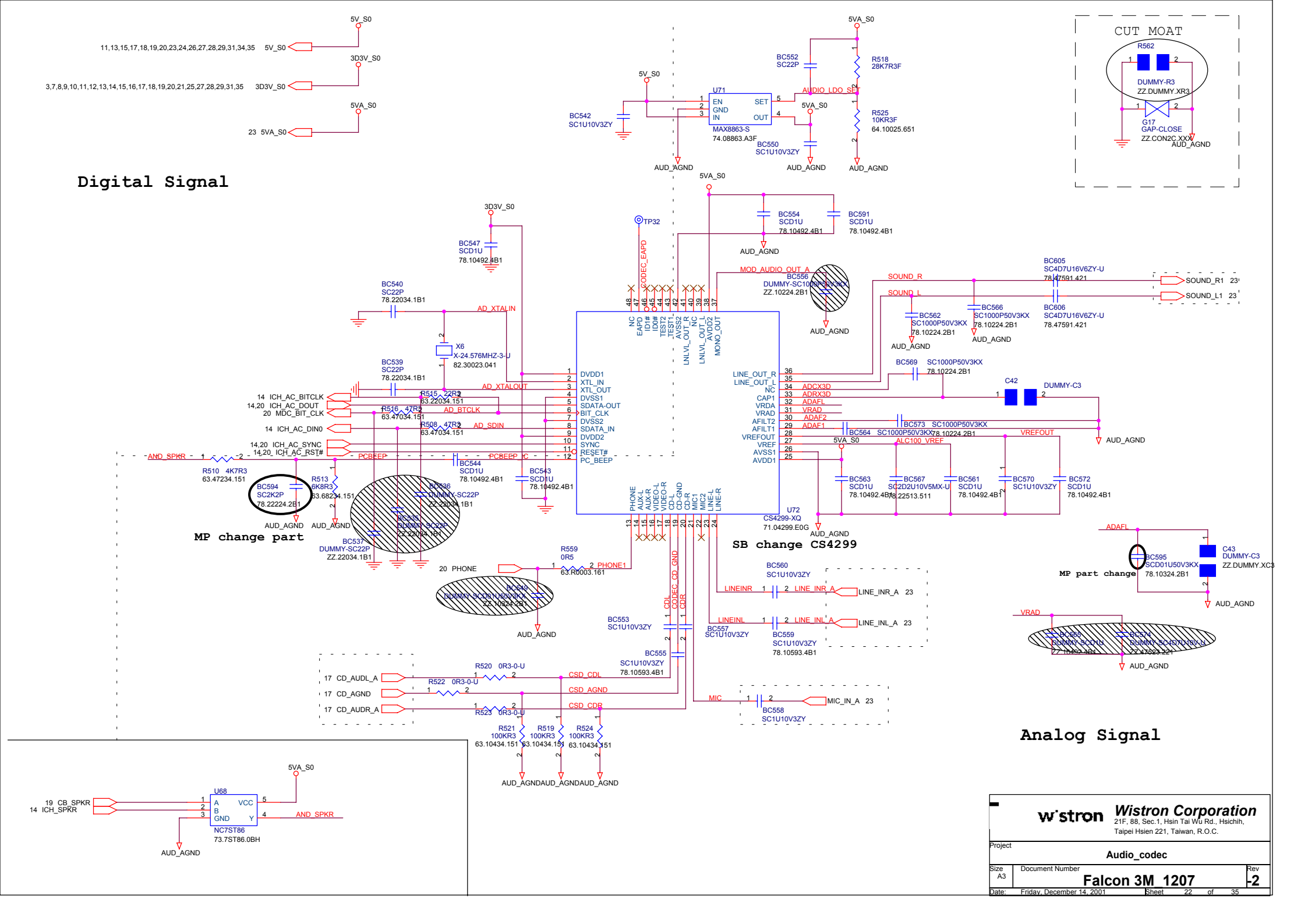
Digital Signal
Analog Signal
MP change part
SB change CS4299
MP part change
CUT MOAT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Project
Audio_codec
Size A3
Document Number
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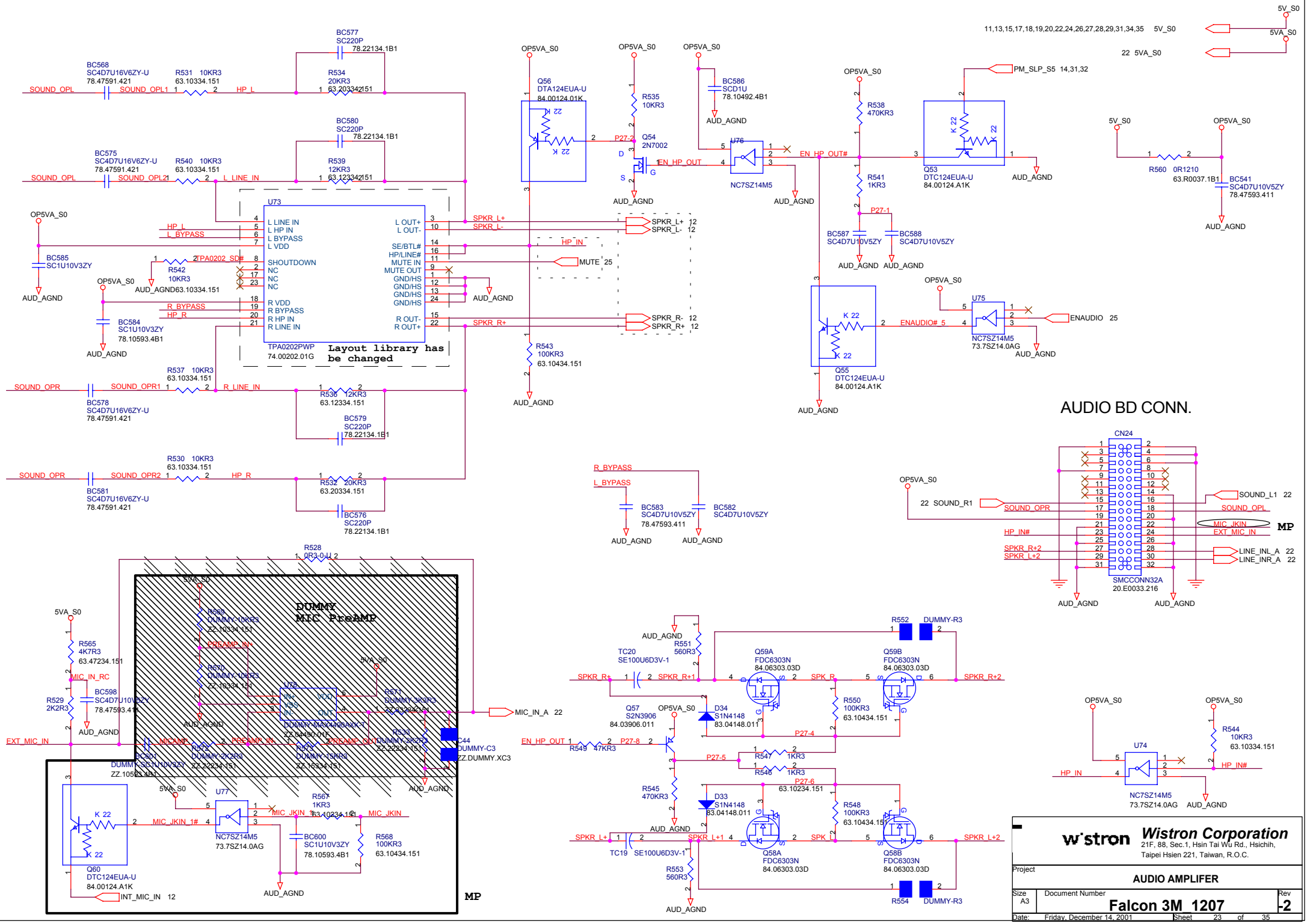
AUDIO BD CONN.
U73
TPA0202PWP
74.00202.01G
Layout library has be changed
DUMMY
MIC PreAMP
MP
MP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Project
AUDIO AMPLIFER
Size
A3
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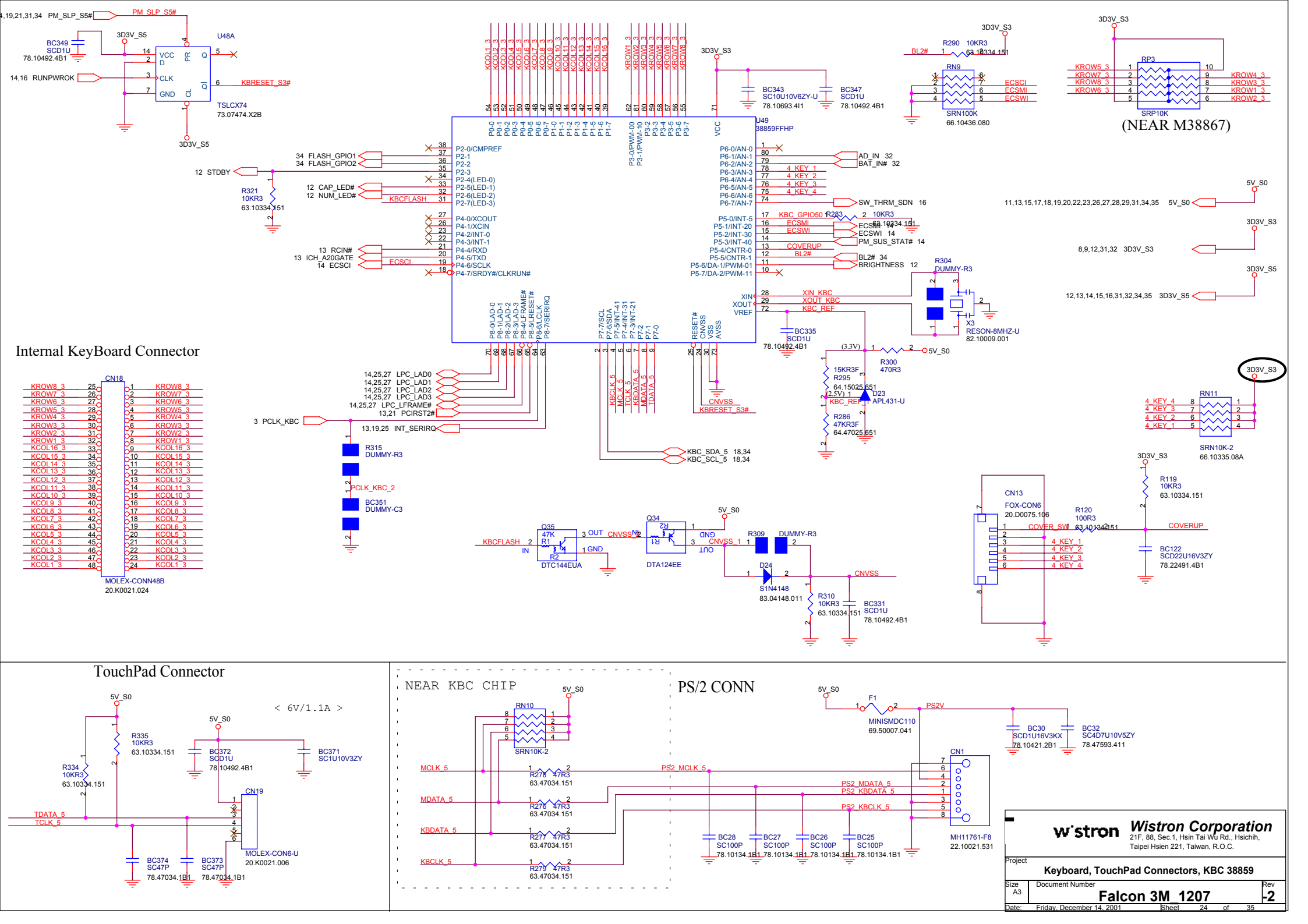
Internal KeyBoard Connector
TouchPad Connector
NEAR KBC CHIP
PS/2 CONN
(NEAR M38867)
U49
38859FFHP
CN18
MOLEX-CONN48B
20.K0021.024
CN19
MOLEX-CON6-U
20.K0021.006
CN13
FOX-CON6
20.D0075.106
CN1
MH11761-F8
22.10021.531
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Project
Keyboard, TouchPad Connectors, KBC 38859
Size
A3
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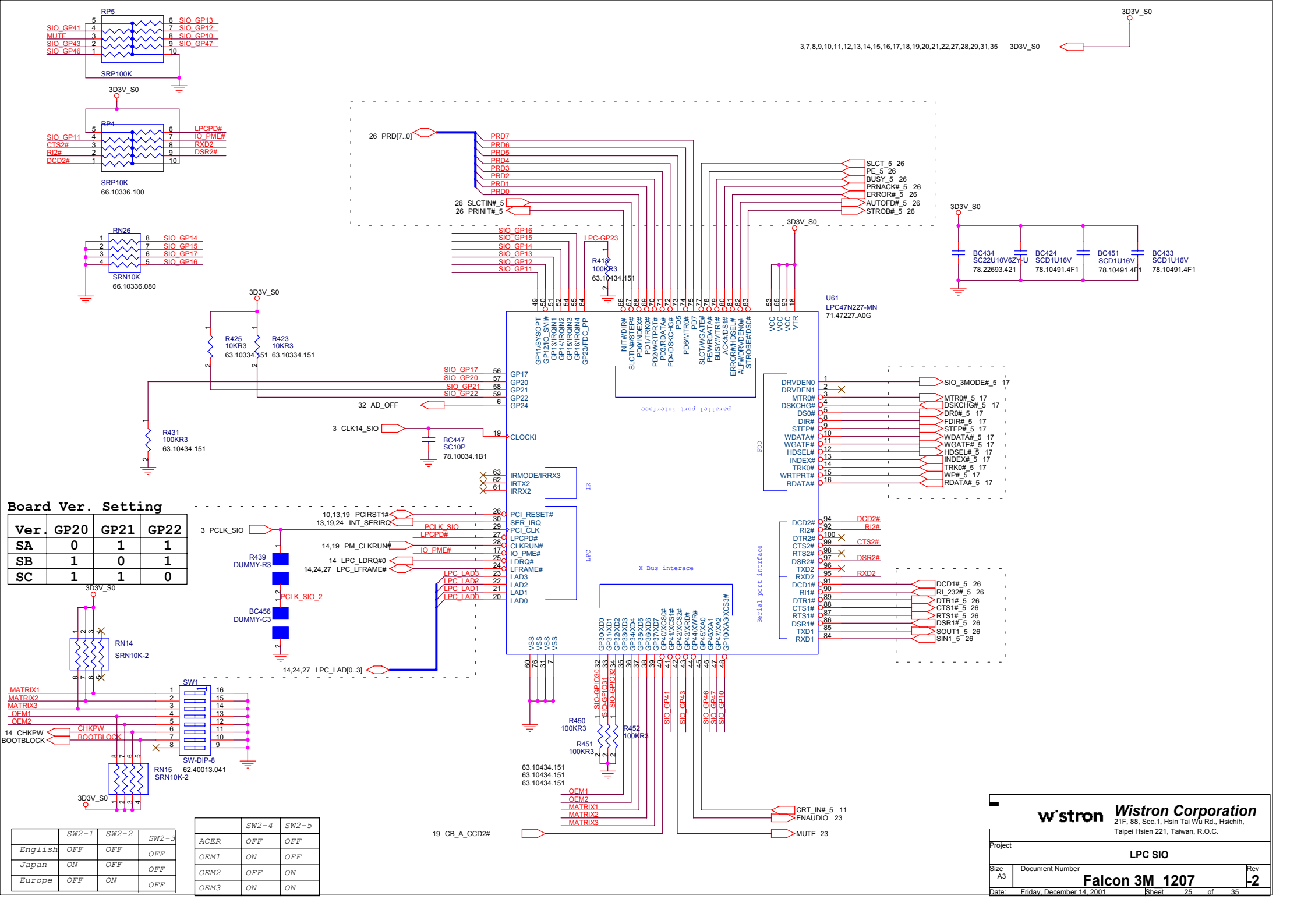
RP5
SIO_GP41
MUTE
SIO_GP43
SIO_GP46
SIO_GP13
SIO_GP12
SIO_GP10
SIO_GP47
SRP100K
3D3V_S0
RP4
SIO_GP11
CTS2#
RI2#
DCD2#
LPCPD#
IO_PME#
RXD2
DSR2#
SRP10K
66.10336.100
RN26
SIO_GP14
SIO_GP15
SIO_GP17
SIO_GP16
SRN10K
66.10336.080
26 PRD[7..0]
PRD7
PRD6
PRD5
PRD4
PRD3
PRD2
PRD1
PRD0
26 SLCTIN#_5
26 PRINIT#_5
SLCT_5 26
PE_5 26
BUSY_5 26
PRNACK#_5 26
ERROR#_5 26
AUTOFD#_5 26
STROB#_5 26
3,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,27,28,29,31,35 3D3V_S0
BC434
SC22U10V6ZY-U
78.22693.421
BC424
SCD1U16V
78.10491.4F1
BC451
SCD1U16V
78.10491.4F1
BC433
SCD1U16V
78.10491.4F1
SIO_GP16
SIO_GP15
SIO_GP14
SIO_GP13
SIO_GP12
SIO_GP11
LPC-GP23
R418
100KR3
63.10434.151
U61
LPC47N227-MN
71.47227.A0G
R425
10KR3
63.10334.151
R423
10KR3
63.10334.151
SIO_GP17
SIO_GP20
SIO_GP21
SIO_GP22
32 AD_OFF
R431
100KR3
63.10434.151
3 CLK14_SIO
BC447
SC10P
78.10034.1B1
CLOCKI
IRMODE/IRRX3
IRTX2
IRRX2
IR
parallel port interface
FDD
DRVDEN0
DRVDEN1
MTR0#
DSKCHG#
DS0#
DIR#
STEP#
WDATA#
WGATE#
HDSEL#
INDEX#
TRK0#
WRTPRT#
RDATA#
SIO_3MODE#_5 17
MTR0#_5 17
DSKCHG#_5 17
DR0#_5 17
FDIR#_5 17
STEP#_5 17
WDATA#_5 17
WGATE#_5 17
HDSEL#_5 17
INDEX#_5 17
TRK0#_5 17
WP#_5 17
RDATA#_5 17
Board Ver. Setting
Ver. GP20 GP21 GP22
SA 0 1 1
SB 1 0 1
SC 1 1 1
3D3V_S0
3 PCLK_SIO
R439
DUMMY-R3
PCLK_SIO_2
BC456
DUMMY-C3
10,13,19 PCIRST1#
13,19,24 INT_SERIRQ
PCLK_SIO
LPCPD#
14,19 PM_CLKRUN#
IO_PME#
14 LPC_LDRQ#0
14,24,27 LPC_LFRAME#
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
14,24,27 LPC_LAD[0..3]
PCI_RESET#
SER_IRQ
PCI_CLK
LPCPD#
CLKRUN#
IO_PME#
LDRQ#
LFRAME#
LAD3
LAD2
LAD1
LAD0
LPC
X-Bus interace
Serial port intrface
DCD2#
RI2#
DTR2#
CTS2#
RTS2#
DSR2#
TXD2
RXD2
DCD1#
RI1#
DTR1#
CTS1#
RTS1#
DSR1#
TXD1
RXD1
DCD1#_5 26
RI_232#_5 26
DTR1#_5 26
CTS1#_5 26
RTS1#_5 26
DSR1#_5 26
SOUT1_5 26
SIN1_5 26
VSS
GP30/XD0
GP31/XD1
GP32/XD2
GP33/XD3
GP34/XD4
GP35/XD5
GP36/XD6
GP37/XD7
GP40/XCS0#
GP41/XCS1#
GP42/XCS2#
GP43/XRD#
GP44/XWR#
GP45/XA0
GP46/XA1
GP47/XA2
GP10/XA3/XCS3#
SIO-GPIO30
SIO-GPIO31
SIO-GPIO32
R450
100KR3
R451
100KR3
R452
100KR3
SIO_GP41
SIO_GP43
SIO_GP46
SIO_GP47
SIO_GP10
63.10434.151
63.10434.151
63.10434.151
OEM1
OEM2
MATRIX1
MATRIX2
MATRIX3
CRT_IN#_5 11
ENAUDIO 23
19 CB_A_CCD2#
MUTE 23
MATRIX1
MATRIX2
MATRIX3
OEM1
OEM2
14 CHKPW
BOOTBLOCK
CHKPW
BOOTBLOCK
SW1
SW-DIP-8
RN14
SRN10K-2
RN15 62.40013.041
SRN10K-2
3D3V_S0
SW2-1 SW2-2 SW2-3
English OFF OFF OFF
Japan ON OFF OFF
Europe OFF ON OFF
SW2-4 SW2-5
ACER OFF OFF
OEM1 ON OFF
OEM2 OFF ON
OEM3 ON ON
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Project
LPC SIO
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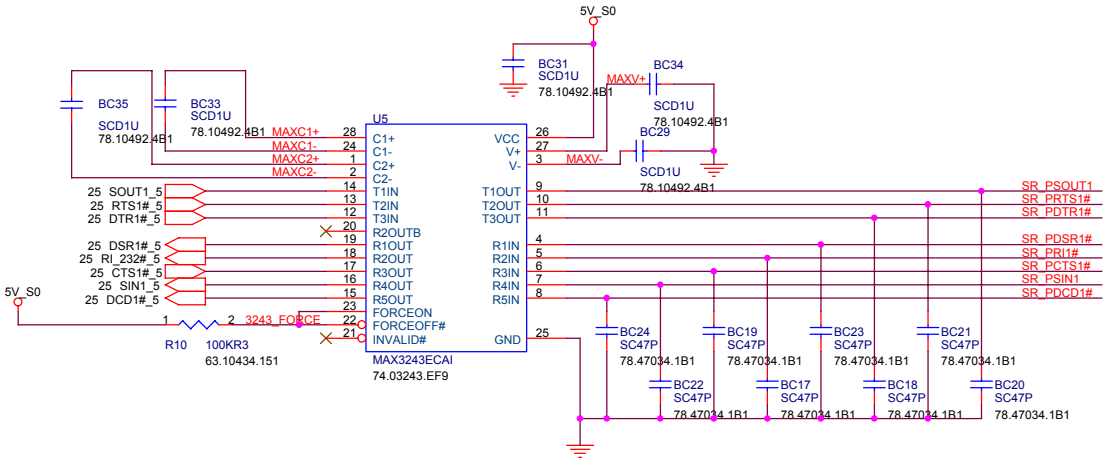
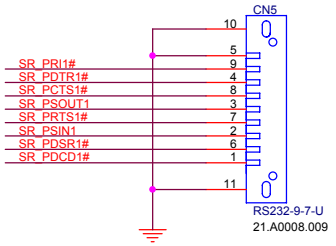
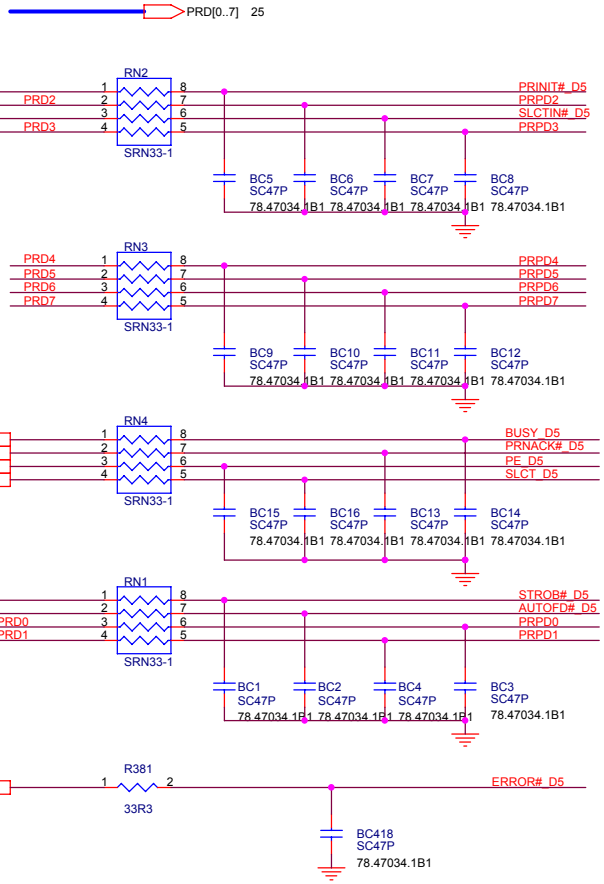
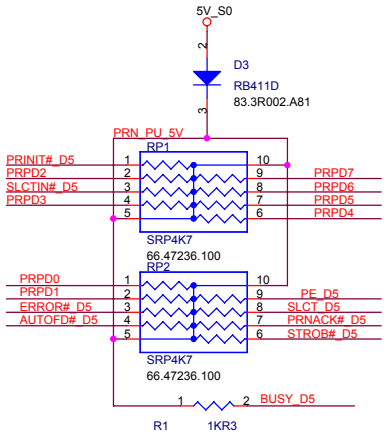
SERIAL PORT

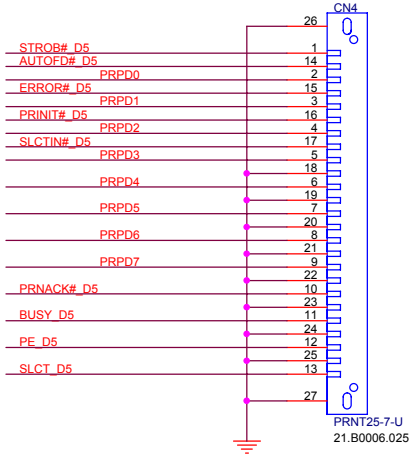




PRINTER PORT







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Project	SERIAL/PRINTER PORT	
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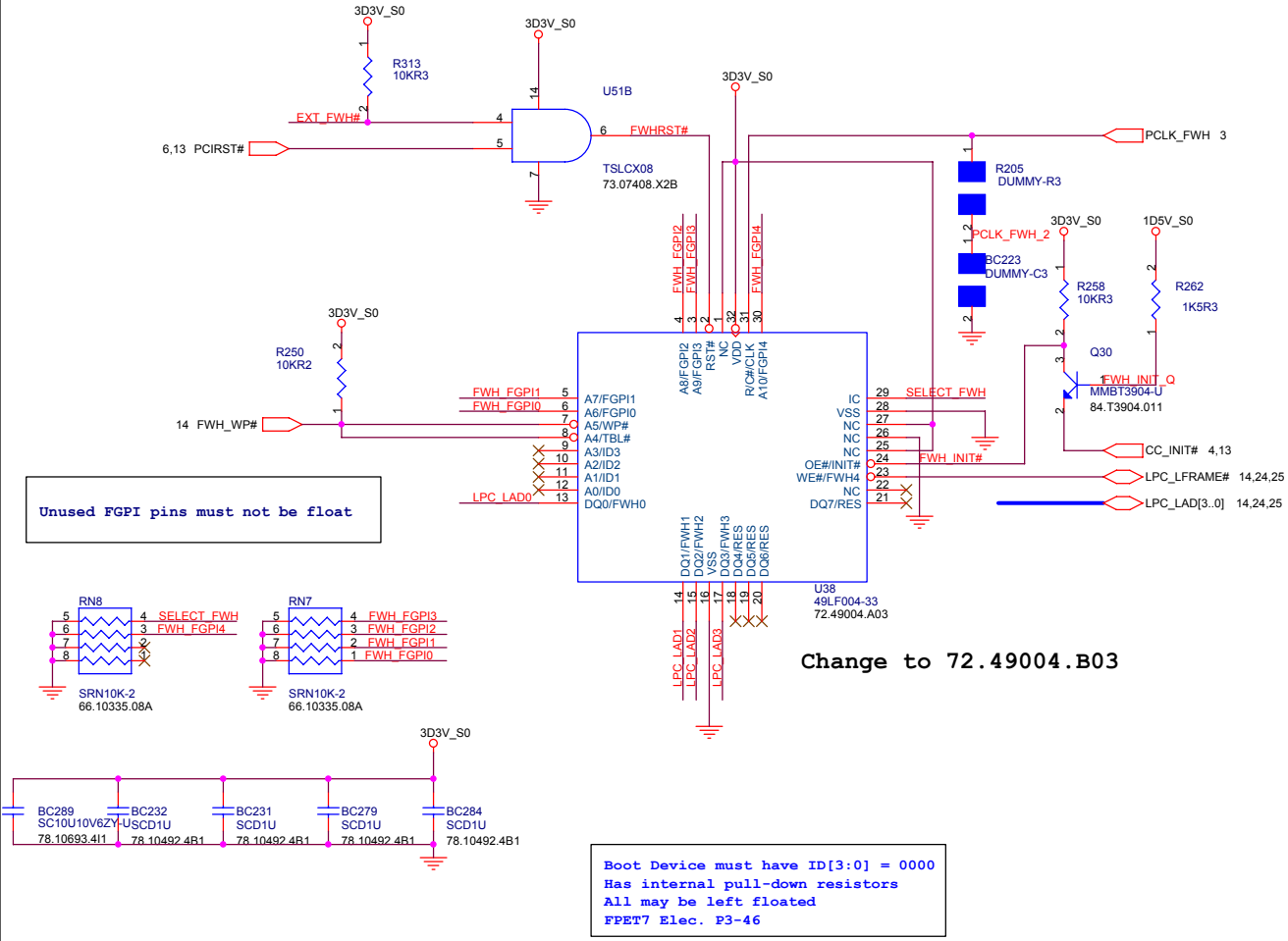
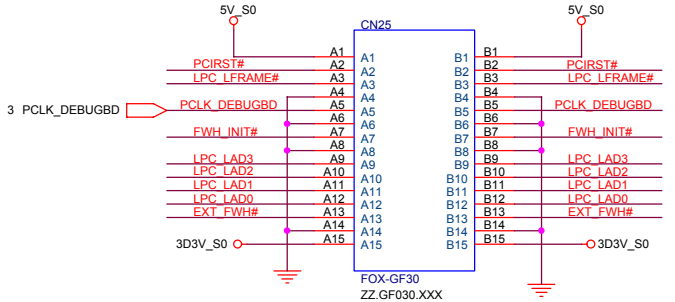


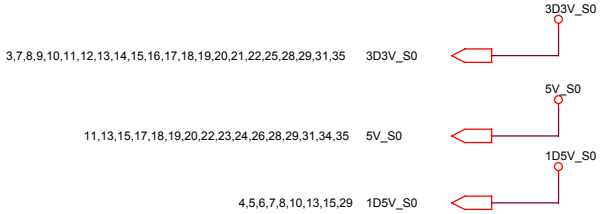
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD





Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Project: FIRMWARE HUB & DEBUG PORT		
Size: A3	Document Number: Falcon 3M_1207	Rev: -2
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Mode	Tualitin	Copermine-T	Celeron-933
PERFORMANCE	1.4V	1.70V	1.70V
BATTERY	1.15V	1.35V	1.70
Deeper Sleep	0.85V	Non	Non

Input	Output
Low	ON
High	OFF

D4	D3	D2	D1	D0	Vout (V)
0	0	0	0	0	1.75
0	0	0	0	1	1.70
0	0	0	1	0	1.65
0	0	0	1	1	1.60
0	0	1	0	0	1.55
0	0	1	0	1	1.50
0	0	1	1	0	1.45
0	0	1	1	1	1.40
0	1	0	0	0	1.35
0	1	0	0	1	1.30
0	1	0	1	0	1.25
0	1	0	1	1	1.20
0	1	1	0	0	1.15
0	1	1	0	1	1.10
0	1	1	1	0	1.05
0	1	1	1	1	1.00

S1	S0	Vout (V) Default
GND	GND	0.975
GND	REF	0.950
GND	Float	0.925
GND	VCC	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float	0.825
REF	VCC	0.800
Float	GND	0.775
Float	REF	0.750
Float	Float	0.725
Float	VCC	0.700
VCC	GND	0.675
VCC	REF	0.650
VCC	Float	0.625
VCC	VCC	0.600

ZMODE: SUS — Vout Determined by:
GND — GND — Logic Level of D0 - D4
VCC — GND — Impedance of D0 - D4
X — VCC — Logic Level of S0, S1

For ZMODE=High
Set CPU Voltage 1.4V
D[4:0]=[00111]

For ZMODE=Low
Set CPU Voltage 1.15V
D[4:0]=[01100]

ZMODE Defined Level-Judge Method
If ZMODE=High, Set D[4..0] by Voltage-Level in wire
If ZMODE=Low, Set D[4..0] by R(resistor)
R=100Kohm, High
R=1Kohm, Low

MP change part
SB SCD22U16V3ZY

MP FOR EMI

Offset Truth Table

PM_DPRSLPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

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Project	CPU VCORE
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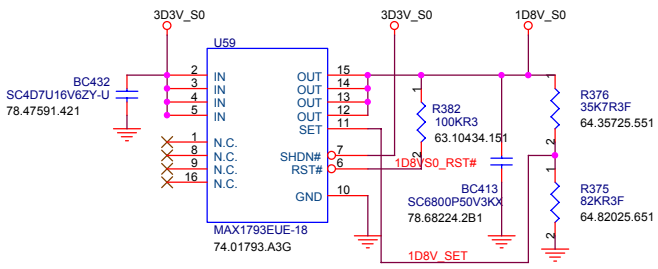
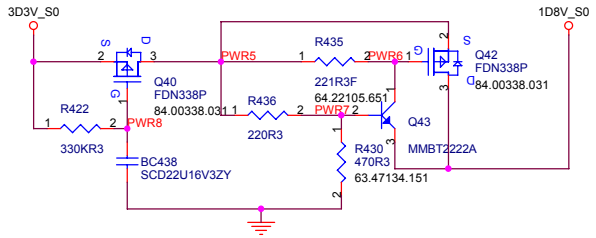
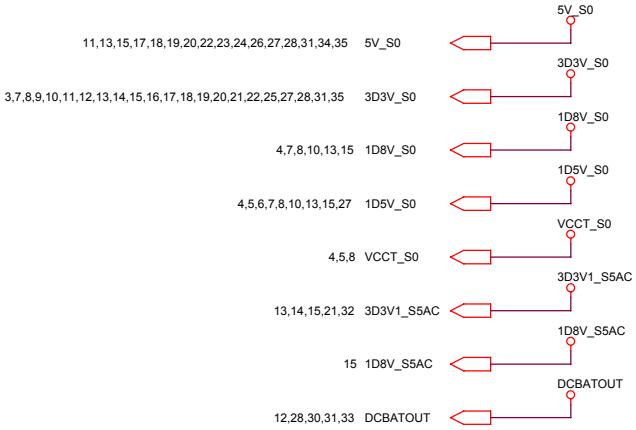
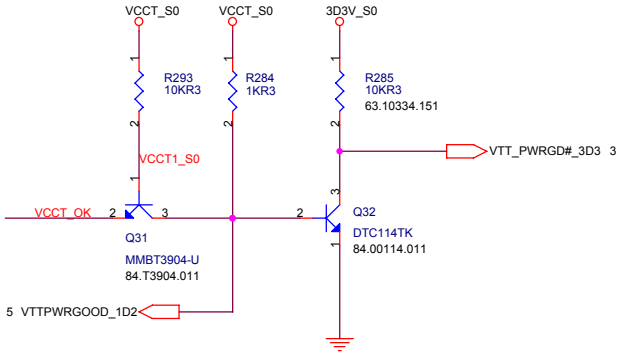
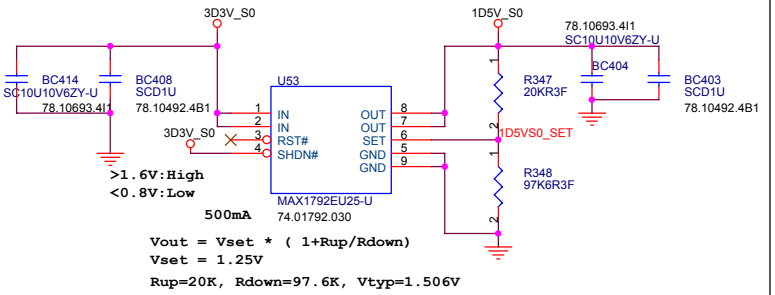
1.8V (750mA)



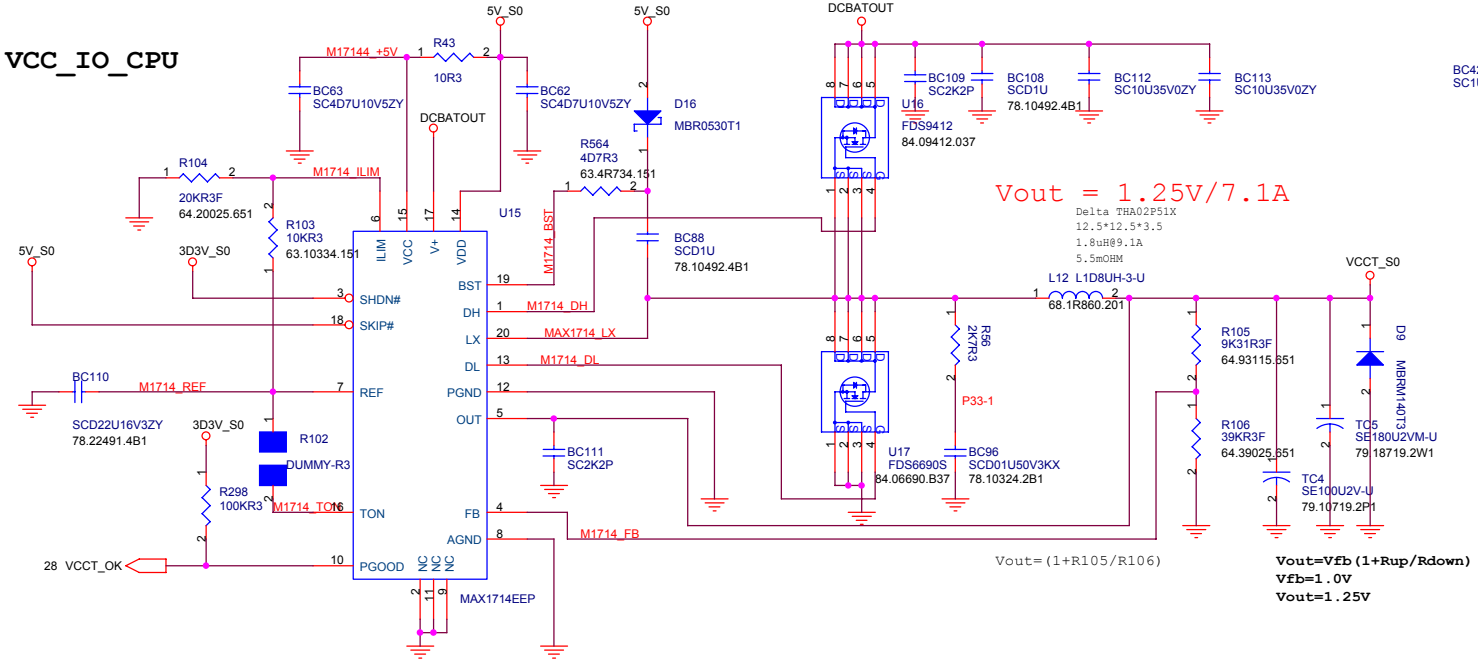


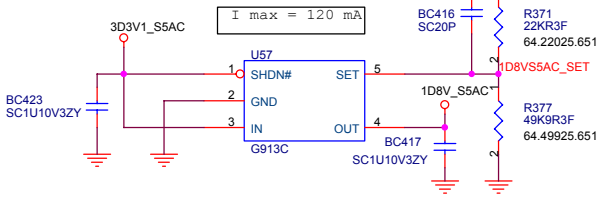


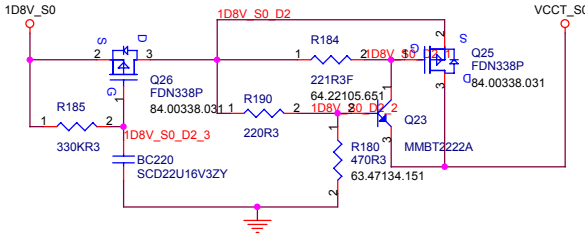




VCC_IO_CPU







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Project	CPUIO,1.5V,1.8V,1.2V
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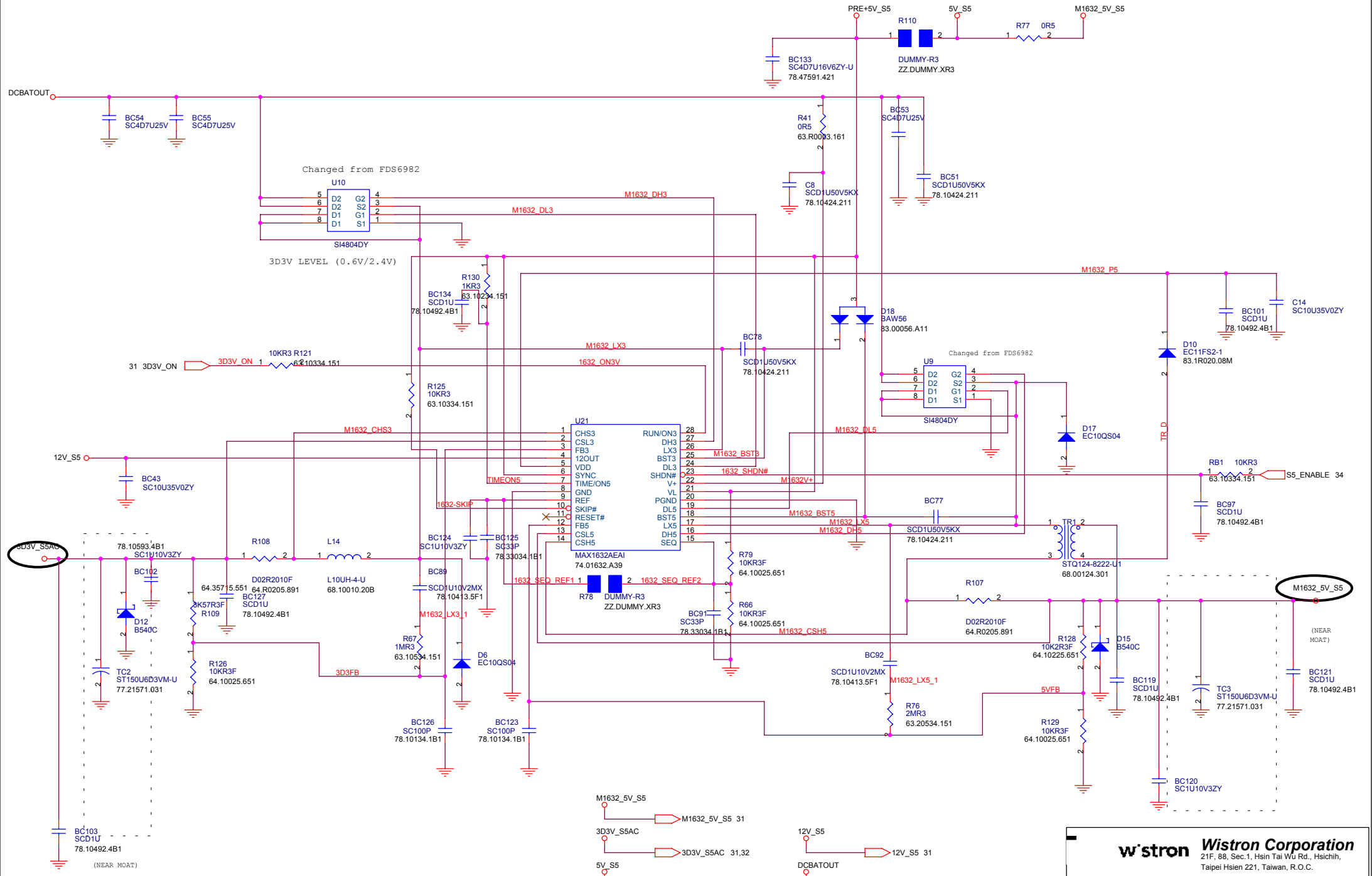

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Taipei Hsien 221, Taiwan, R.O.C.

Project	SYSTEM DC/DC	
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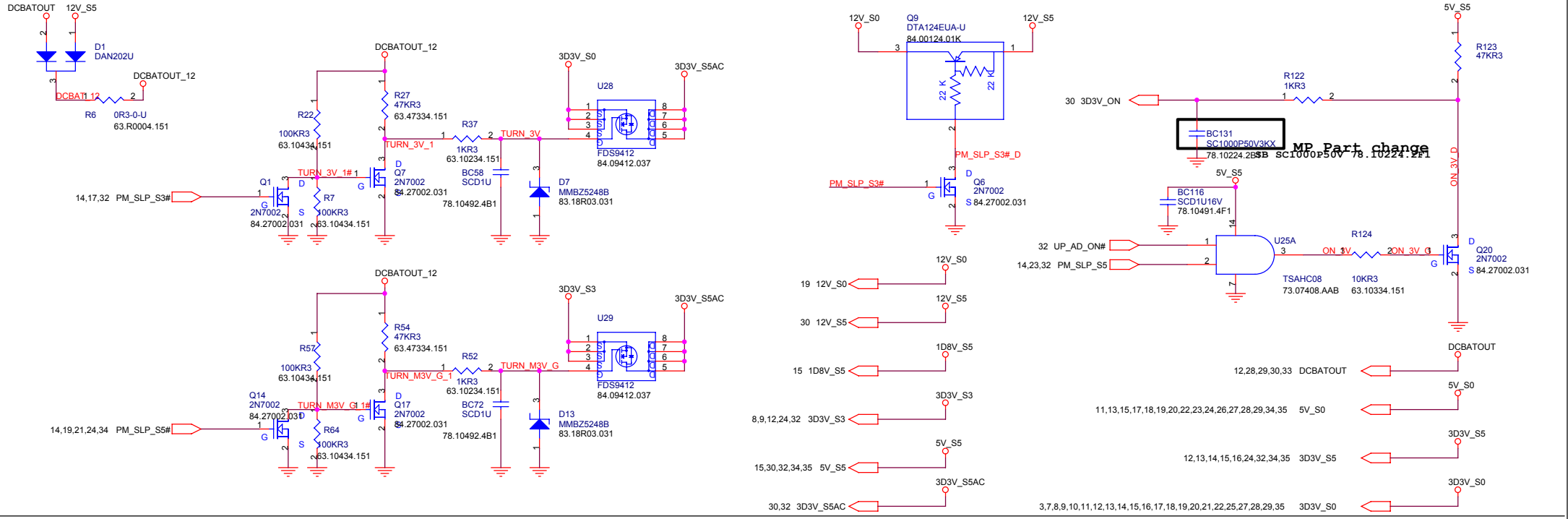

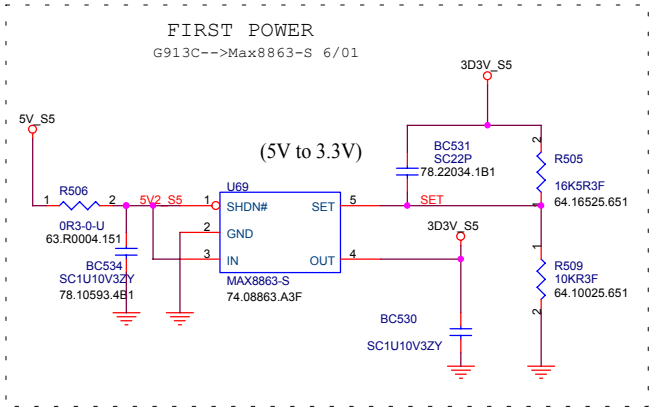

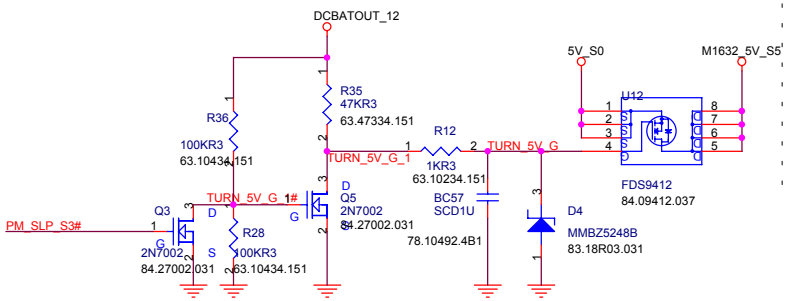

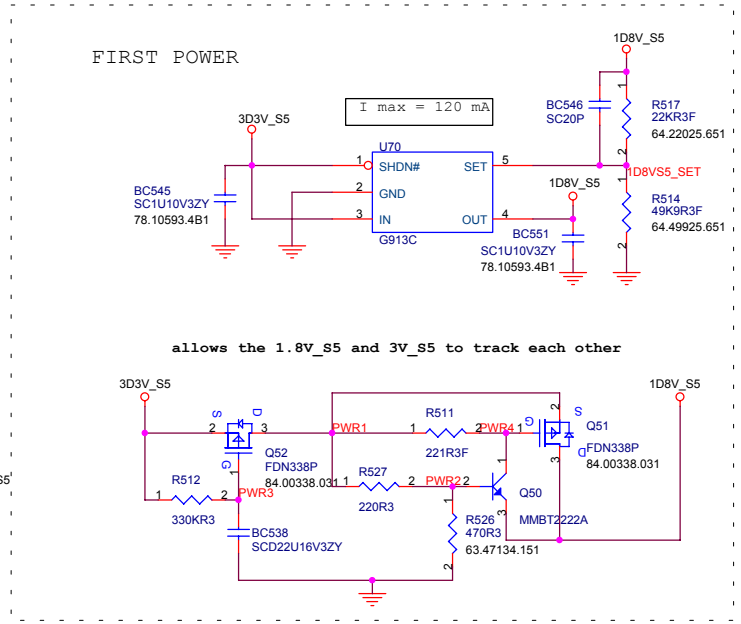

Wistron Corporation		
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Project: POWER3		
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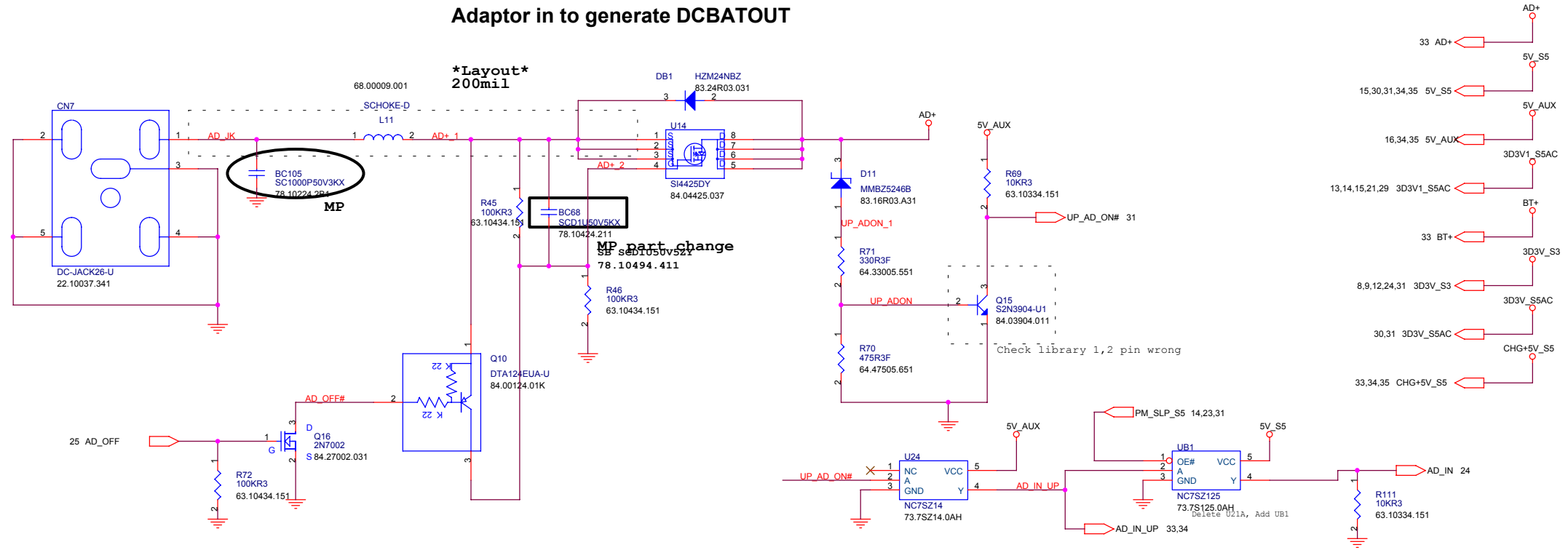
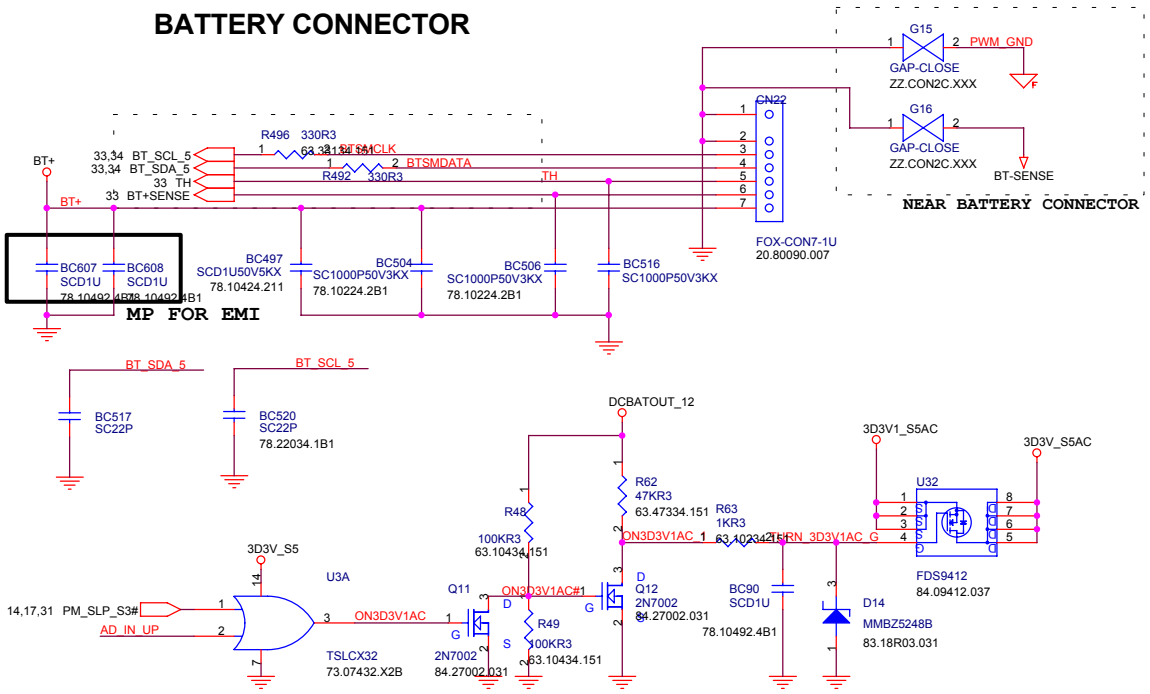
Adaptor in to generate DCBATOUT

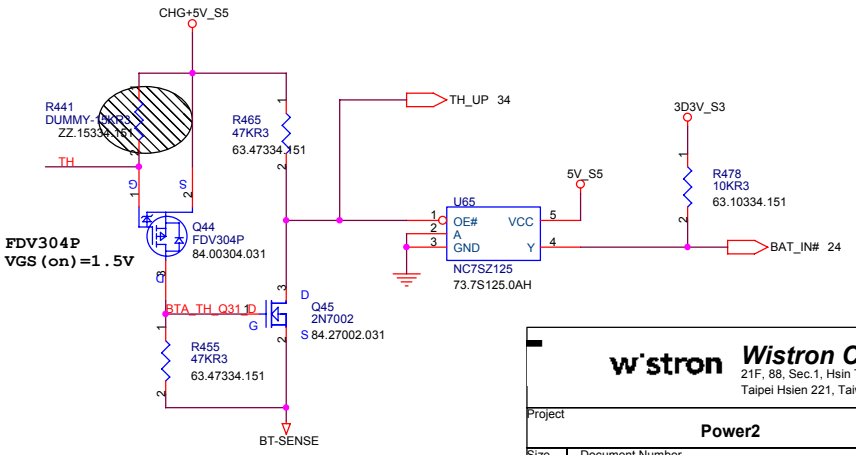


BATTERY CONNECTOR



BAT_TH = 4.371V - 0.314V for NiH
= 390ohm pull-GND for Li

FDV304P
VGS(on)=1.5V



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Project: Power2		
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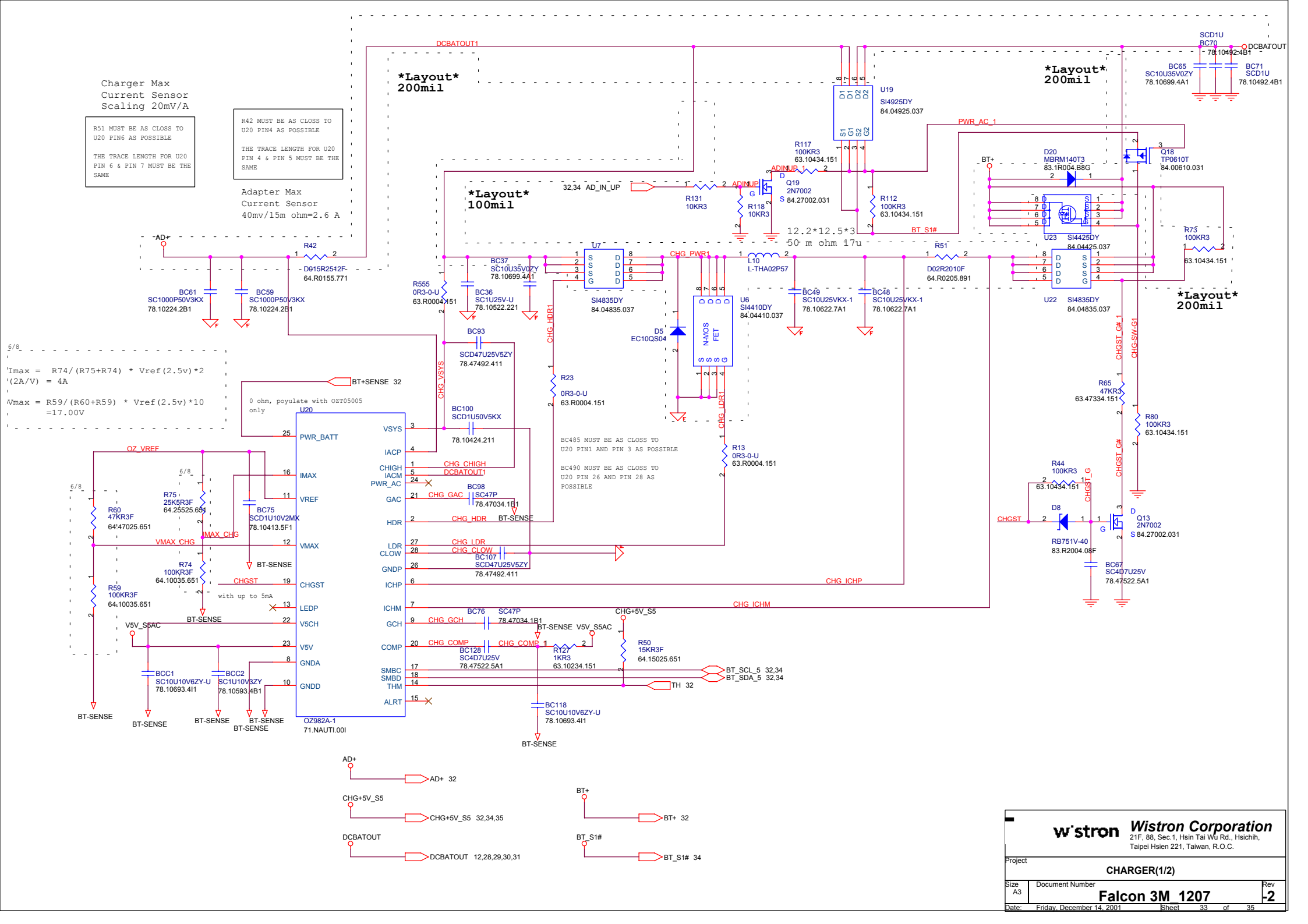

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Project	CHARGER(1/2)	
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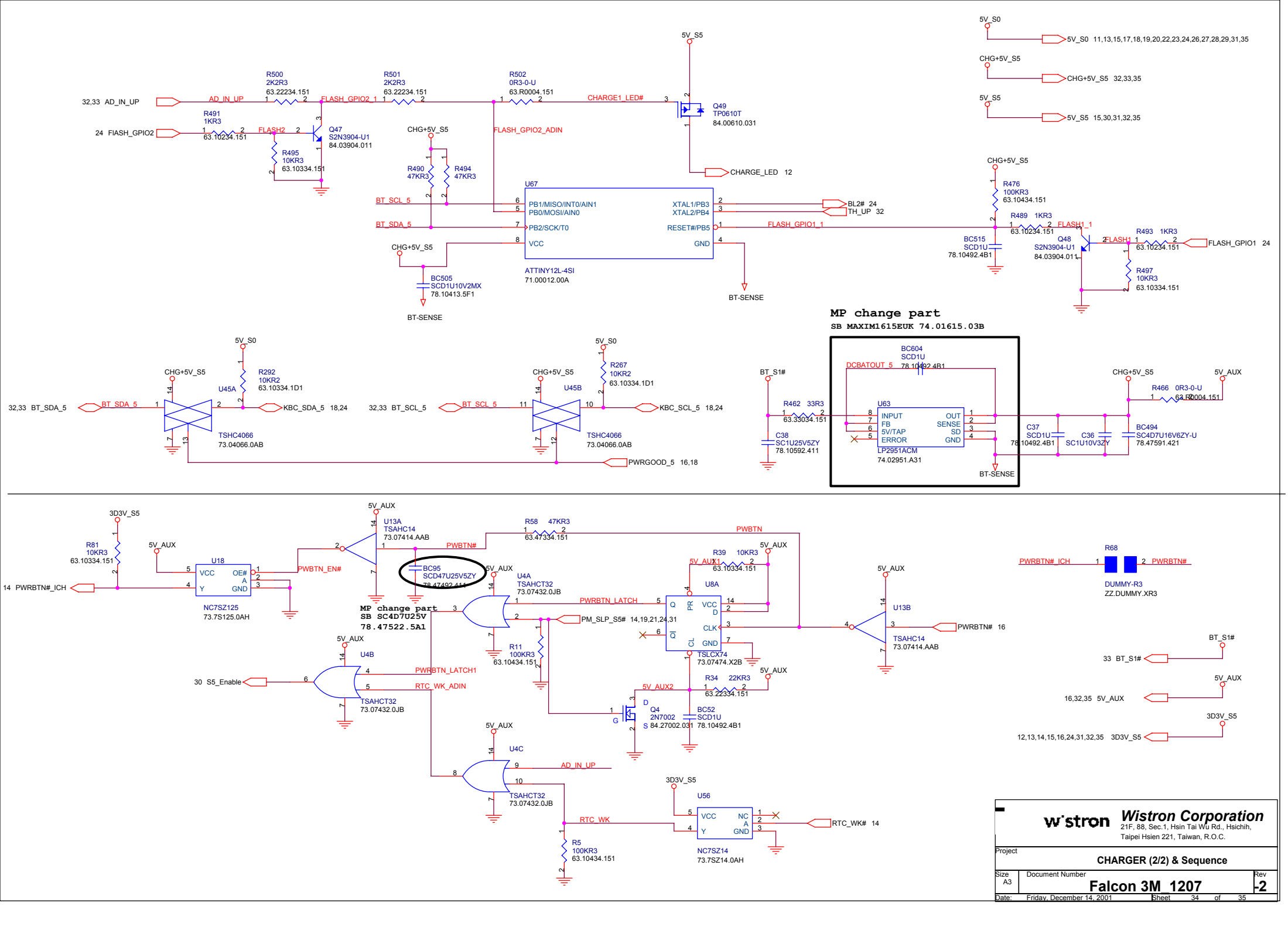

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Project	CHARGER (2/2) & Sequence	
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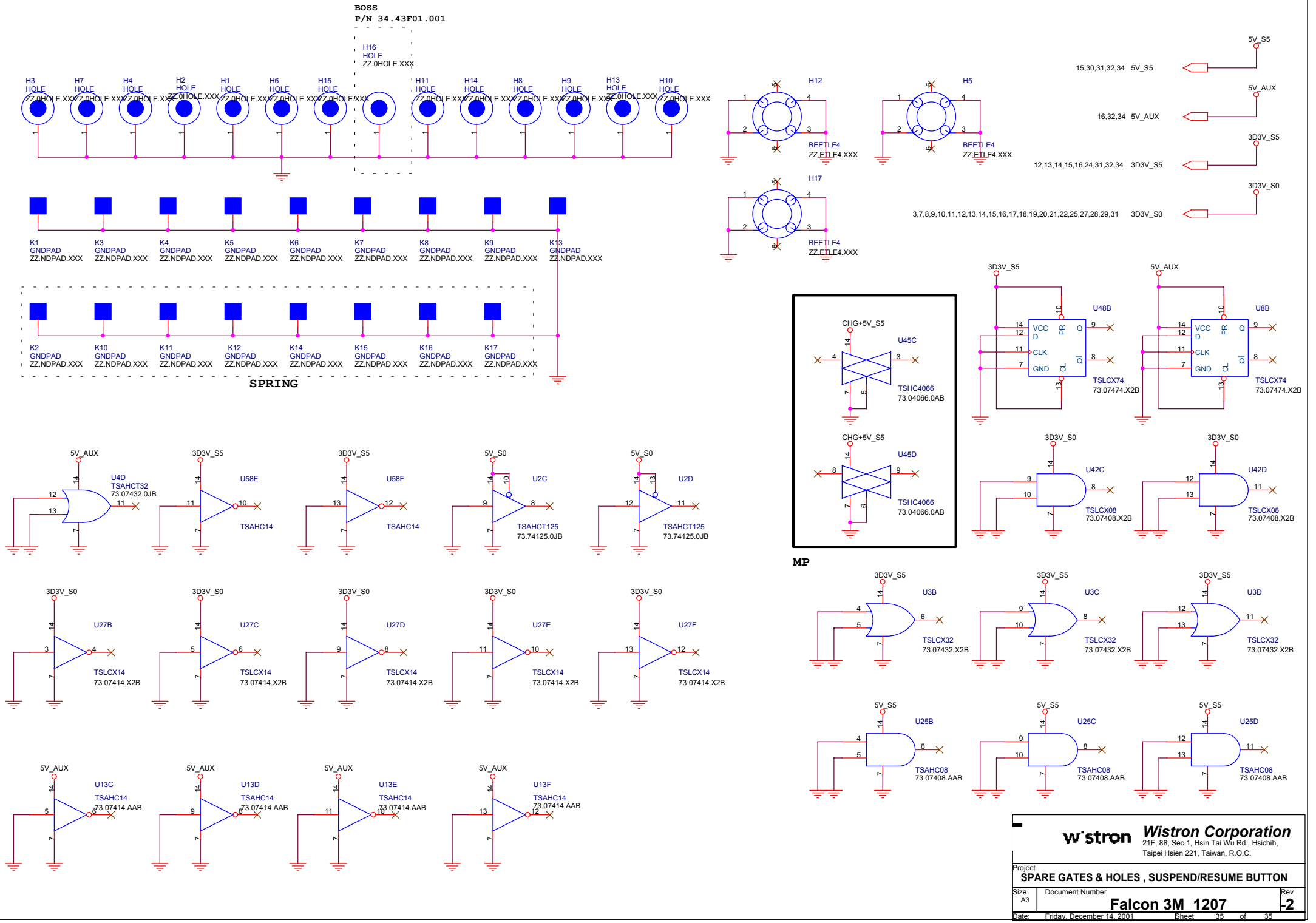

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Project
SPARE GATES & HOLES , SUSPEND/RESUME BUTTON

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