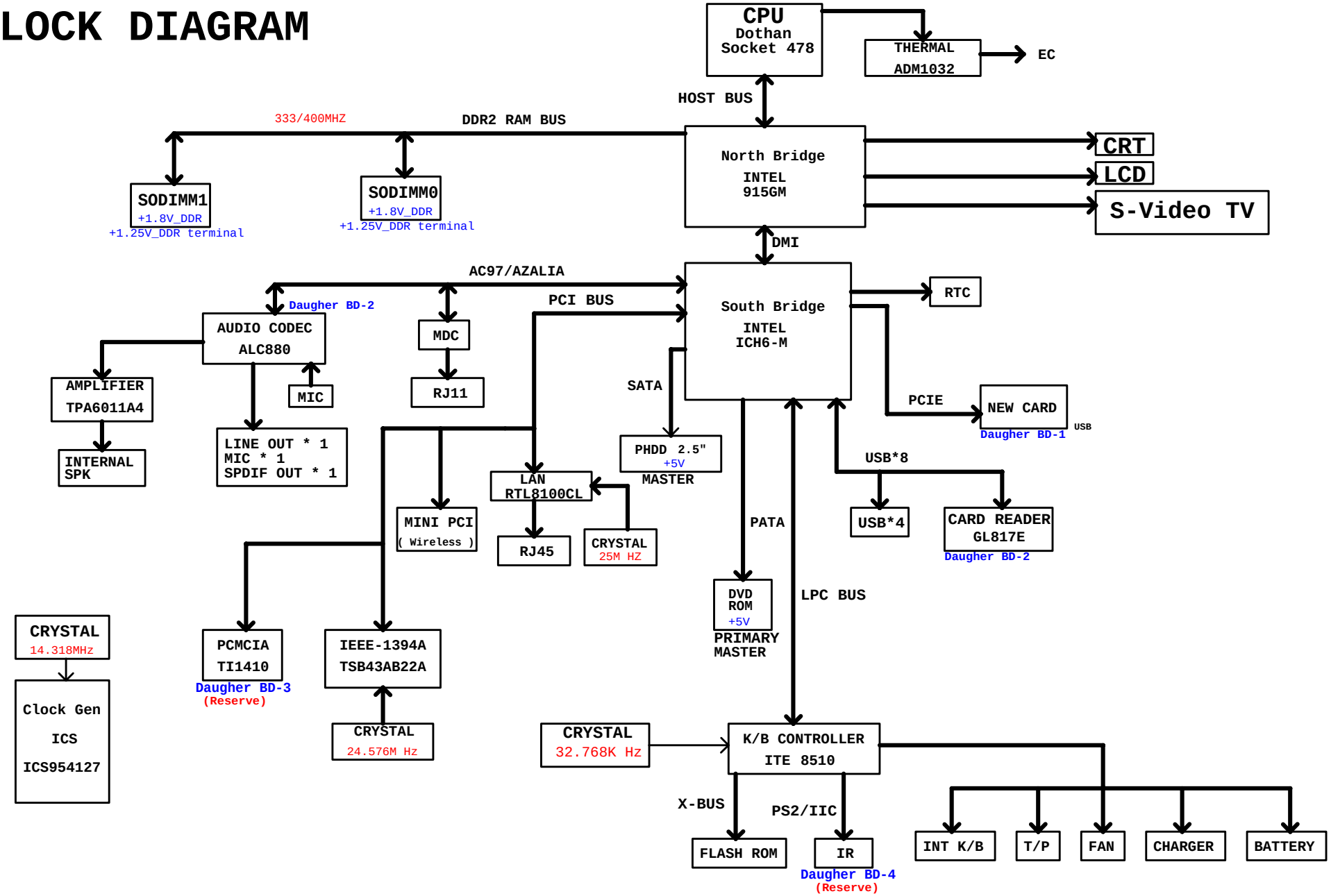
Model : MX0/M40/50 EI0

Mobile Dothan with INTEL 915GM / ICH6-M Chipset

P/N:37GM50100-B0

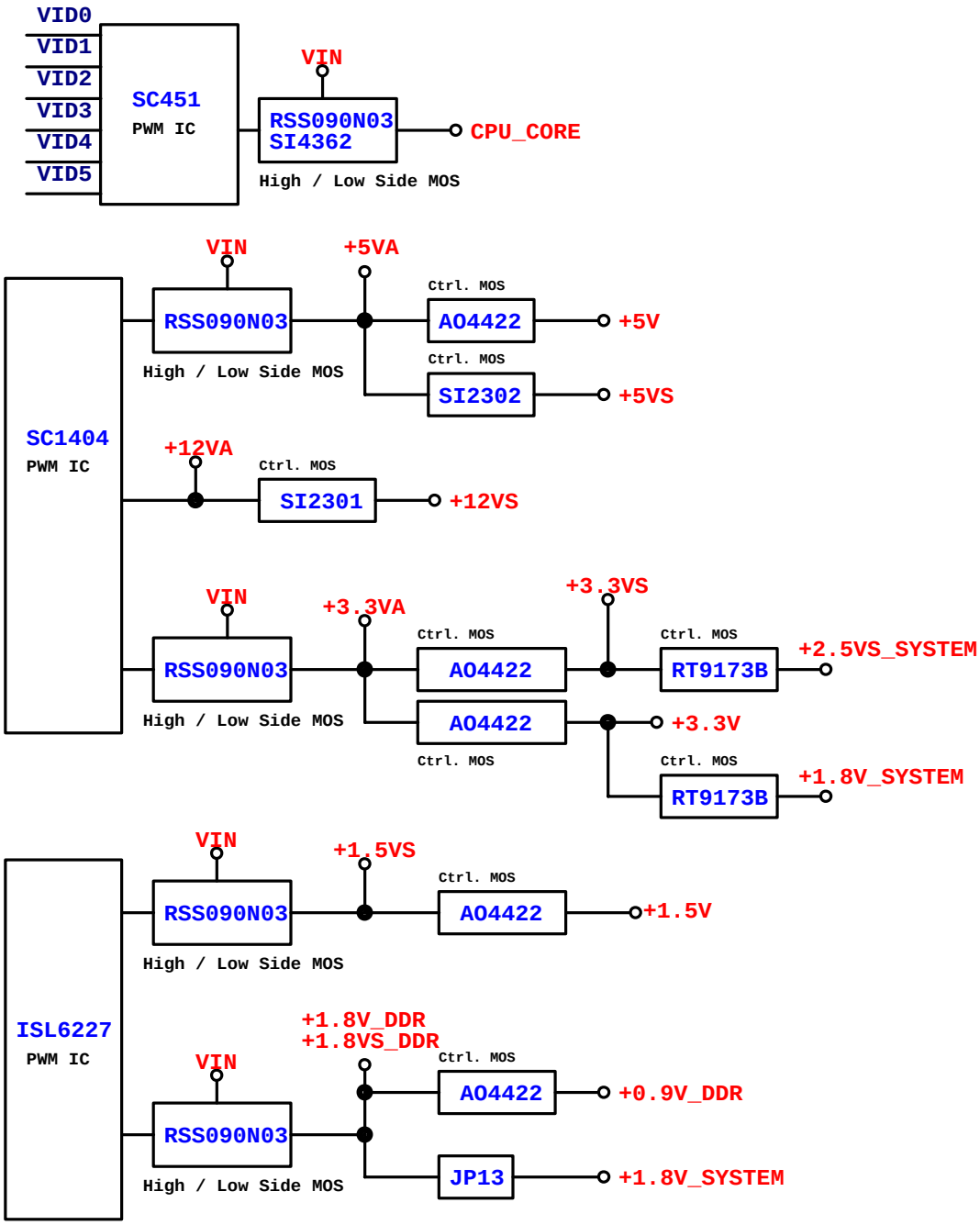
UNIWILL COMPUTER CORP.		
Title: MX0/M40/50EI0		
Size: Custom	Document Number: 3017 INDEX	Rev: C
Date: Monday, July 25, 2005	Sheet 1 of 35	

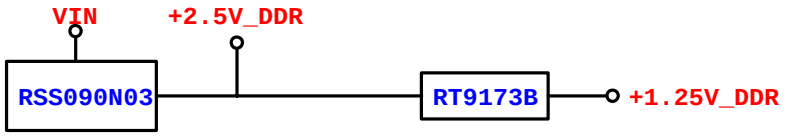
M50EI0
BLOCK DIAGRAM



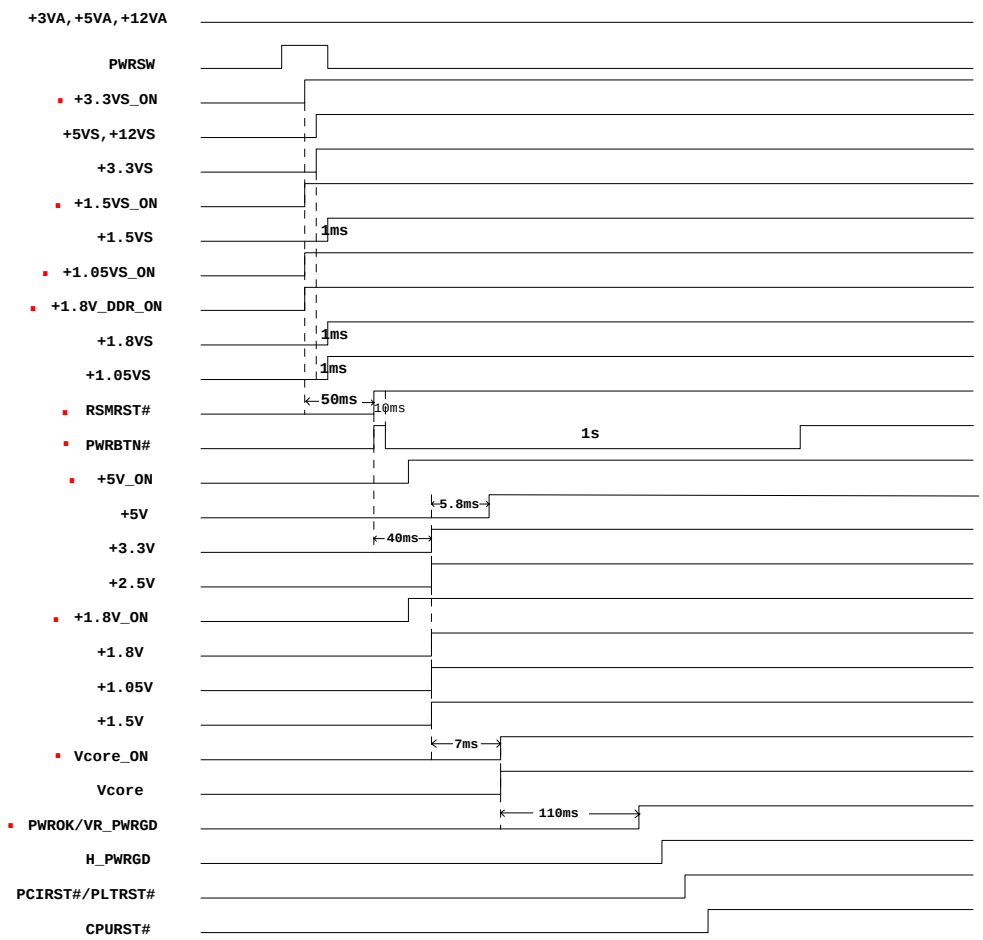
UNIWILL COMPUTER CORP.		
Title	MX0/M40/50EI0	
Size	Document Number: 3017 SYSTEM BLOCK DIAGRAM	Rev C
Date: Monday, July 25, 2005	Sheet 2 of 35	

POWER BLOCK DIAGRAM





POWER Sequence



EC Control Pin

UNIWILL COMPUTER CORP.		
Title: MX0/M40/50EI0		
Size: Custom	Document Number: 3017 POWER DIAGRAM	Rev: C
Date: Monday, July 25, 2005	Sheet 3 of 35	

ICH6-M GPIO

GPI6	BM_BUSY#
GP7	
GP8	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	
GPI13	
GPO18	PM_STPPCI_ICH#
GPO19	
GPO20	PM_STPCPU_ICH#
GPO21	TPM_EN
GPO23	
GPIO24	
GPIO25	
GPIO26	SATA0_GP
GPIO27	
GPIO28	
GPIO29	PNLSW1
GPIO30	PNLSW2
GPIO31	PNLSW0
GPIO32	PM_CLKRUN#
GPIO33	
GPIO34	

ITE8510E GPIO

GPCF0	TURBO#/PHOTO
GPCF1	SILENT#/TV
GPCF2	BAT_SEL
GPCF3	BAT_THROT_EN
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	MAIL#/DVD
GPCF7	BROWSER#/MP3
GPI0	SCROLL#
GPI1	CAPS#
GPI2	NUM#
GPI3	CHGLED_ON#
GPI4	A/W_LED1#
GPI5	SUSLED_ON#
GPI6	A/W_LED2#
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	CELERON_VO_DET
GPB1	TURBO_LED#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	
GPE1	CPU_BSEL0
GPE2	TP_BTU
GPE3	TP_BTD
GPE4	PWRSW
GPE5	LID#
GPE6	RF_OFF
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	AW#/CD
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	
GPD5	
GPD6	CLKREQ#
GPD7	EC_PREST#
GPA0	BTL_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	SMP1_EN#
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO

GPC0	PWROK
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	
GPC4	
GPC5	A/W_LED3#
GPC6	CHG_ON
GPC7	SILENT_LED#

SB INT_PIRQ List

INT_PIRQA	CARD BUS
INT_PIRQB	Mini PCI
INT_PIRQC	1394
INT_PIRQD	LAN
INT_PIRQE	CARD BUS(op)
INT_PIRQF	Mini PCI
INT_PIRQG	NC
INT_PIRQH	NC

CPU

	CPU CORE(V)	ICC(mA)	W	TEMP( )
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE

VCC	ICC(mA)	W	TEMP( )
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_GMCH_CORE	266	0.452	

ICH6-M

VCC	ICC(mA)	W	TEMP( )
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

ITE8510E

VCC	ICC(mA)	W	TEMP( )
+3.3V	300	1	70

CLOCK GENERATOR

VCC	ICC(mA)	W	TEMP( )
+3.3V	180	0.594	70

ADM1032

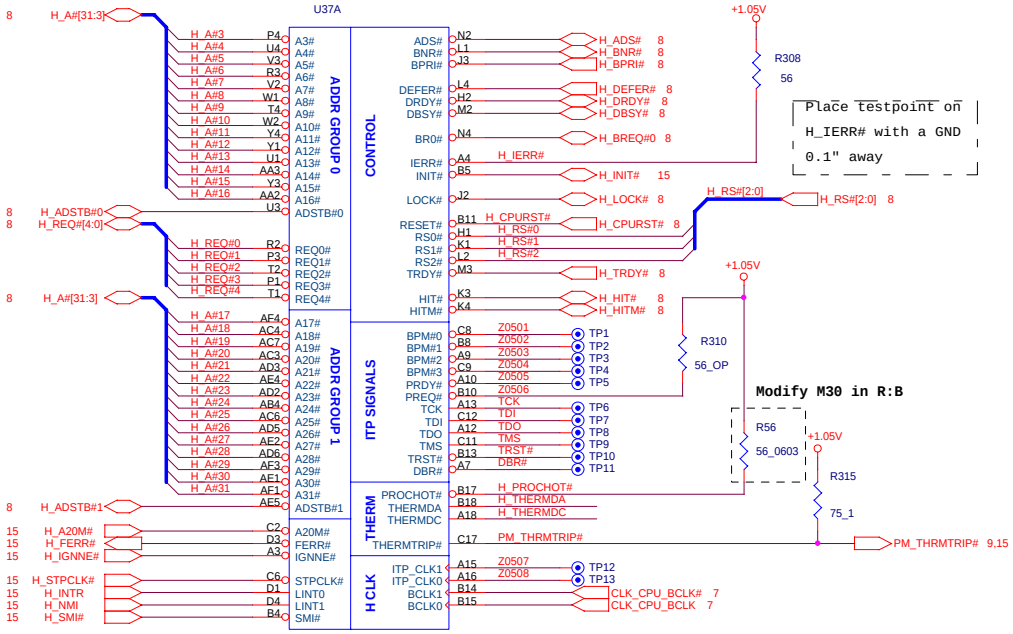
VCC	ICC	W	TEMP( )
+3.3V	170uA	0.56mW	150

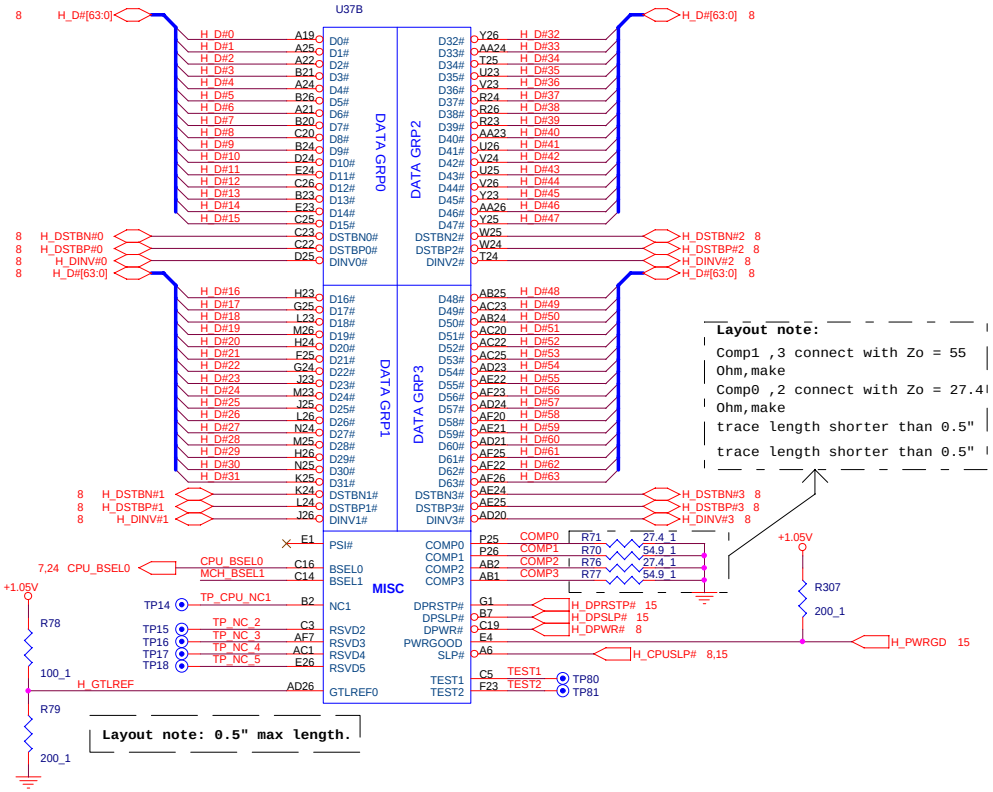
UNIWILL COMPUTER CORP.

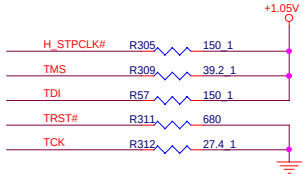
Title: MX0/M40/50EI0

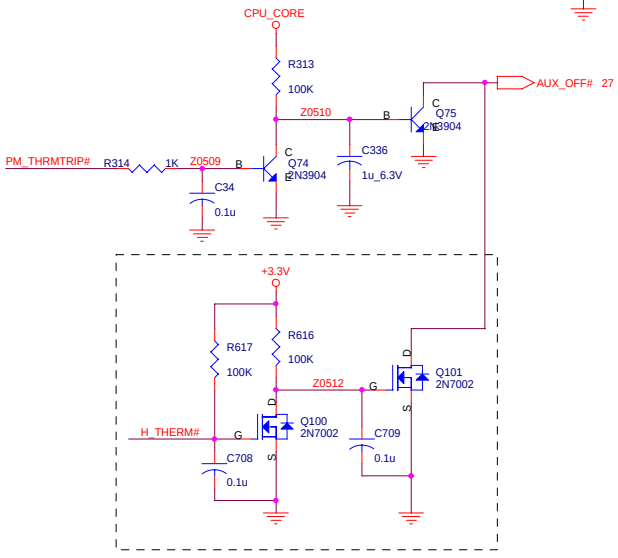
Size: Custom | Document Number: 3017 GPIO & POWER CONSU | Rev: C

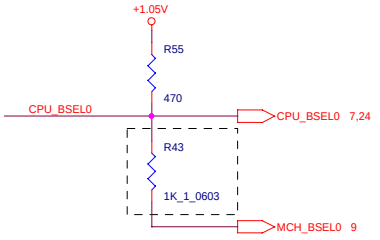
Date: Monday, July 25, 2005 | Sheet 4 of 35

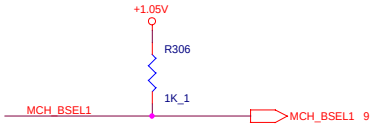




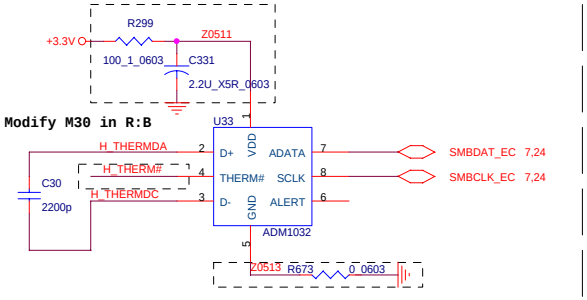








CPU Thermal Sensor



	BSEL0	BSEL1
PSB400	1	0
PSB533(dafault)	0	0

ICS954206 BSEL Settings:

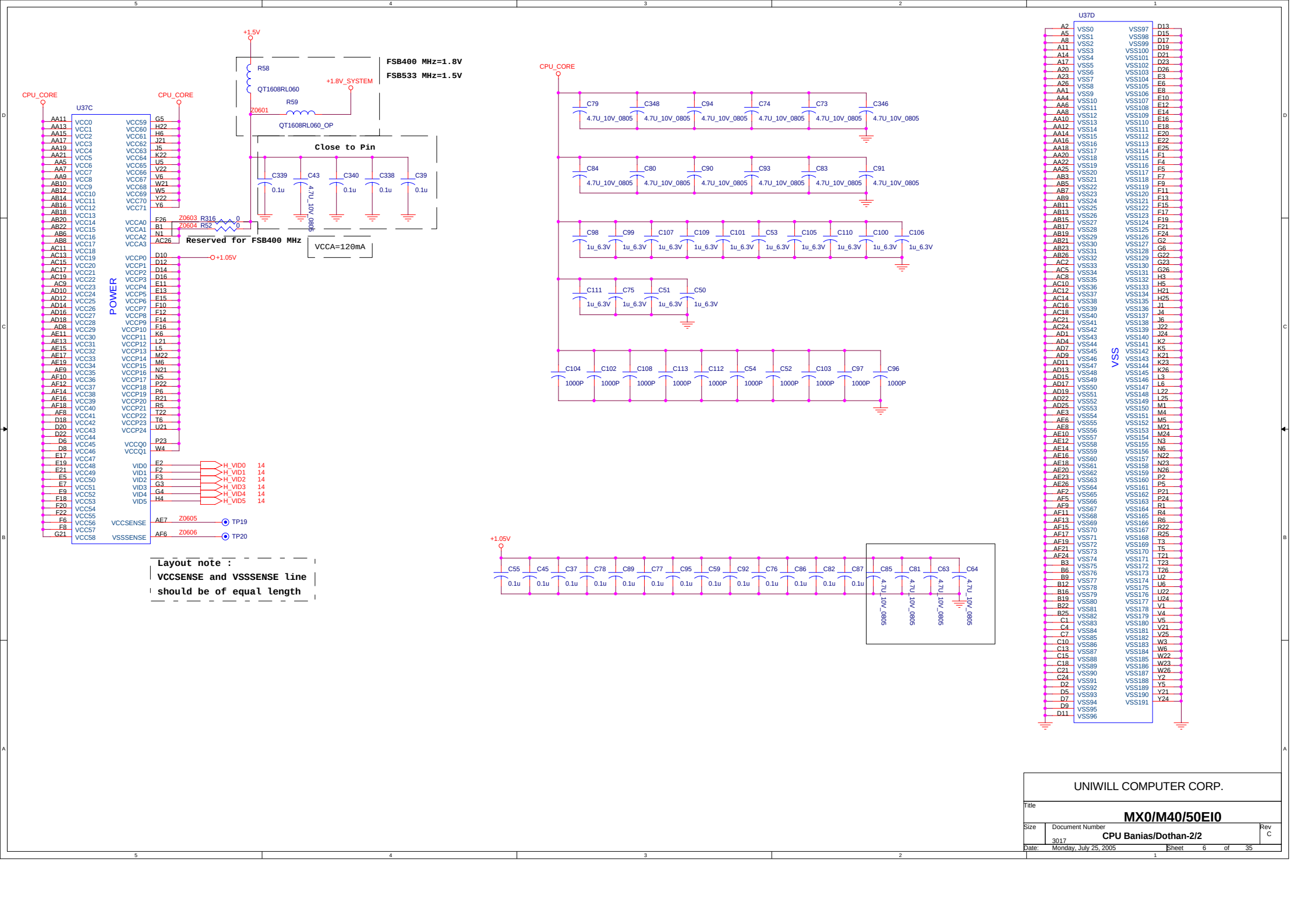
01=PSB400(BSEL0=1 BSEL1=0)
00=PSB533(BSEL1=0 BSEL0=0)

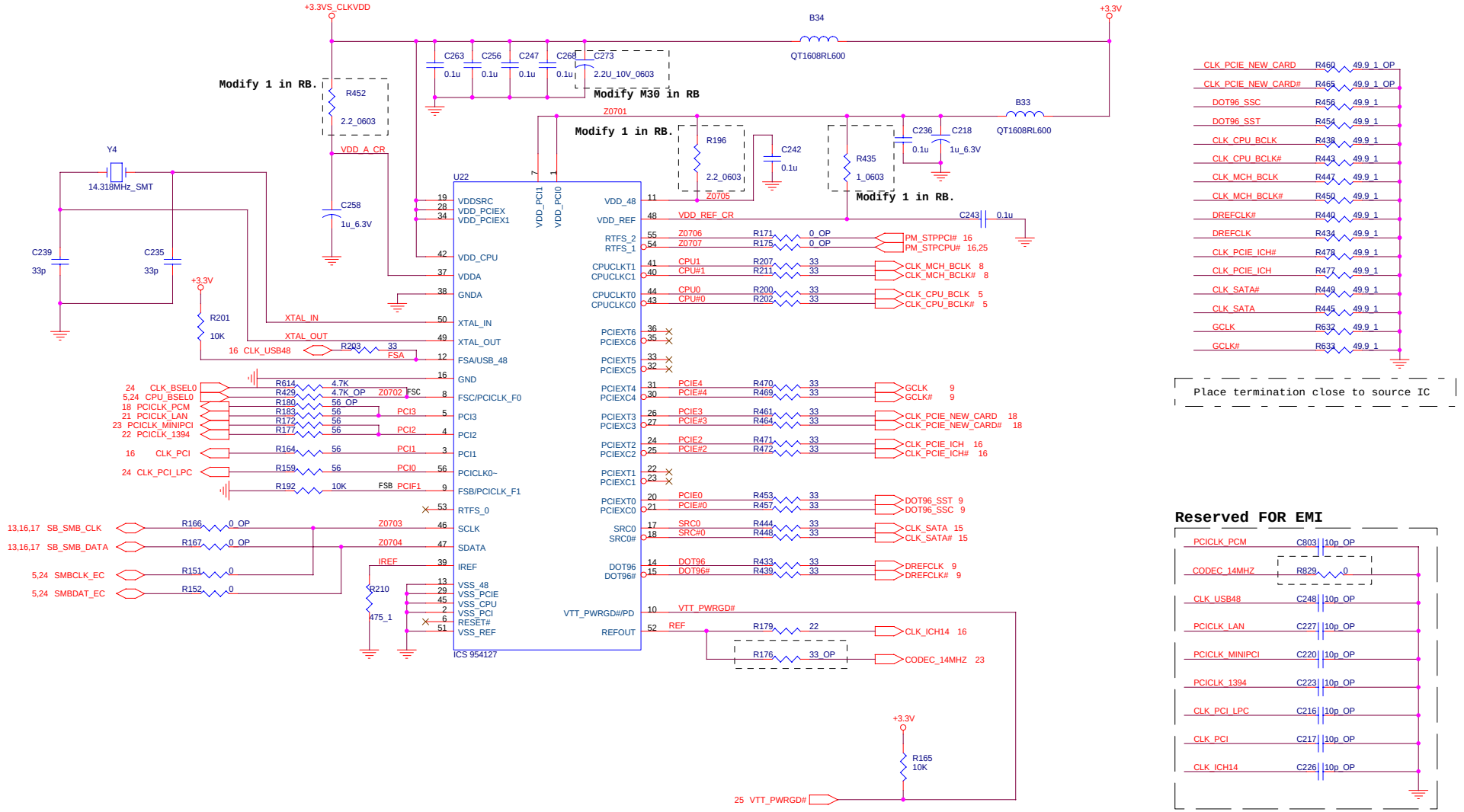
UNIWILL COMPUTER CORP.

Title: **MX0/M40/50EI0**

Size	Document Number	Rev
	CPU Banias/Dothan-1/2	C
	3017	

Date: Monday, July 25, 2005 Sheet 5 of 35


U37C
POWER
CPU_CORE
+1.5V
R58
QT1608RL060
R59
QT1608RL060_OP
+1.8V_SYSTEM
Z0601
FSB400 MHz=1.8V
FSB533 MHz=1.5V
Close to Pin
C339 0.1u
C43 4.7U_10V_0805
C340 0.1u
C338 0.1u
C39 0.1u
Z0603 R316 0
Z0604 R52 0
Reserved for FSB400 MHz
VCCA=120mA
+1.05V
H_VID0 14
H_VID1 14
H_VID2 14
H_VID3 14
H_VID4 14
H_VID5 14
Z0605
Z0606
TP19
TP20
Layout note :
VCCSENSE and VSSSENSE line
should be of equal length
C79 C348 C94 C74 C73 C346
C84 C80 C90 C93 C83 C91
4.7U_10V_0805
C98 C99 C107 C109 C101 C53 C105 C110 C100 C106
1u_6.3V
C111 C75 C51 C50
C104 C102 C108 C113 C112 C54 C52 C103 C97 C96
1000P
C55 C45 C37 C78 C89 C77 C95 C59 C92 C76 C86 C82 C87 C85 C81 C63 C64
0.1u
U37D
VSS
UNIWILL COMPUTER CORP.
Title
MX0/M40/50EI0
Size
Document Number
CPU Banias/Dothan-2/2
3017
Rev
C
Date: Monday, July 25, 2005
Sheet 6 of 35



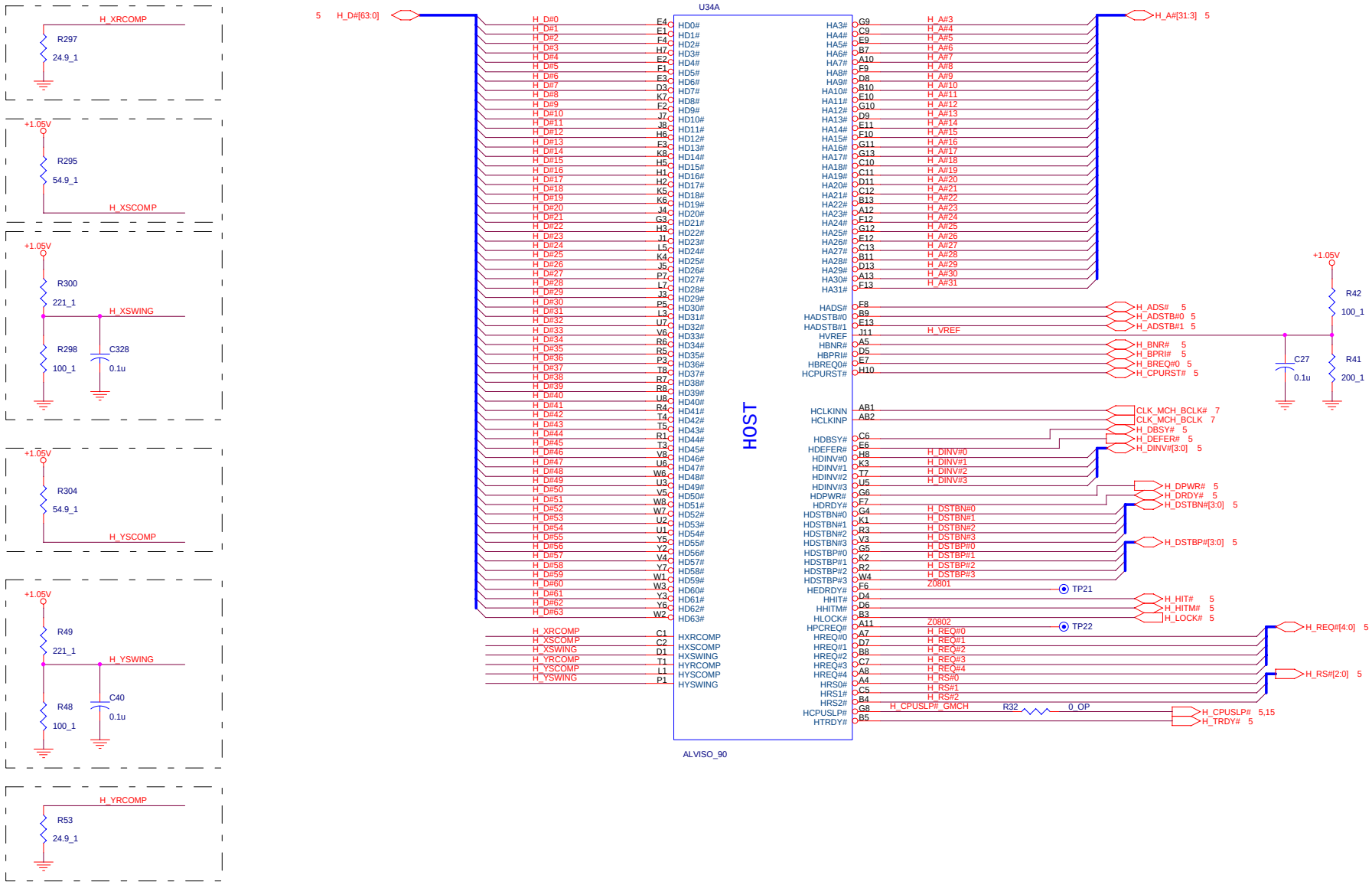
FSA BSEL2	FSB BSEL1	FSC BSEL0	Host Clock frequency
1	0	1	100
1	0	0	133

UNIWILL COMPUTER CORP.

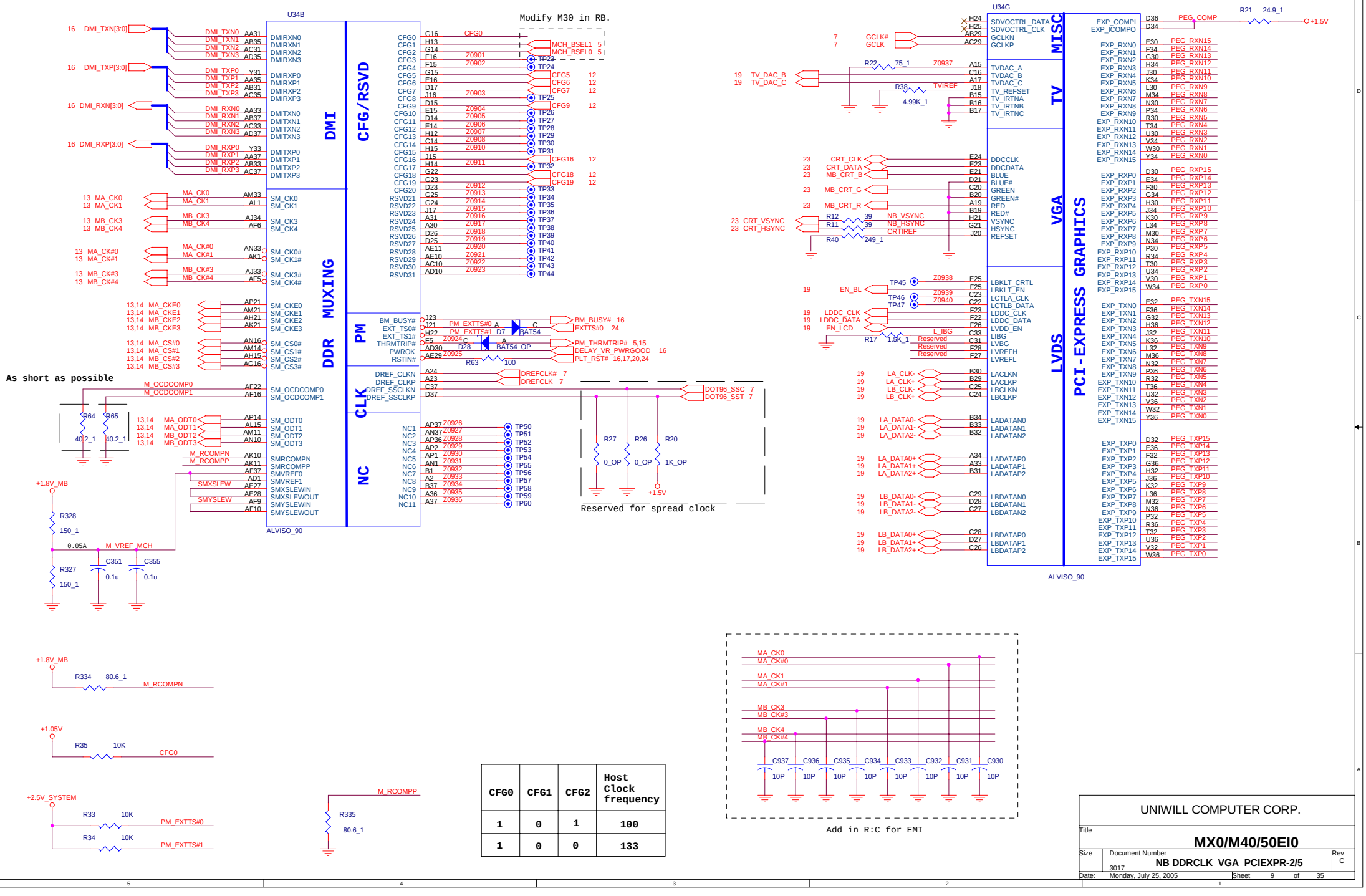
Title: **MX0/M40/50EI0**

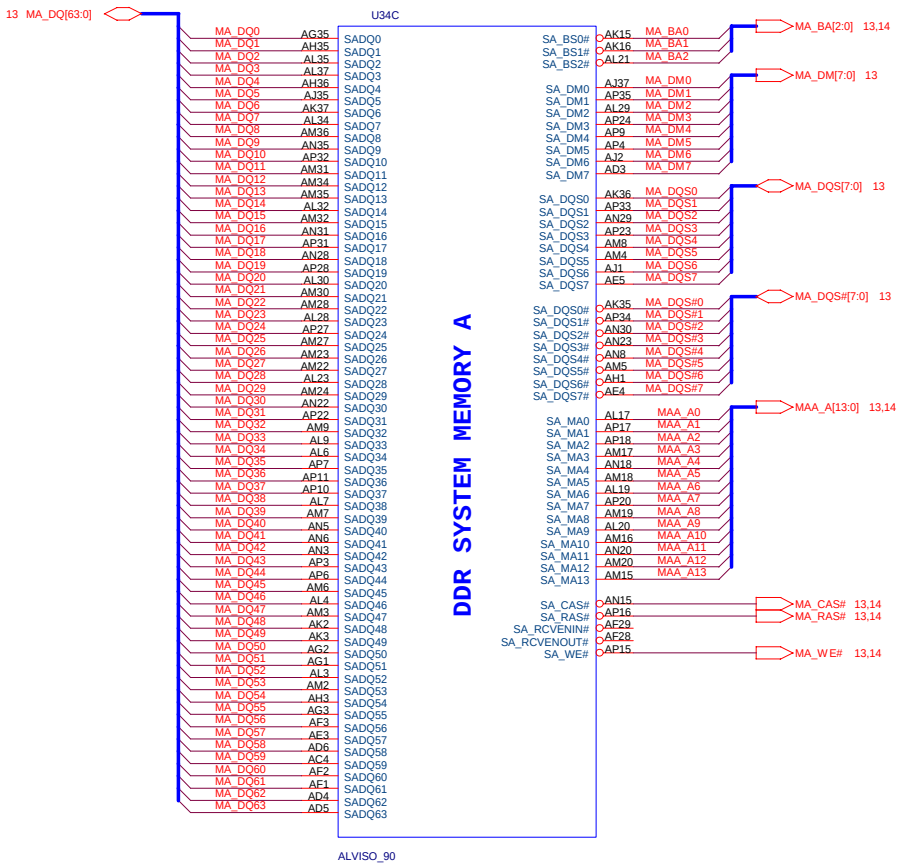
Size | Document Number: 3017 — CLOCK GEN ICS954206 | Rev C

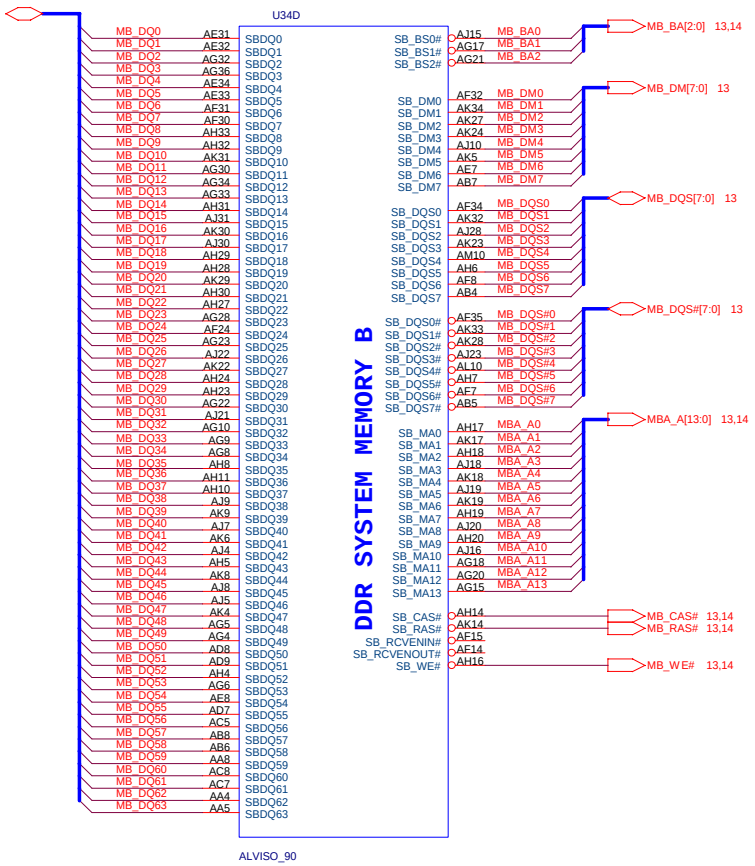
Date: Monday, July 25, 2005 | Sheet 7 of 35



UNIWILL COMPUTER CORP.			
Title: MX0/M40/50EI0			
Size	Document Number: NB_Alviso Host-1/5		Rev: C
	3017		
Date: Monday, July 25, 2005	Sheet 8 of 35		


U34B
DMI
DMIRXN0
DMIRXN1
DMIRXN2
DMIRXN3
DMIRXP0
DMIRXP1
DMIRXP2
DMIRXP3
DMITXN0
DMITXN1
DMITXN2
DMITXN3
DMITXP0
DMITXP1
DMITXP2
DMITXP3
DDR MUXING
SM_CK0
SM_CK1
SM_CK3
SM_CK4
SM_CK0#
SM_CK1#
SM_CK3#
SM_CK4#
SM_CKE0
SM_CKE1
SM_CKE2
SM_CKE3
SM_CS0#
SM_CS1#
SM_CS2#
SM_CS3#
SM_OCDCOMP0
SM_OCDCOMP1
SM_ODT0
SM_ODT1
SM_ODT2
SM_ODT3
SMRCOMPN
SMRCOMPP
SMVREF0
SMVREF1
SMXSLEWIN
SMXSLEWOUT
SMYSLEWIN
SMYSLEWOUT
ALVISO_90
CFG/RSVD
PM
CLK
NC
Modify M30 in RB.
As short as possible
Reserved for spread clock
U34G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
ALVISO_90
Add in R:C for EMI
CFG0
CFG1
CFG2
Host Clock frequency
100
133
UNIWILL COMPUTER CORP.
MX0/M40/50EI0
NB DDRCLK_VGA_PCIEXPR-2/5
3017
Rev C
Monday, July 25, 2005
Sheet 9 of 35



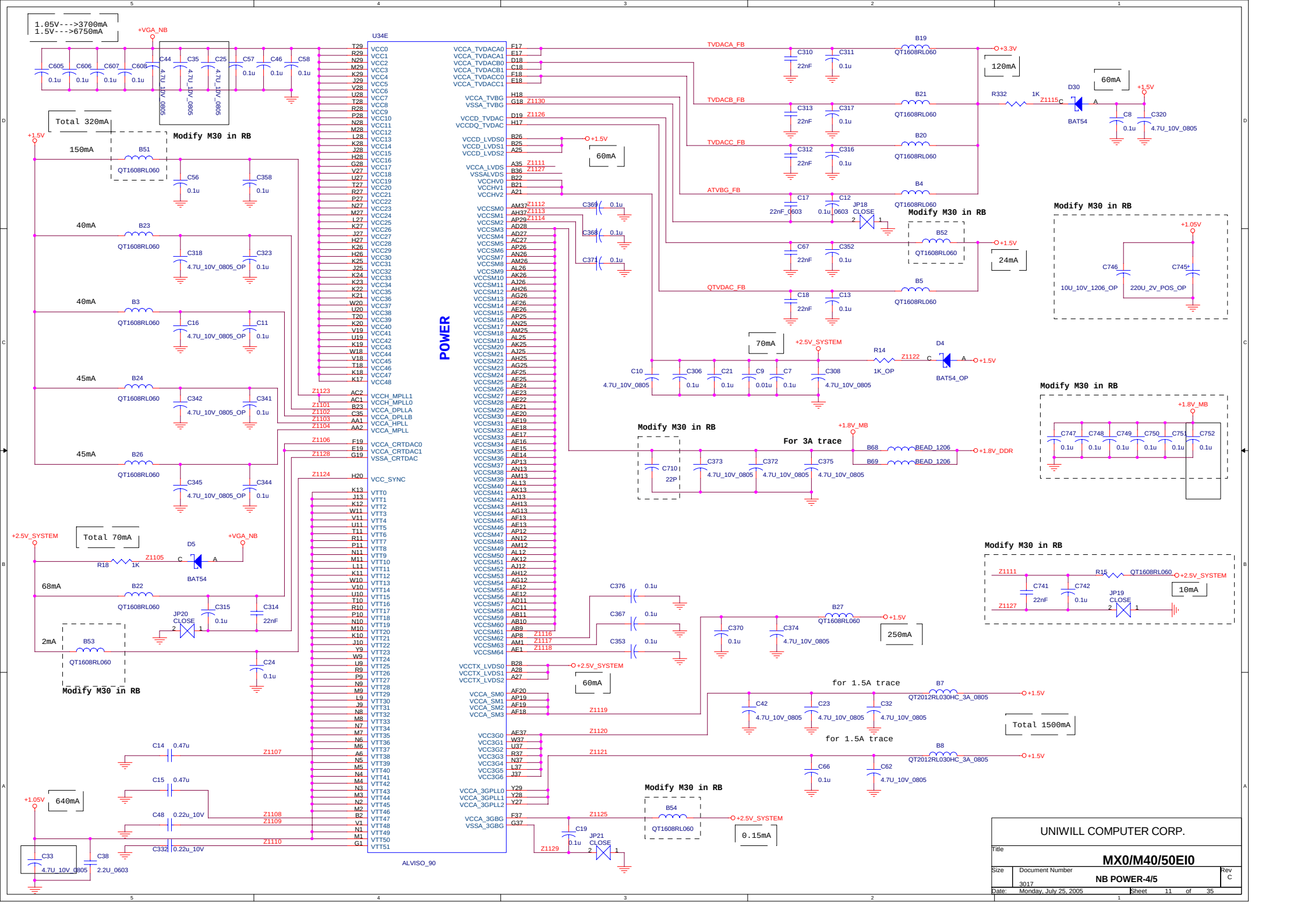


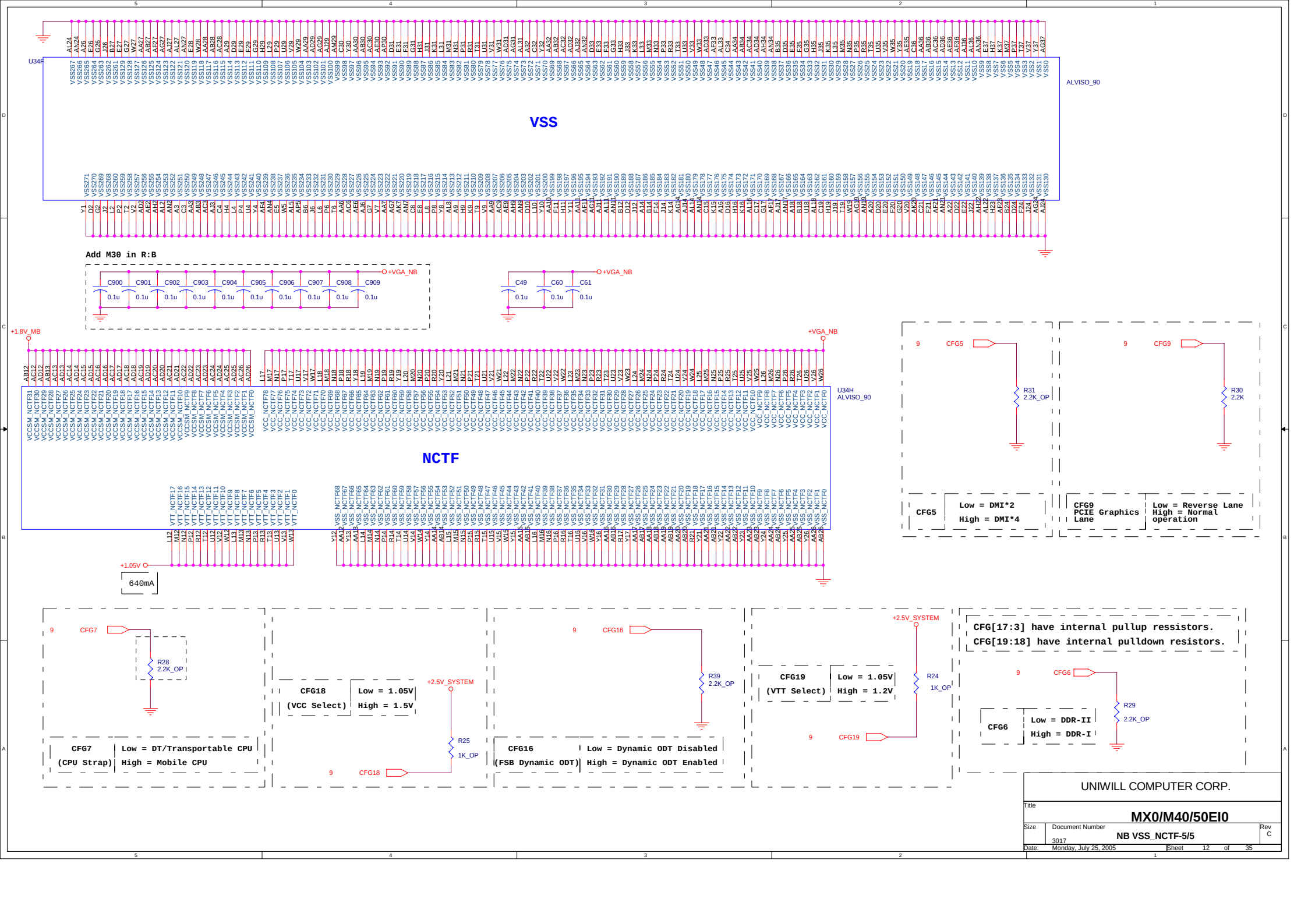
UNIWILL COMPUTER CORP.

Title: **MX0/M40/50EI0**

Size	Document Number	Rev
	3017 NB DDR_MEM SYSTEM-3/5	C

Date: Monday, July 25, 2005 Sheet 10 of 35


1.05V--->3700mA
1.5V--->6750mA
+VGA_NB
C605 0.1u
C606 0.1u
C607 0.1u
C608 0.1u
C44 4.7U_10V_0805
C35 4.7U_10V_0805
C25 4.7U_10V_0805
C57 0.1u
C46 0.1u
C58 0.1u
U34E
POWER
VCC0
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
VCC7
VCC8
VCC9
VCC10
VCC11
VCC12
VCC13
VCC14
VCC15
VCC16
VCC17
VCC18
VCC19
VCC20
VCC21
VCC22
VCC23
VCC24
VCC25
VCC26
VCC27
VCC28
VCC29
VCC30
VCC31
VCC32
VCC33
VCC34
VCC35
VCC36
VCC37
VCC38
VCC39
VCC40
VCC41
VCC42
VCC43
VCC44
VCC45
VCC46
VCC47
VCC48
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCA_TVBG
VSSA_TVBG
VCCD_TVDAC
VCCDQ_TVDAC
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCA_LVDS
VSSALVDS
VCCHV0
VCCHV1
VCCHV2
VCCSM0
VCCSM1
VCCSM2
VCCSM3
VCCSM4
VCCSM5
VCCSM6
VCCSM7
VCCSM8
VCCSM9
VCCSM10
VCCSM11
VCCSM12
VCCSM13
VCCSM14
VCCSM15
VCCSM16
VCCSM17
VCCSM18
VCCSM19
VCCSM20
VCCSM21
VCCSM22
VCCSM23
VCCSM24
VCCSM25
VCCSM26
VCCSM27
VCCSM28
VCCSM29
VCCSM30
VCCSM31
VCCSM32
VCCSM33
VCCSM34
VCCSM35
VCCSM36
VCCSM37
VCCSM38
VCCSM39
VCCSM40
VCCSM41
VCCSM42
VCCSM43
VCCSM44
VCCSM45
VCCSM46
VCCSM47
VCCSM48
VCCSM49
VCCSM50
VCCSM51
VCCSM52
VCCSM53
VCCSM54
VCCSM55
VCCSM56
VCCSM57
VCCSM58
VCCSM59
VCCSM60
VCCSM61
VCCSM62
VCCSM63
VCCSM64
VCCTX_LVDS0
VCCTX_LVDS1
VCCTX_LVDS2
VCCA_SM0
VCCA_SM1
VCCA_SM2
VCCA_SM3
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL0
VCCA_3GPLL1
VCCA_3GPLL2
VCCA_3GBG
VSSA_3GBG
VCCH_MPLL1
VCCH_MPLL0
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCC_SYNC
VTT0
VTT1
VTT2
VTT3
VTT4
VTT5
VTT6
VTT7
VTT8
VTT9
VTT10
VTT11
VTT12
VTT13
VTT14
VTT15
VTT16
VTT17
VTT18
VTT19
VTT20
VTT21
VTT22
VTT23
VTT24
VTT25
VTT26
VTT27
VTT28
VTT29
VTT30
VTT31
VTT32
VTT33
VTT34
VTT35
VTT36
VTT37
VTT38
VTT39
VTT40
VTT41
VTT42
VTT43
VTT44
VTT45
VTT46
VTT47
VTT48
VTT49
VTT50
VTT51
ALVISO_90
Total 320mA
Modify M30 in RB
+1.5V
150mA
B51
QT1608RL060
C56 0.1u
C358 0.1u
40mA
B23
QT1608RL060
C318 4.7U_10V_0805_OP
C323 0.1u
40mA
B3
QT1608RL060
C16 4.7U_10V_0805_OP
C11 0.1u
45mA
B24
QT1608RL060
C342 4.7U_10V_0805_OP
C341 0.1u
45mA
B26
QT1608RL060
C345 4.7U_10V_0805_OP
C344 0.1u
+2.5V_SYSTEM
Total 70mA
+VGA_NB
D5
R18 1K
Z1105
BAT54
68mA
B22
QT1608RL060
C315 0.1u
C314 22nF
JP20 CLOSE
2mA
B53
QT1608RL060
C24 0.1u
Modify M30 in RB
+1.05V
640mA
C33 4.7U_10V_0805
C38 2.2U_0603
C14 0.47u
C15 0.47u
C48 0.22u_10V
C332 0.22u_10V
Z1107
Z1108
Z1109
Z1110
Z1123
Z1101
Z1102
Z1103
Z1104
Z1106
Z1128
Z1124
Z1130
Z1126
Z1111
Z1127
Z1112
Z1113
Z1114
Z1116
Z1117
Z1118
Z1119
Z1120
Z1121
Z1125
Z1129
+1.5V
60mA
C369 0.1u
C368 0.1u
C371 0.1u
+2.5V_SYSTEM
60mA
C376 0.1u
C367 0.1u
C353 0.1u
C370 0.1u
C374 4.7U_10V_0805
B27
QT1608RL060
+1.5V
250mA
for 1.5A trace
B7
QT2012RL030HC_3A_0805
+1.5V
C42 4.7U_10V_0805
C23 4.7U_10V_0805
C32 4.7U_10V_0805
Total 1500mA
for 1.5A trace
B8
QT2012RL030HC_3A_0805
+1.5V
C66 0.1u
C62 4.7U_10V_0805
Modify M30 in RB
B54
QT1608RL060
+2.5V_SYSTEM
0.15mA
C19 0.1u
JP21 CLOSE
TVDACA_FB
TVDACB_FB
TVDACC_FB
ATVBG_FB
QTVDAC_FB
C310 22nF
C311 0.1u
B19
QT1608RL060
C313 22nF
C317 0.1u
B21
QT1608RL060
C312 22nF
C316 0.1u
B20
QT1608RL060
C17 22nF_0603
C12 0.1u_0603
B4
QT1608RL060
C67 22nF
C352 0.1u
B52
QT1608RL060
C18 22nF
C13 0.1u
B5
QT1608RL060
+3.3V
120mA
R332 1K
Z1115
D30
BAT54
60mA
+1.5V
C8 0.1u
C320 4.7U_10V_0805
JP18 CLOSE
Modify M30 in RB
+1.5V
24mA
Modify M30 in RB
+1.05V
C746 10U_10V_1206_OP
C745+ 220U_2V_POS_OP
70mA
+2.5V_SYSTEM
R14 1K_OP
Z1122
D4
BAT54_OP
+1.5V
C10 4.7U_10V_0805
C306 0.1u
C21 0.1u
C9 0.01u
C7 0.1u
C308 4.7U_10V_0805
Modify M30 in RB
+1.8V_MB
For 3A trace
C710 22P
C373 4.7U_10V_0805
C372 4.7U_10V_0805
C375 4.7U_10V_0805
B68 BEAD_1206
B69 BEAD_1206
+1.8V_DDR
Modify M30 in RB
+1.8V_MB
C747 0.1u
C748 0.1u
C749 0.1u
C750 0.1u
C751 0.1u
C752 0.1u
Modify M30 in RB
Z1111
Z1127
C741 22nF
C742 0.1u
R15 QT1608RL060
+2.5V_SYSTEM
10mA
JP19 CLOSE
UNIWILL COMPUTER CORP.
Title
MX0/M40/50EI0
Size
Document Number
NB POWER-4/5
3017
Rev C
Date: Monday, July 25, 2005
Sheet 11 of 35

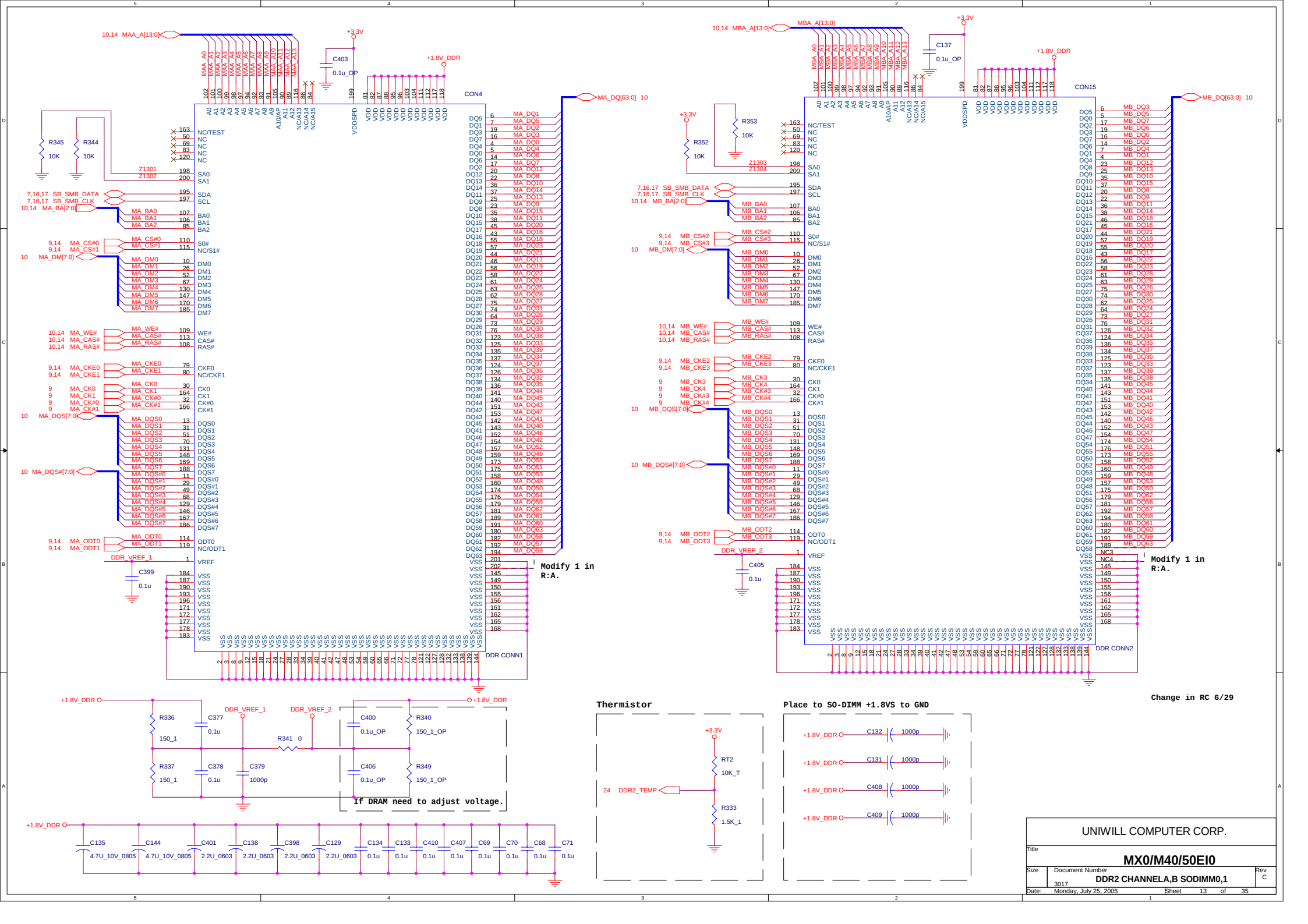


UNIWILL COMPUTER CORP.

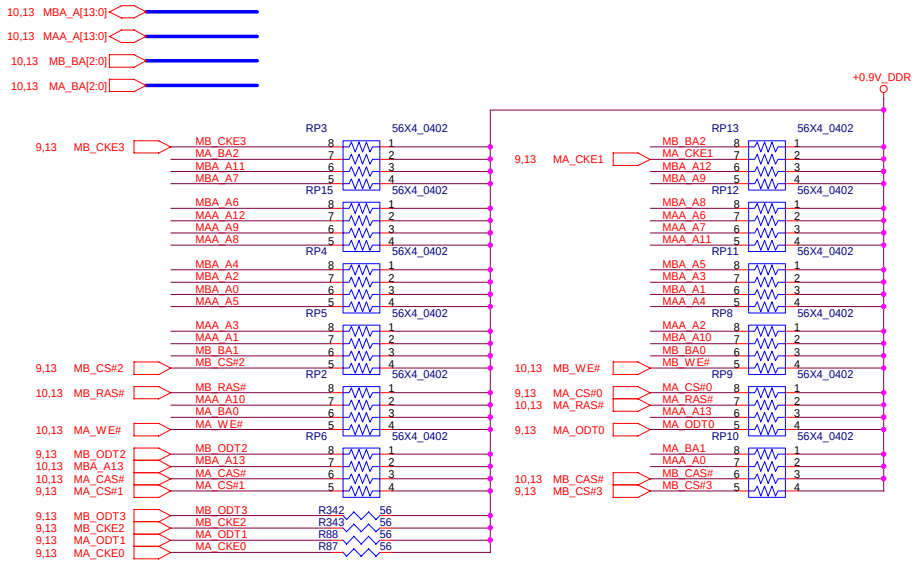
Title: MX0/M40/50EI0

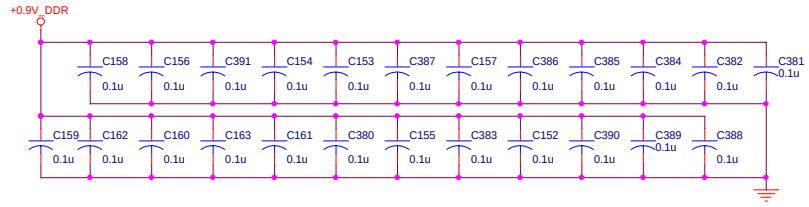
Size | Document Number: 3017 NB VSS_NCTF-5/5 | Rev C

Date: Monday, July 25, 2005 | Sheet 12 of 35

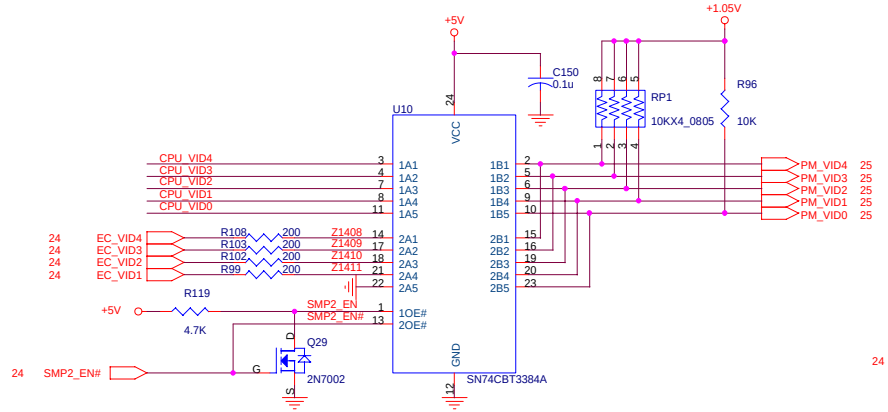

10,14 MAA_A[13:0]
+3.3V
C403
0.1u_OP
+1.8V_DDR
CON4
R345
10K
R344
10K
Z1301
Z1302
7,16,17 SB_SMB_DATA
7,16,17 SB_SMB_CLK
10,14 MA_BA[2:0]
9,14 MA_CS#0
9,14 MA_CS#1
10 MA_DM[7:0]
10,14 MA_WE#
10,14 MA_CAS#
10,14 MA_RAS#
9,14 MA_CKE0
9,14 MA_CKE1
9 MA_CK0
9 MA_CK1
9 MA_CK#0
9 MA_CK#1
10 MA_DQS[7:0]
10 MA_DQS#[7:0]
9,14 MA_ODT0
9,14 MA_ODT1
DDR_VREF_1
C399
0.1u
MA_DQ[63:0] 10
Modify 1 in R:A.
DDR CONN1
10,14 MBA_A[13:0]
C137
0.1u_OP
R353
10K
R352
10K
7,16,17 SB_SMB_DATA
7,16,17 SB_SMB_CLK
10,14 MB_BA[2:0]
9,14 MB_CS#2
9,14 MB_CS#3
10 MB_DM[7:0]
10,14 MB_WE#
10,14 MB_CAS#
10,14 MB_RAS#
9,14 MB_CKE2
9,14 MB_CKE3
9 MB_CK3
9 MB_CK4
9 MB_CK#3
9 MB_CK#4
10 MB_DQS[7:0]
10 MB_DQS#[7:0]
9,14 MB_ODT2
9,14 MB_ODT3
DDR_VREF_2
C405
0.1u
CON15
MB_DQ[63:0] 10
Modify 1 in R:A.
DDR CONN2
Change in RC 6/29
+1.8V_DDR
R336
150_1
C377
0.1u
DDR_VREF_1
DDR_VREF_2
R341 0
C400
0.1u_OP
R340
150_1_OP
R337
150_1
C378
0.1u
C379
1000p
C406
0.1u_OP
R349
150_1_OP
If DRAM need to adjust voltage.
C135
4.7U_10V_0805
C144
4.7U_10V_0805
C401
2.2U_0603
C138
2.2U_0603
C398
2.2U_0603
C129
2.2U_0603
C134
0.1u
C133
0.1u
C410
0.1u
C407
0.1u
C69
0.1u
C70
0.1u
C68
0.1u
C71
0.1u
Thermistor
+3.3V
RT2
10K_T
24 DDR2_TEMP
R333
1.5K_1
Place to SO-DIMM +1.8VS to GND
C132
1000p
C131
1000p
C408
1000p
C409
1000p
UNIWILL COMPUTER CORP.
Title
MX0/M40/50EI0
Size
Document Number
DDR2 CHANNELA,B SODIMM0,1
3017
Rev
C
Date: Monday, July 25, 2005
Sheet 13 of 35

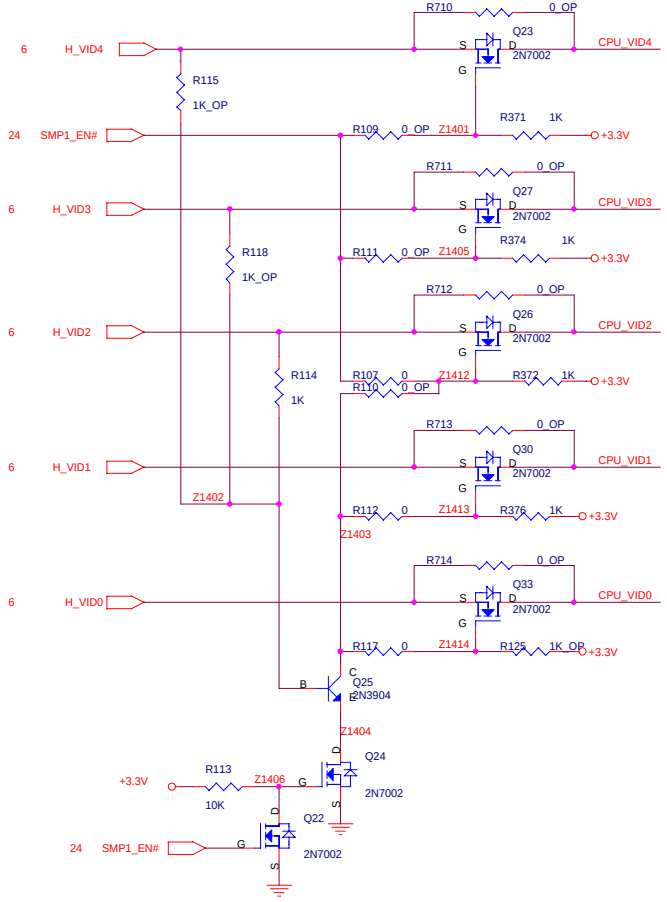
SMART POWER





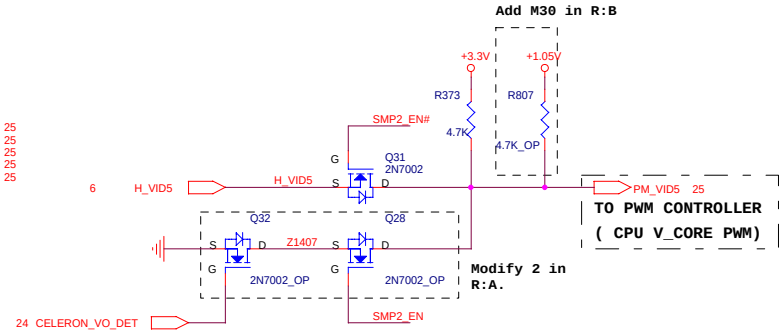
Layout note: Place one cap close to every 2 pullup resistors terminated to DDR_VREF





VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	1	1	0	1	1	1.276	
0	1	1	1	0	0	1.260	
0	1	1	1	1	0	1.228	
1	0	0	0	0	0	1.196	
1	0	0	0	1	0	1.164	
1	0	0	1	0	1	1.116	
1	0	0	1	1	0	1.100	
1	0	1	0	1	0	1.036	
1	0	1	0	1	1	1.020	
1	0	1	1	0	0	1.004	
1	0	1	1	0	1	0.988	
1	0	1	1	1	0	0.972	
1	0	1	1	1	1	0.956	
1	1	0	1	1	0	0.844	
1	1	1	1	1	1	0.716	

VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	1.708	-0mV
0	0	0	0	1	0	1.676	-32mV
0	0	0	1	0	0	1.644	-64mV
0	0	1	0	0	0	1.580	-128mV
0	1	0	0	0	0	1.452	-256mV
0	0	1	0	1	0	1.548	
0	0	1	0	1	1	1.532	
0	0	1	1	0	0	1.516	
0	0	1	1	1	0	1.484	
0	1	0	0	0	1	1.436	
0	1	0	0	1	0	1.420	
0	1	0	1	0	0	1.388	
0	1	0	1	1	0	1.356	
0	1	1	0	0	1	1.308	
0	1	1	0	1	0	1.292	

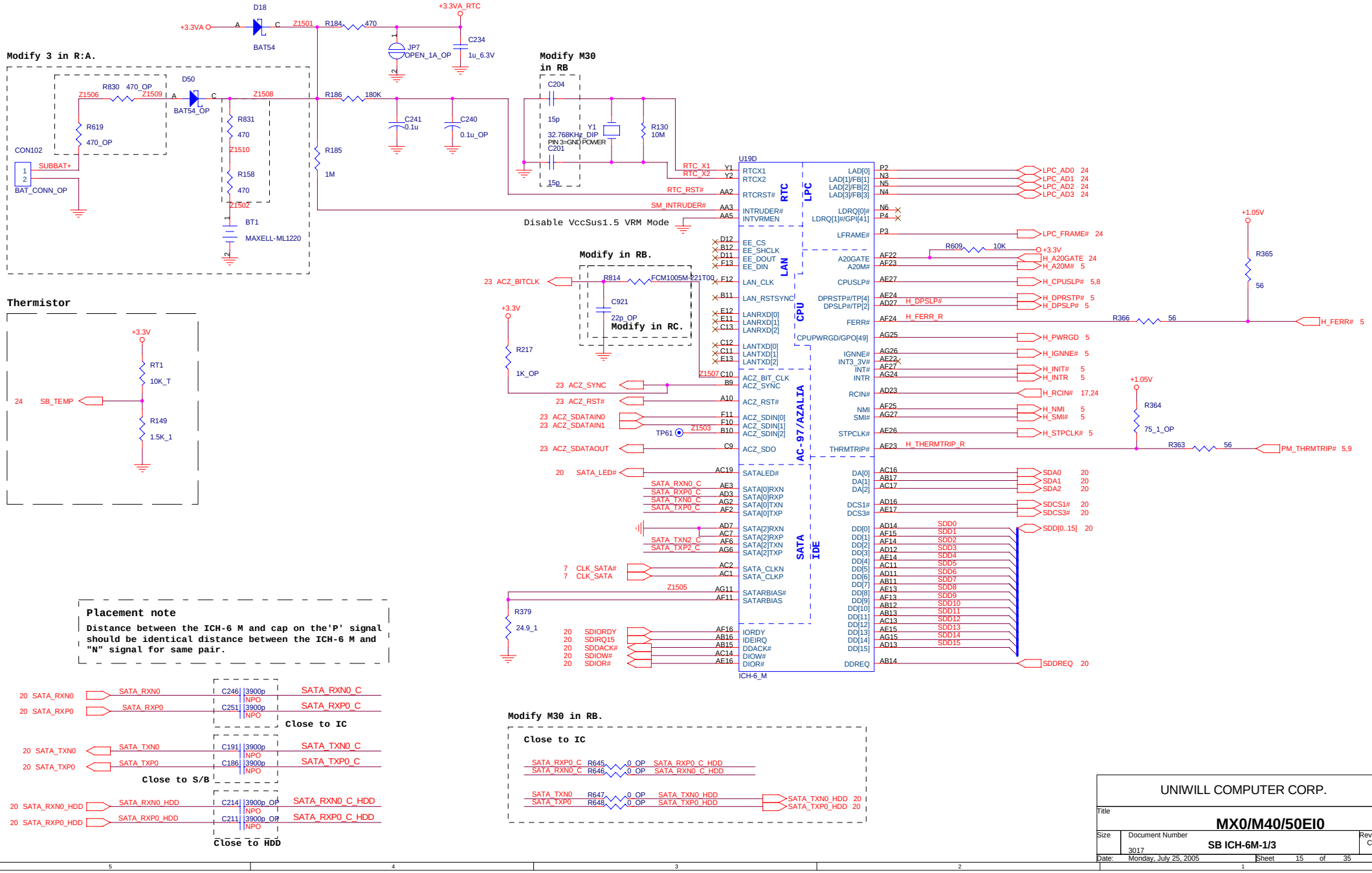


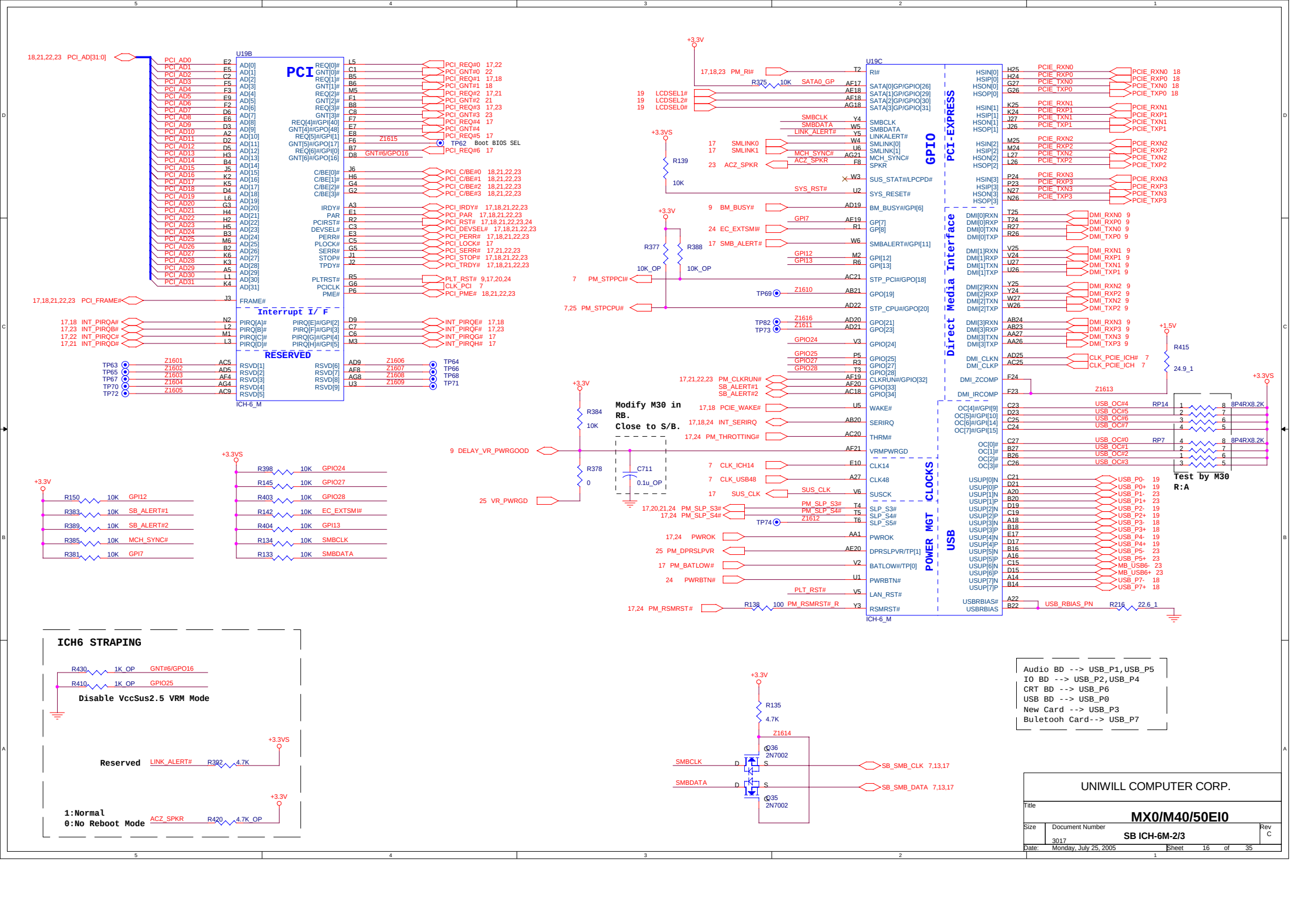
UNIWILL COMPUTER CORP.

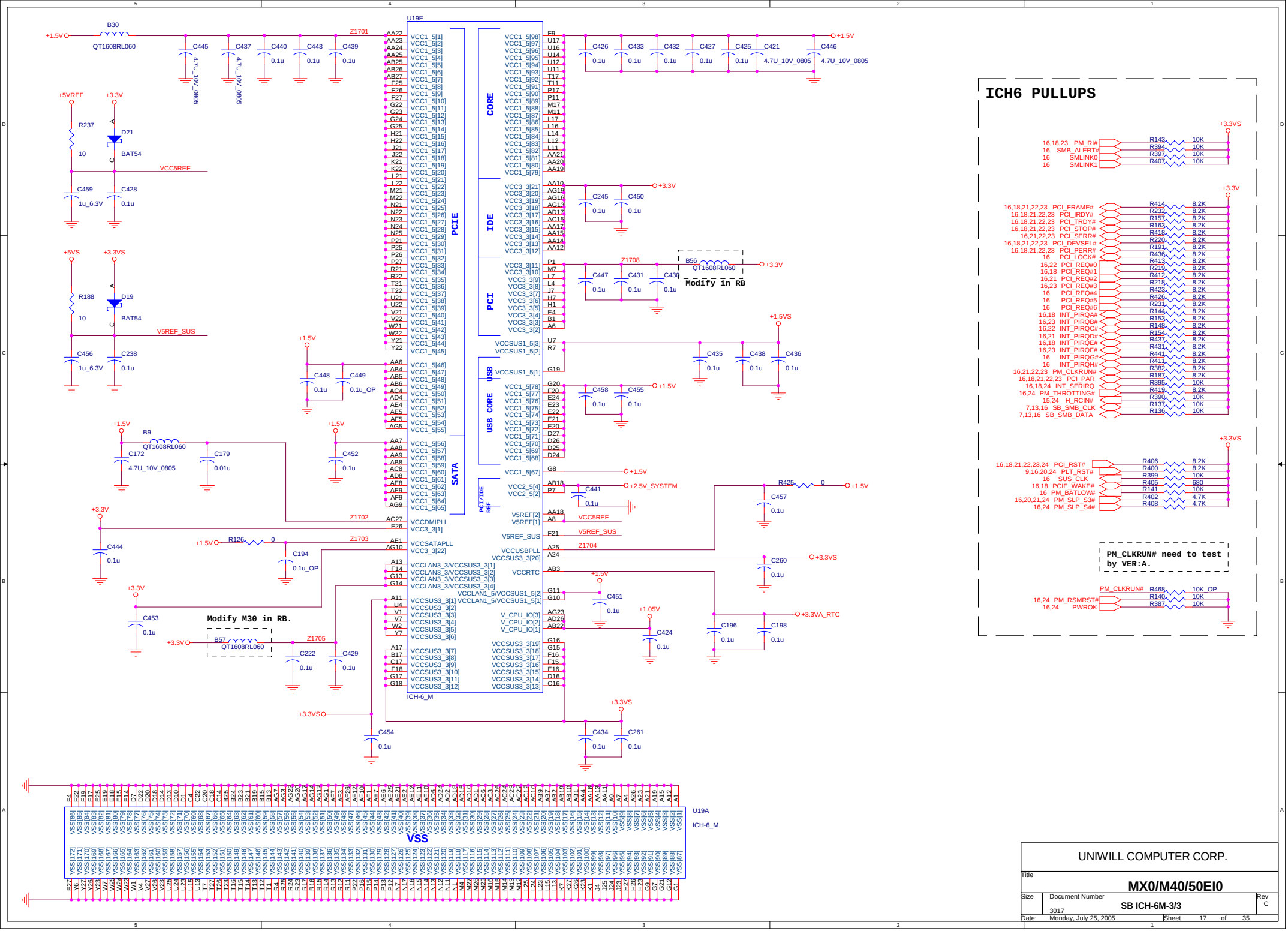
Title: **MX0/M40/50EI0**

Size | Document Number: 3017 | **DDR Terminate / Smart Power** | Rev C

Date: Monday, July 25, 2005 | Sheet 14 of 35


Modify 3 in R:A.
D18
BAT54
+3.3VA
+3.3VA_RTC
Z1501
R184
470
JP7
OPEN_1A_OP
C234
1u_6.3V
D50
BAT54_OP
R830
470_OP
Z1506
Z1509
Z1508
R186
180K
R619
470_OP
R831
470
Z1510
R158
470
Z1502
R185
1M
C241
0.1u
C240
0.1u_OP
CON102
SUBBAT+
BAT_CONN_OP
BT1
MAXELL-ML1220
Modify M30
in RB
C204
15p
C201
15p
Y1
32.768KHz_DIP
PIN3=GND POWER
R130
10M
RTC_X1
RTC_X2
RTC_RST#
SM_INTRUDER#
Disable VccSus1.5 VRM Mode
U19D
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
LAD[0]
LAD[1]/FB[1]
LAD[2]/FB[2]
LAD[3]/FB[3]
LDRQ[0]#
LDRQ[1]#/GPI[41]
LFRAME#
LPC_AD0 24
LPC_AD1 24
LPC_AD2 24
LPC_AD3 24
LPC_FRAME# 24
Modify in RB.
Modify in RC.
R814
FCM1005M-221T00
C921
22p_OP
23 ACZ_BITCLK
R217
1K_OP
+3.3V
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LANRXD[0]
LANRXD[1]
LANRXD[2]
LANTXD[0]
LANTXD[1]
LANTXD[2]
LAN
CPU
A20GATE
A20M#
CPUSLP#
DPRSTP#/TP[4]
DPSLP#/TP[2]
FERR#
CPUPWRGD/GPO[49]
IGNNE#
INT3_3V#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
R609
10K
+3.3V
H_A20GATE 24
H_A20M# 5
H_CPUSLP# 5,8
H_DPRSTP# 5
H_DPSLP# 5
H_FERR# 5
H_PWRGD 5
H_IGNNE# 5
H_INIT# 5
H_INTR 5
H_RCIN# 17,24
H_NMI 5
H_SMI# 5
H_STPCLK# 5
H_THERMTRIP# 5,9
R365
56
R366
56
R364
75_1_OP
R363
56
+1.05V
PM_THRMTRIP# 5,9
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN[0]
ACZ_SDIN[1]
ACZ_SDIN[2]
ACZ_SDO
AC-97/AZALIA
23 ACZ_SYNC
23 ACZ_RST#
23 ACZ_SDATAIN0
23 ACZ_SDATAIN1
23 ACZ_SDATAOUT
TP61
Z1503
Z1507
SATALED#
SATA[0]RXN
SATA[0]RXP
SATA[0]TXN
SATA[0]TXP
SATA[2]RXN
SATA[2]RXP
SATA[2]TXN
SATA[2]TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
20 SATA_LED#
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_TXN2_C
SATA_TXP2_C
7 CLK_SATA#
7 CLK_SATA
Z1505
R379
24.9_1
SATA
IDE
IORDY
IDEIRQ
DDACK#
DIOW#
DIOR#
DDREQ
DA[0]
DA[1]
DA[2]
DCS1#
DCS3#
DD[0]
DD[1]
DD[2]
DD[3]
DD[4]
DD[5]
DD[6]
DD[7]
DD[8]
DD[9]
DD[10]
DD[11]
DD[12]
DD[13]
DD[14]
DD[15]
SDA0 20
SDA1 20
SDA2 20
SDCS1# 20
SDCS3# 20
SDD[0..15] 20
SDDREQ 20
20 SDIORDY
20 SDIRQ15
20 SDDACK#
20 SDIOW#
20 SDIOR#
Thermistor
RT1
10K_T
24 SB_TEMP
R149
1.5K_1
Placement note
Distance between the ICH-6 M and cap on the'P' signal should be identical distance between the ICH-6 M and "N" signal for same pair.
20 SATA_RXN0
20 SATA_RXP0
SATA_RXN0
SATA_RXP0
C246 3900p NPO
C251 3900p NPO
SATA_RXN0_C
SATA_RXP0_C
Close to IC
20 SATA_TXN0
20 SATA_TXP0
SATA_TXN0
SATA_TXP0
C191 3900p NPO
C186 3900p NPO
SATA_TXN0_C
SATA_TXP0_C
Close to S/B
20 SATA_RXN0_HDD
20 SATA_RXP0_HDD
SATA_RXN0_HDD
SATA_RXP0_HDD
C214 3900p_OP NPO
C211 3900p_OP NPO
SATA_RXN0_C_HDD
SATA_RXP0_C_HDD
Close to HDD
Modify M30 in RB.
Close to IC
SATA_RXP0_C R645 0_OP SATA_RXP0_C_HDD
SATA_RXN0_C R646 0_OP SATA_RXN0_C_HDD
SATA_TXN0 R647 0_OP SATA_TXN0_HDD
SATA_TXP0 R648 0_OP SATA_TXP0_HDD
SATA_TXN0_HDD 20
SATA_TXP0_HDD 20
UNIWILL COMPUTER CORP.
Title
MX0/M40/50EI0
Size
Document Number
3017
SB ICH-6M-1/3
Rev C
Date: Monday, July 25, 2005
Sheet 15 of 35


U19B
PCI
Interrupt I/ F
RESERVED
ICH-6_M
U19C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
POWER MGT
USB
ICH-6_M
Modify M30 in RB.
Close to S/B.
Test by M30 R:A
ICH6 STRAPING
Disable VccSus2.5 VRM Mode
Reserved
1:Normal
0:No Reboot Mode
Audio BD --> USB_P1,USB_P5
IO BD --> USB_P2,USB_P4
CRT BD --> USB_P6
USB BD --> USB_P0
New Card --> USB_P3
Buletooh Card--> USB_P7
UNIWILL COMPUTER CORP.
MX0/M40/50EI0
SB ICH-6M-2/3
Rev C
Monday, July 25, 2005
Sheet 16 of 35

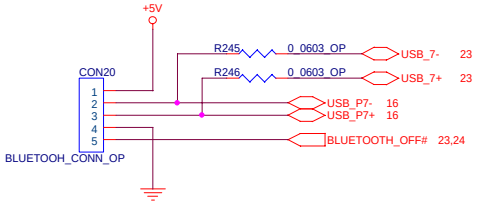


Title	MX0/M40/50EI0
Size	Document Number: SB ICH-6M-3/3
Rev	C
Date:	Monday, July 25, 2005
Sheet	17 of 35

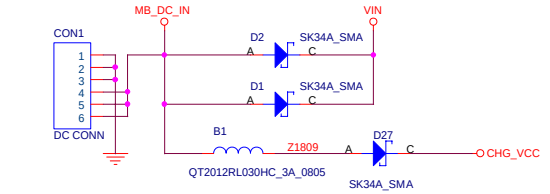
UNIWILL COMPUTER CORP.

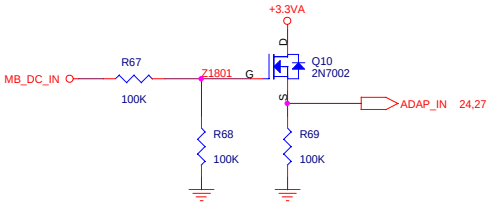
MIC CON

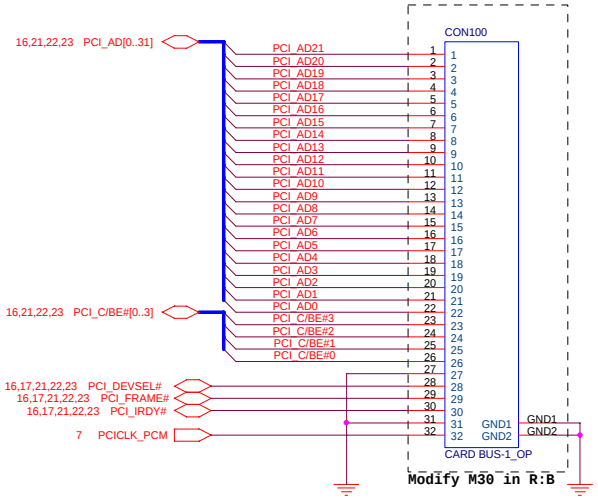
BLUETOOH CONN

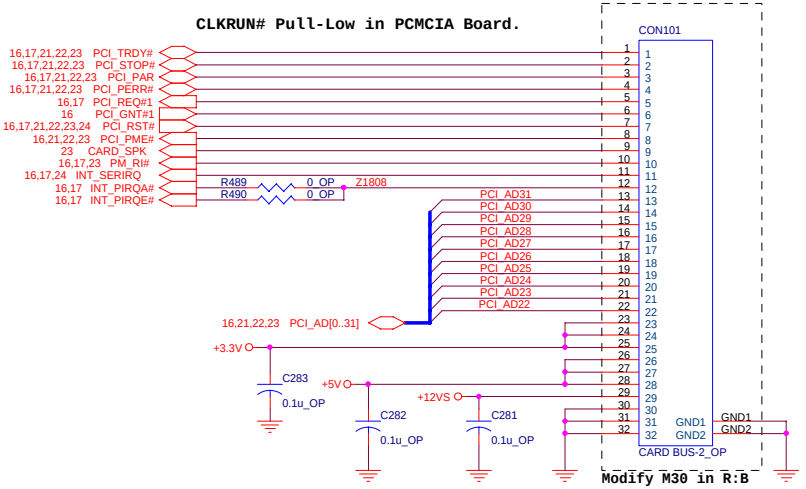


DC IN

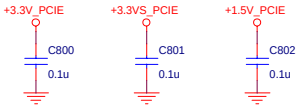


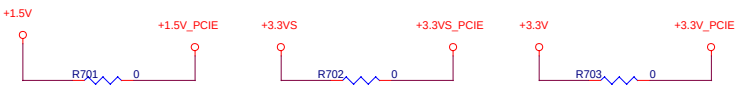


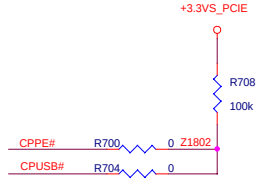




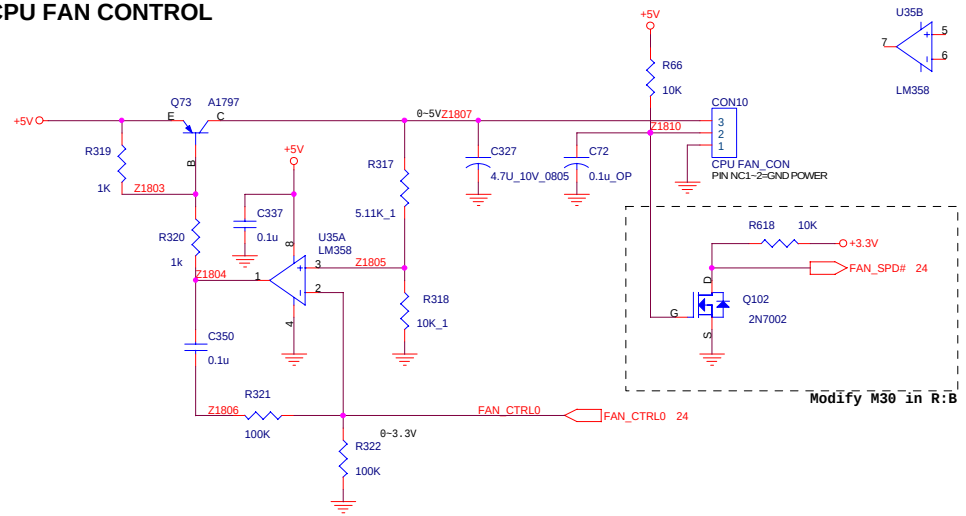
NEW CARD

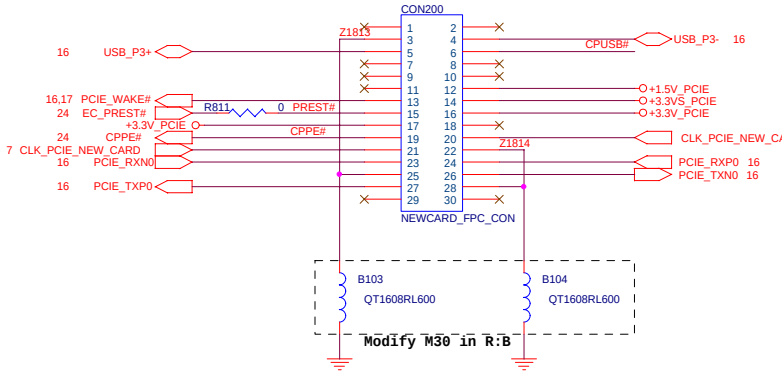




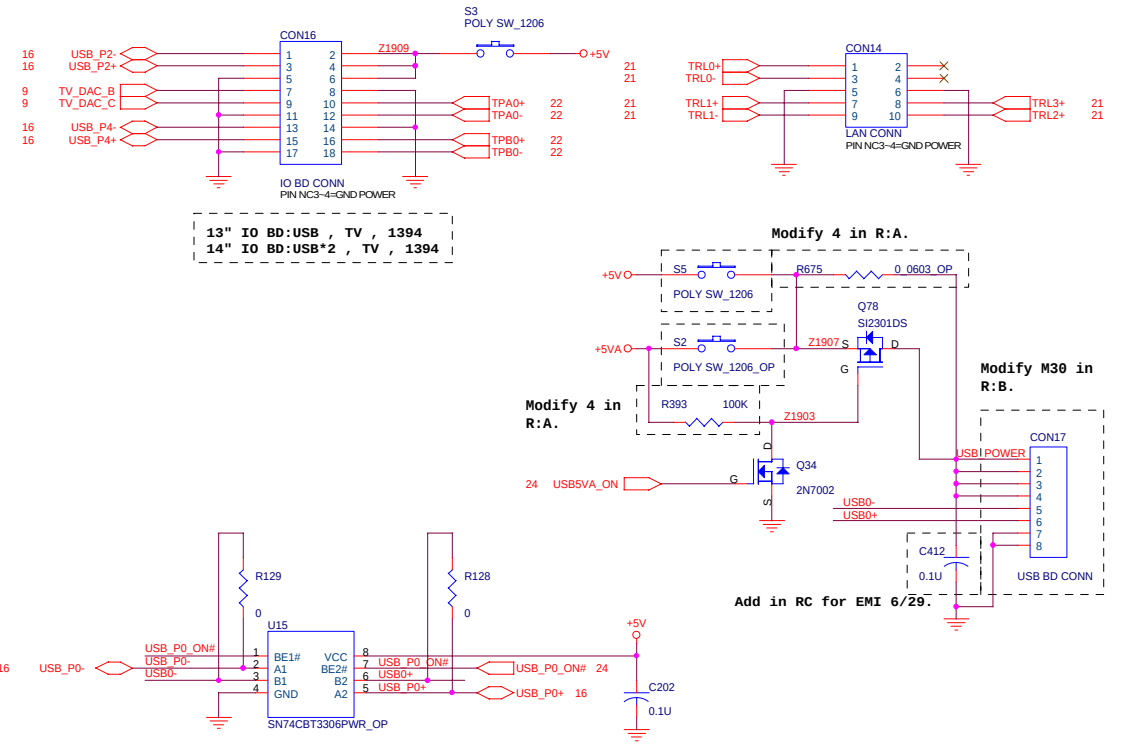


CPU FAN CONTROL

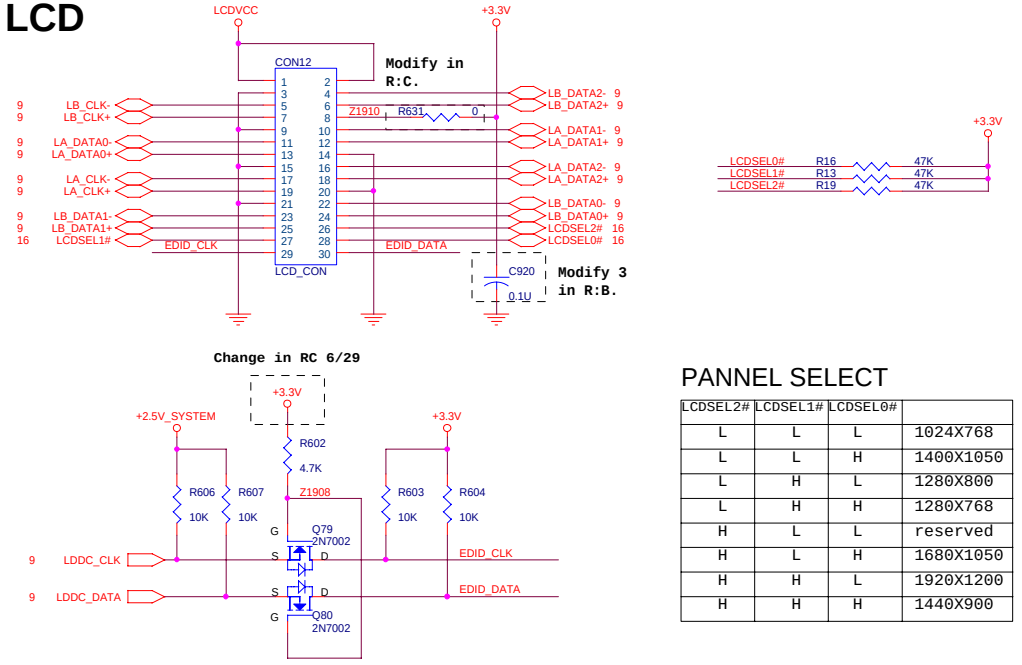




UNIWILL COMPUTER CORP.		
Title: MX0/M40/50EI0		
Size	Document Number: DC IN / CARD BUS / FAN / MIC / BLUETOOH	Rev: C
Date: Monday, July 25, 2005	Sheet 18 of 35	



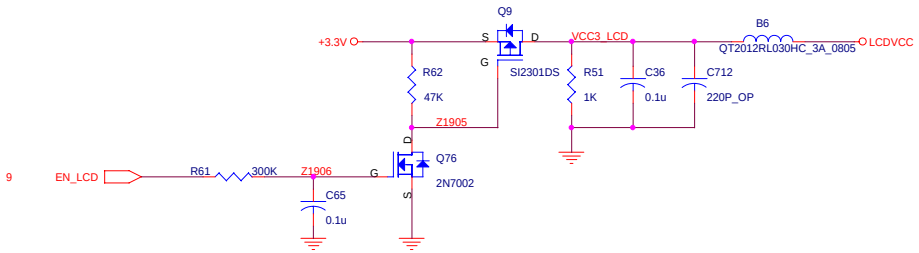
LCD

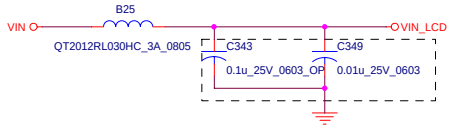


PANNEL SELECT

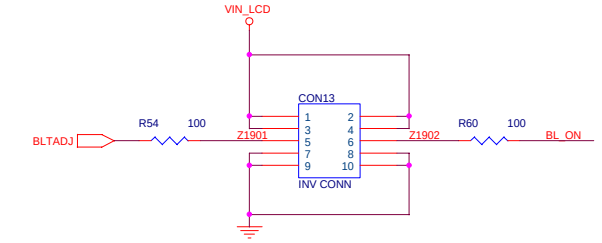
LCDSEL2#	LCDSEL1#	LCDSEL0#	
L	L	L	1024X768
L	L	H	1400X1050
L	H	L	1280X800
L	H	H	1280X768
H	L	L	reserved
H	L	H	1680X1050
H	H	L	1920X1200
H	H	H	1440X900

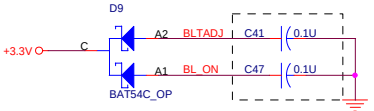
INVERTER



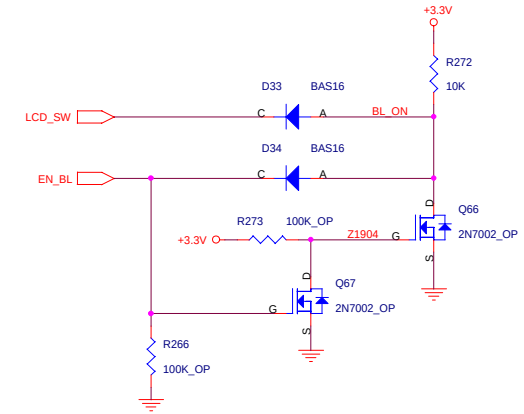


Modify M30 in R:B.

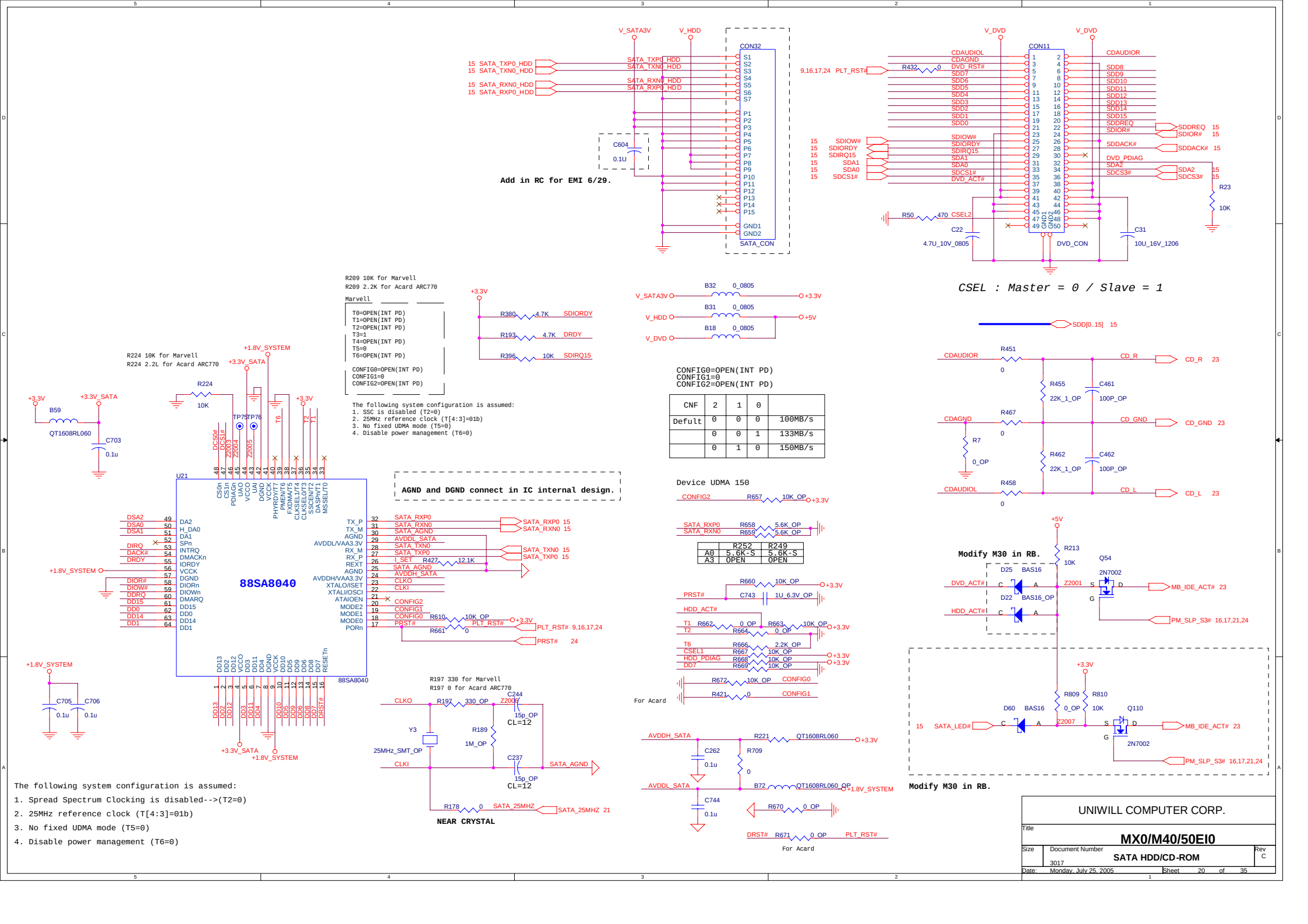




Add in RC for EMI 6/29.

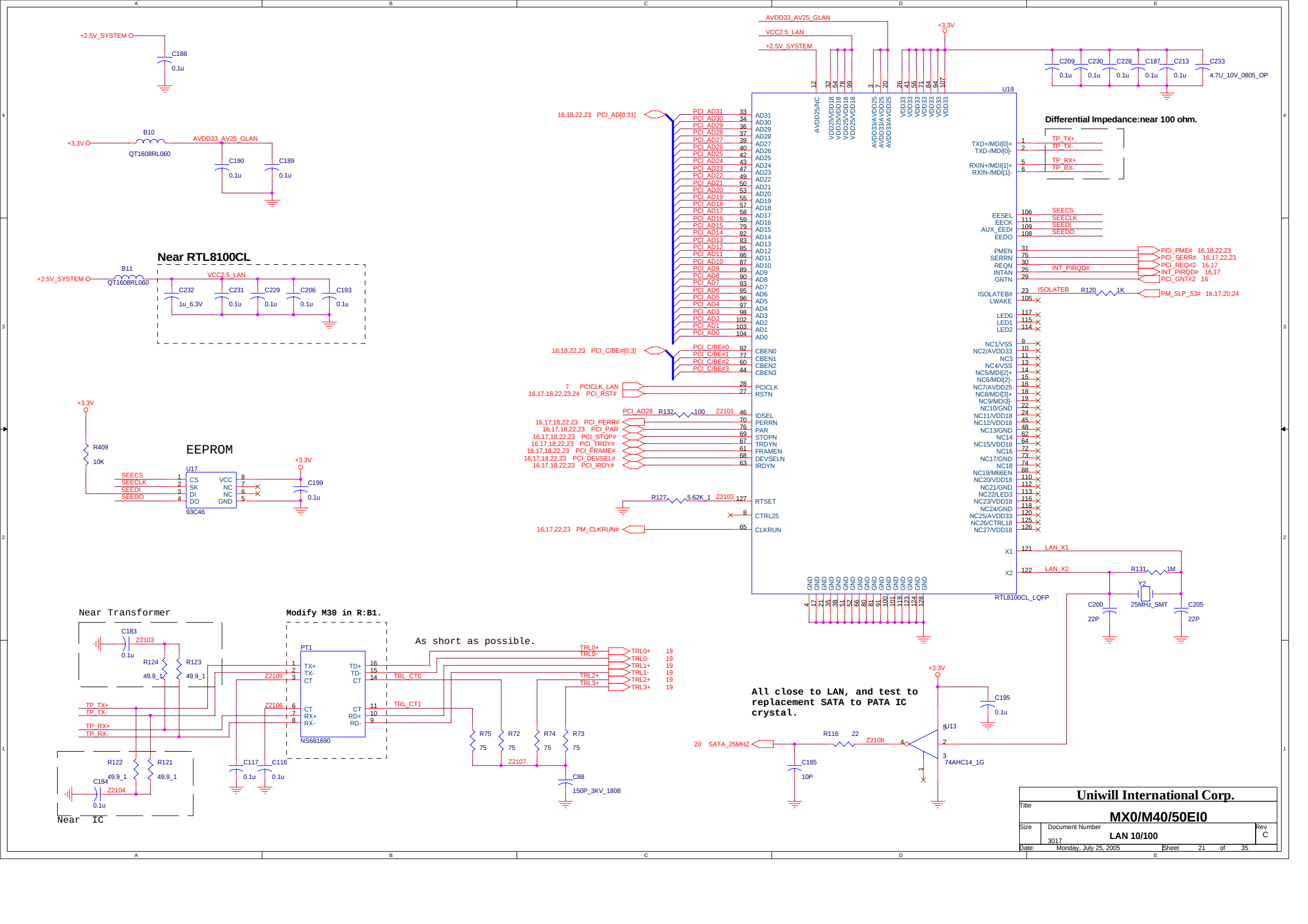


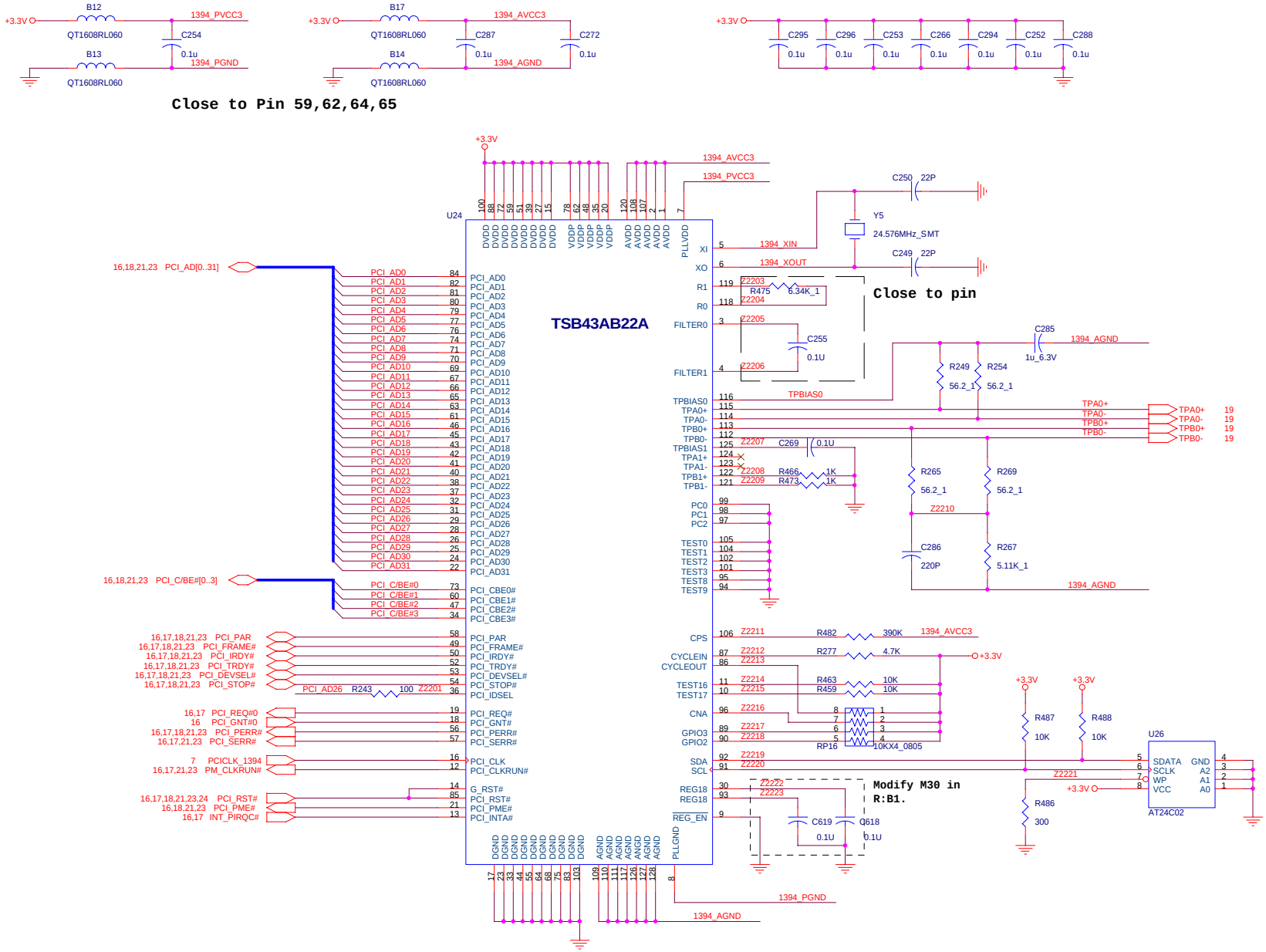
UNIWILL COMPUTER CORP.		
Title: MX0/M40/50EI0		
Size	Document Number: LCD/INVERTOR/CRT/TV 3017	Rev C
Date: Monday, July 25, 2005	Sheet 19 of 35	



The following system configuration is assumed:

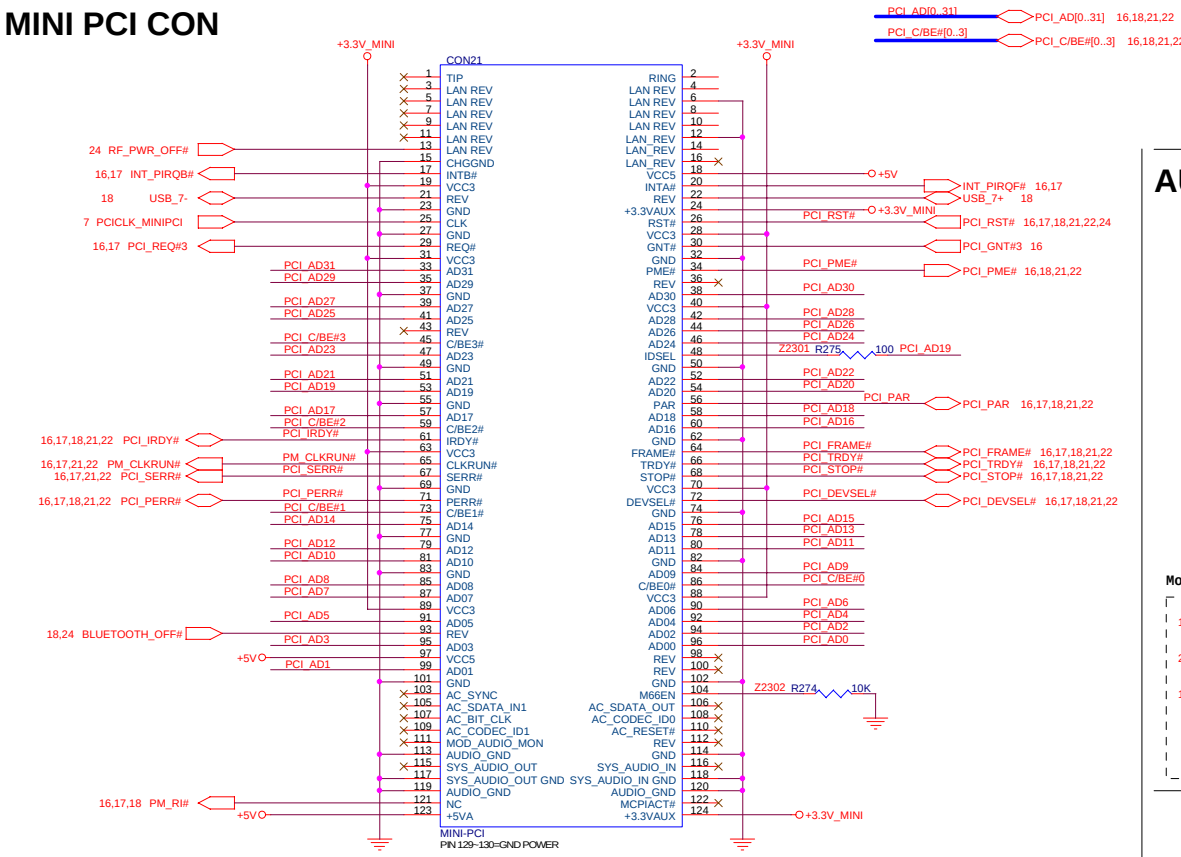
1. Spread Spectrum Clocking is disabled-->(T2=0)
2. 25MHz reference clock (T[4:3]=01b)
3. No fixed UDMA mode (T5=0)
4. Disable power management (T6=0)

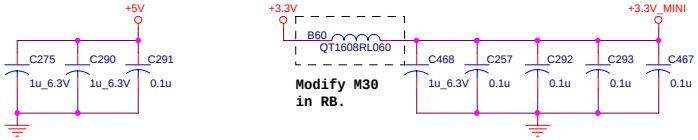

+2.5V_SYSTEM
C188
0.1u
+3.3V
B10
QT1608RL060
AVDD33_AV25_GLAN
C190
C189
0.1u
0.1u
Near RTL8100CL
B11
+2.5V_SYSTEM
QT1608RL060
VCC2.5_LAN
C232
C231
C229
C206
C193
1u_6.3V
0.1u
0.1u
0.1u
0.1u
+3.3V
R409
10K
EEPROM
U17
SEECS
SEECLK
SEEDI
SEEDO
CS
SK
DI
DO
VCC
NC
NC
GND
93C46
+3.3V
C199
0.1u
AVDD33_AV25_GLAN
VCC2.5_LAN
+2.5V_SYSTEM
+3.3V
C209
C230
C228
C187
C213
C233
0.1u
0.1u
0.1u
0.1u
0.1u
4.7U_10V_0805_OP
U18
AVDD25/NC
VDD25/VDD18
AVDD33/AVDD25
VDD33
16,18,22,23 PCI_AD[0:31]
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_AD23
PCI_AD22
PCI_AD21
PCI_AD20
PCI_AD19
PCI_AD18
PCI_AD17
PCI_AD16
PCI_AD15
PCI_AD14
PCI_AD13
PCI_AD12
PCI_AD11
PCI_AD10
PCI_AD9
PCI_AD8
PCI_AD7
PCI_AD6
PCI_AD5
PCI_AD4
PCI_AD3
PCI_AD2
PCI_AD1
PCI_AD0
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
16,18,22,23 PCI_C/BE#[0:3]
PCI_C/BE#0
PCI_C/BE#1
PCI_C/BE#2
PCI_C/BE#3
CBEN0
CBEN1
CBEN2
CBEN3
7 PCICLK_LAN
16,17,18,22,23,24 PCI_RST#
PCICLK
RSTN
PCI_AD28 R132 100 Z2101
IDSEL
16,17,18,22,23 PCI_PERR#
16,17,18,22,23 PCI_PAR
16,17,18,22,23 PCI_STOP#
16,17,18,22,23 PCI_TRDY#
16,17,18,22,23 PCI_FRAME#
16,17,18,22,23 PCI_DEVSEL#
16,17,18,22,23 PCI_IRDY#
PERRN
PAR
STOPN
TRDYN
FRAMEN
DEVSELN
IRDYN
R127 5.62K_1 Z2102
RTSET
CTRL25
16,17,22,23 PM_CLKRUN#
CLKRUN
Differential Impedance:near 100 ohm.
TXD+/MDI[0]+
TXD-/MDI[0]-
RXIN+/MDI[1]+
RXIN-/MDI[1]-
TP_TX+
TP_TX-
TP_RX+
TP_RX-
EESEL
EECK
AUX_EEDI
EEDO
SEECS
SEECLK
SEEDI
SEEDO
PMEN
SERRN
REQN
INTAN
GNTN
INT_PIRQD#
PCI_PME# 16,18,22,23
PCI_SERR# 16,17,22,23
PCI_REQ#2 16,17
INT_PIRQD# 16,17
PCI_GNT#2 16
ISOLATEB#
LWAKE
ISOLATEB R120 1K
PM_SLP_S3# 16,17,20,24
LED0
LED1
LED2
NC1/VSS
NC2/AVDD33
NC3
NC4/VSS
NC5/MDI[2]+
NC6/MDI[2]-
NC7/AVDD25
NC8/MDI[3]+
NC9/MDI3]-
NC10/GND
NC11/VDD18
NC12/VDD18
NC13/GND
NC14
NC15/VDD18
NC16
NC17/GND
NC18
NC19/M66EN
NC20/VDD18
NC21/GND
NC22/LED3
NC23/VDD18
NC24/GND
NC25/AVDD33
NC26/CTRL18
NC27/VDD18
X1
X2
LAN_X1
LAN_X2
R131 1M
Y2
25MHz_SMT
C200
C205
22P
22P
RTL8100CL_LQFP
GND
Near Transformer
Modify M30 in R:B1.
As short as possible.
C183
Z2103
0.1u
R124
R123
49.9_1
49.9_1
PT1
TX+
TX-
CT
TD+
TD-
CT
CT
RX+
RX-
CT
RD+
RD-
NS681690
Z2105
Z2106
TRL_CT0
TRL_CT1
TRL0+
TRL0-
TRL1+
TRL1-
TRL2+
TRL3+
19
TP_TX+
TP_TX-
TP_RX+
TP_RX-
R122
R121
49.9_1
49.9_1
C184
Z2104
0.1u
C117
C116
0.1u
0.1u
R75
R72
R74
R73
75
75
75
75
Z2107
C88
150P_3KV_1808
Near IC
All close to LAN, and test to replacement SATA to PATA IC crystal.
+3.3V
C195
0.1u
20 SATA_25MHZ
R116 22 Z2108
C185
10P
U13
74AHC14_1G
Uniwill International Corp.
Title
MX0/M40/50EI0
Size
Document Number
3017
LAN 10/100
Rev
C
Date: Monday, July 25, 2005
Sheet 21 of 35



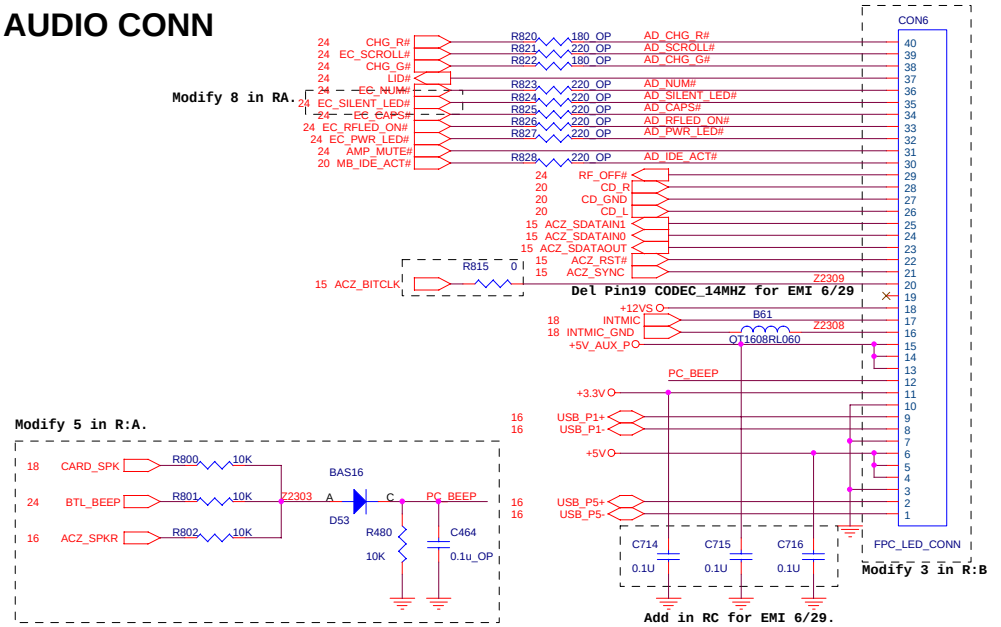
Uniwill International Corp.			
Title	MX0/M40/50EI0		
Size	Document Number 3017 1394		Rev C
Date: Monday, July 25, 2005	Sheet 22 of 35		

MINI PCI CON

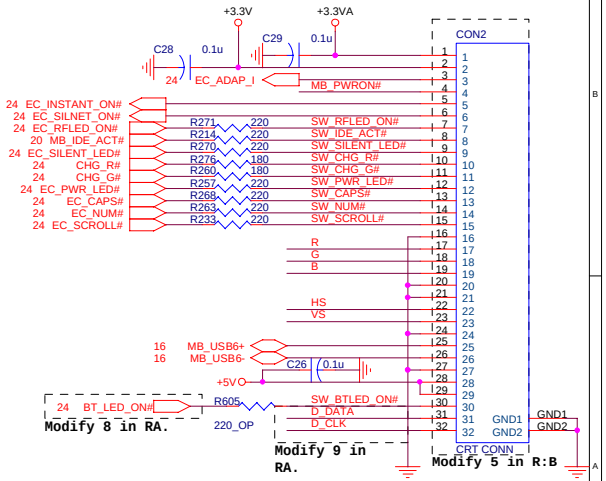


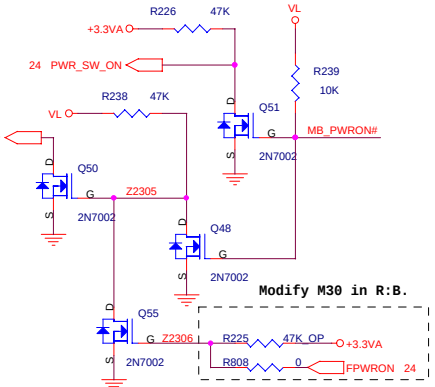


AUDIO CONN

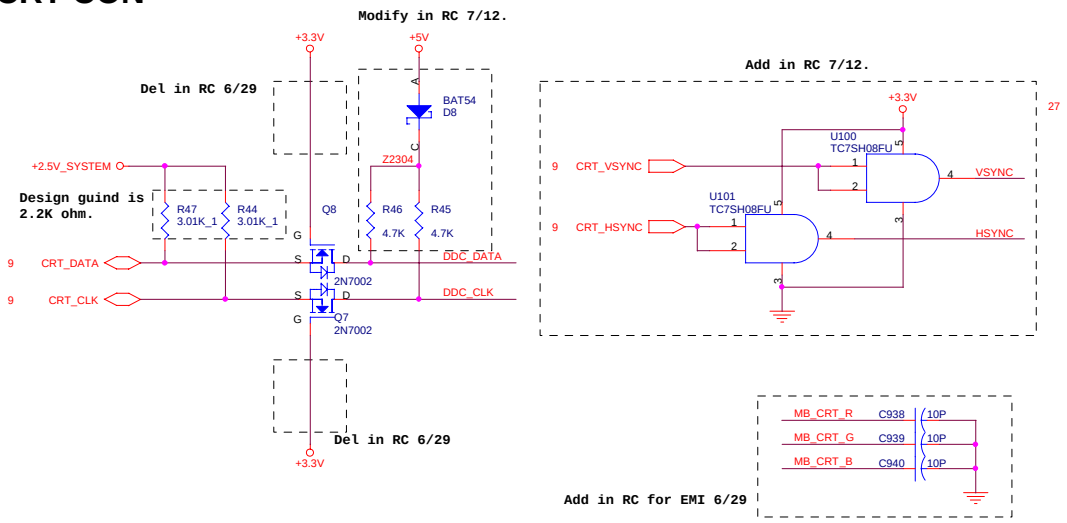


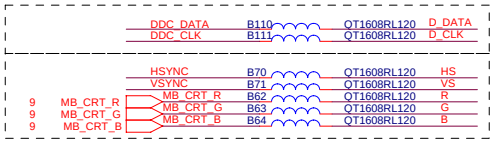
SWITCH CONN





CRT CON





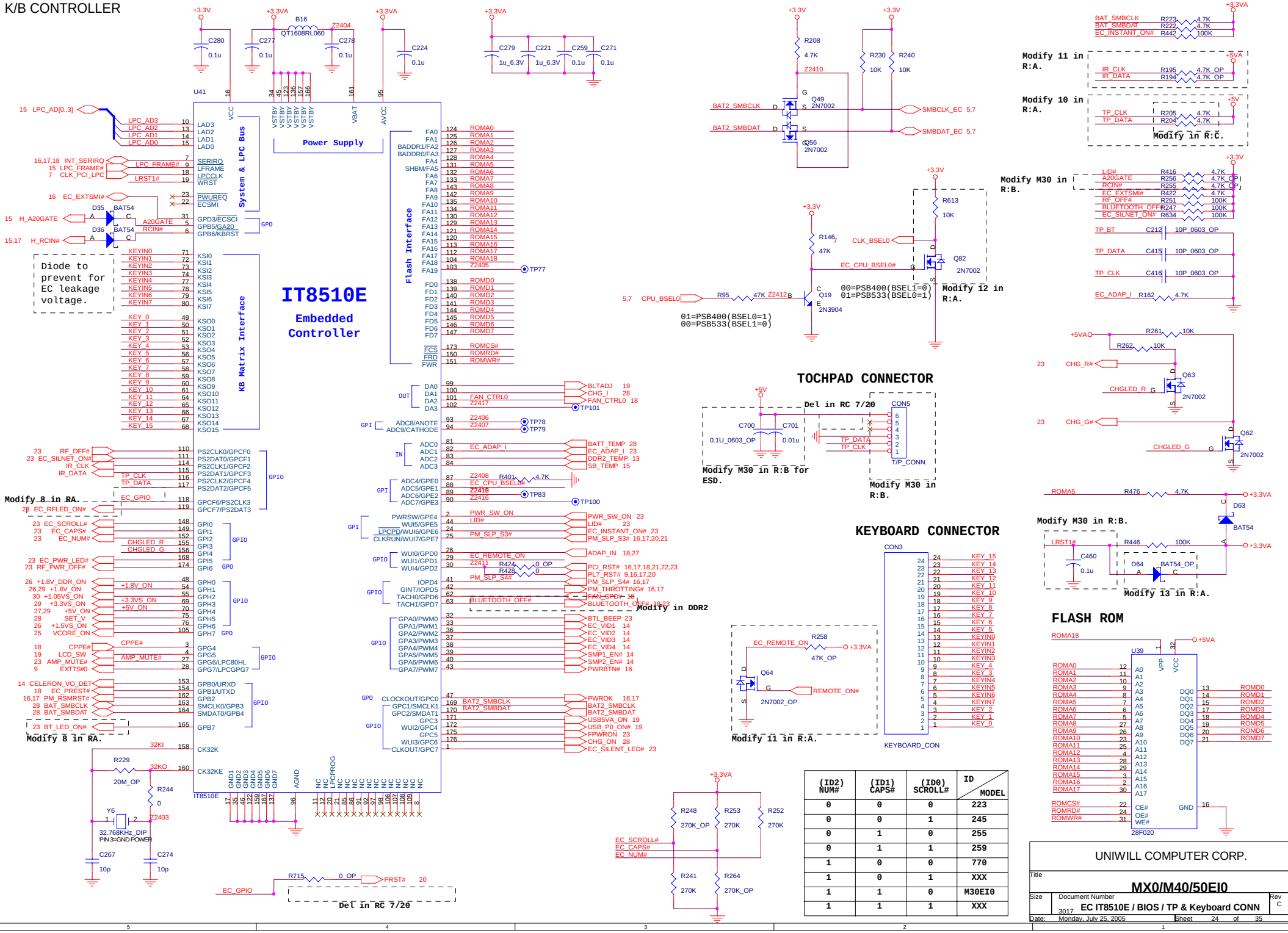
UNIWILL COMPUTER CORP.

Title: MX0/M40/50EI0

Size: Document Number: 3017 — MINI PCI / AUDIO CON / CRT CONN — Rev: C

Date: Monday, July 25, 2005 — Sheet 23 of 35

K/B CONTROLLER



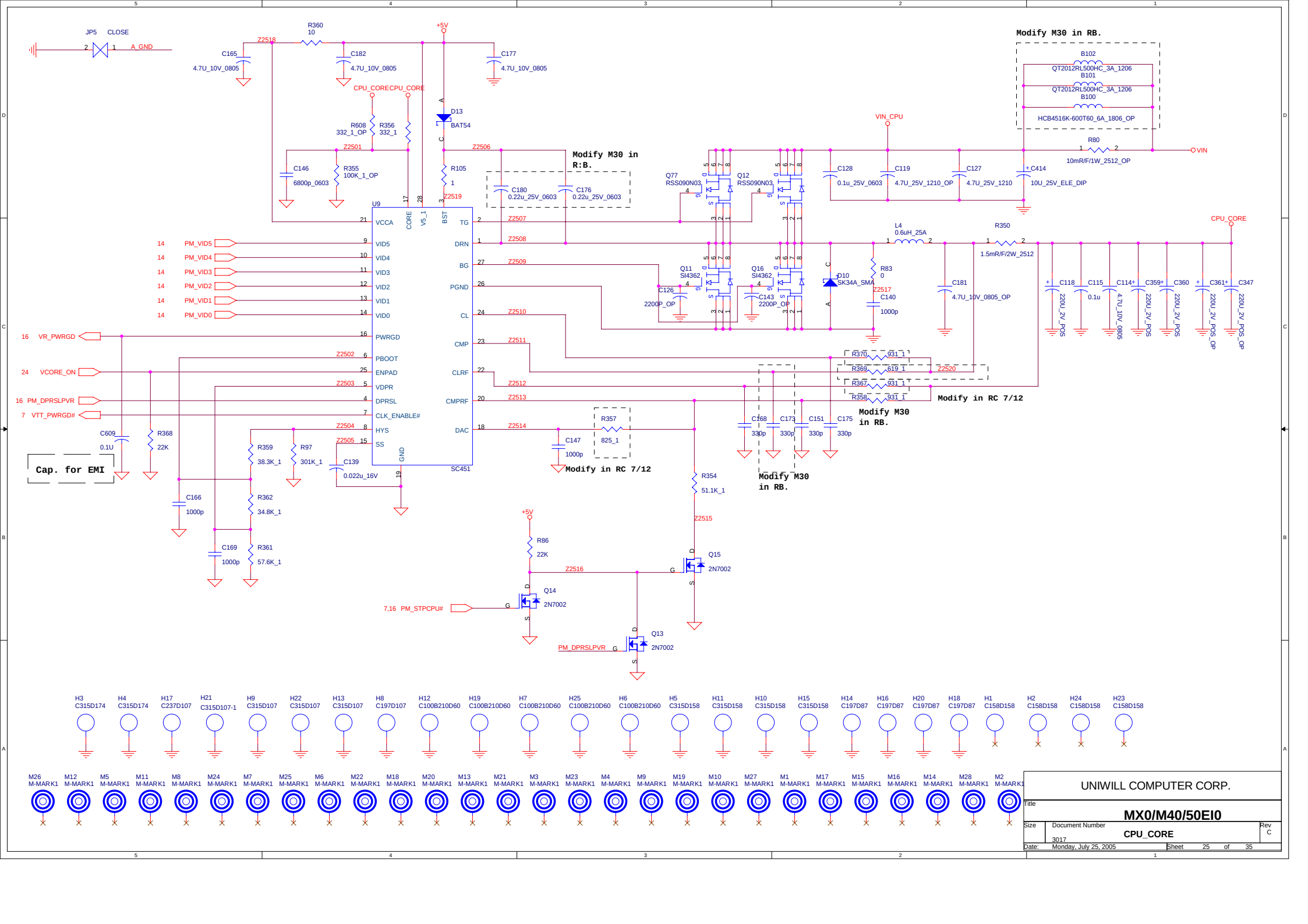
(ID2) NUM#	(ID1) CAPS#	(ID0) SCROLL#	ID / MODEL
0	0	0	223
0	0	1	245
0	1	0	255
0	1	1	259
1	0	0	770
1	0	1	XXX
1	1	0	M30EI0
1	1	1	XXX

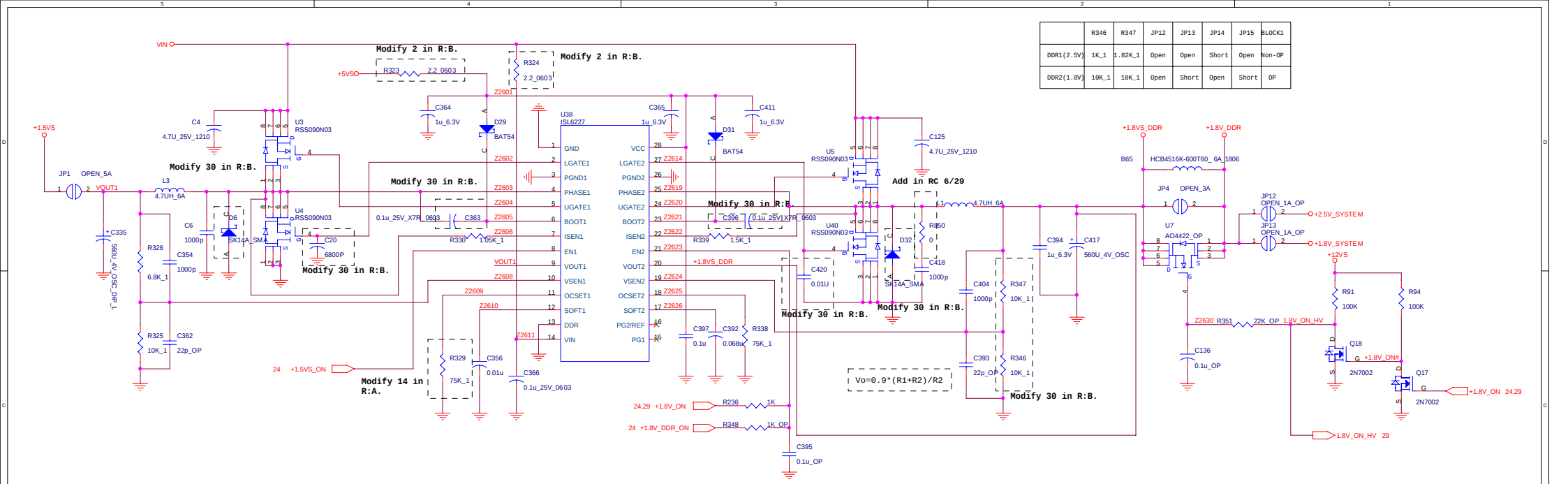
UNIWILL COMPUTER CORP.

Title: MX0/M40/50EI0

Size: | Document Number: 3017 EC IT8510E / BIOS / TP & Keyboard CONN | Rev: C

Date: Monday, July 25, 2005 | Sheet 24 of 35

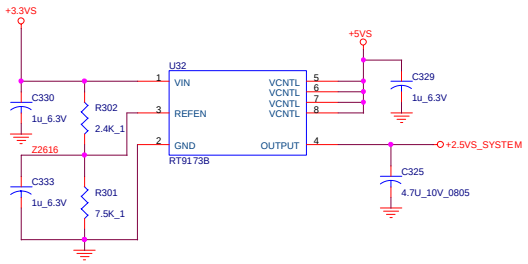

JP5 CLOSE
A_GND
R360 10
C165 4.7U_10V_0805
C182 4.7U_10V_0805
C177 4.7U_10V_0805
+5V
CPU_CORE
D13 BAT54
R608 332_1_OP
R356 332_1
R355 100K_1_OP
C146 6800p_0603
R105 1
C180 0.22u_25V_0603
C176 0.22u_25V_0603
Modify M30 in R:B.
Modify M30 in RB.
B102 QT2012RL500HC_3A_1206
B101 QT2012RL500HC_3A_1206
B100 HCB4516K-600T60_6A_1806_OP
VIN_CPU
R80 10mR/F/1W_2512_OP
VIN
C128 0.1u_25V_0603
C119 4.7U_25V_1210_OP
C127 4.7U_25V_1210
C414 10U_25V_ELE_DIP
Q77 RSS090N03
Q12 RSS090N03
Q11 SI4362
Q16 SI4362
C126 2200P_OP
C143 2200P_OP
D10 SK34A_SMA
R83 0
C140 1000p
L4 0.6uH_25A
R350 1.5mR/F/2W_2512
C181 4.7U_10V_0805_OP
C118 220U_2V_POS
C115 0.1u
C114 4.7U_10V_0805
C359 220U_2V_POS
C360 220U_2V_POS
C361 220U_2V_POS_OP
C347 220U_2V_POS_OP
U9
VCCA
CORE
V5_1
BST
TG
DRN
BG
PGND
CL
CMP
CLRF
CMPRF
DAC
SC451
VID5
VID4
VID3
VID2
VID1
VID0
PWRGD
PBOOT
ENPAD
VDPR
DPRSL
CLK_ENABLE#
HYS
SS
GND
PM_VID5
PM_VID4
PM_VID3
PM_VID2
PM_VID1
PM_VID0
VR_PWRGD
VCORE_ON
PM_DPRSLPVR
VTT_PWRGD#
Z2501
Z2506
Z2507
Z2508
Z2509
Z2510
Z2511
Z2512
Z2513
Z2514
Z2517
Z2519
Z2520
Z2502
Z2503
Z2504
Z2505
R370 931_1
R369 619_1
R367 931_1
R358 931_1
Modify in RC 7/12
Modify M30 in RB.
C168 330p
C173 330p
C151 330p
C175 330p
R357 825_1
C147 1000p
Modify in RC 7/12
Modify M30 in RB.
Cap. for EMI
C609 0.1U
R368 22K
C139 0.022u_16V
R359 38.3K_1
R97 301K_1
C166 1000p
R362 34.8K_1
C169 1000p
R361 57.6K_1
R354 51.1K_1
Z2515
R86 22K
Z2516
Q15 2N7002
Q14 2N7002
Q13 2N7002
7,16 PM_STPCPU#
PM_DPRSLPVR
H3 C315D174
H4 C315D174
H17 C237D107
H21 C315D107-1
H9 C315D107
H22 C315D107
H13 C315D107
H8 C197D107
H12 C100B210D60
H19 C100B210D60
H7 C100B210D60
H25 C100B210D60
H6 C100B210D60
H5 C315D158
H11 C315D158
H10 C315D158
H15 C315D158
H14 C197D87
H16 C197D87
H20 C197D87
H18 C197D87
H1 C158D158
H2 C158D158
H24 C158D158
H23 C158D158
M26 M-MARK1
M12 M-MARK1
M5 M-MARK1
M11 M-MARK1
M8 M-MARK1
M24 M-MARK1
M7 M-MARK1
M25 M-MARK1
M6 M-MARK1
M22 M-MARK1
M18 M-MARK1
M20 M-MARK1
M13 M-MARK1
M21 M-MARK1
M3 M-MARK1
M23 M-MARK1
M4 M-MARK1
M9 M-MARK1
M19 M-MARK1
M10 M-MARK1
M27 M-MARK1
M1 M-MARK1
M17 M-MARK1
M15 M-MARK1
M16 M-MARK1
M14 M-MARK1
M28 M-MARK1
M2 M-MARK1
UNIWILL COMPUTER CORP.
Title
MX0/M40/50EI0
Size
Document Number
CPU_CORE
3017
Rev C
Date: Monday, July 25, 2005
Sheet 25 of 35



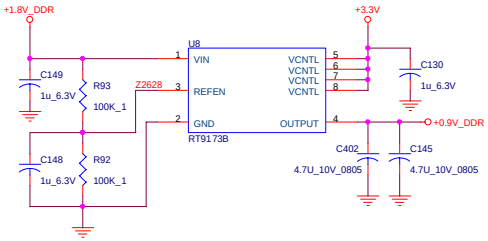
	R346	R347	JP12	JP13	JP14	JP15	BLOCK1
DDR1(2.5V)	1K_1	1.82K_1	Open	Open	Short	Open	Non-OP
DDR2(1.8V)	10K_1	10K_1	Open	Short	Open	Short	OP

Modify 30 in R:B.

Modify 30 in R:B.

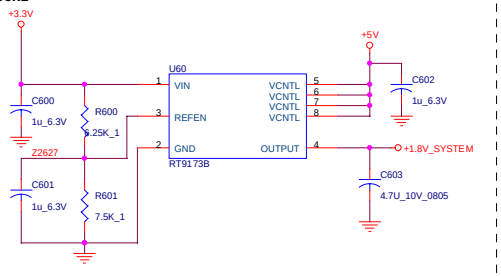


DDR Termination Power



Modify 30 in R:B.

BLOCK1

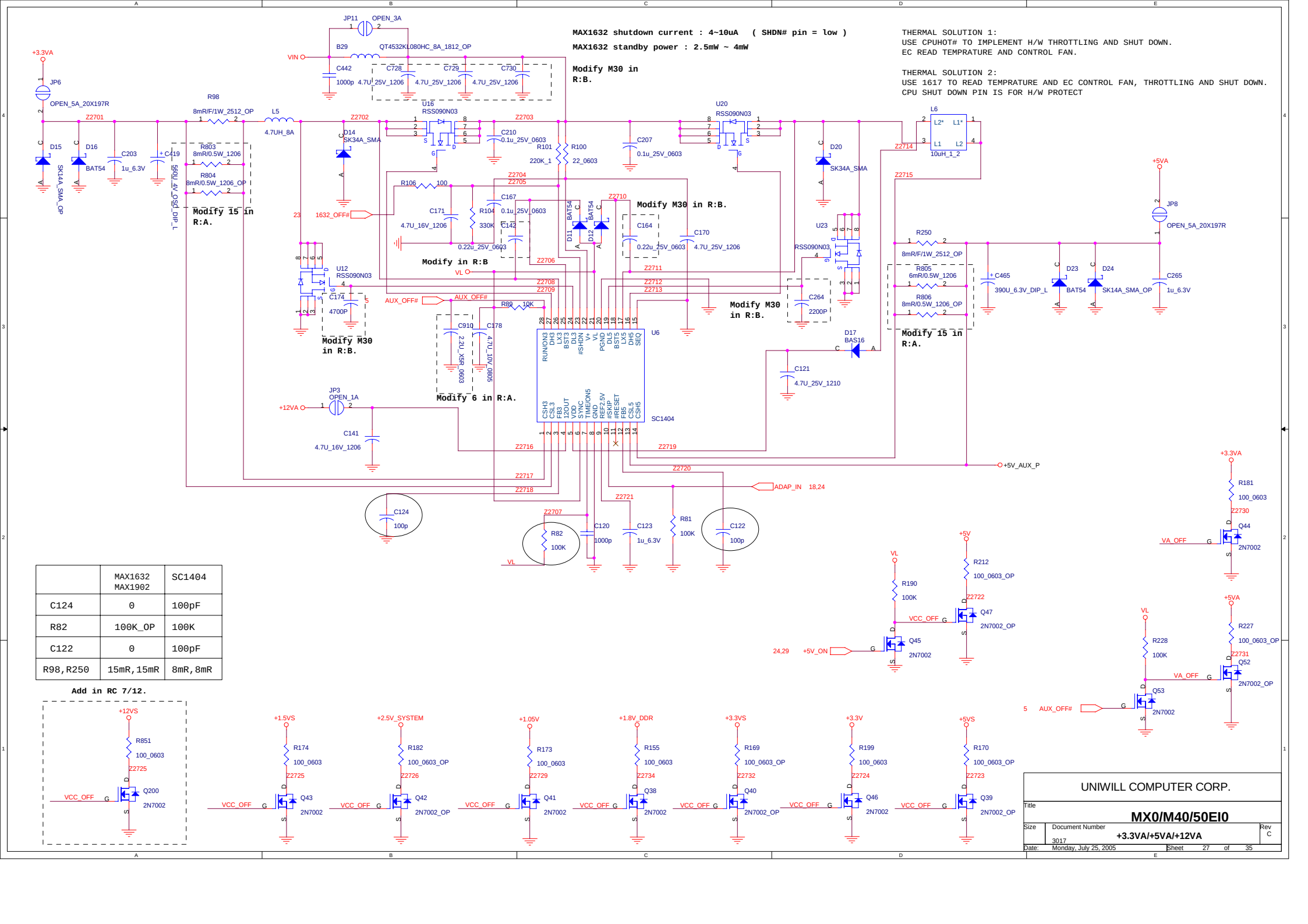


UNIWILL COMPUTER CORP.

Title: MX0/M40/50EI0

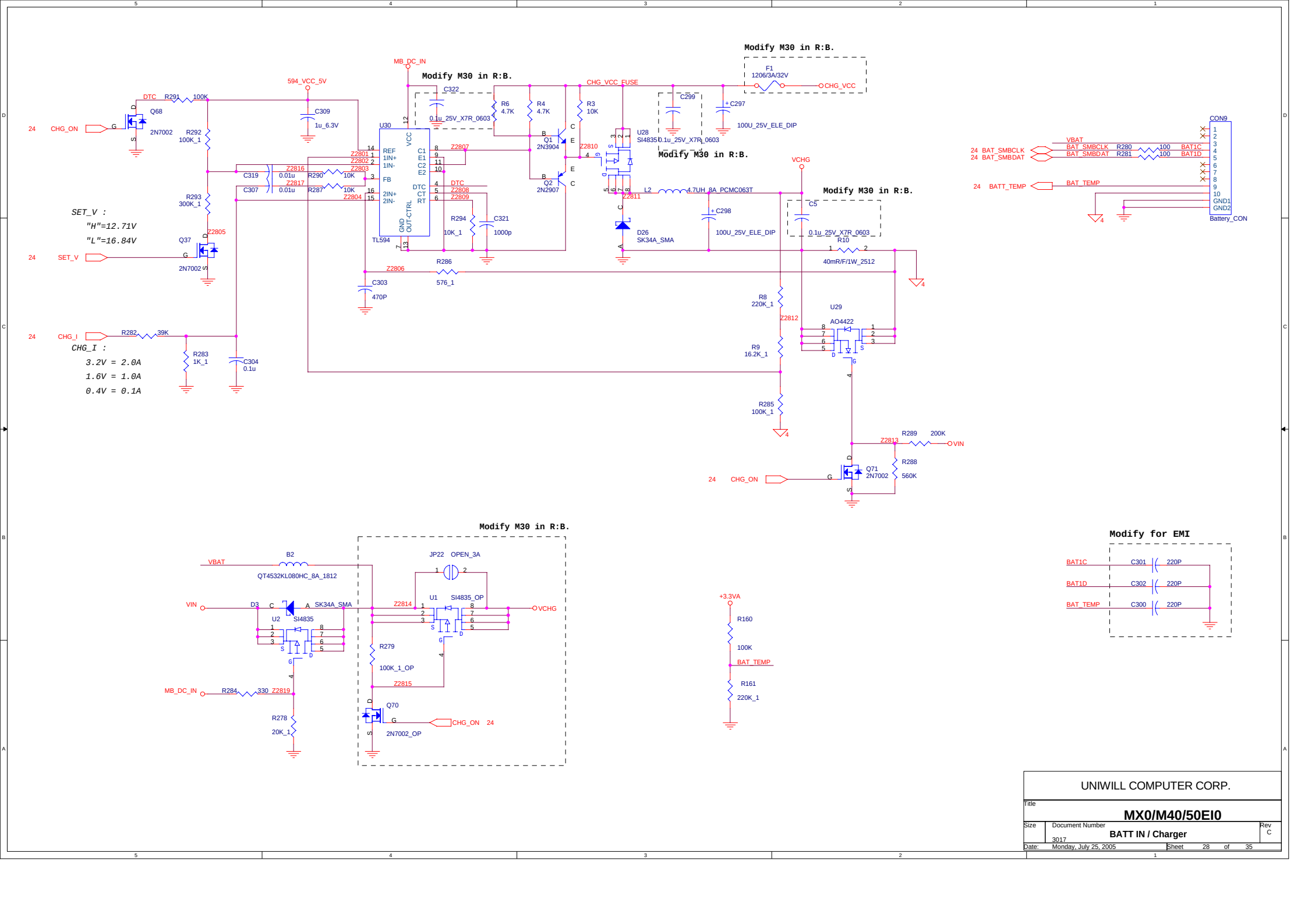
Size: | Document Number: 3017 1.05V/1.5V/1.8V/2.5V/0.9V | Rev: C

Date: Monday, July 25, 2005 | Sheet 26 of 35



	MAX1632 MAX1902	SC1404
C124	0	100pF
R82	100K_OP	100K
C122	0	100pF
R98,R250	15mR,15mR	8mR,8mR

Add in RC 7/12.



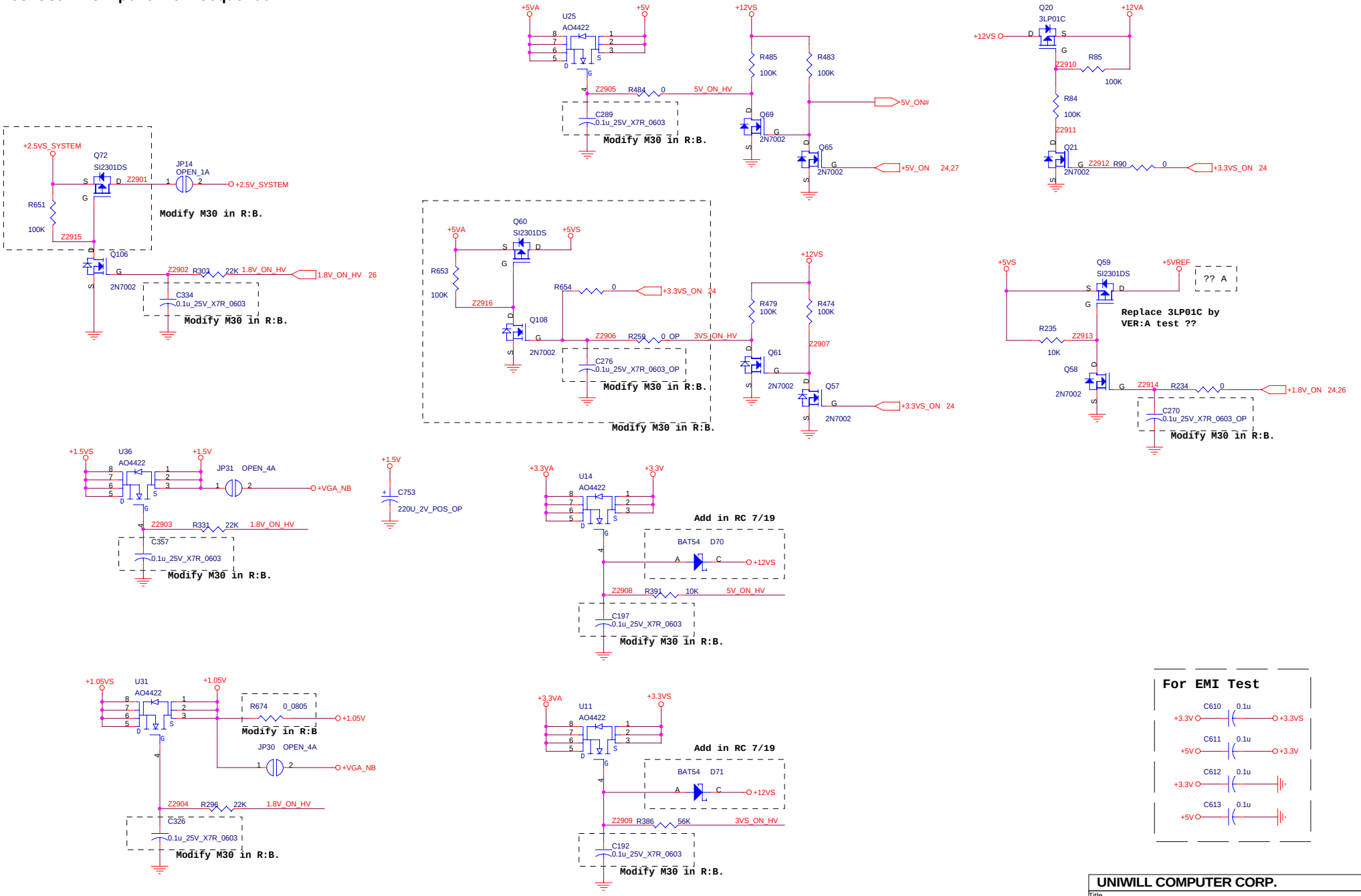
UNIWILL COMPUTER CORP.

Title: **MX0/M40/50EI0**

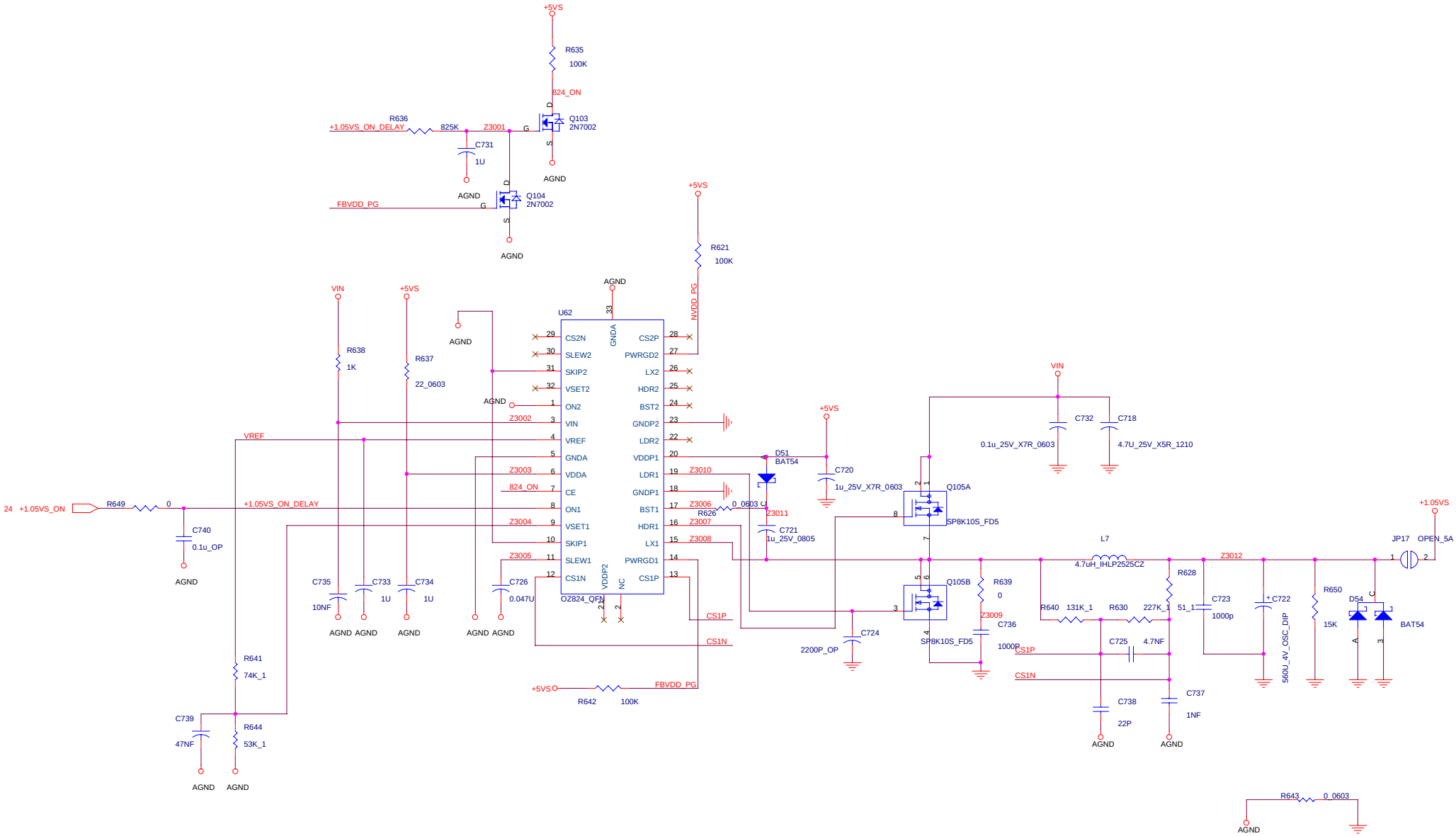
Size	Document Number	Rev
	3017 **BATT IN / Charger**	C

Date: Monday, July 25, 2005 Sheet 28 of 35

@Modify resister for power on sequence.



UNIWILL COMPUTER CORP.		
Title: M30EI0		
Size: Custom	Document Number: MX0/M40/50EI0 3017	Rev: C
Date: Monday, July 25, 2005	Sheet 29 of 35	



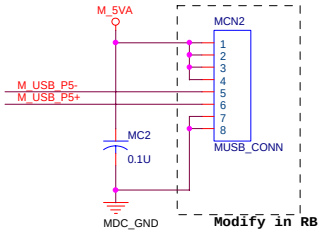
UNIWILL COMPUTER CORP.

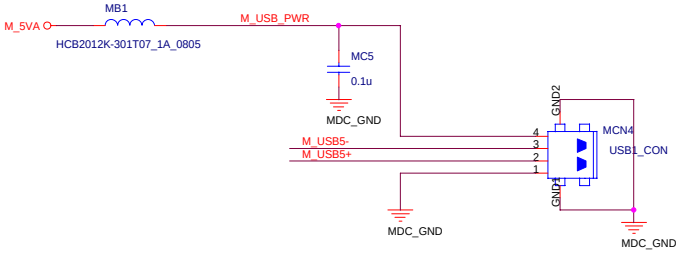
Title: **MX0/M40/50EI0**

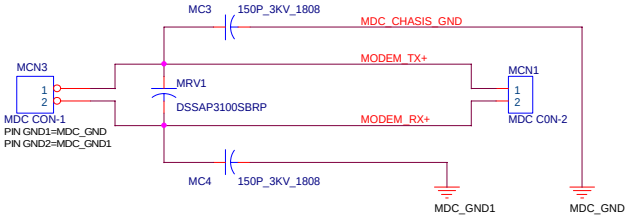
Size: Document Number: 3017 — **1.05V/1.5V/1.8V/2.5V/0.9V** — Rev: C

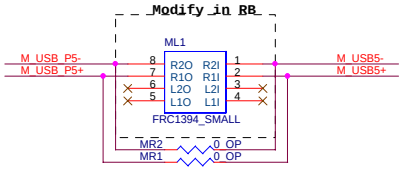
Date: Monday, July 25, 2005 — Sheet 30 of 35

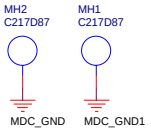
USB BD



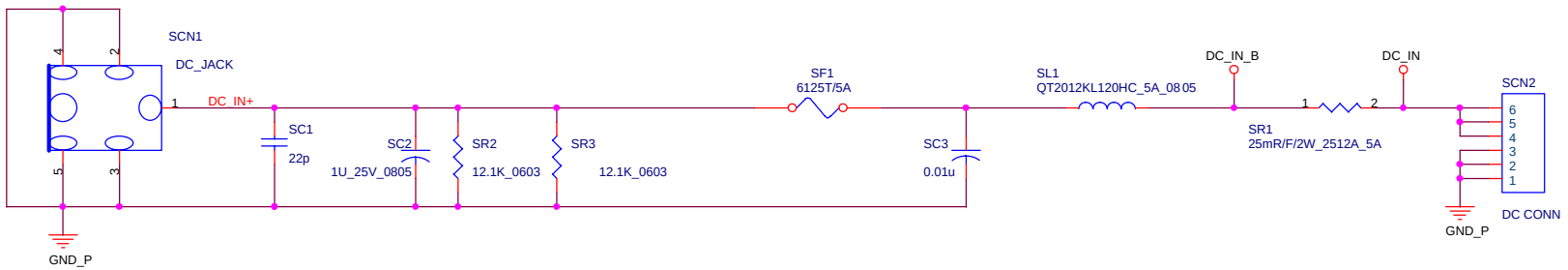


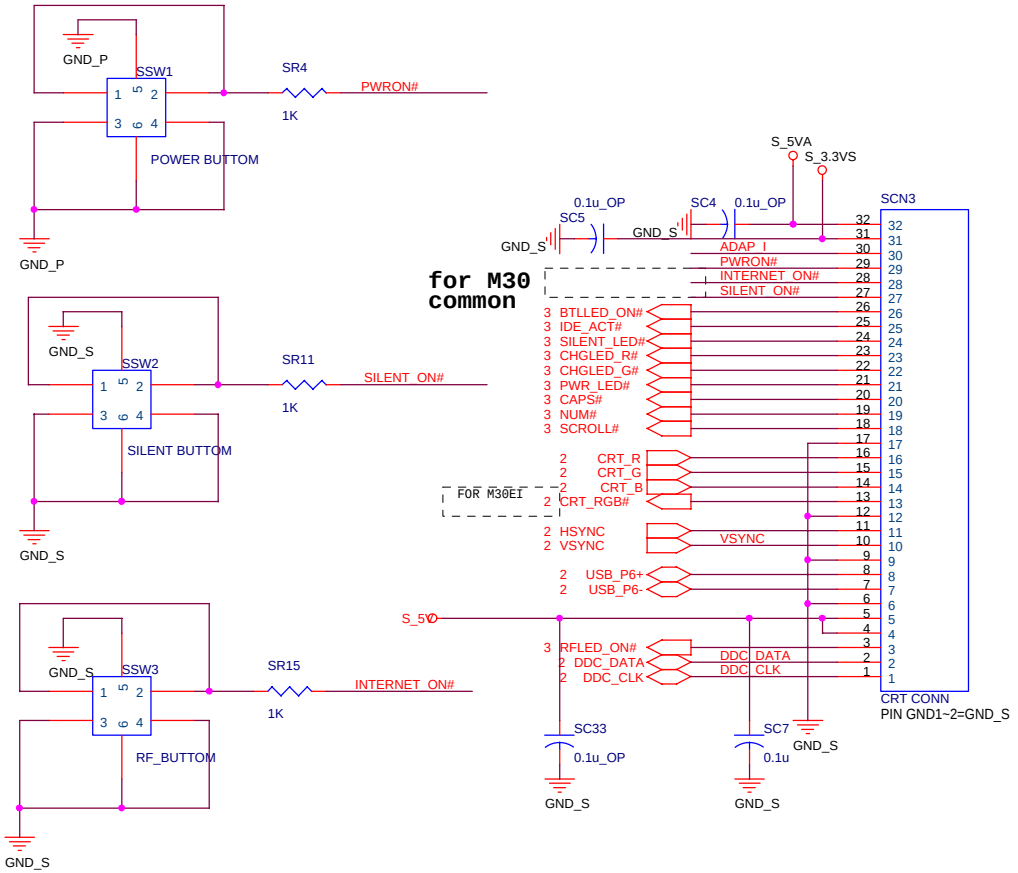


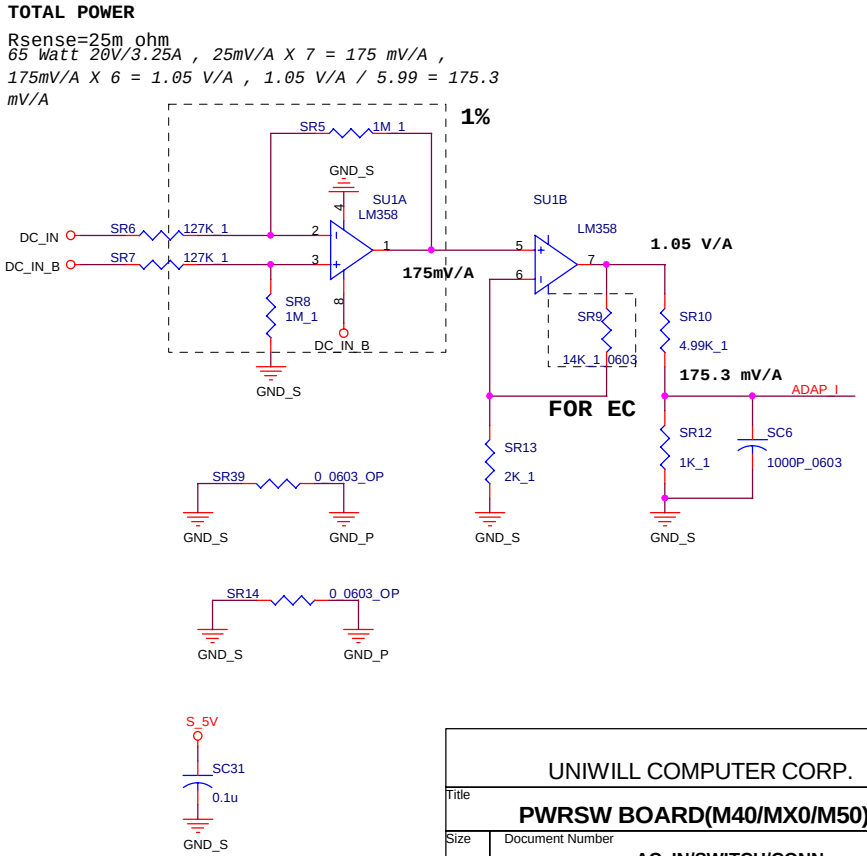




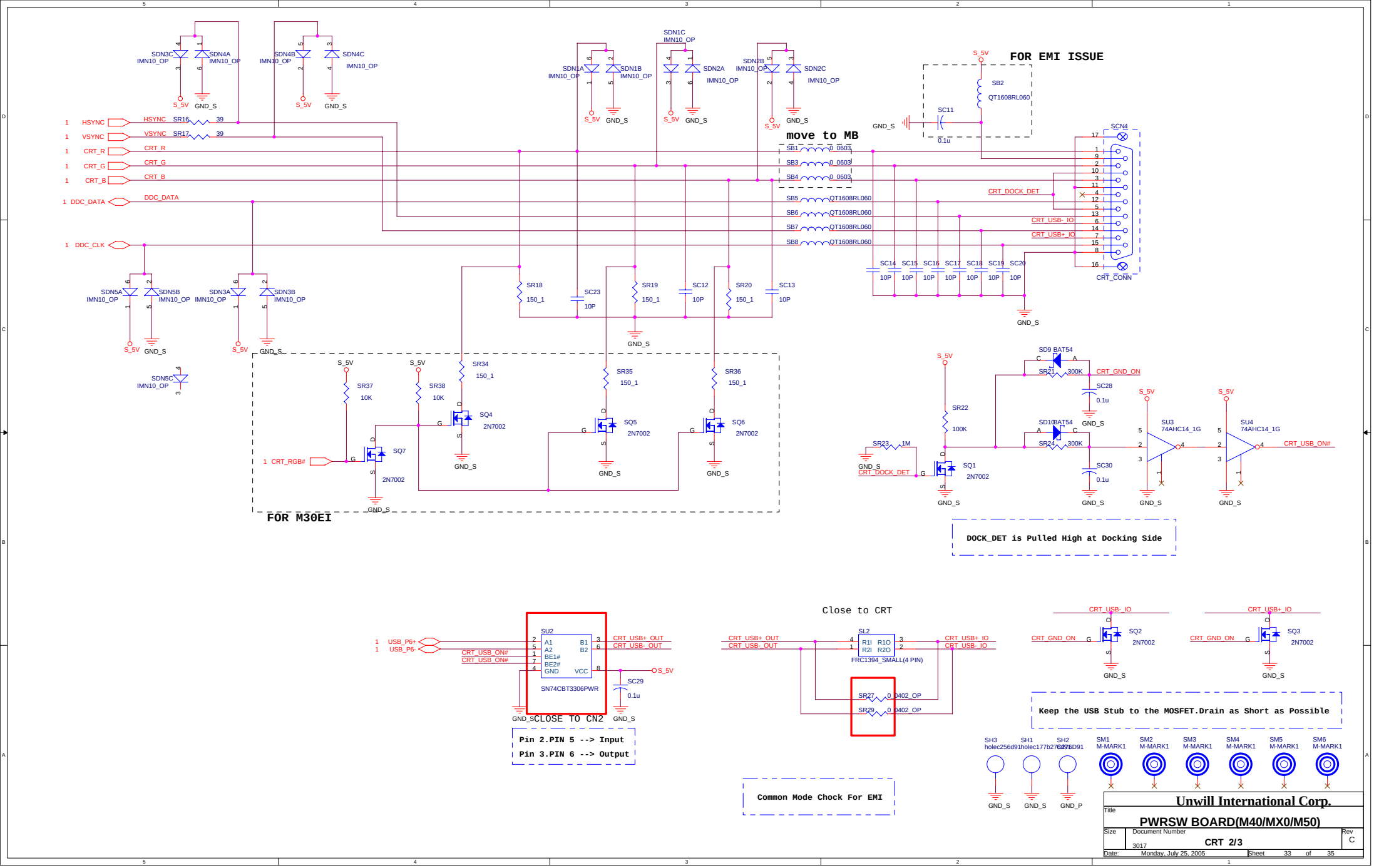
UNIWILL COMPUTER CORP.		
Title: M50EA0		
Size	Document Number: M30EI0 3017 MDC BD	Rev: C
Date: Monday, July 25, 2005	Sheet 31 of 35	



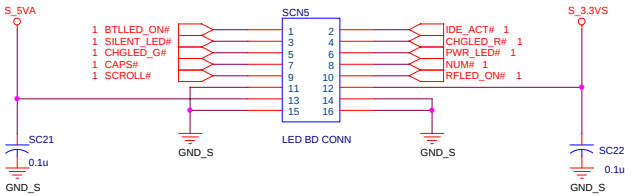




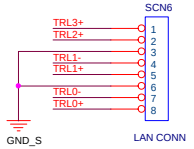
UNIWILL COMPUTER CORP.		
Title: PWRSW BOARD(M40/MX0/M50)		
Size	Document Number: AC_IN/SWITCH/CONN 3017	Rev C
Date: Monday, July 25, 2005	Sheet 32 of 35	


FOR EMI ISSUE
move to MB
FOR M30EI
DOCK_DET is Pulled High at Docking Side
Close to CRT
CLOSE TO CN2
Pin 2.PIN 5 --> Input
Pin 3.PIN 6 --> Output
Keep the USB Stub to the MOSFET.Drain as Short as Possible
Common Mode Chock For EMI
SN74CBT3306PWR
FRC1394_SMALL(4 PIN)
CRT_CONN
Unwill International Corp.
PWRSW BOARD(M40/MX0/M50)
CRT 2/3
3017
Monday, July 25, 2005

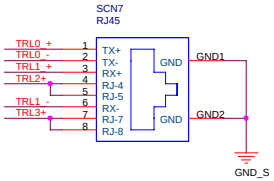
LED

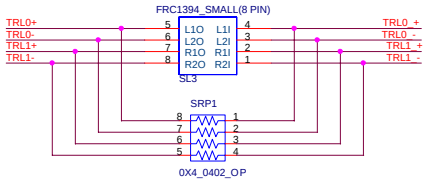


LAN



RJ45





Unwill International Corp.		
Title: PWRSW BOARD(M40/MX0/M50)		
Size	Document Number: 3017 LAN/LED 3/3	Rev: C
Date: Monday, July 25, 2005	Sheet 34 of 35	

M30 to M40/50 R:A Change Note:

Page 13->1.DDR SODIMM fixed pin connect to GND by EMI solution.

Page 14->2.No smart power 2 function so del. Q28 and Q32.

Page 15->3.Del. R619,D50 and add R158,BT1 for ME assembling.

Page 19->4.Del. USB always have power design for new customer.

Page 23->5.Modify system beep sound circuit for wrong design.

Page 27->6.Add R910 to improvent AUX_OFF# signal.

Page 23->7.Add B70 and B71 for EMI solution.

Page 23->8.Change signal name for right control.

Page 23->9.Change DDC_CLK/DDC_DATA to 31 and 32 pin.

Page 24->10.Del touch pad pull high resister(R204/R205).

Page 24->11.No IR function so del pull high resister(R194/R195).

Page 24->12.Add Q82 and R613 for selecting CPU function.

Page 24->13.Add R446 and D63 to prevent EC leakage currect issue.

Page 26->14.Adjust R329 value for 1.5V over current protect.

Page 27->15.Change R803 and R805 value for 3V and 5V over currect protect.

M40/50 R:A to R:B Change Note:

Page 13->1.DDR SODIMM fixed pin connect to GND by EMI solution.

Uniwill International Corp.		
Title: M40/50EI0		
Size	Document Number: Chang Note 3017	Rev: C
Date: Monday, July 25, 2005	Sheet 35 of 35	