

Compal Confidential

KAWF0/KAWH0 M/B Schematics Document Intel Penryn Processor with Cantiga + DDRII + ICH9M

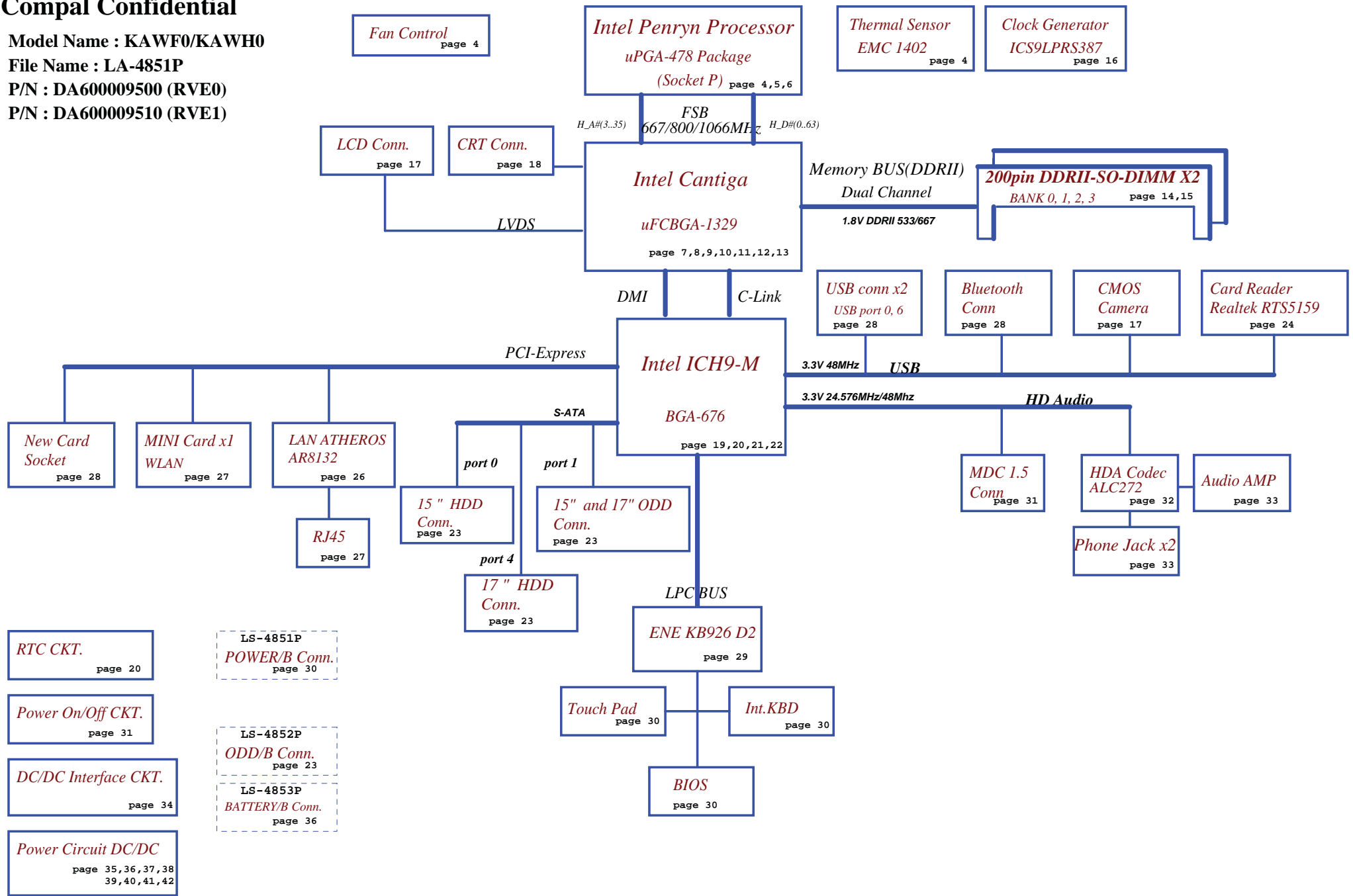
2009-01-21

REV:1.0

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Model Name : KAWF0/KAWH0
 File Name : LA-4851P
 P/N : DA600009500 (RVE0)
 P/N : DA600009510 (RVE1)



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Power On/Off CKT.
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DC/DC Interface CKT.
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45	GM@
GL40	GL@
15"	15@
17"	17@
8114	8114@
8132	8132@

PCIE table

PCIE port1	Express Card(Reserved)
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

USB table

	UHCI1	Port0	MB USB Conn.
EHCI1	UHCI2	Port1	
		Port2	
		Port3	CMOS Camera
		Port4	Card Reader
EHCI2	UHCI3	Port5	New Card(Reserved)
		Port6	MB USB Conn.
		Port7	
		Port8	Blue Tooth
		Port9	
		Port10	Wireless Card
		Port11	

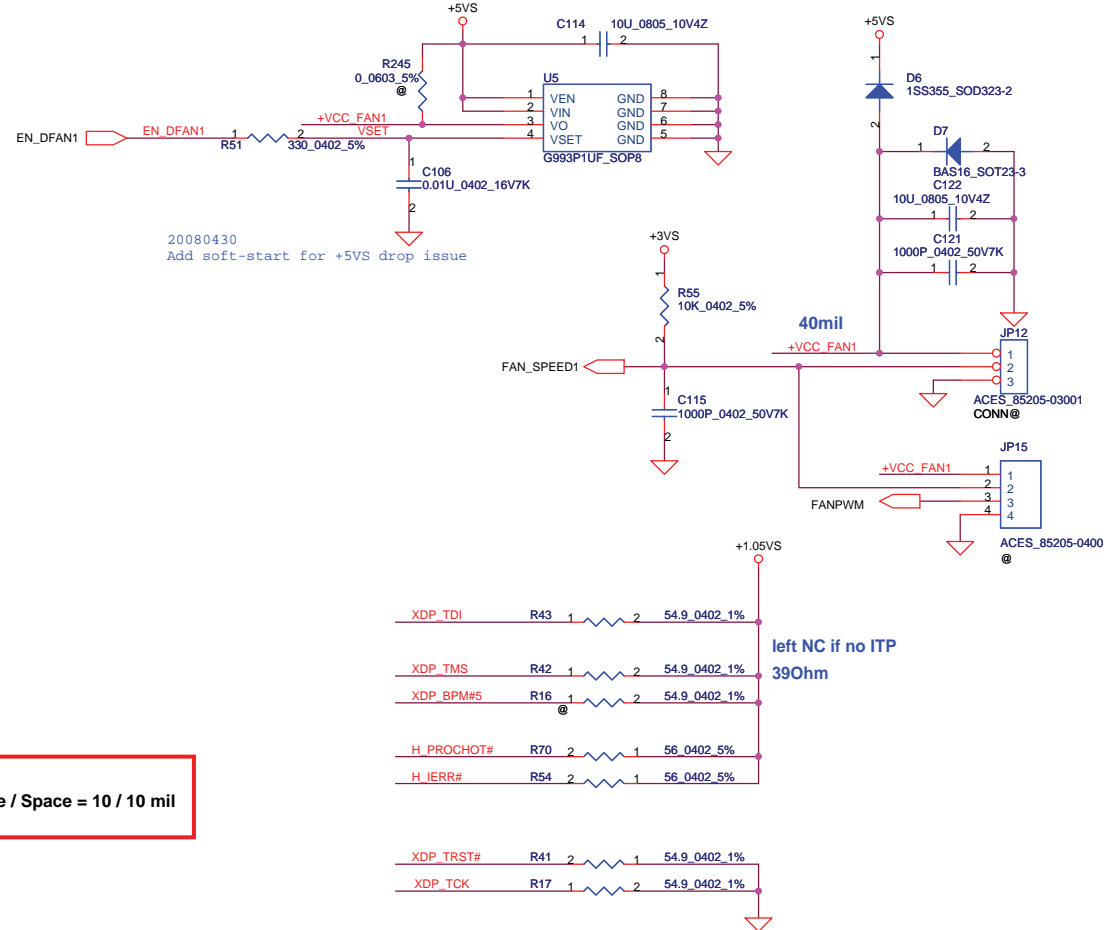
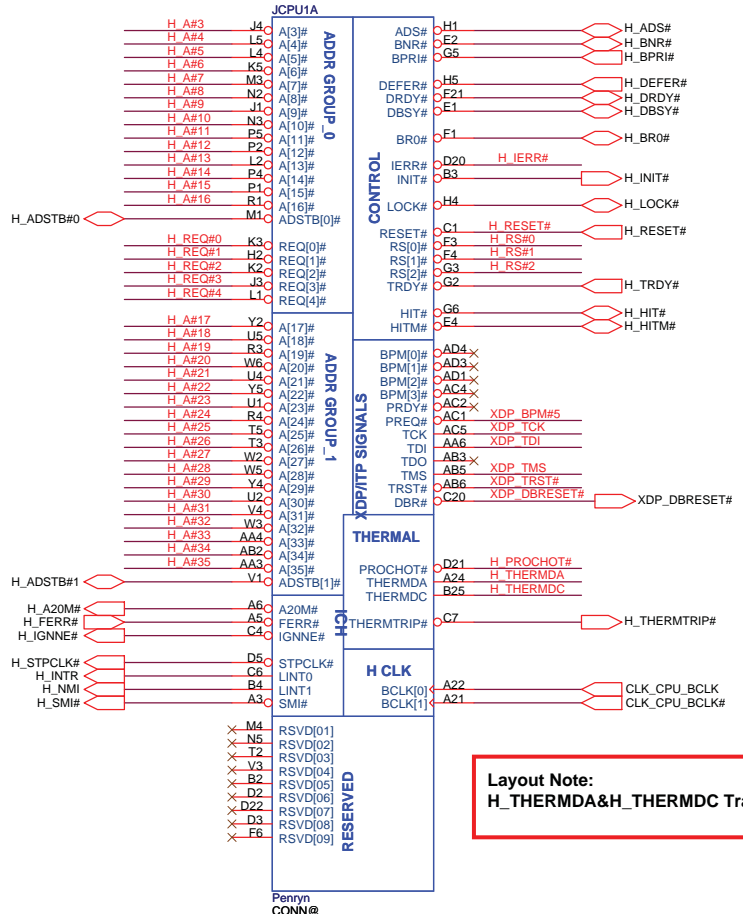
SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	for 17" 2nd HDD
SATA port5	

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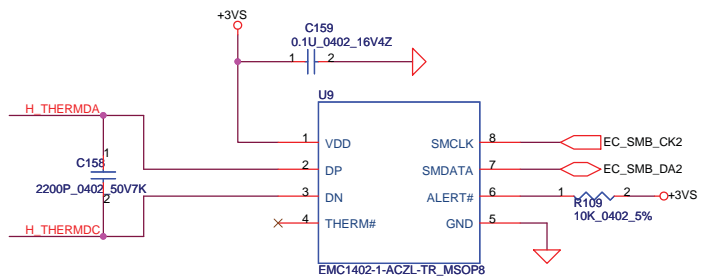
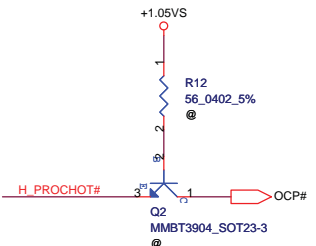
H_A#[3..35] H_A#[3..35]
 H_REQ#[0..4] H_REQ#[0..4]
 H_RS#[0..2] H_RS#[0..2]

FAN1 Conn

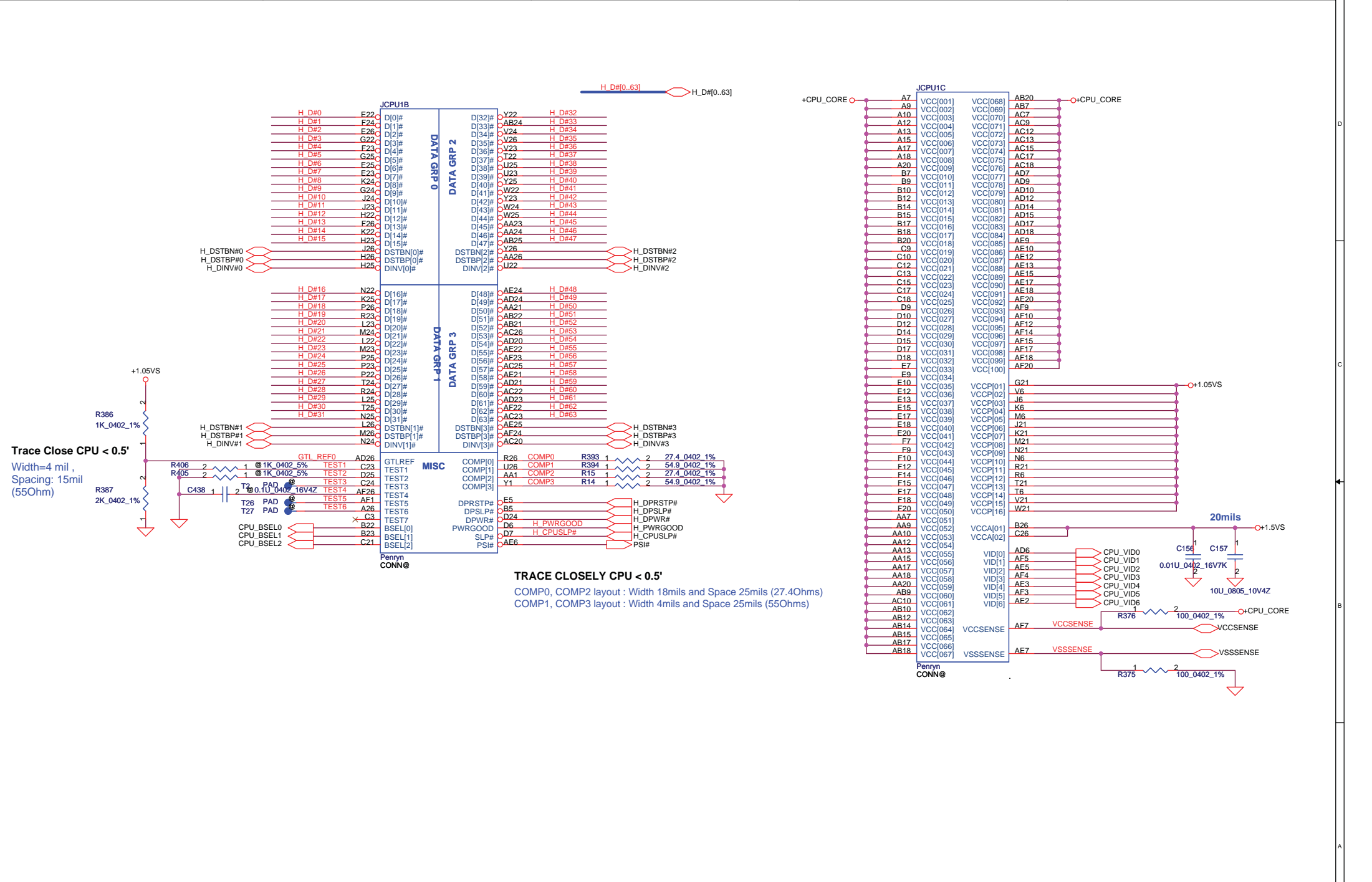


Layout Note:
H_THERMDA&H_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166



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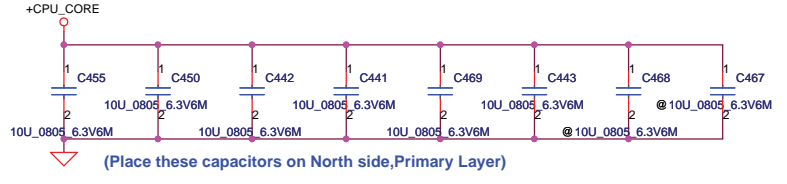
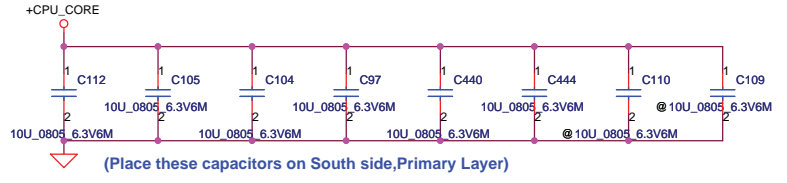
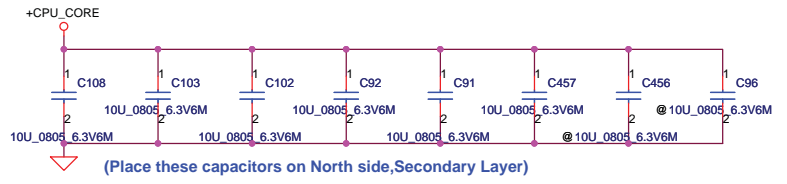
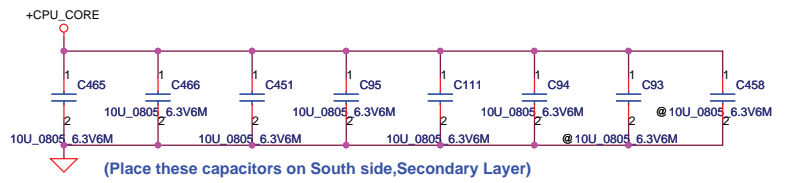
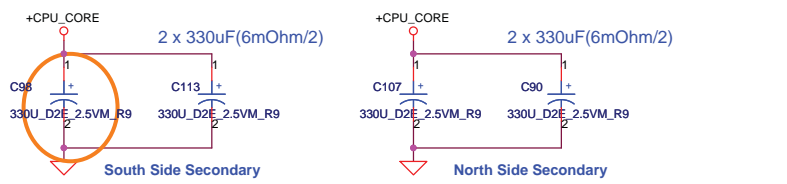
Trace Close CPU < 0.5'
 Width=4 mil,
 Spacing: 15mil
 (55Ohm)

TRACE CLOSELY CPU < 0.5'
 COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
 COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

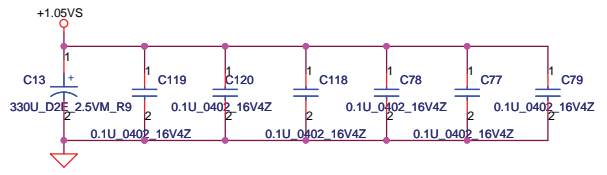
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JCPU1D		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A19	VSS[006]	VSS[087]
A23	VSS[007]	VSS[088]
AF2	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C2	VSS[023]	VSS[104]
C22	VSS[024]	VSS[105]
C25	VSS[025]	VSS[106]
D1	VSS[026]	VSS[107]
D4	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D13	VSS[030]	VSS[111]
D16	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F5	VSS[044]	VSS[125]
F8	VSS[045]	VSS[126]
F11	VSS[046]	VSS[127]
F13	VSS[047]	VSS[128]
F16	VSS[048]	VSS[129]
F19	VSS[049]	VSS[130]
F2	VSS[050]	VSS[131]
F22	VSS[051]	VSS[132]
F25	VSS[052]	VSS[133]
G4	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
G26	VSS[056]	VSS[137]
H3	VSS[057]	VSS[138]
H6	VSS[058]	VSS[139]
H21	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J5	VSS[062]	VSS[143]
J22	VSS[063]	VSS[144]
J25	VSS[064]	VSS[145]
K1	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L3	VSS[069]	VSS[150]
L6	VSS[070]	VSS[151]
L21	VSS[071]	VSS[152]
L24	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]
		VSS[163]

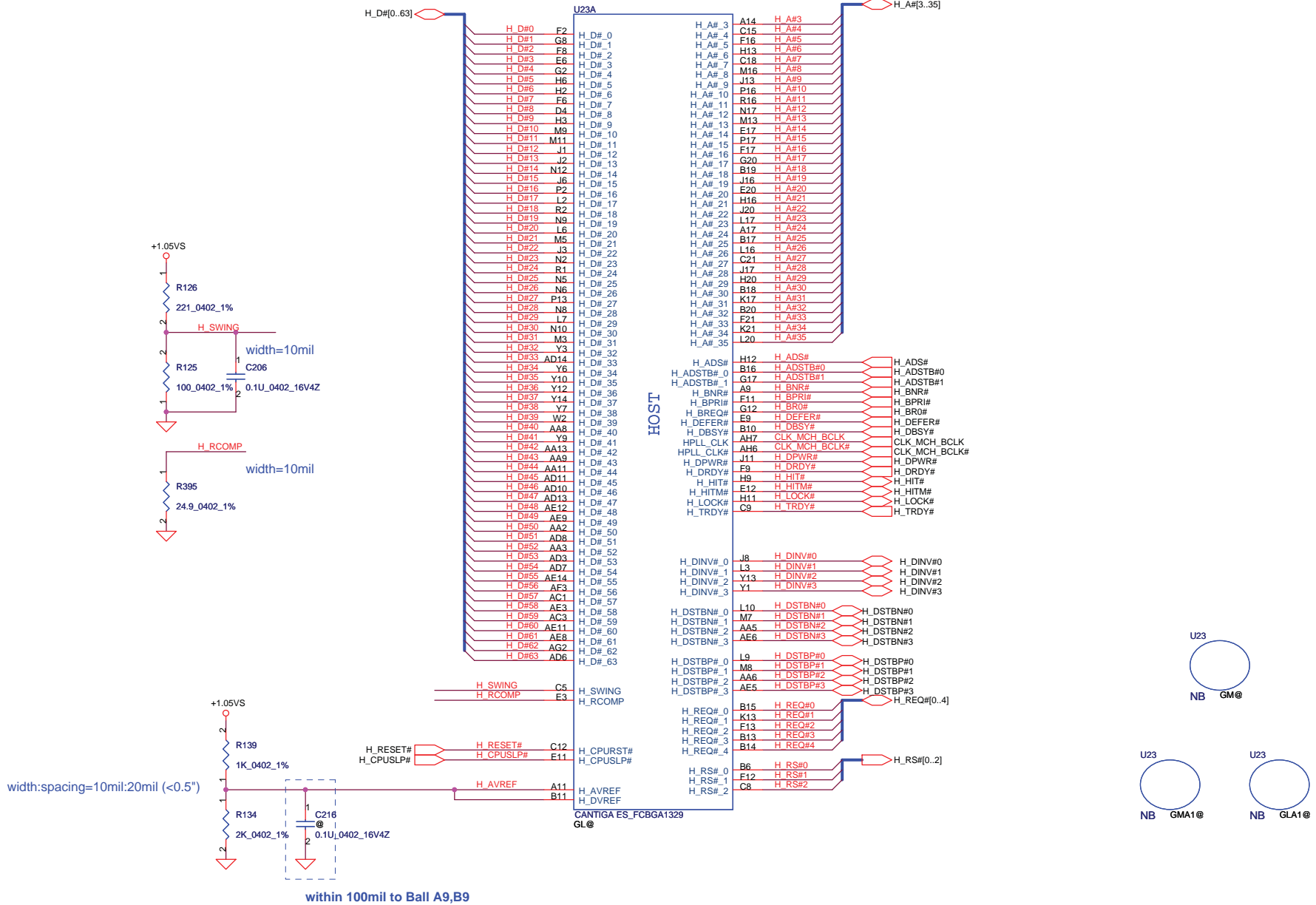
Pennyn
CONN@



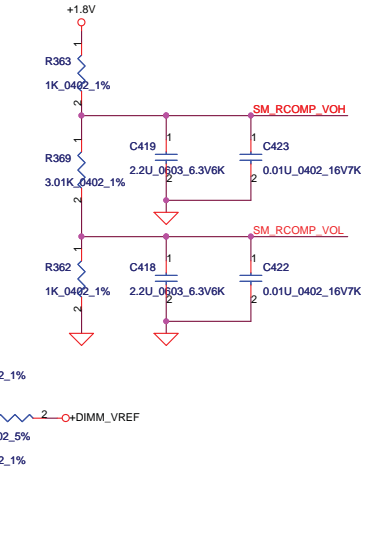
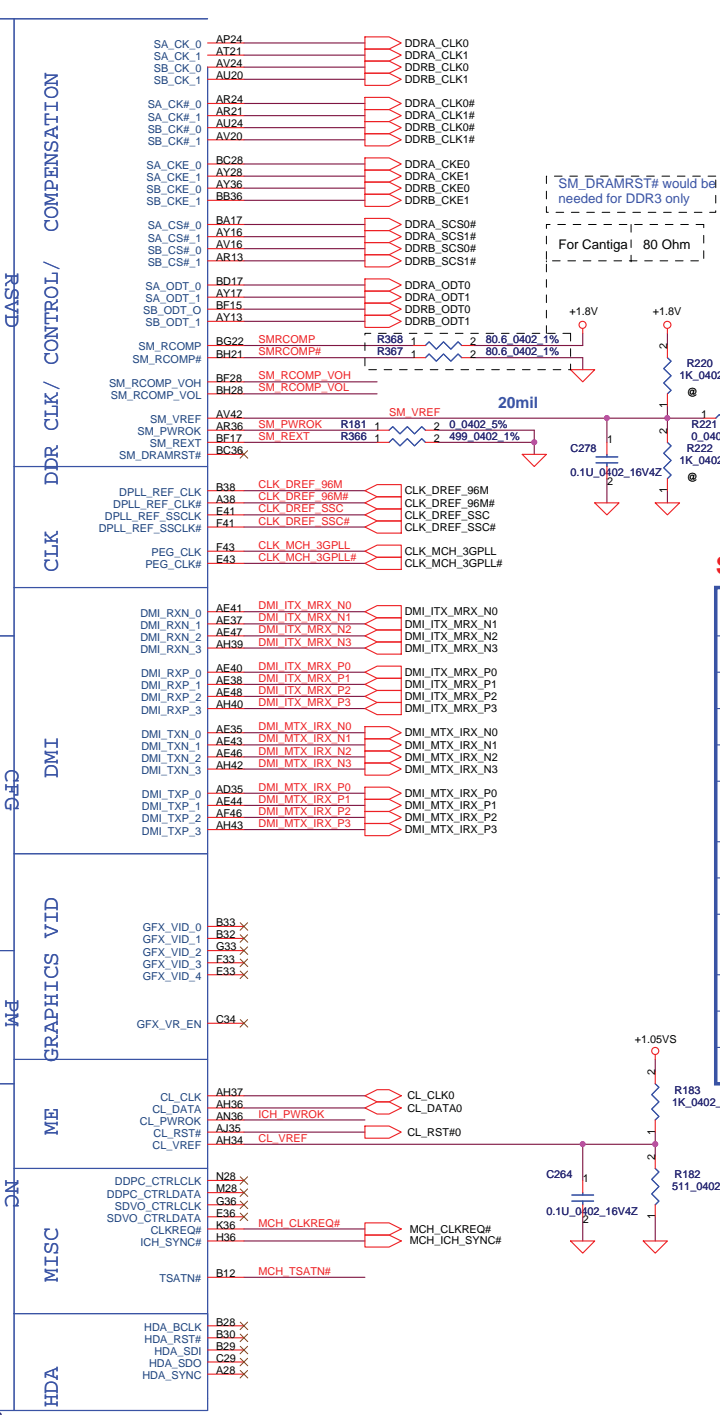
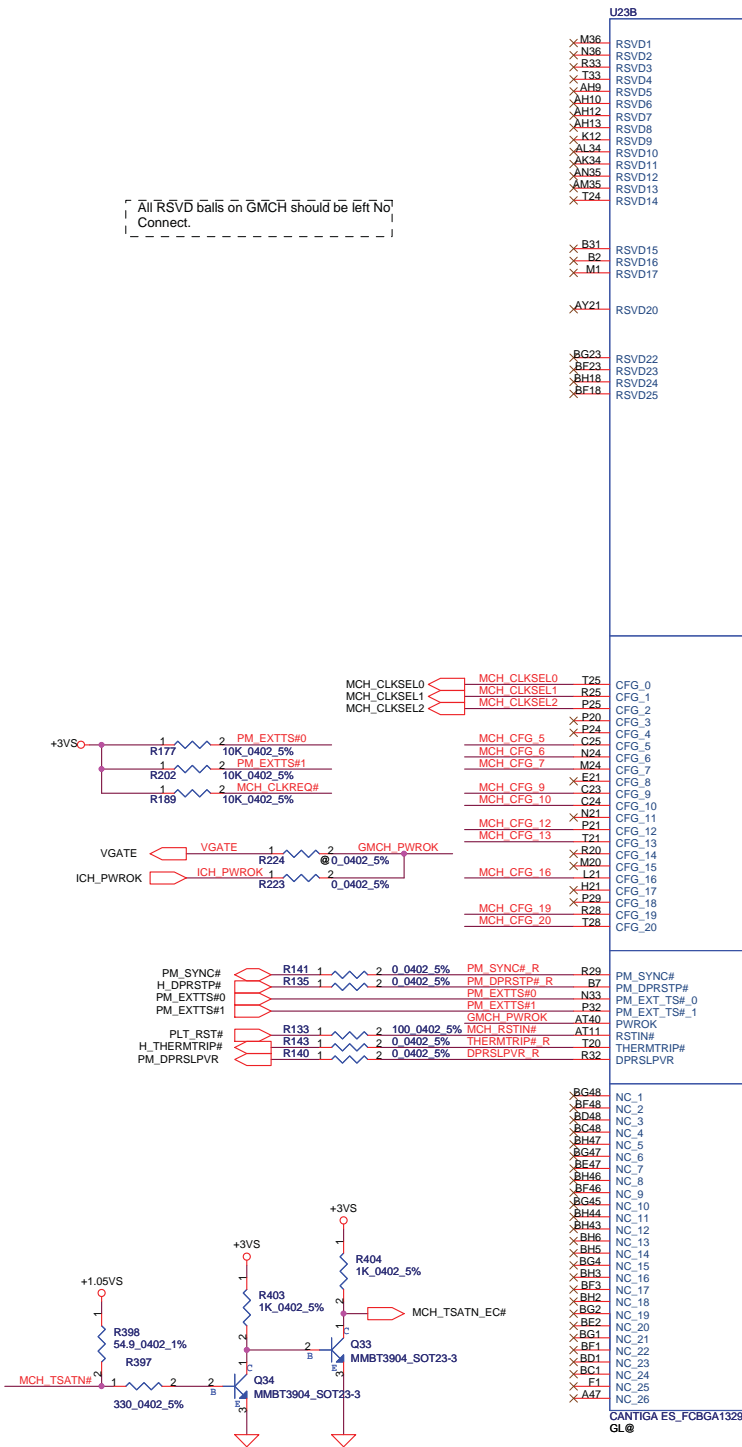
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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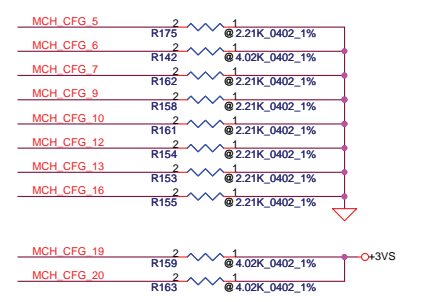


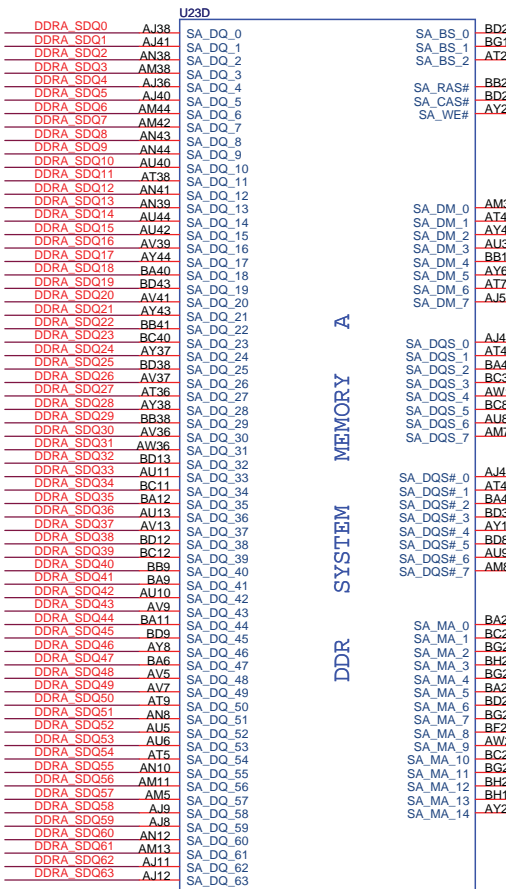
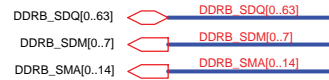
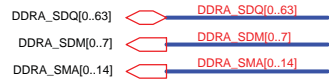
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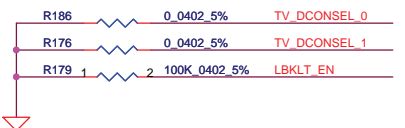
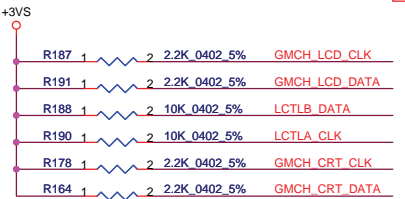
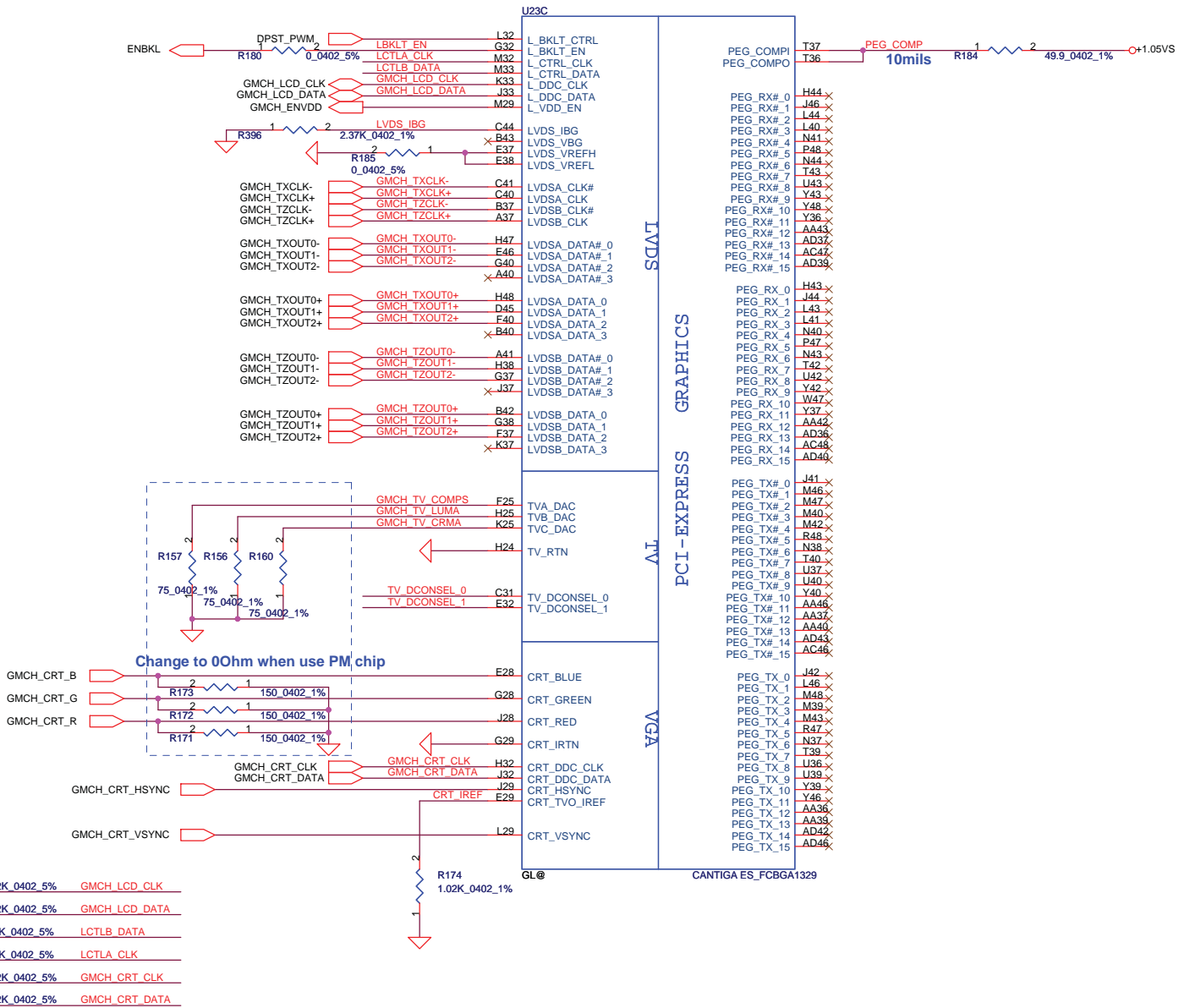
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB900 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)

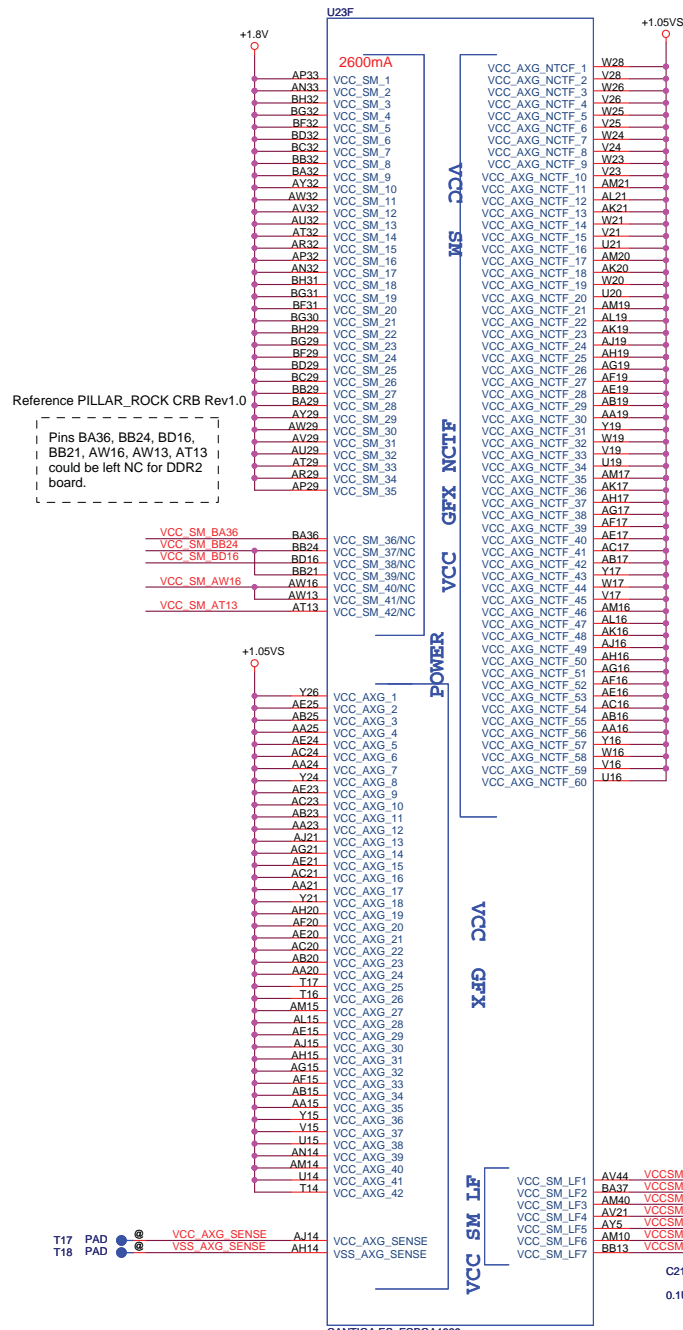




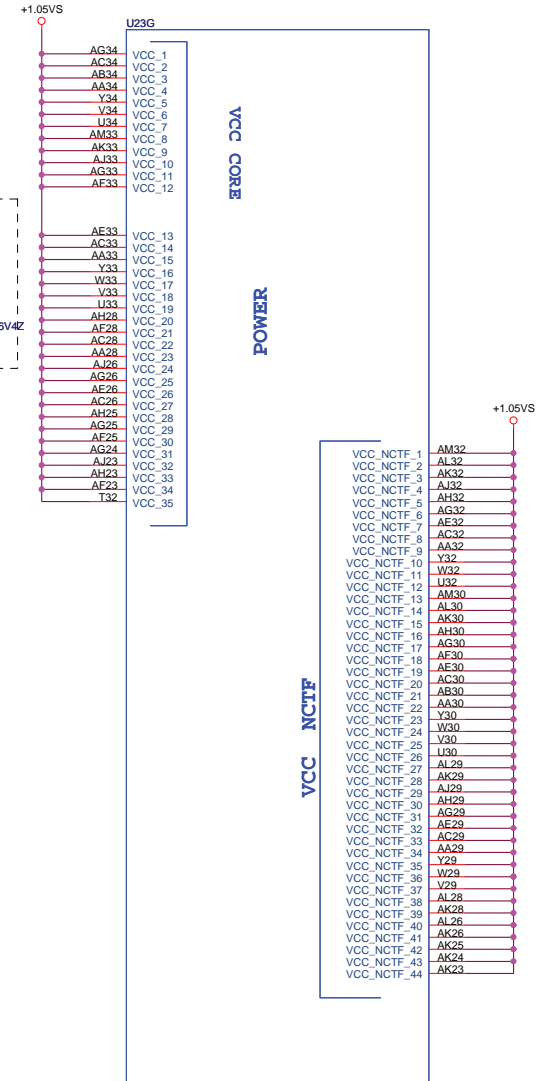
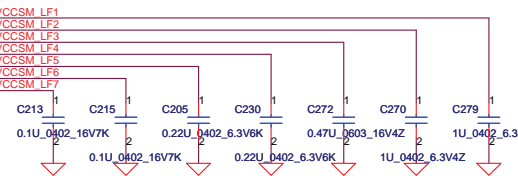
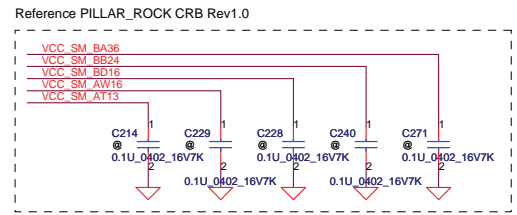
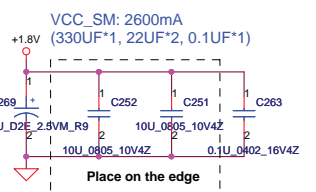
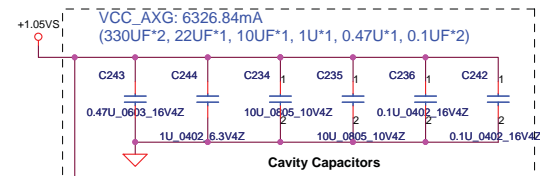
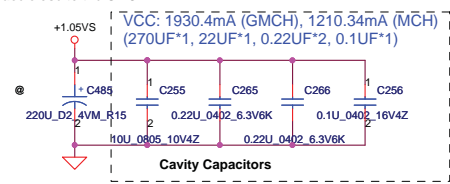
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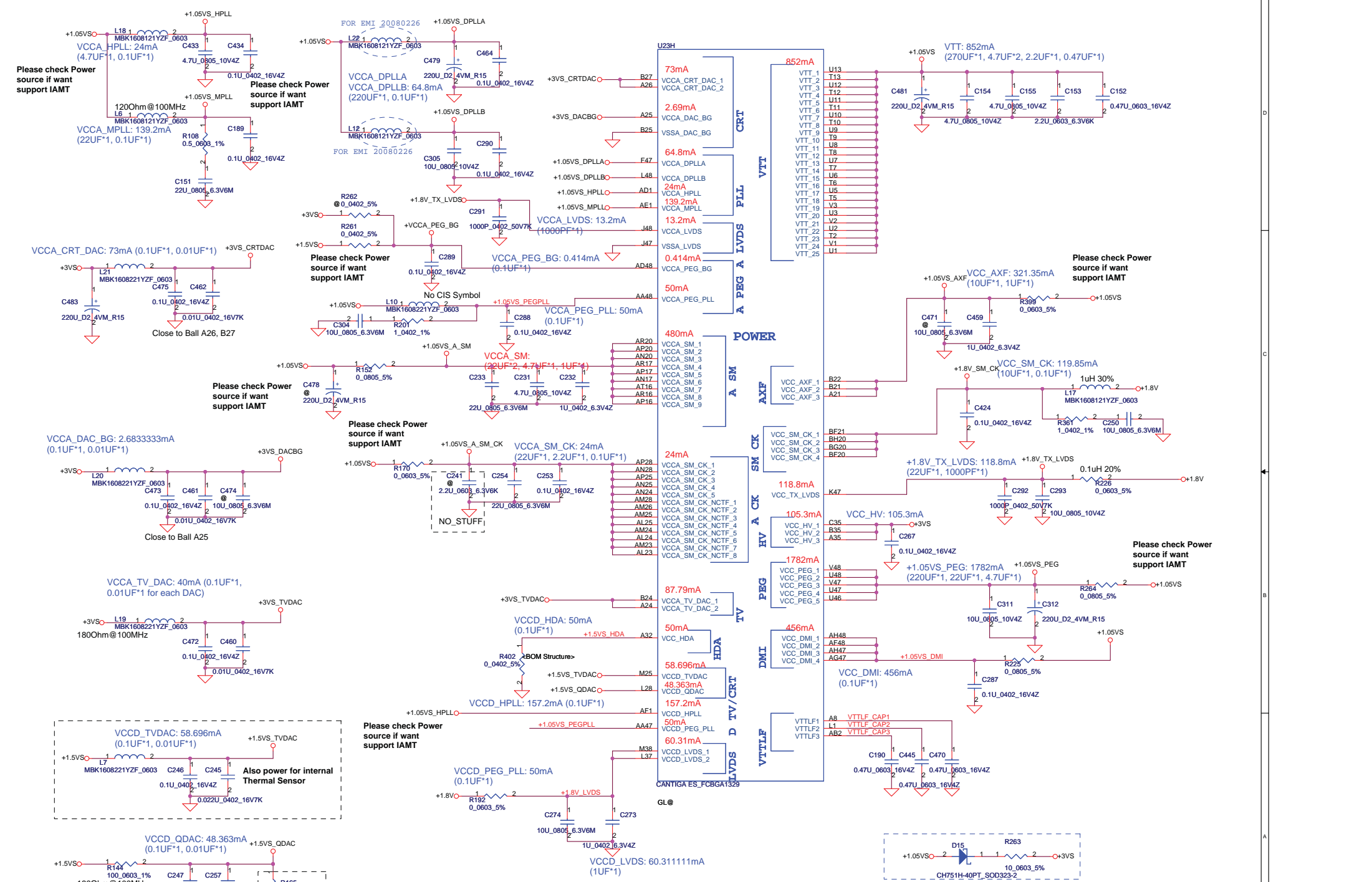
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Place close to the GMCH



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Compal Electronics, Inc.

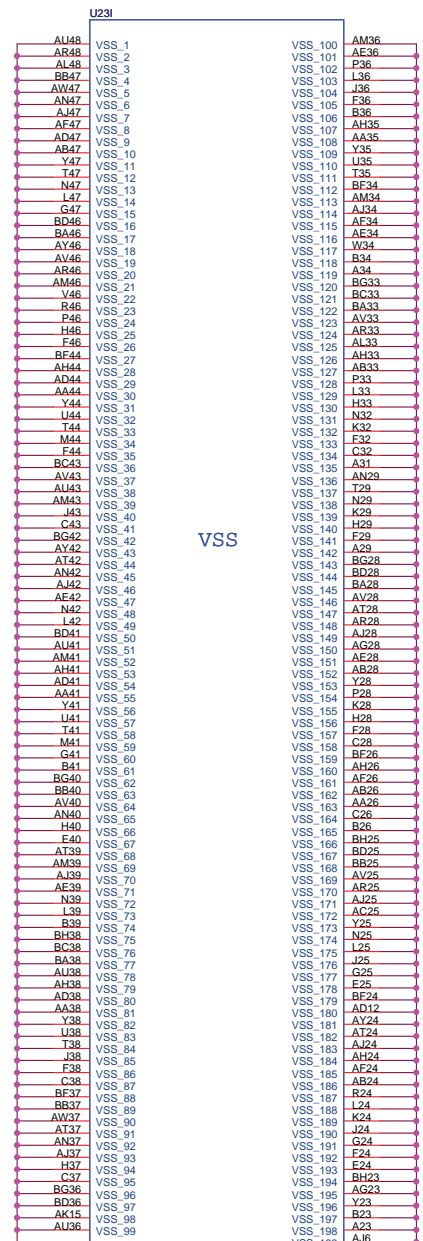
SCHMATIC, M/B A4851

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401636

Rev D

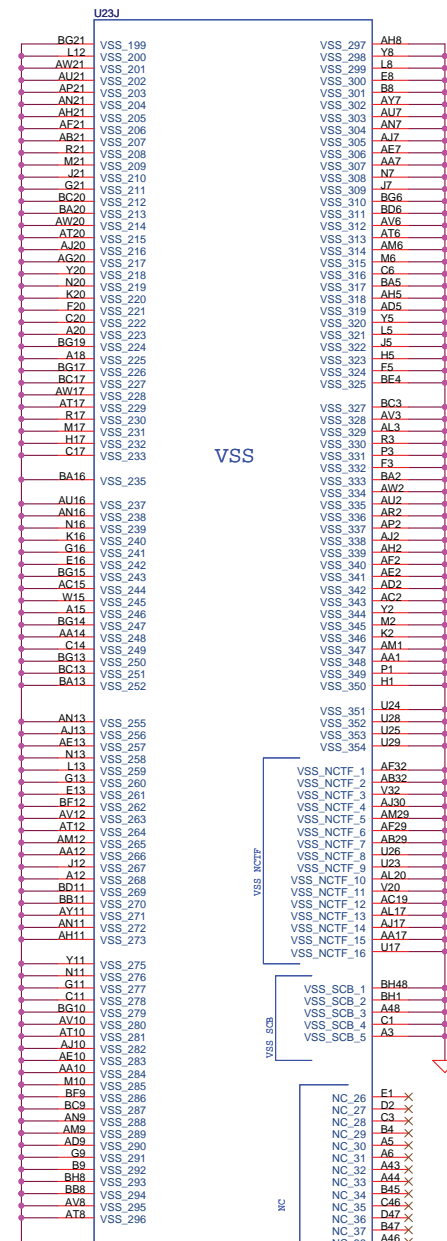
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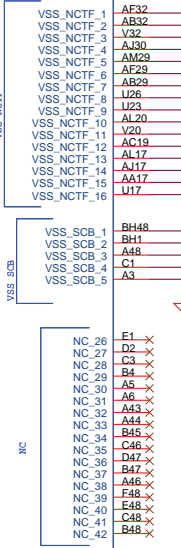
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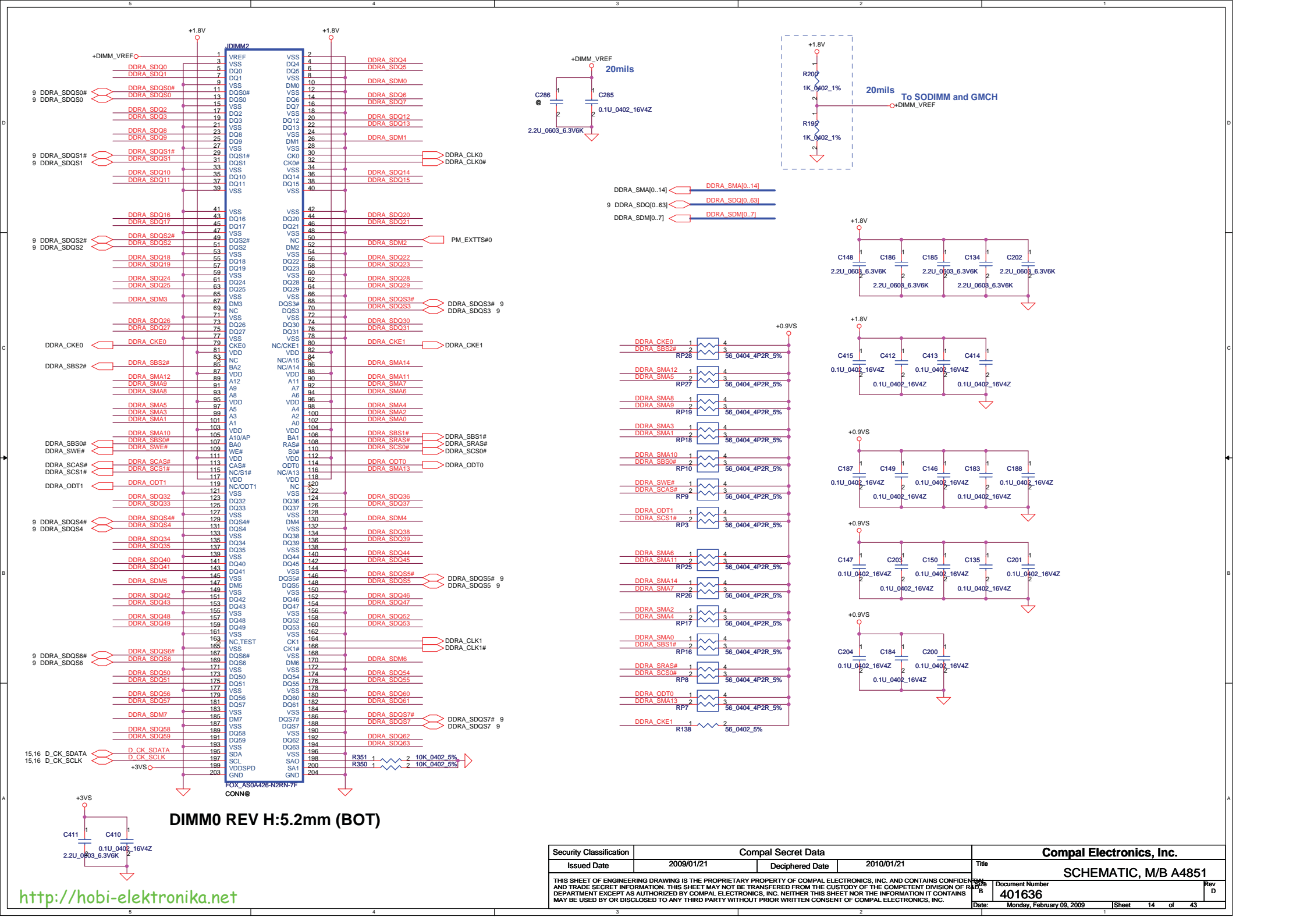
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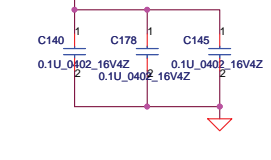
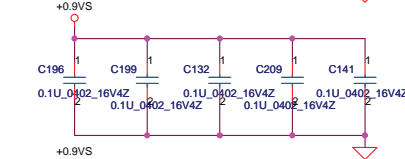
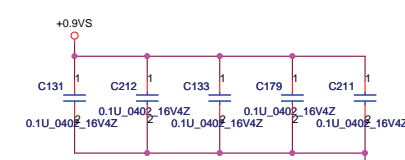
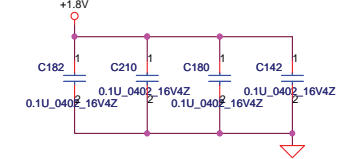
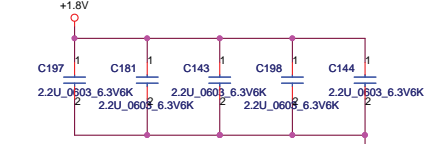
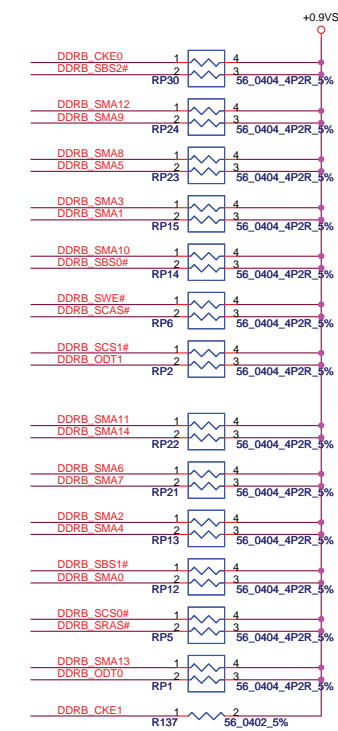
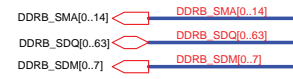
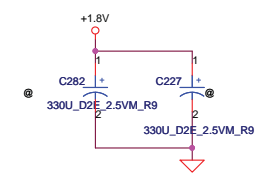
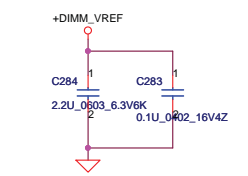
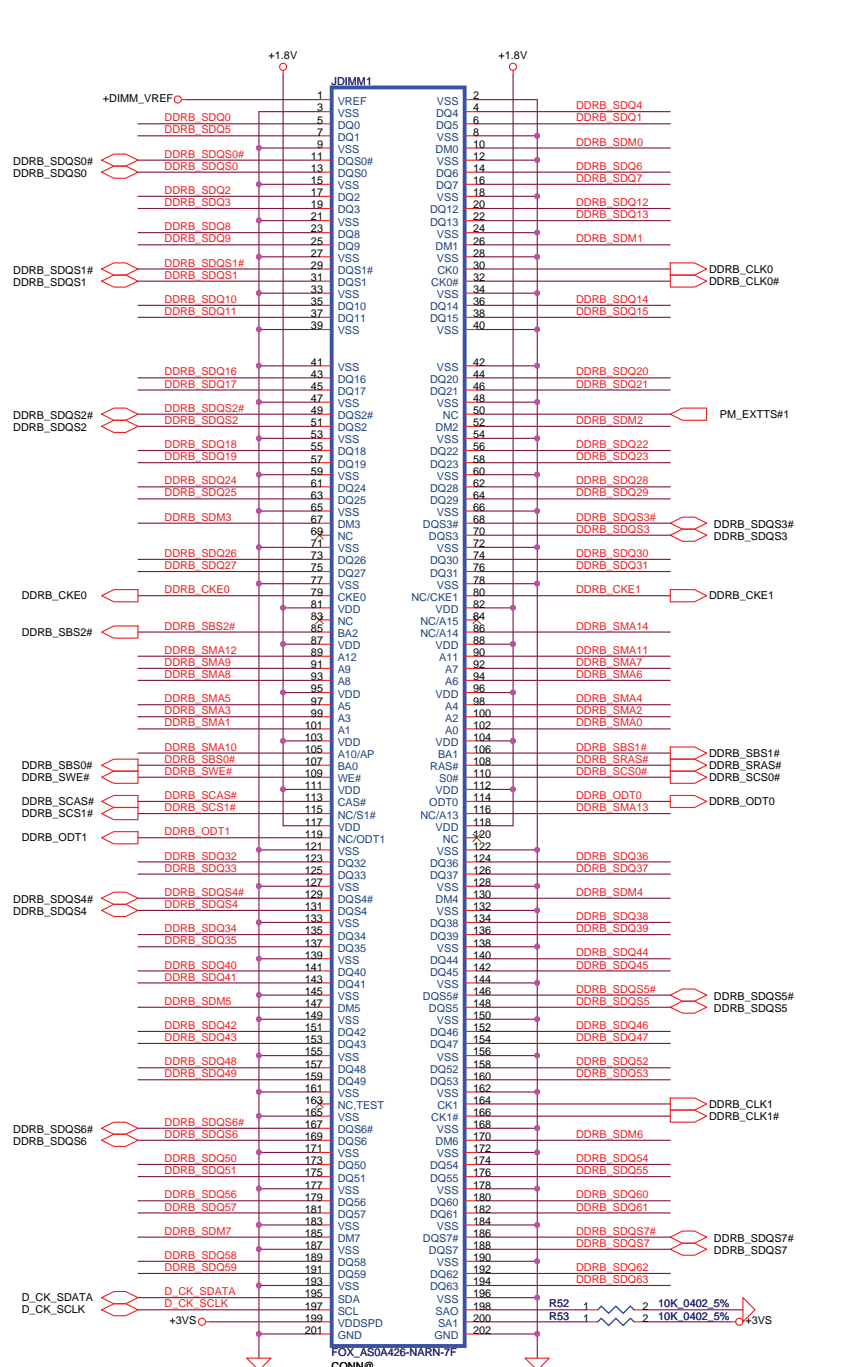
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DIMM1 REV H:9.2mm (BOT)

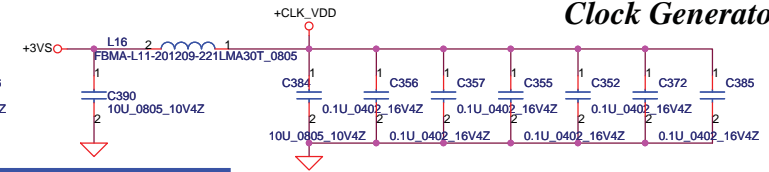
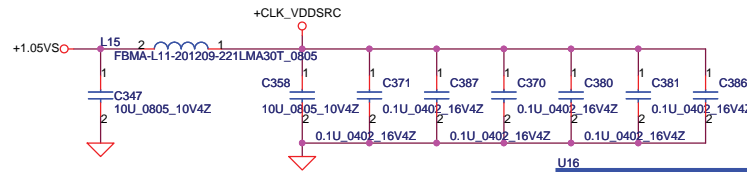
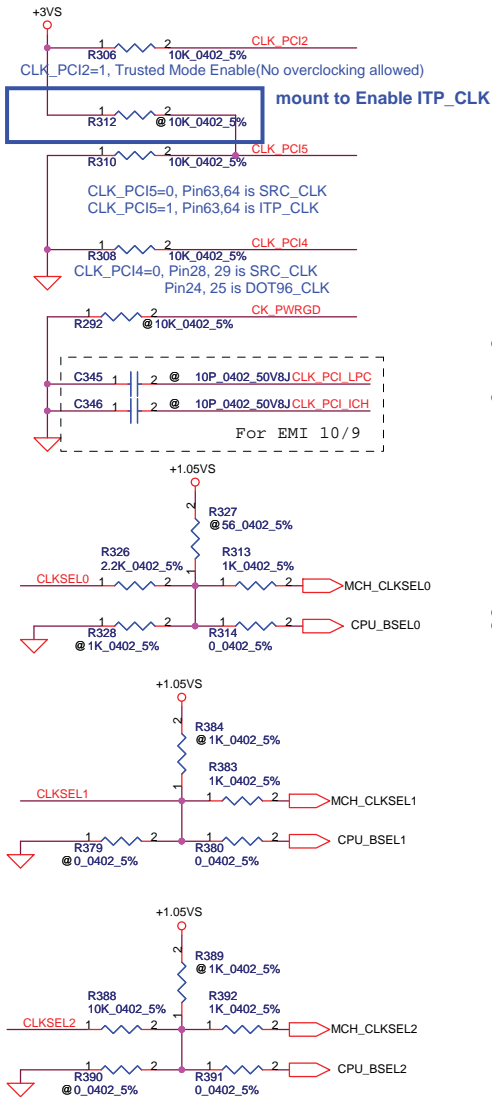
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FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

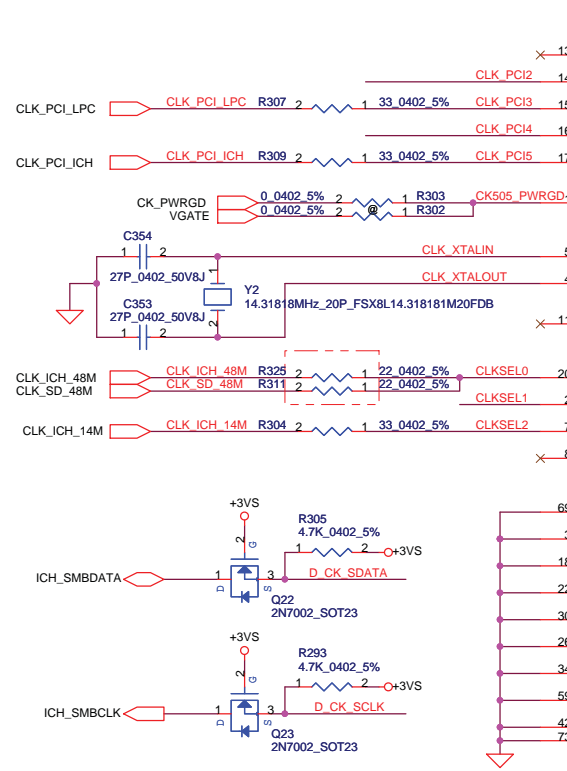
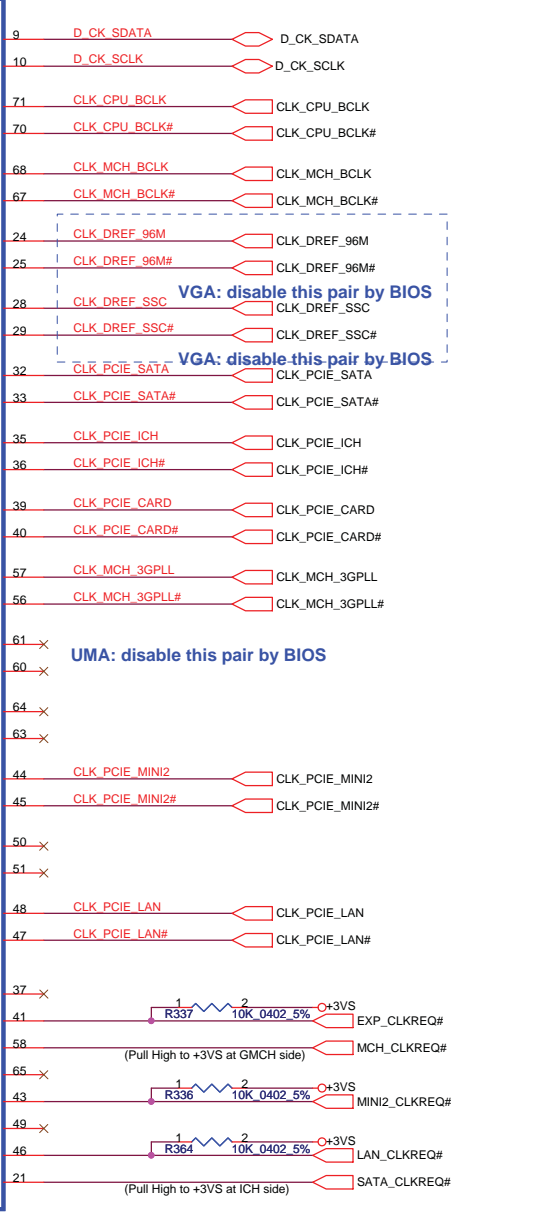
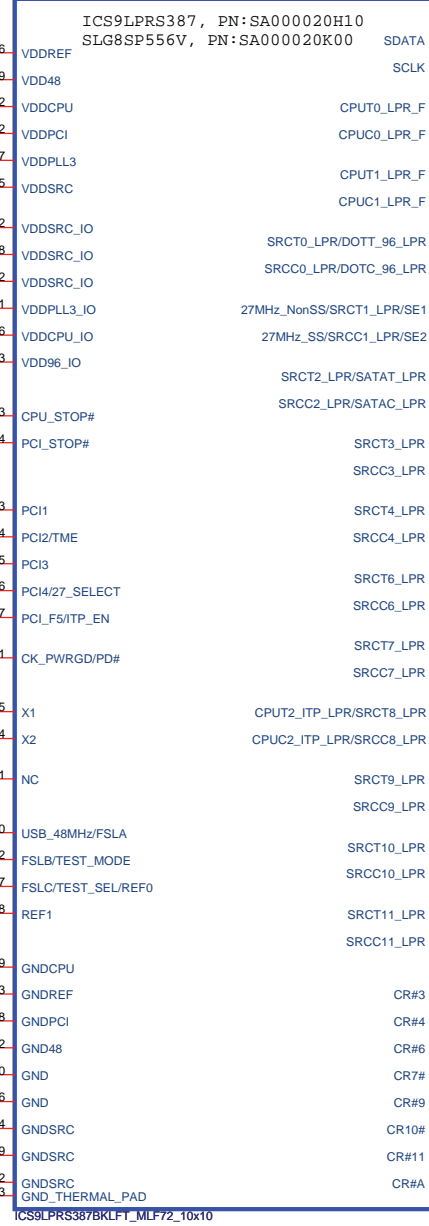
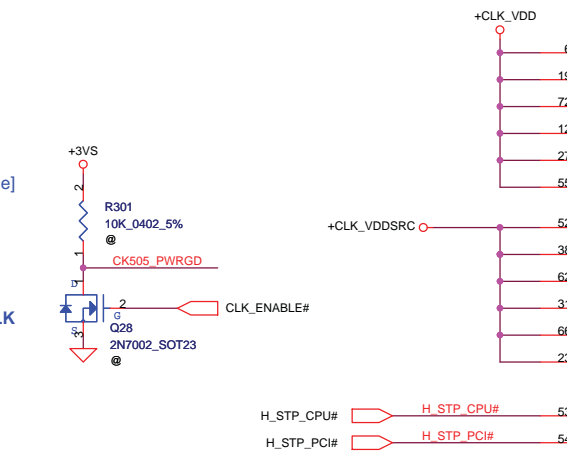
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

SRC7(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

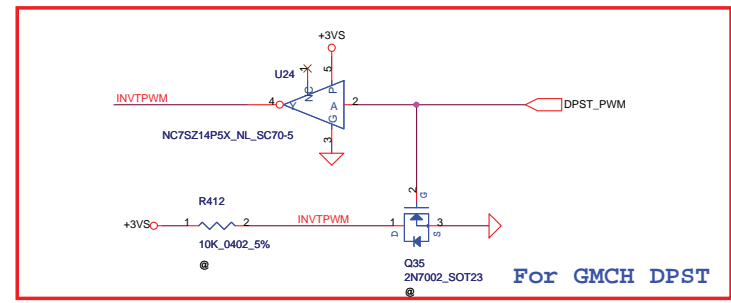
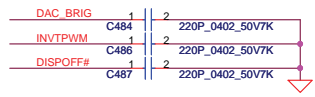
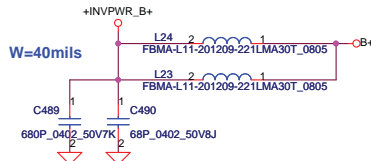
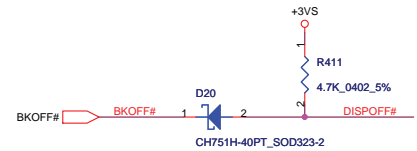
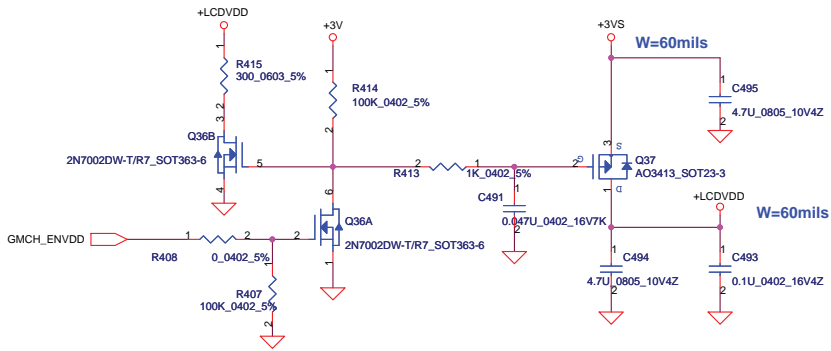


Clock Generator

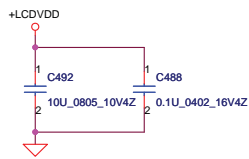
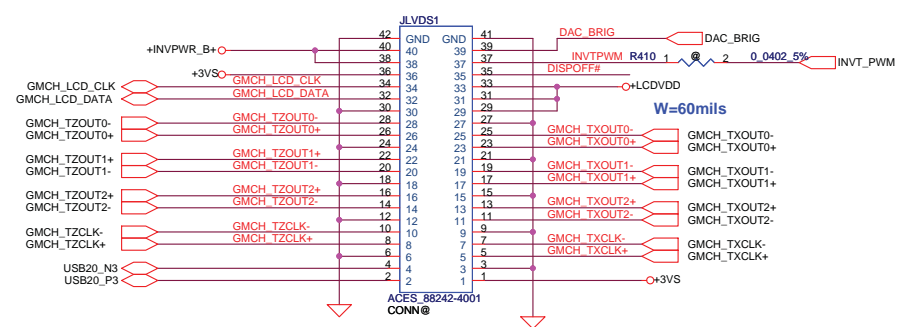


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LCD POWER CIRCUIT

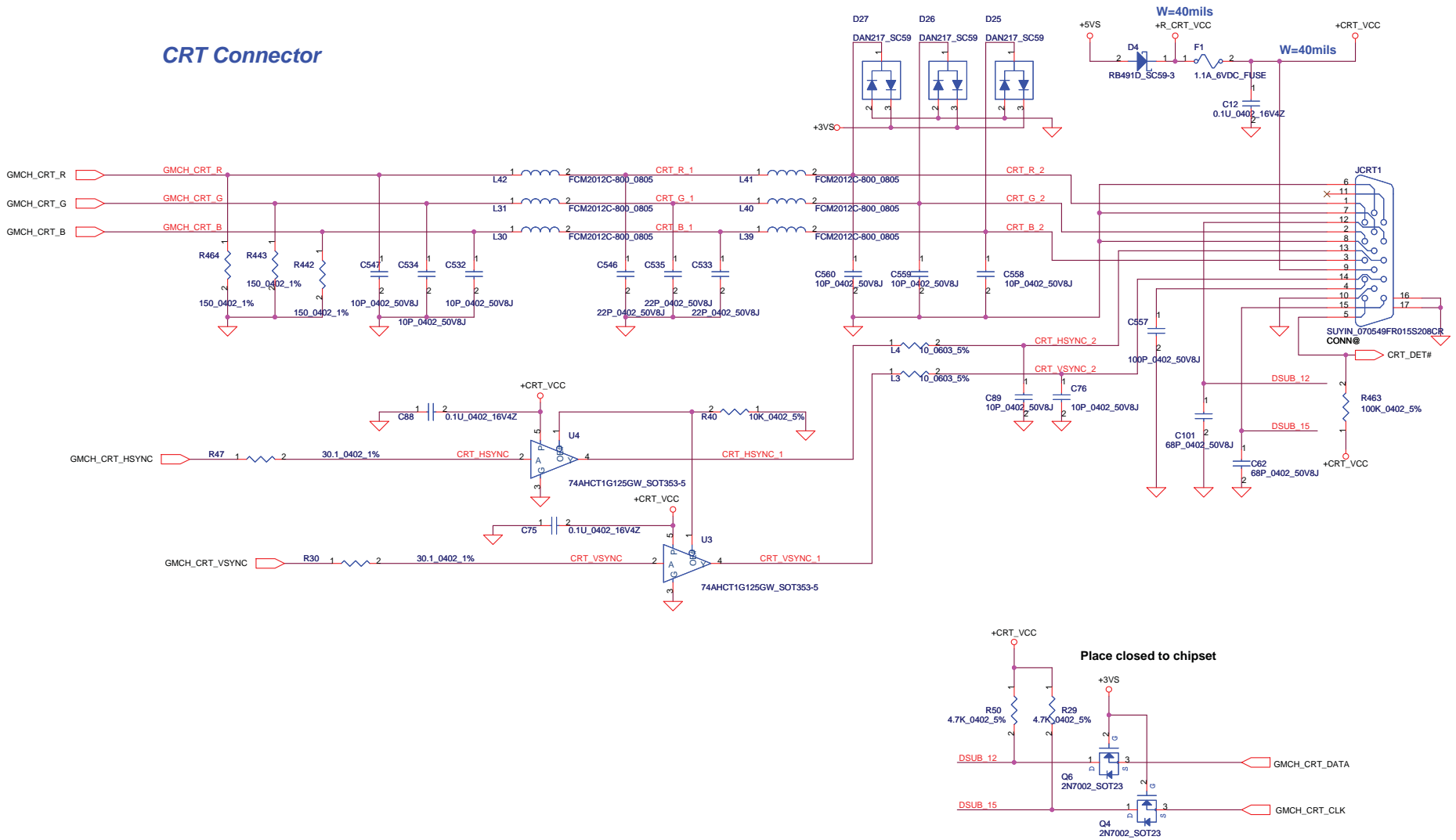


LCD/PANEL BD. Conn.

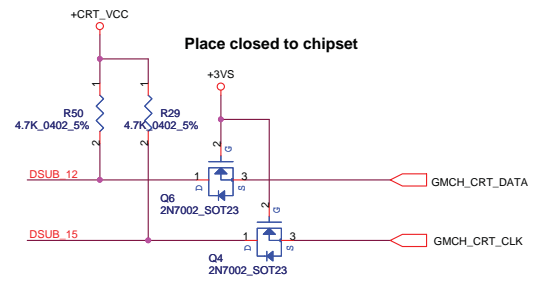


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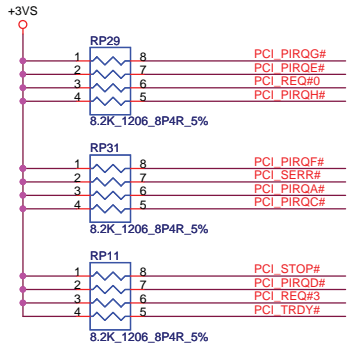
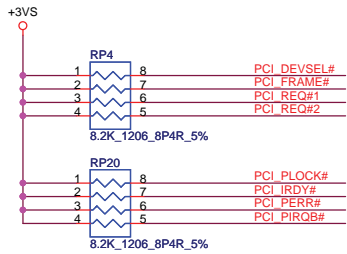
CRT Connector



Place closed to chipset

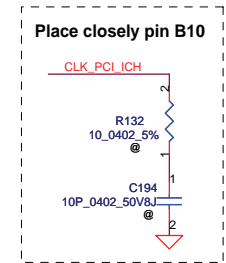
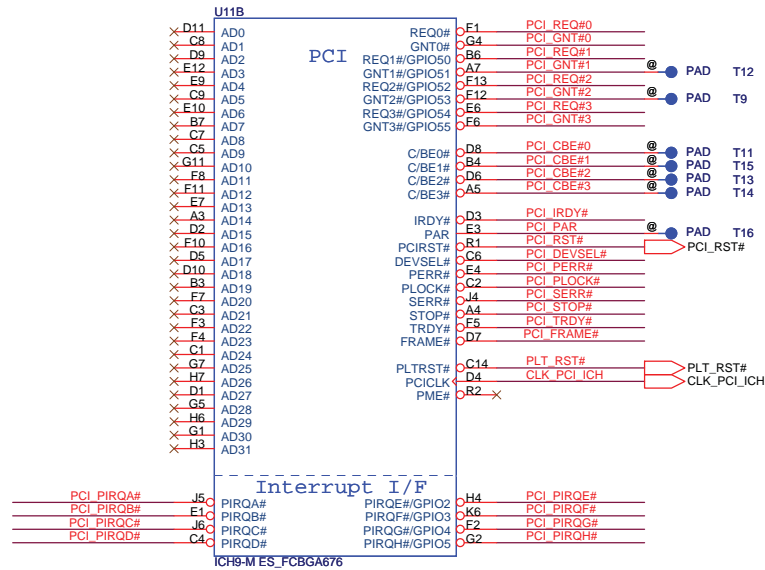


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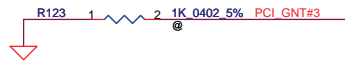
DMI for ESI-compatible operation

PCI_GNT#1	Low= DMI for ESI-compatible operation High= Default* (Internal pull-up)
------------------	--

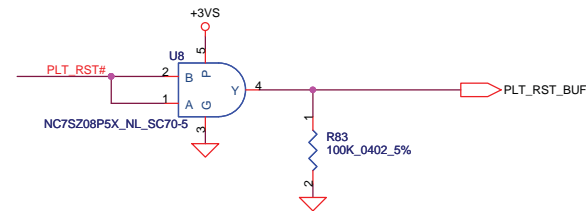
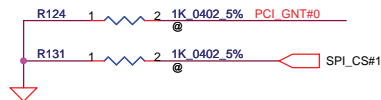


A16 Swap Override Strap

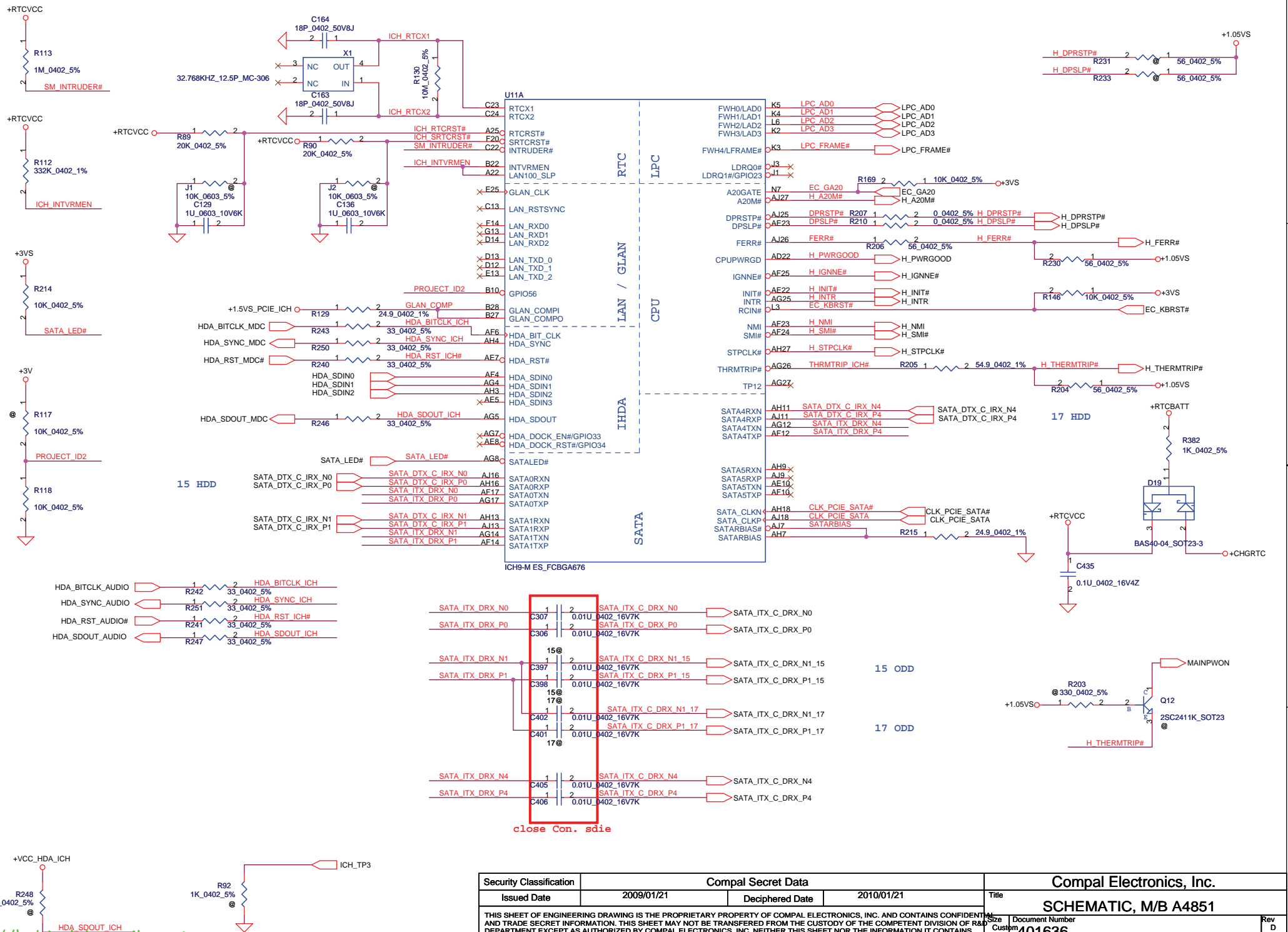
PCI_GNT#3	Low= A16 swap override Enable High= Default*
------------------	---



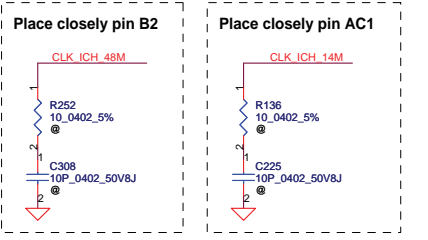
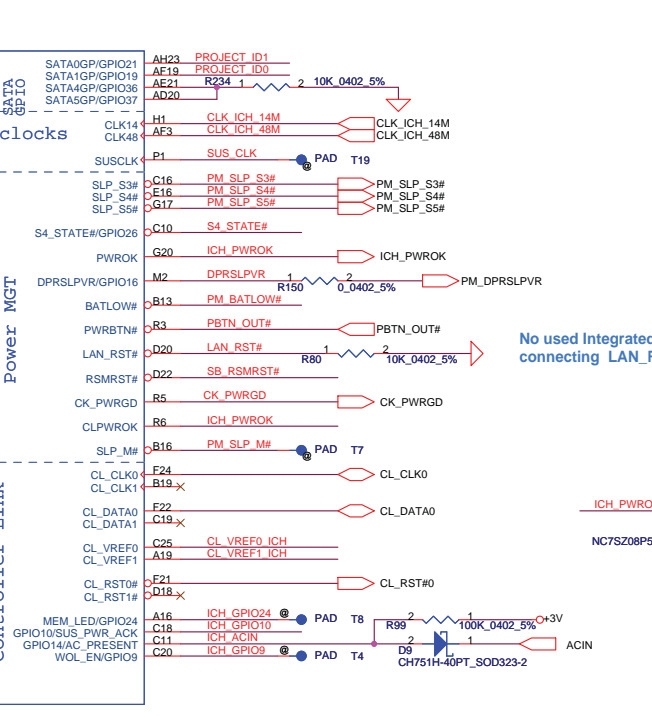
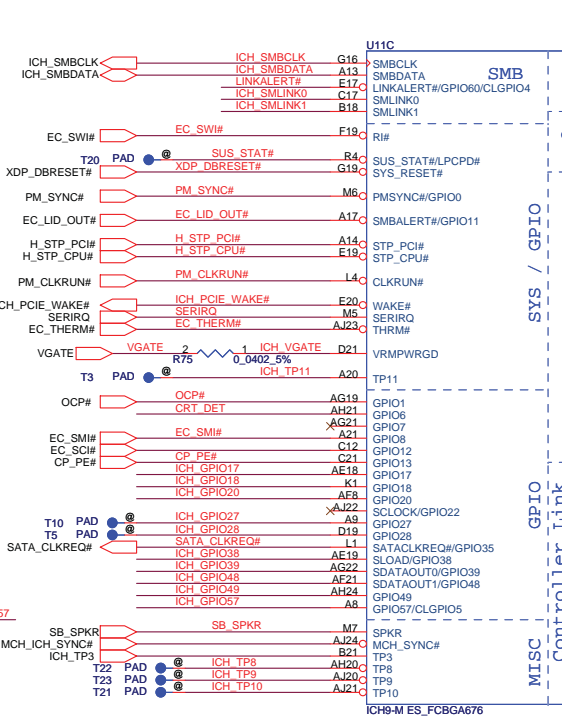
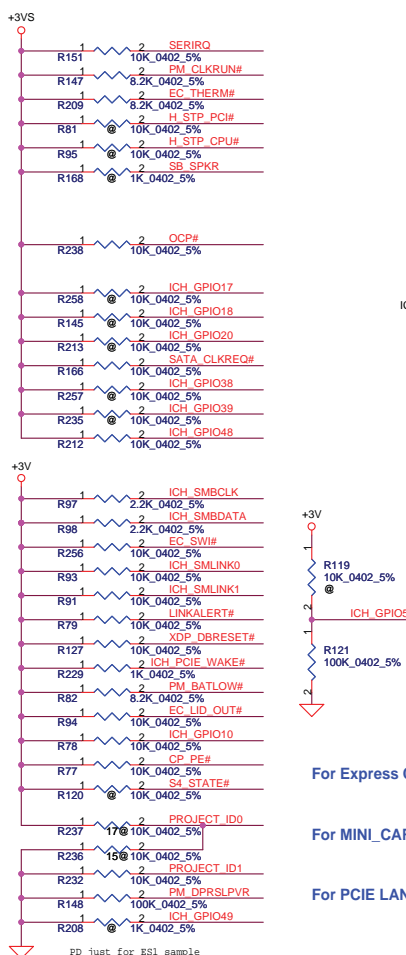
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



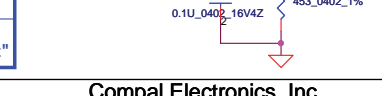
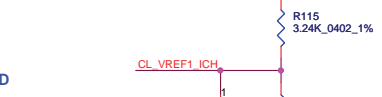
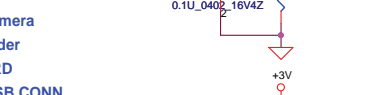
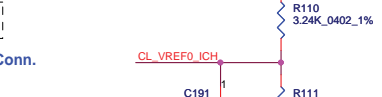
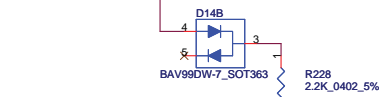
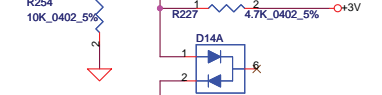
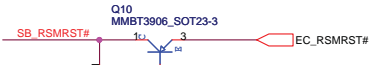
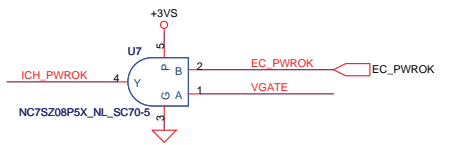
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No used Integrated LAN, connecting LAN_RST# to GND

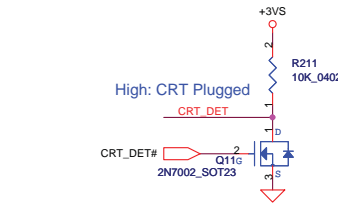


No Reboot Strap
SB_SPKR Low= Default* High= "No Reboot"

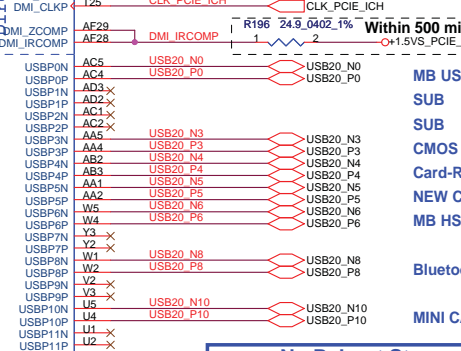
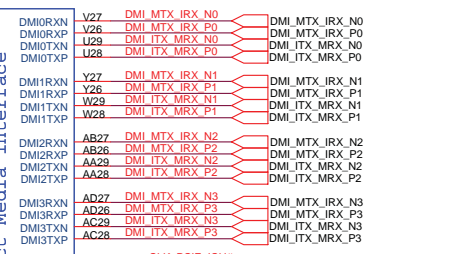
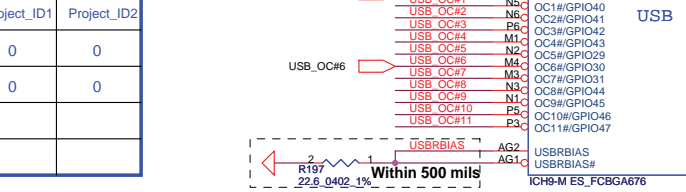
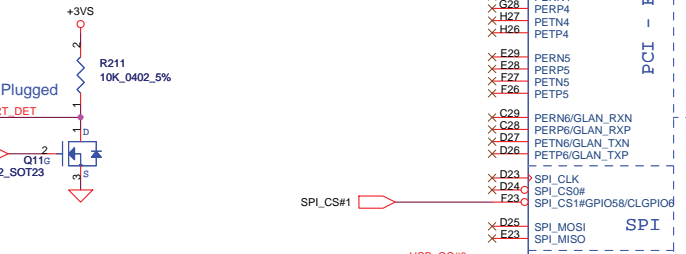
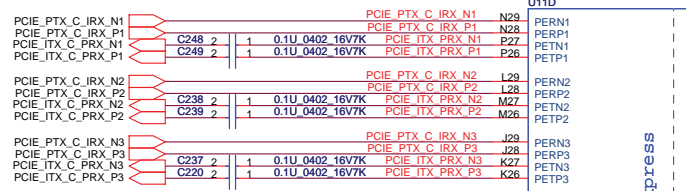
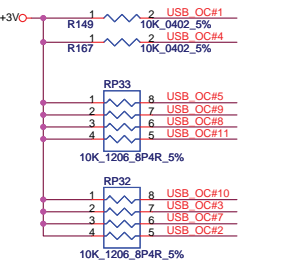
For Express Card

For MINI_CARD1

For PCIE LAN



	Project_ID0	Project_ID1	Project_ID2
KAWF0	0	0	0
KAWH0	1	0	0



Internal TPM Strap
SPI_MOSI Low= Disable* High= iTPM enable by MCH strap

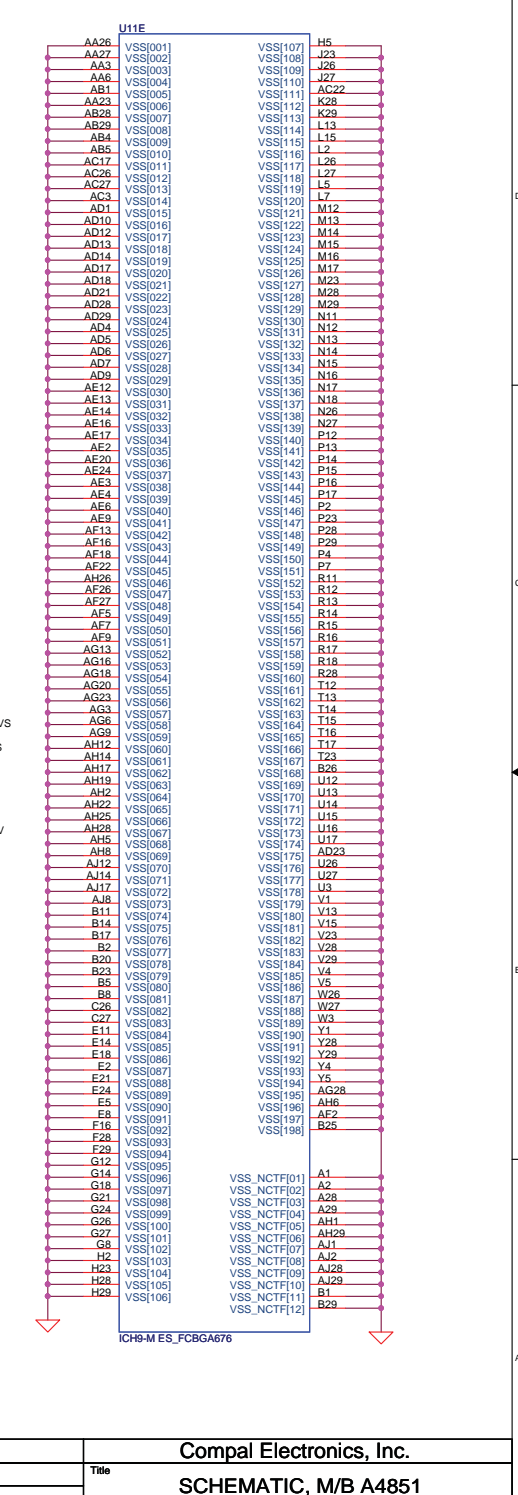
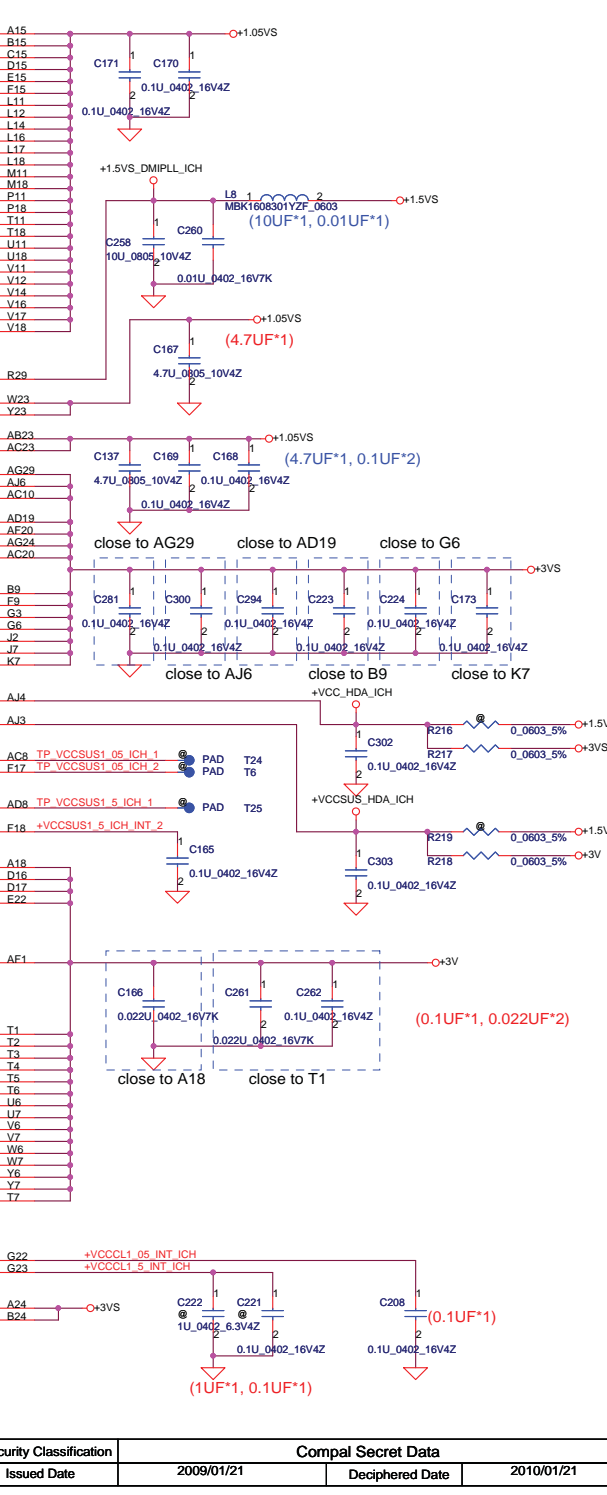
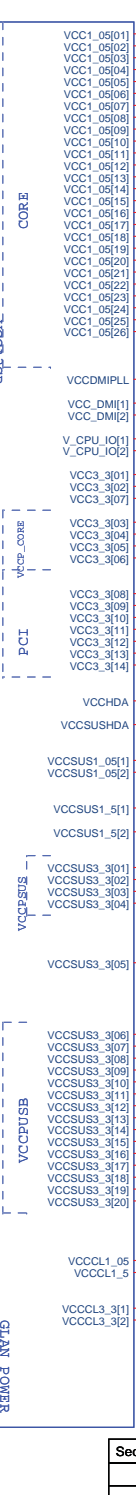
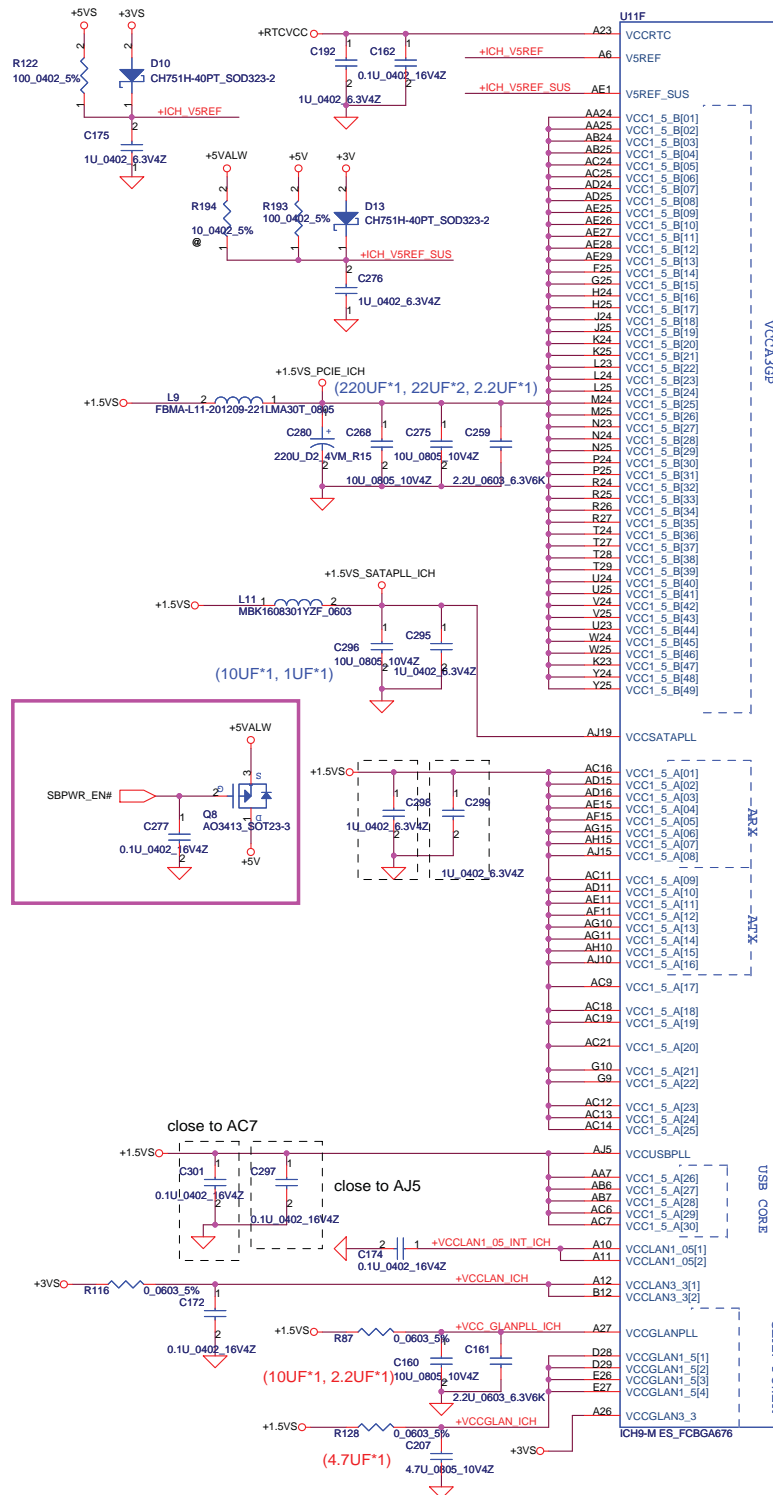
DMI Termination Voltage
GPIO49 Low= Desktop used High= Mobile* (Internal pull-up)

Security Classification	Compal Secret Date
Issued Date	2009/01/21
Deciphered Date	2010/01/21

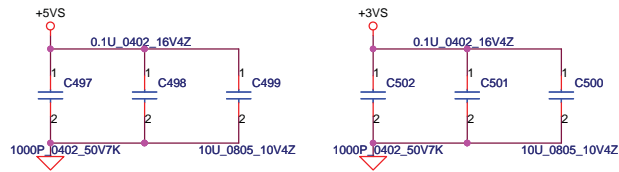
Compal Electronics, Inc.
SCHEMATIC, M/B A4851

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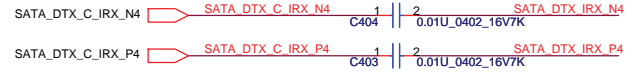
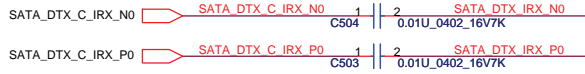
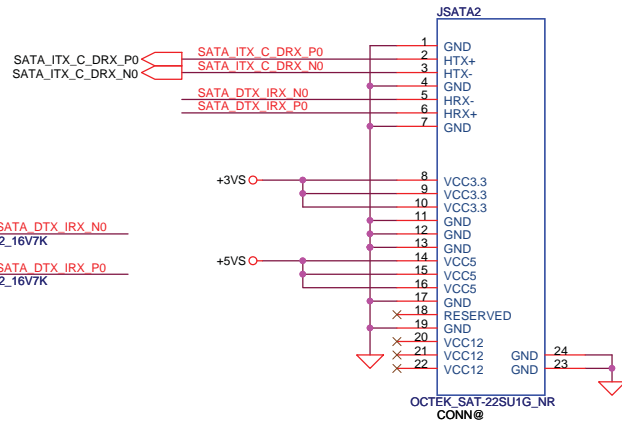
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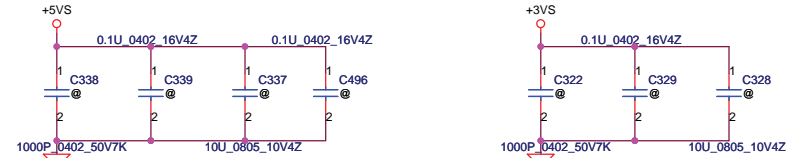
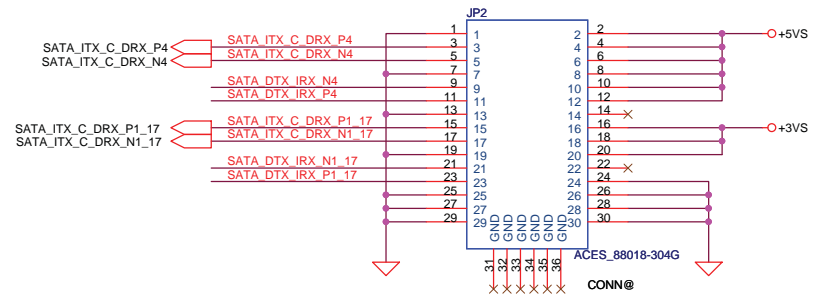
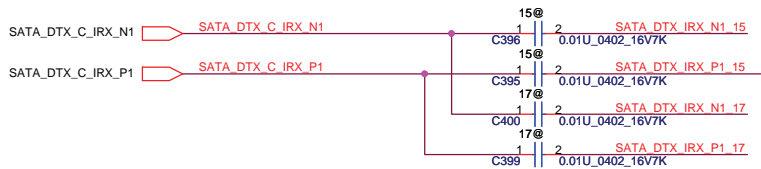
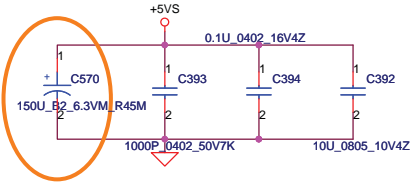
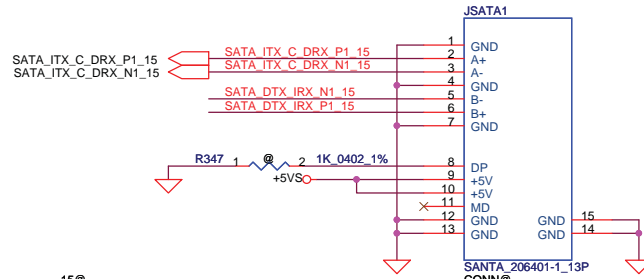
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SATA HDD Conn.

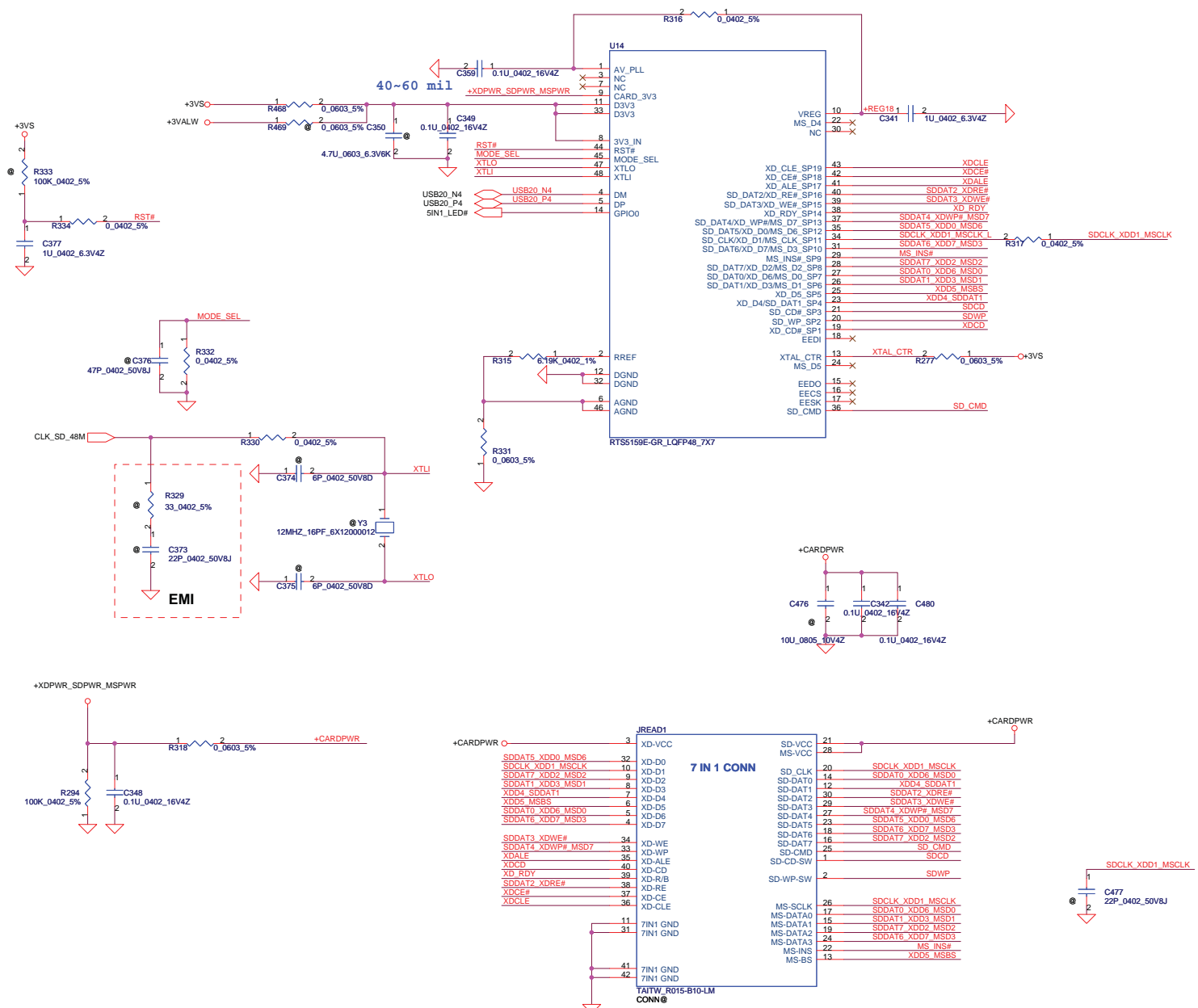


SATA ODD Conn.

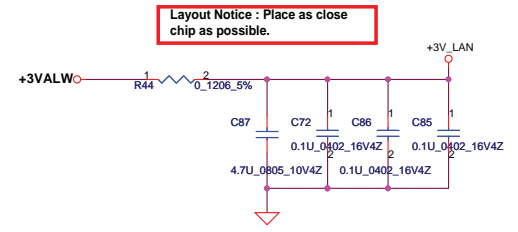
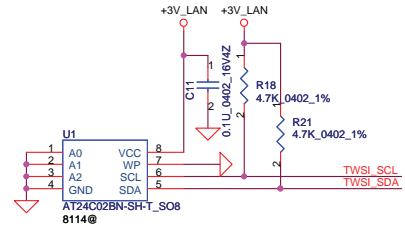
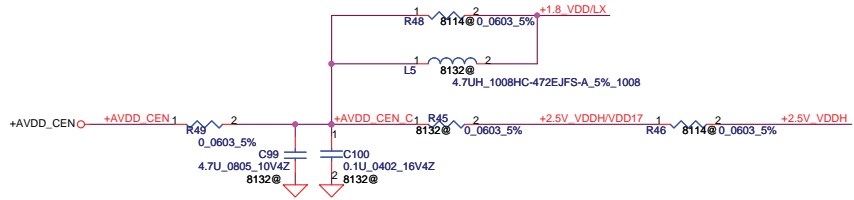


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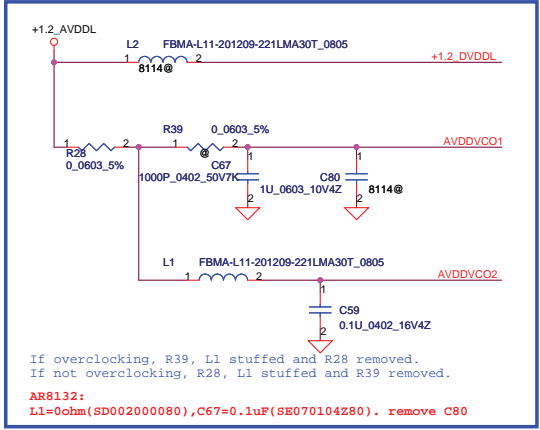
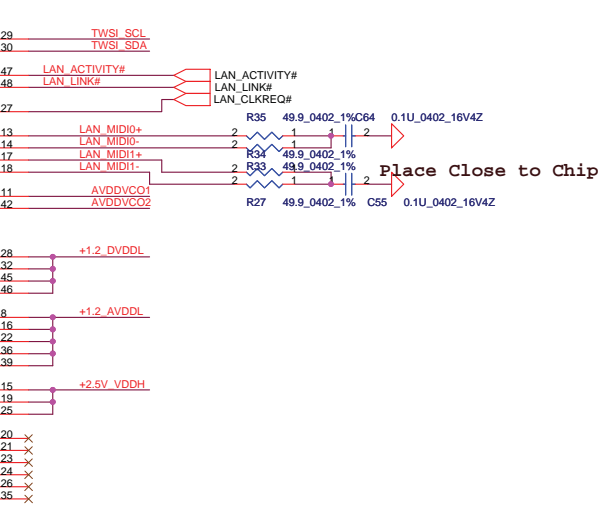
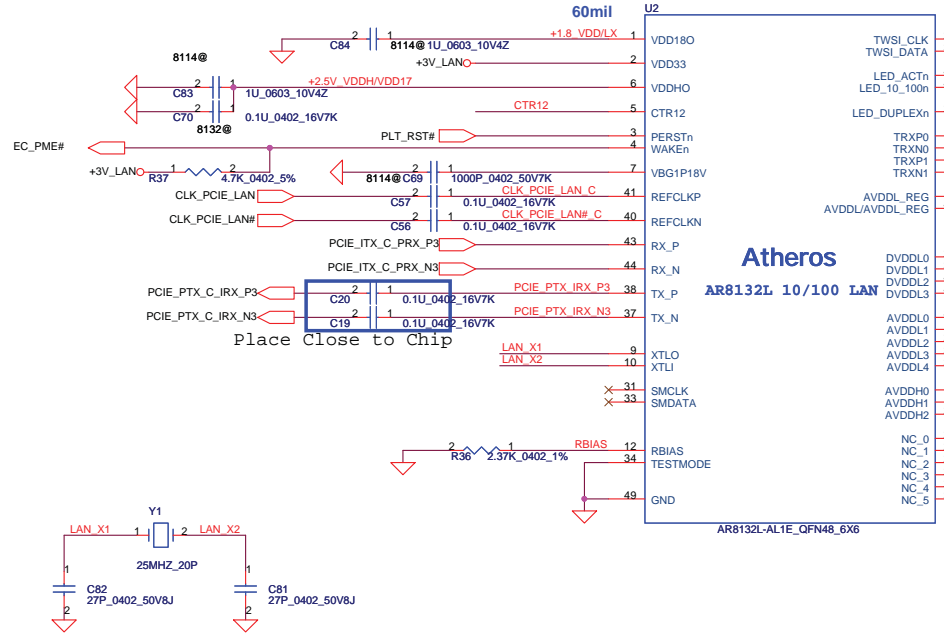
Vender suggestion



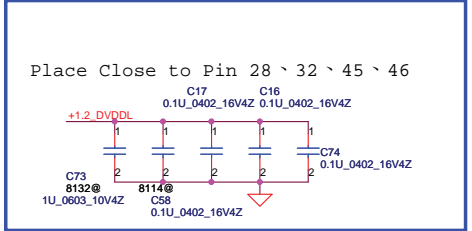
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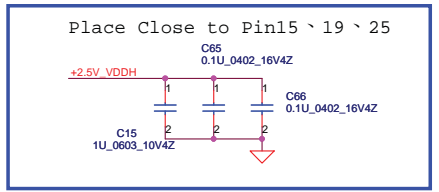
Layout Notice : Place as close chip as possible.



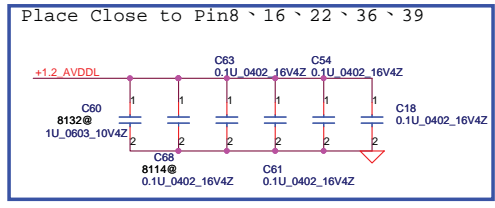
If overclocking, R39, L1 stuffed and R28 removed.
If not overclocking, R28, L1 stuffed and R39 removed.
AR8132:
L1=0ohm(SD00200080), C67=0.1uF(SE070104280). remove C80



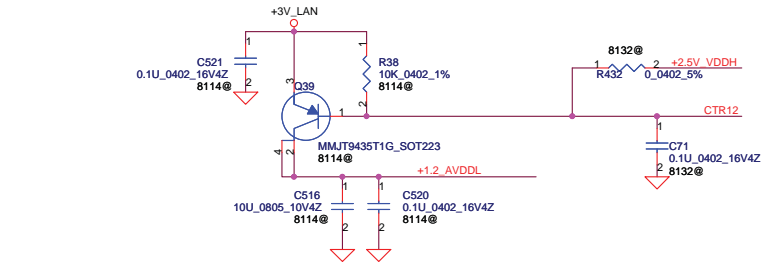
Place Close to Pin 28 \ 32 \ 45 \ 46



Place Close to Pin15 \ 19 \ 25

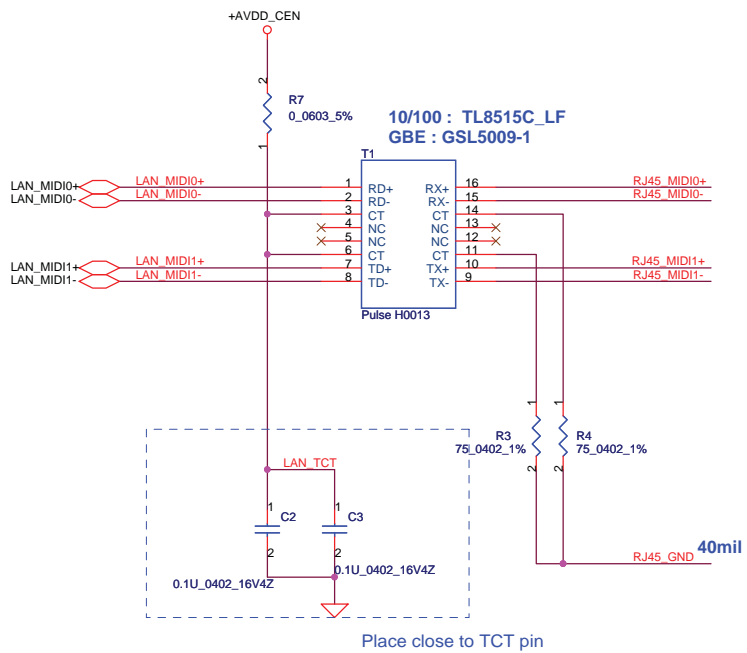


Place Close to Pin8 \ 16 \ 22 \ 36 \ 39

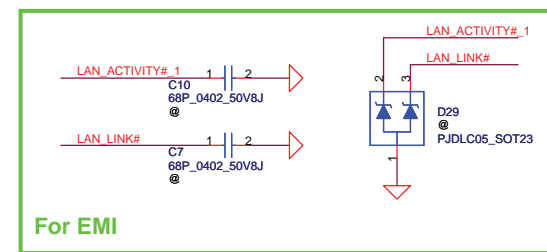
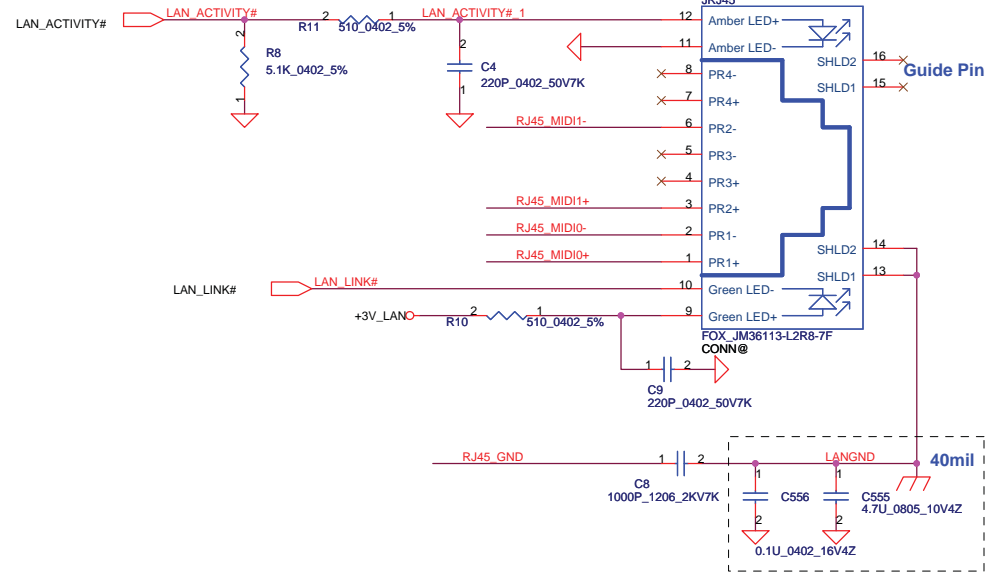


Place Close to Chip

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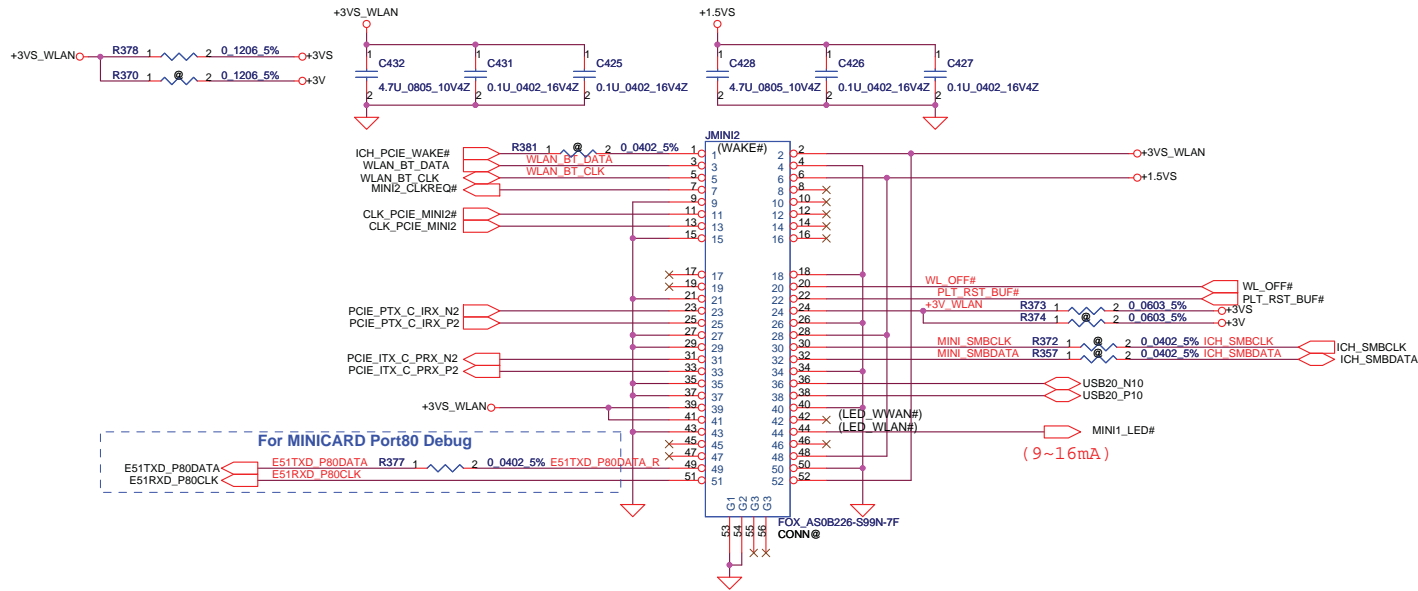


Place close to TCT pin

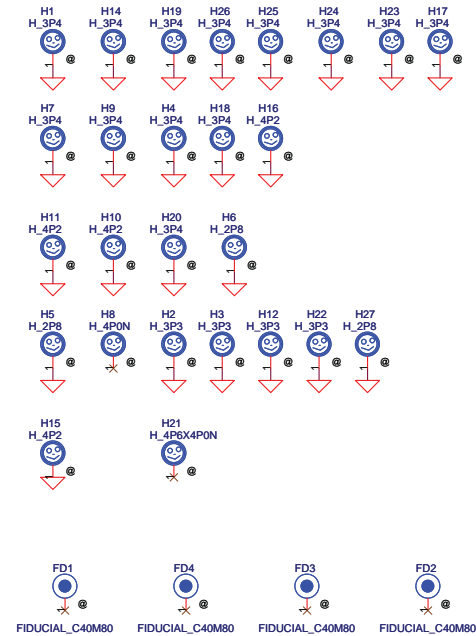


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For Wireless LAN

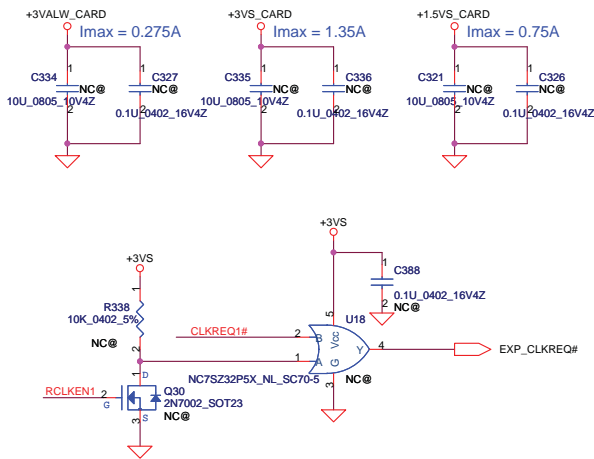
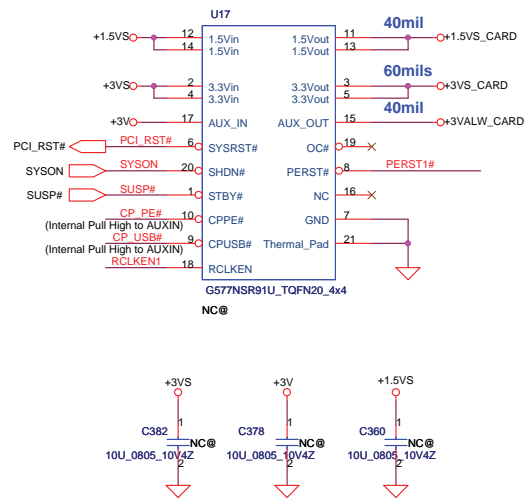


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

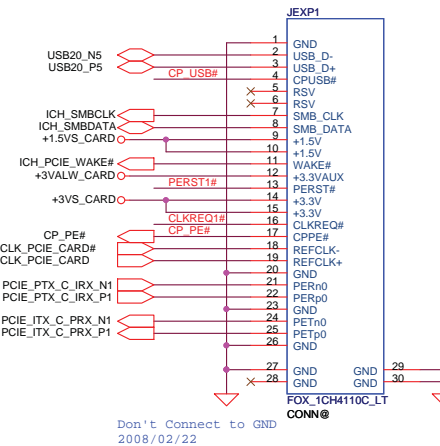


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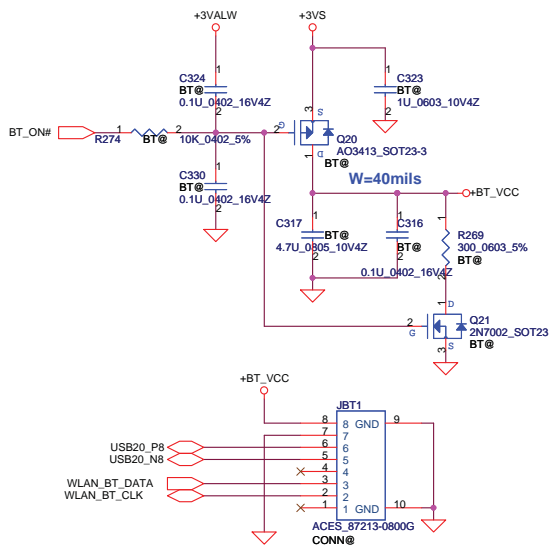
New Card Power Switch



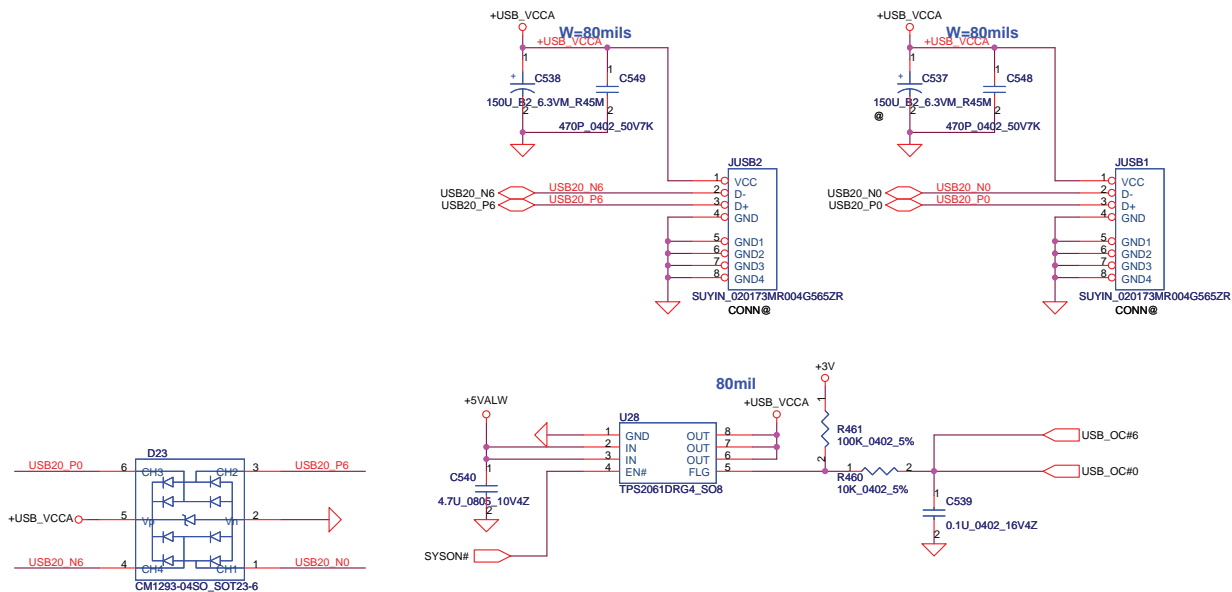
New Card Socket (Left/TOP)



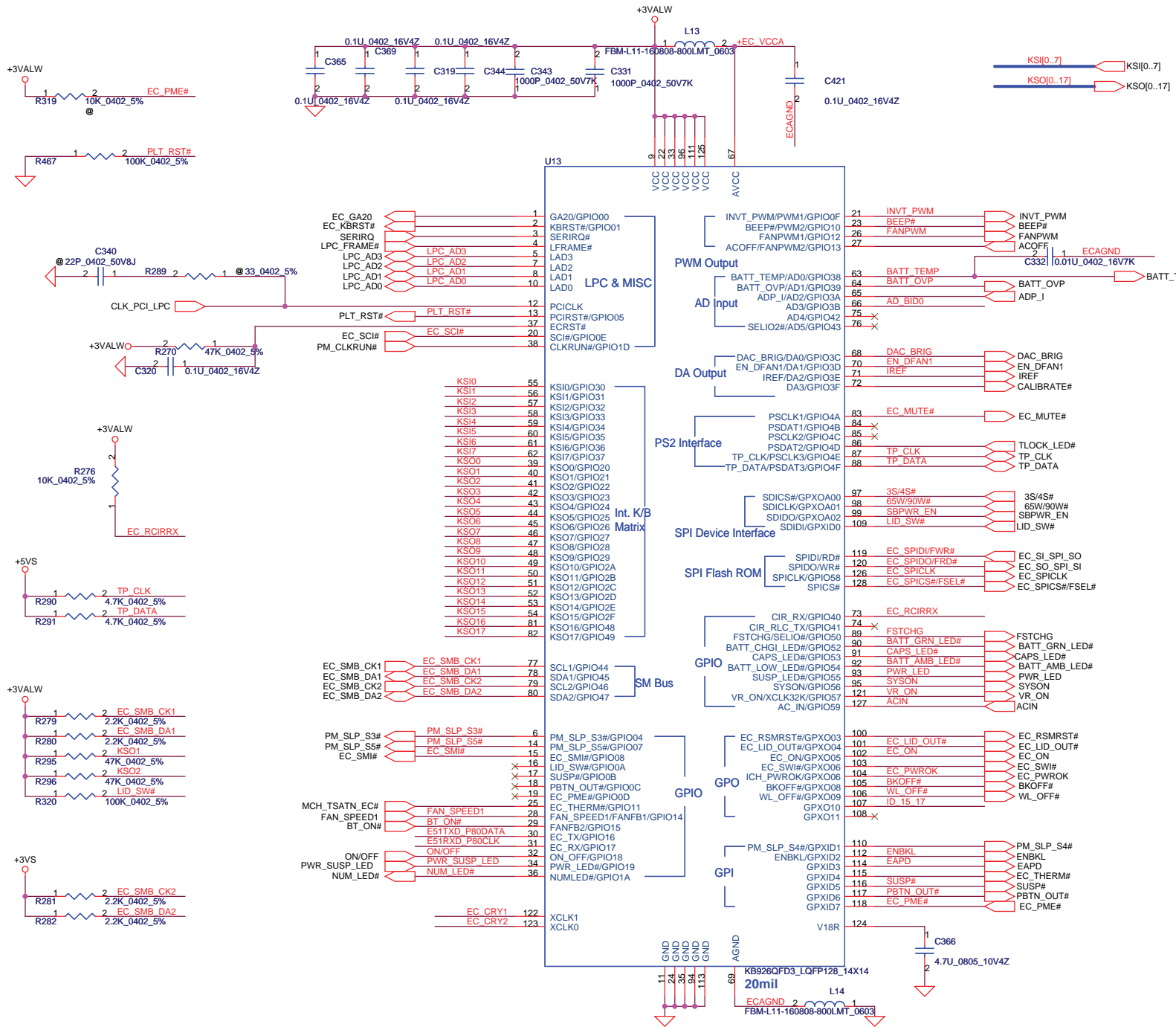
Bluetooth Conn.



USB CONN.

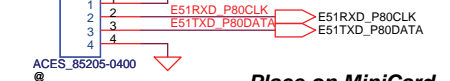


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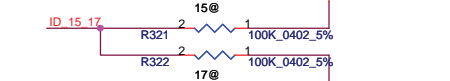
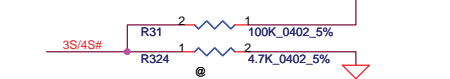
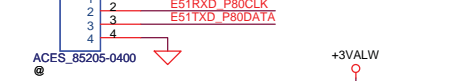


For EC Tools

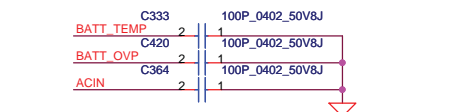
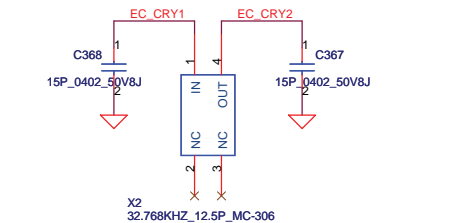
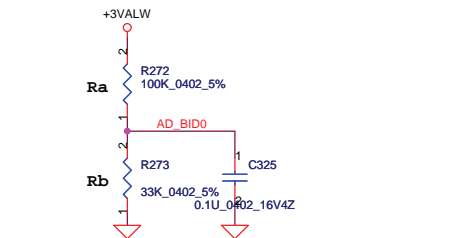
Place on RAM door



Place on MiniCard

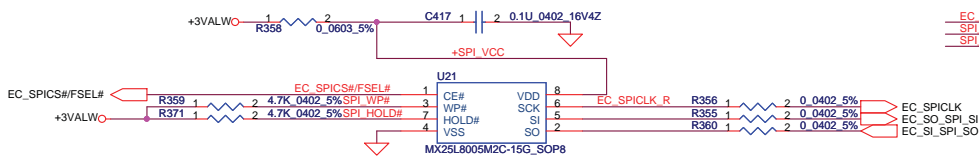


Analog Board ID definition, Please see page 3.

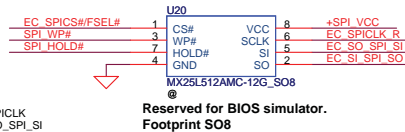


<BOM Structure>

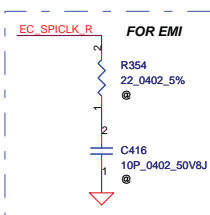
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ENE suggestion SPI Frequency over 66MHz
 SST: 50MHz
 MXIC: 70MHz
 ST: 40MHz



Reserved for BIOS simulator.
 Footprint S08



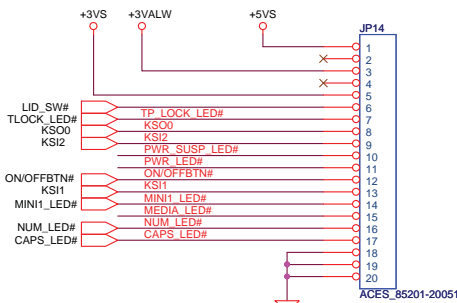
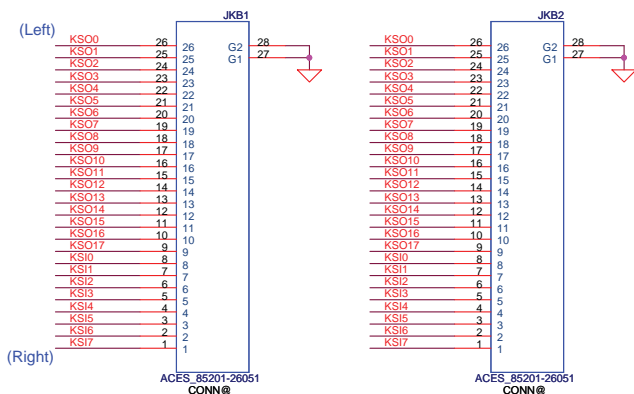
To POWER/B

INT_KBD Conn.

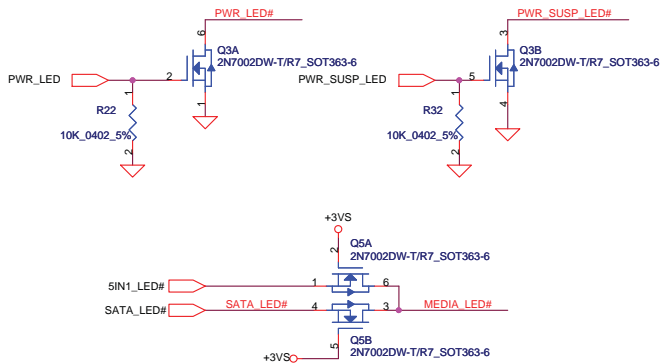
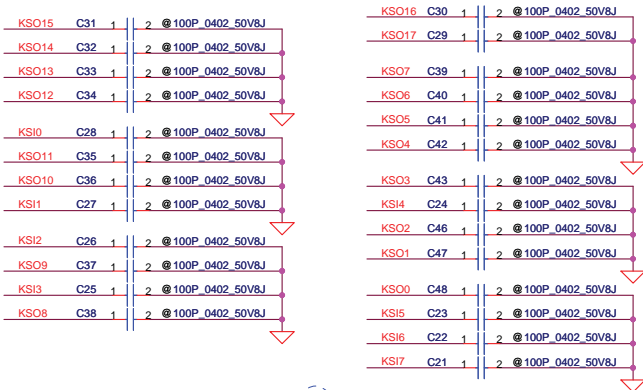
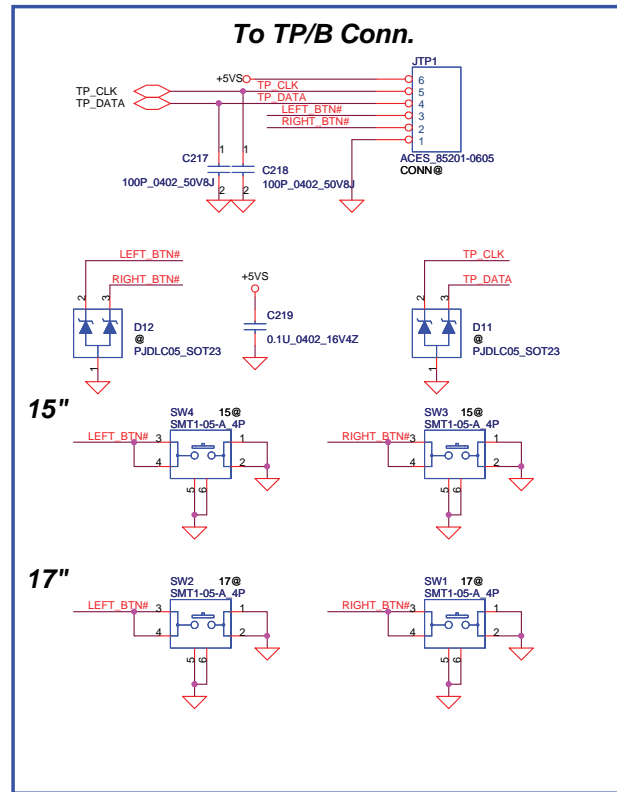


15"

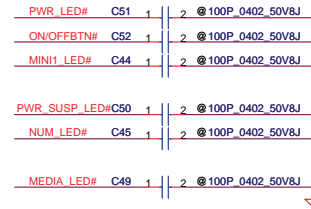
17"



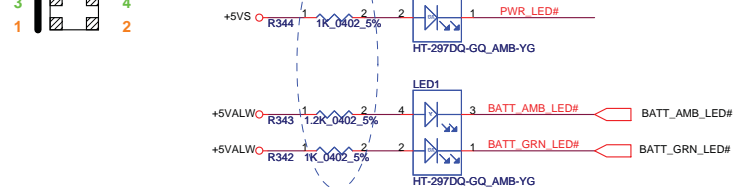
	KSO0
KSI1	WL_BTN#
KSI2	TLOCK_BTN#
KSI3	
KSI4	
KSI5	



FOR EMI



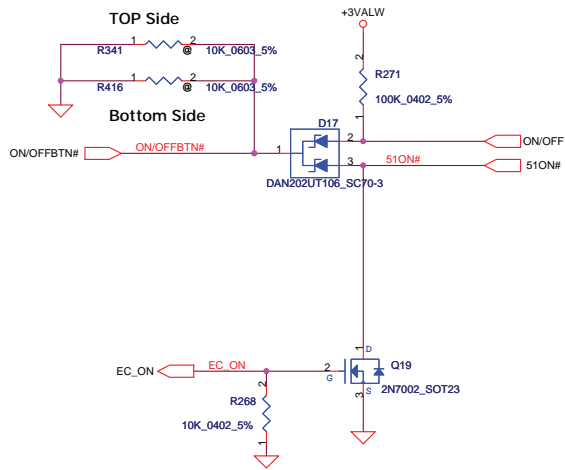
Compal Footprint



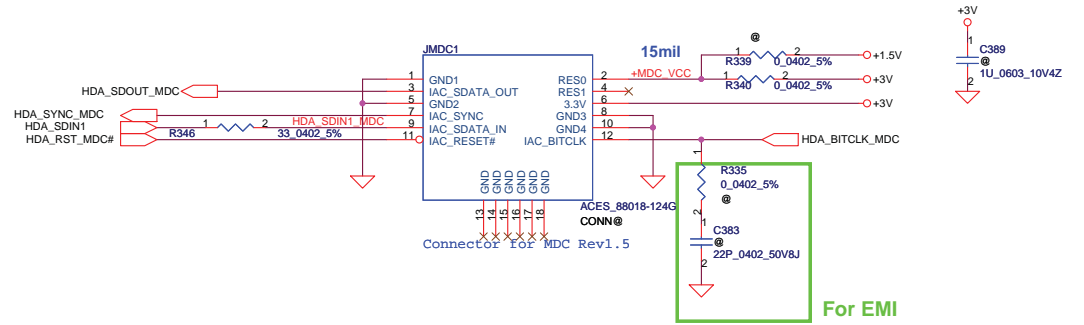
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Power Button

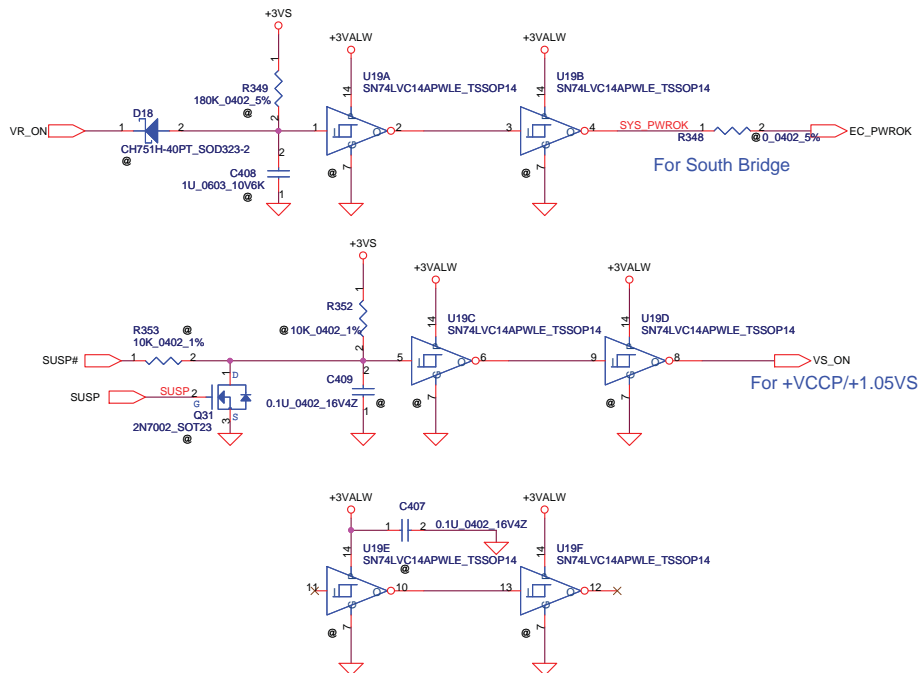
ON/OFF switch



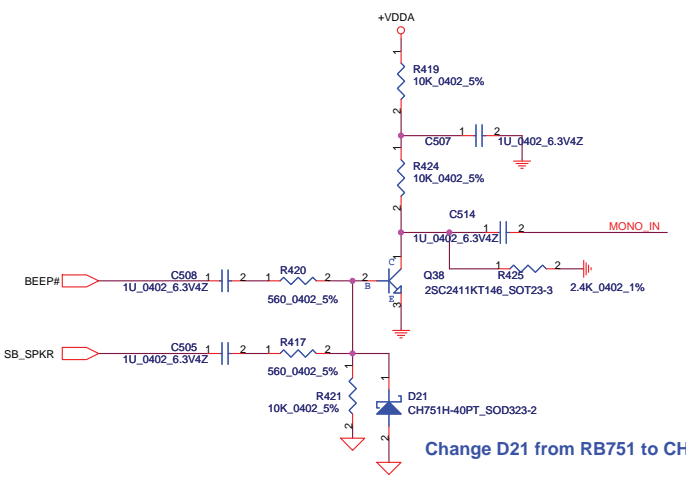
HDA MDC Conn.



Power ON Circuit

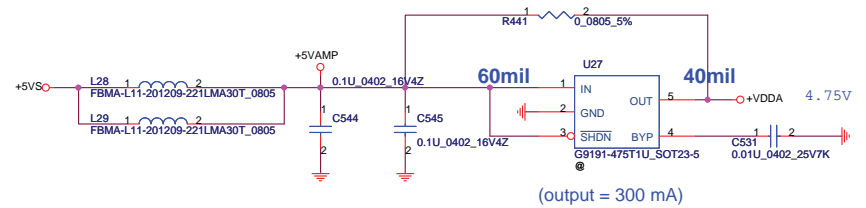


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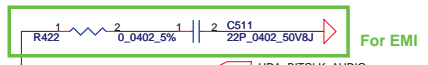
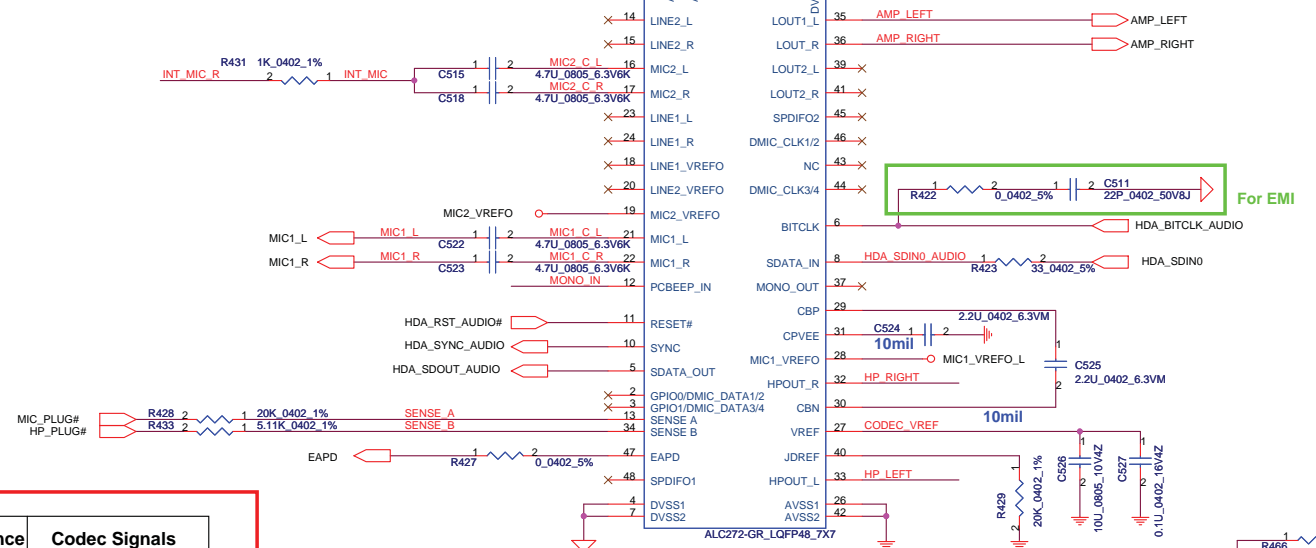
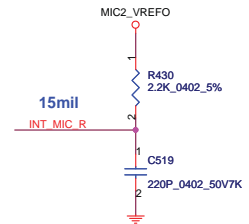
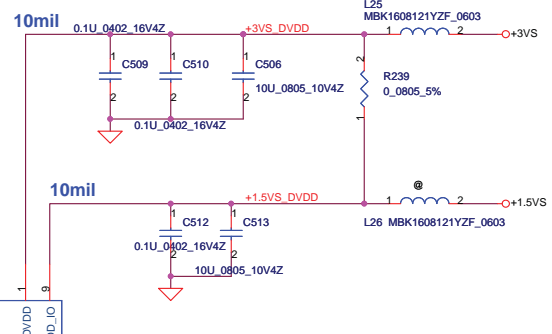
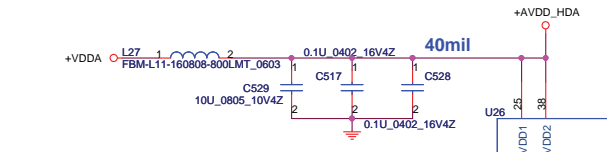


HD Audio Codec

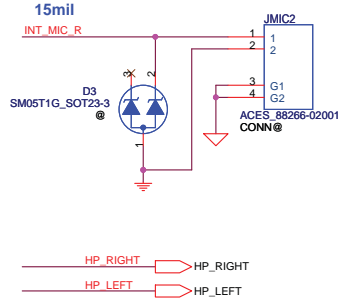
Change D21 from RB751 to CH751



(output = 300 mA)

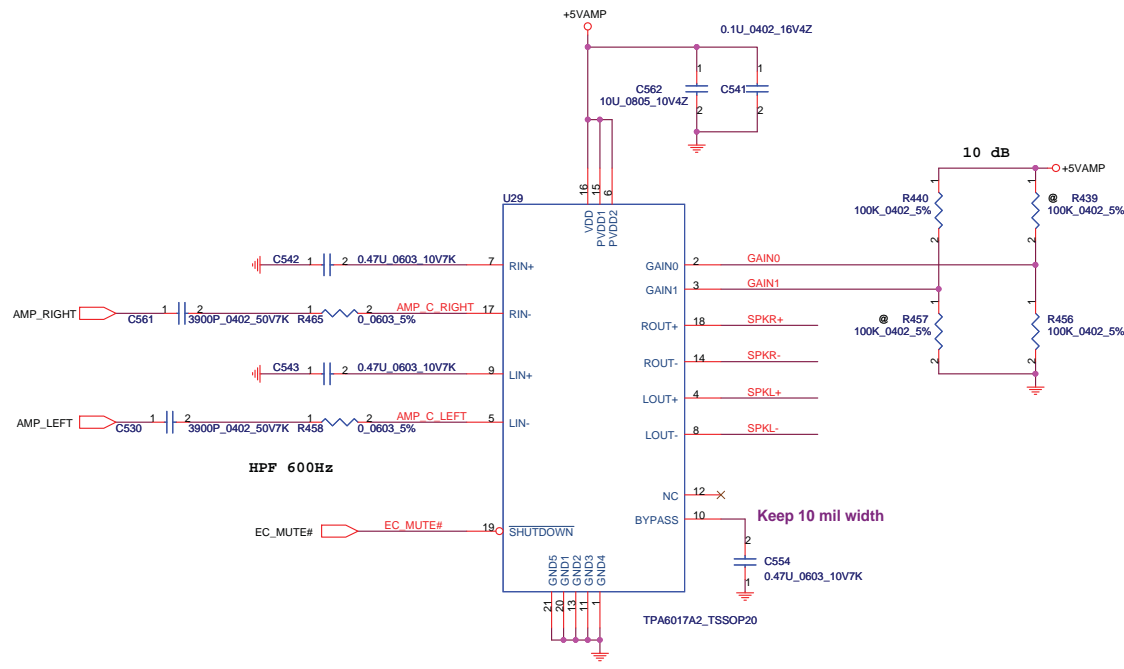


For EMI

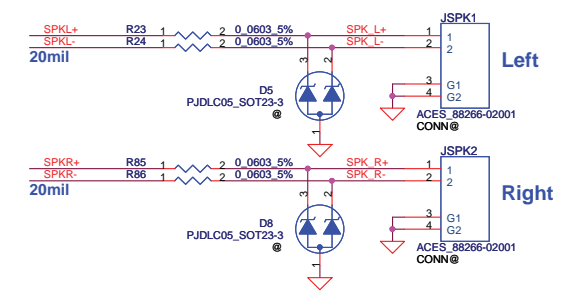


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	
	20K	PORT-B (PIN 21, 22)
	10K	
	5.1K	
SENSE B	39.2K	
	20K	
	10K	
	5.1K	PORT-H (PIN 32,33)

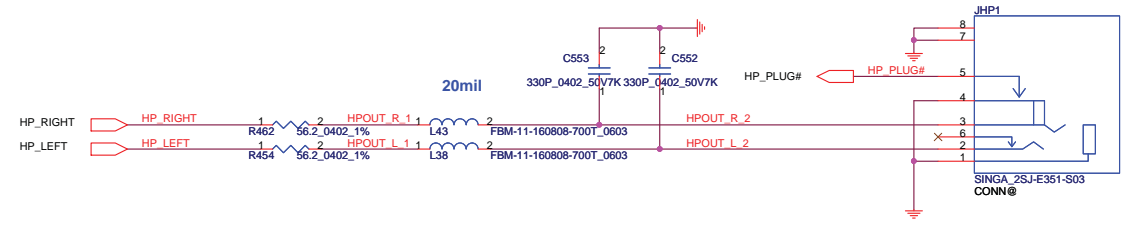
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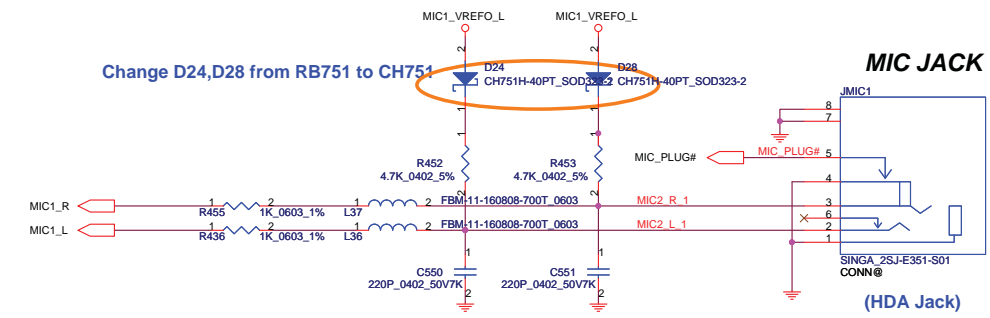
Int. Speaker Conn.



LINE Out/Headphone Out

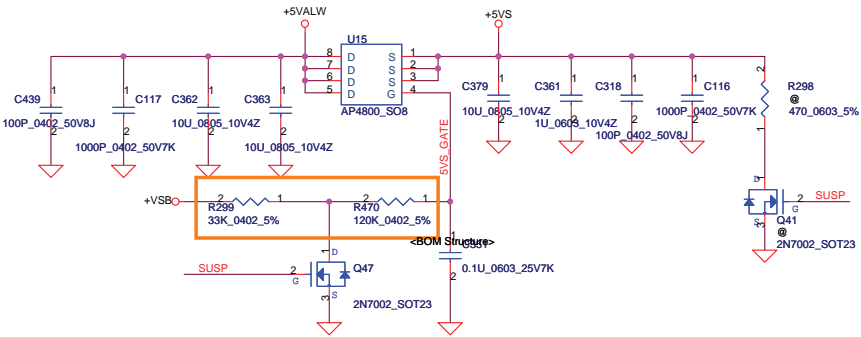


Change D24,D28 from RB751 to CH751

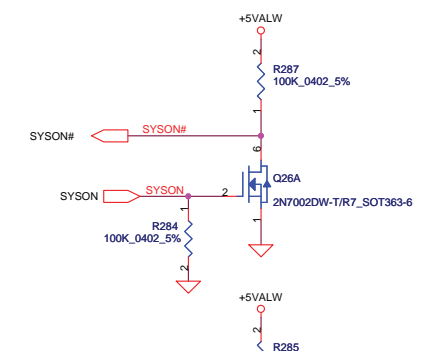
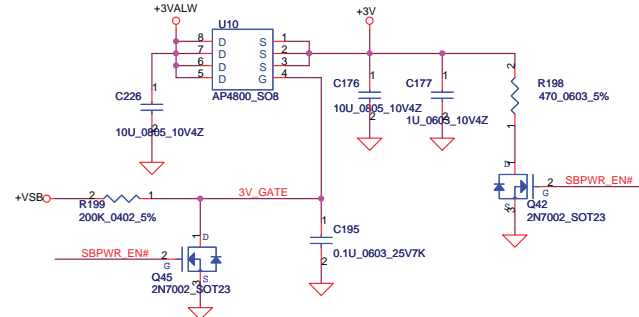


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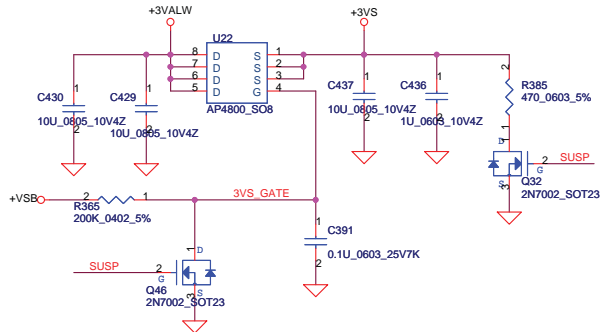
+5VALW TO +5VS



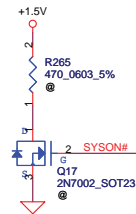
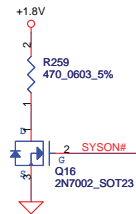
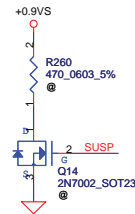
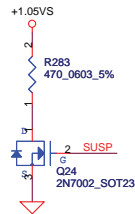
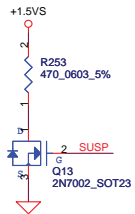
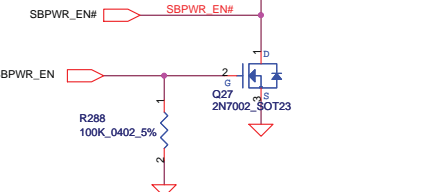
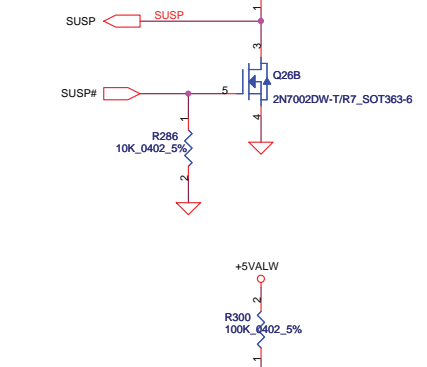
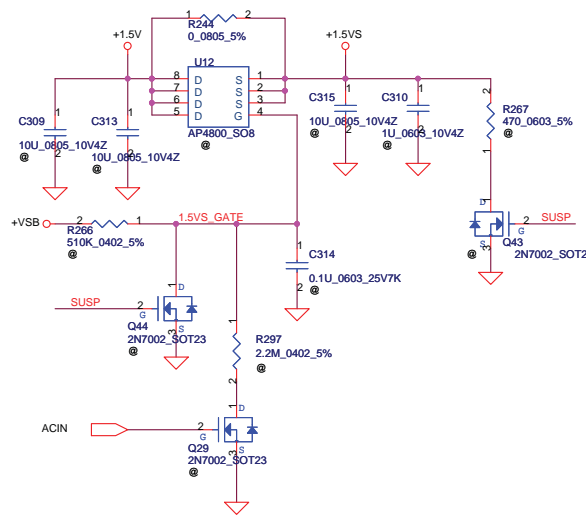
+3VALW TO +3V_SB(ICH8M AUX Power)



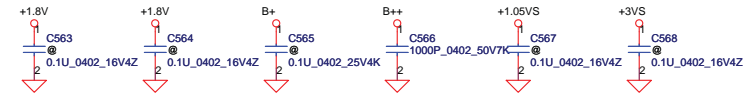
+3VALW TO +3VS



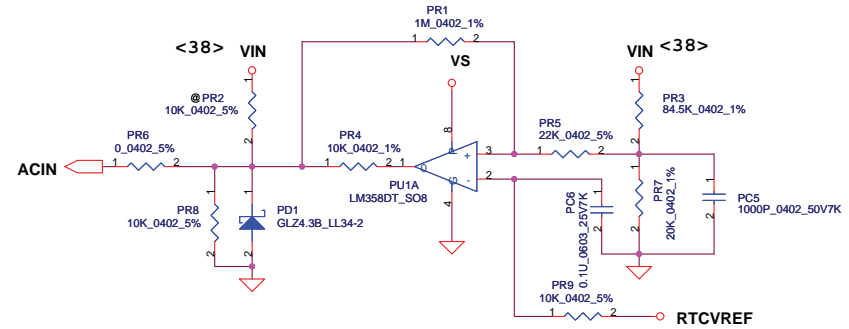
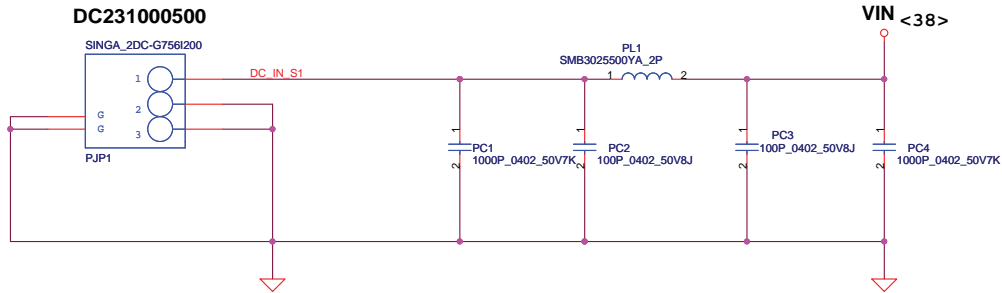
+1.5V to +1.5VS



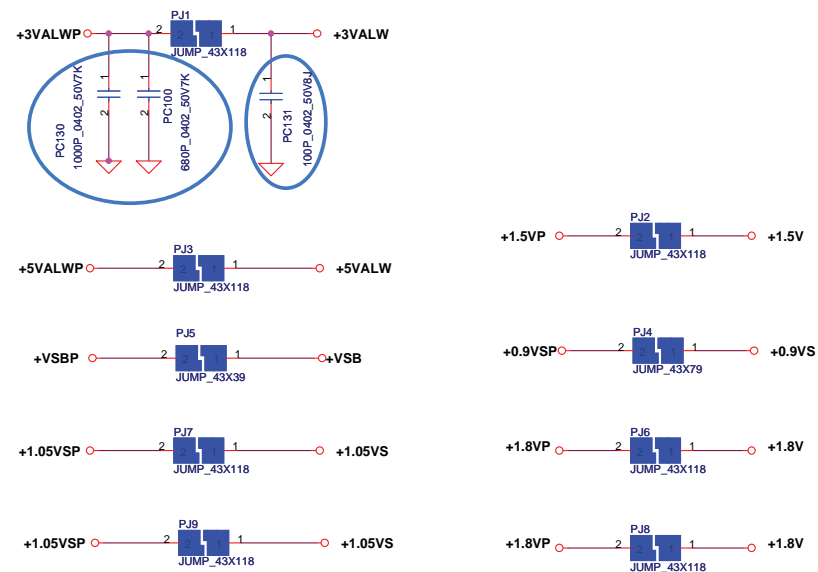
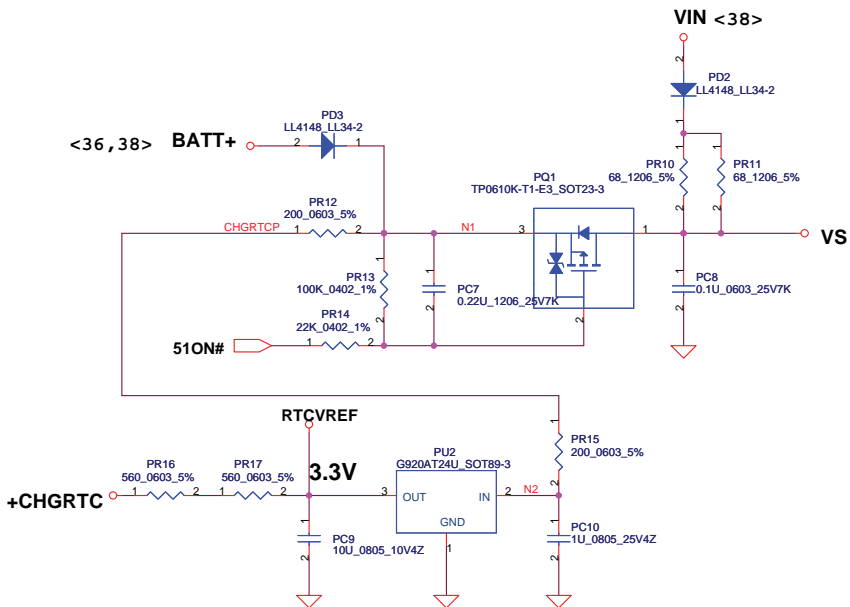
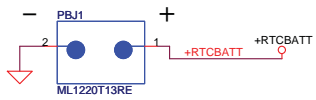
Reserve for EMI request



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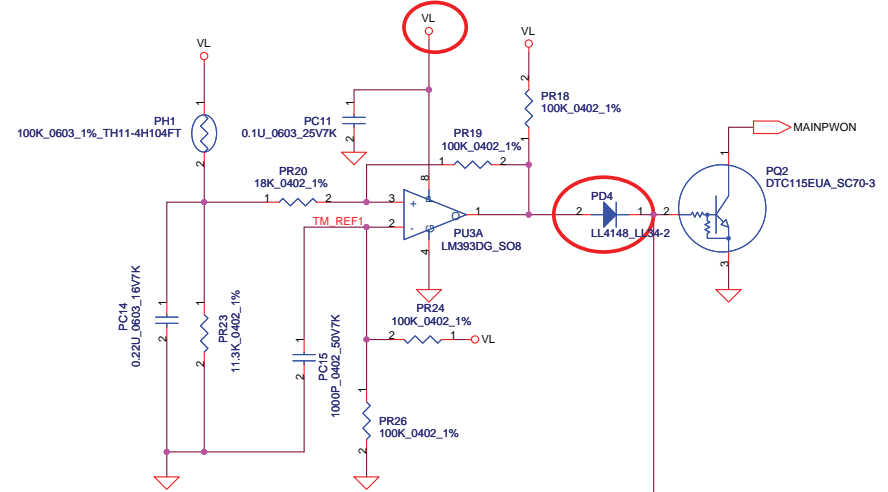
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



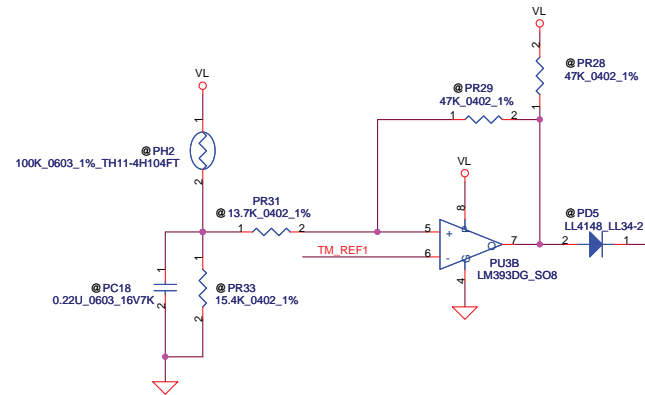
<http://hobi-elektronika.net>

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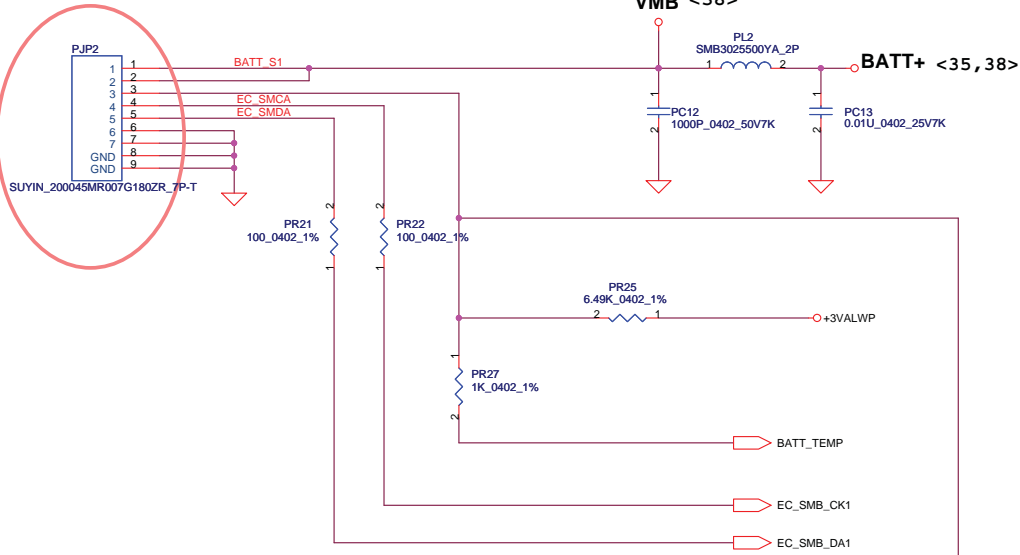
PH1 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 70 degree C



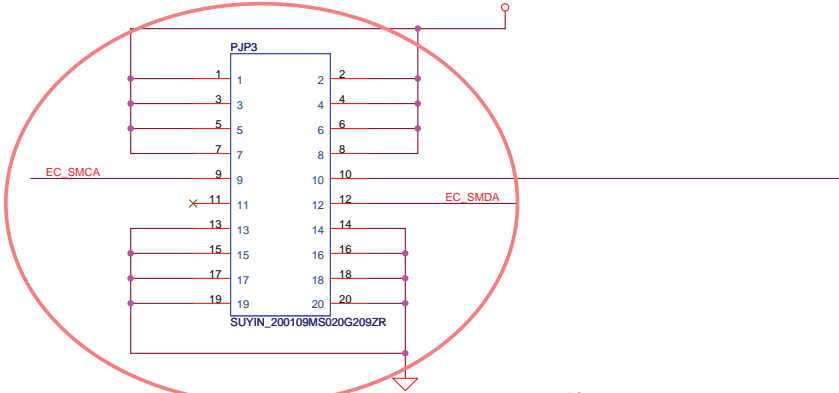
PH2 near main Battery CONN :
 BAT. thermal protection at 90 degree C
 Recovery at 70 degree C



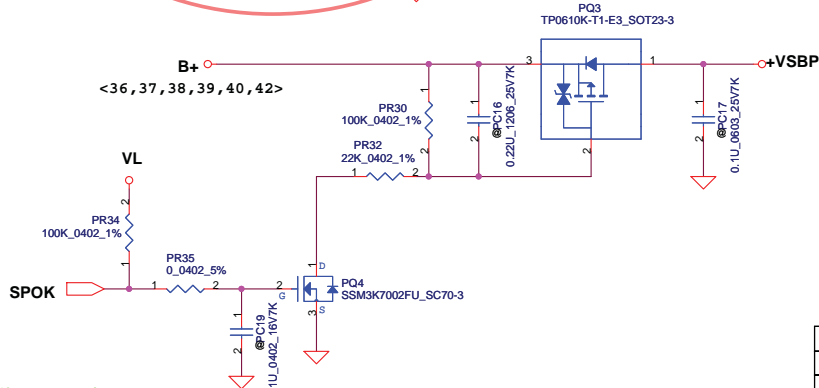
VMB <38>
 BATT+ <35, 38>



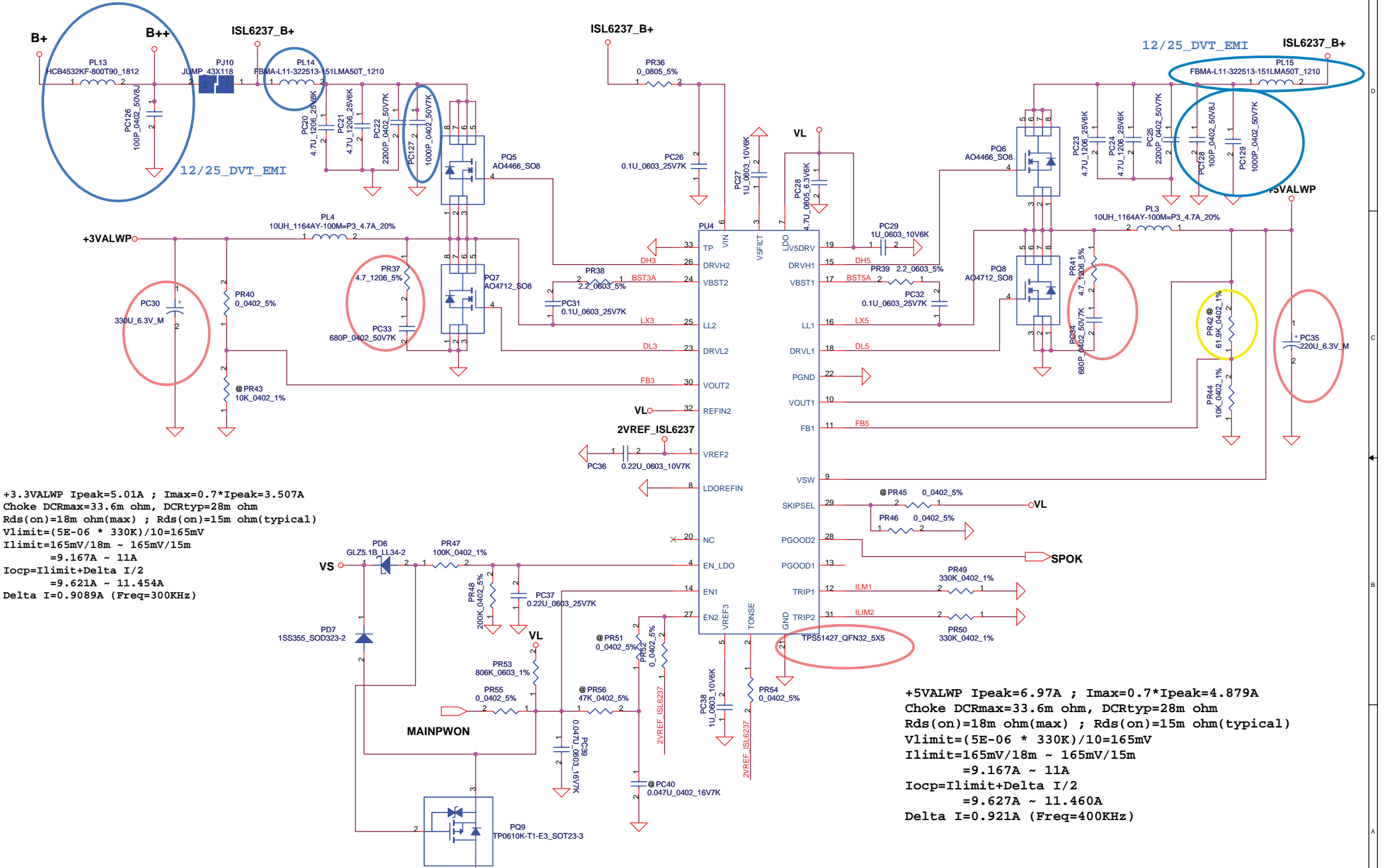
VMB <38>



B+ <36, 37, 38, 39, 40, 42>
 +VSBP



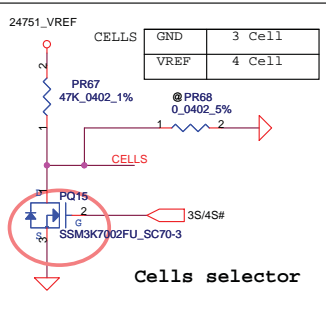
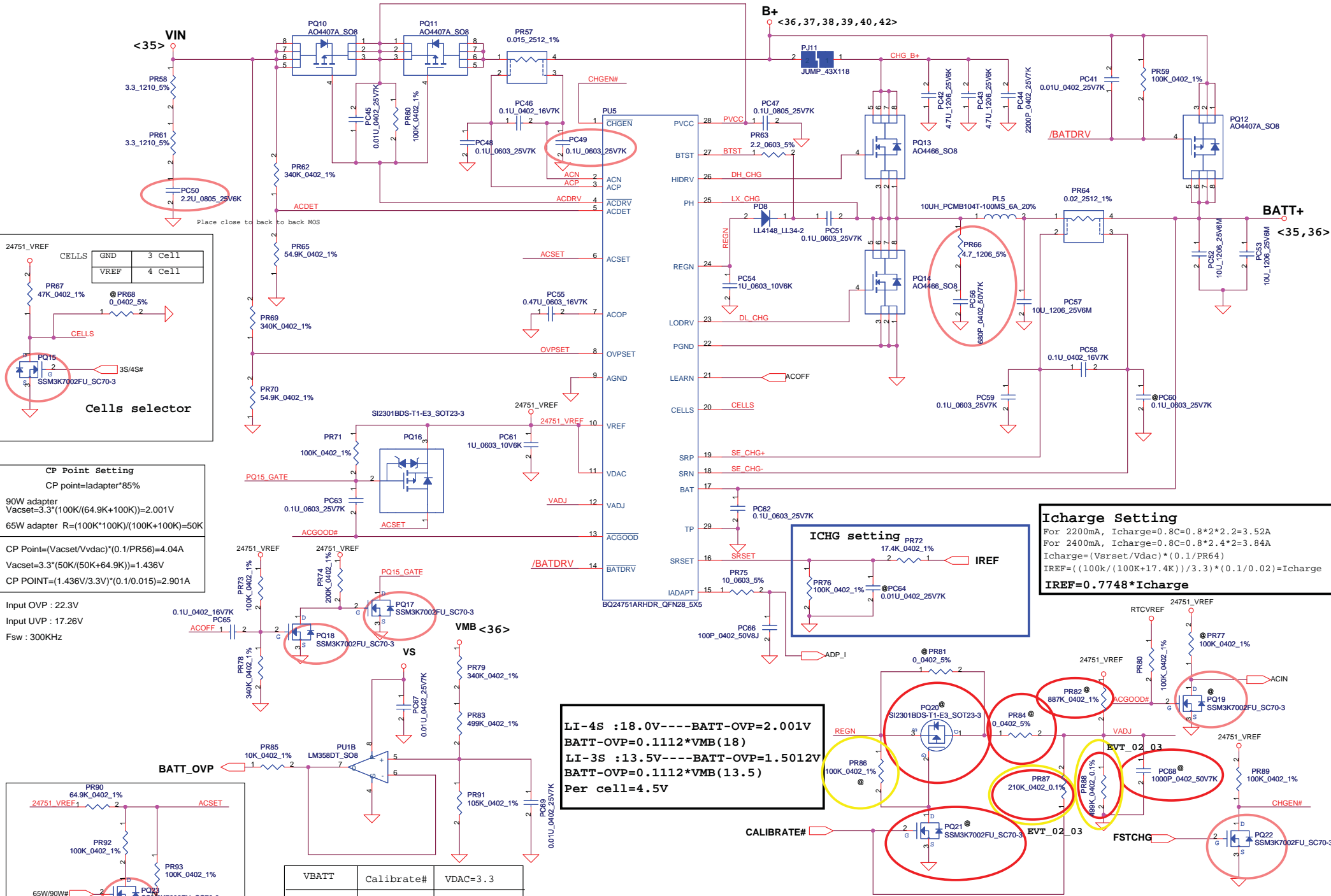
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+3.3VALWP Ipeak=5.01A ; Imax=0.7*Ipeak=3.507A
 Choke DCRmax=33.6m ohm, DCRtyp=28m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =9.621A ~ 11.454A
 Delta I=0.9089A (Freq=300KHz)

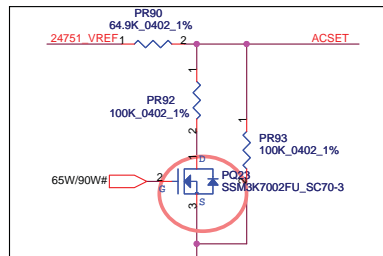
+5VALWP Ipeak=6.97A ; Imax=0.7*Ipeak=4.879A
 Choke DCRmax=33.6m ohm, DCRtyp=28m ohm
 Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
 Vlimit=(5E-06 * 330K)/10=165mV
 Ilimit=165mV/18m ~ 165mV/15m
 =9.167A ~ 11A
 Iocp=Ilimit+Delta I/2
 =9.627A ~ 11.460A
 Delta I=0.921A (Freq=400KHz)

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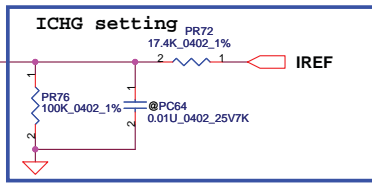
CP Point Setting
 CP point=ladapter*85%
 90W adapter
 $V_{acset}=3.3 \cdot (100K / (64.9K + 100K)) = 2.001V$
 65W adapter $R = (100K \cdot 100K) / (100K + 100K) = 50K$
 $CP\ Point = (V_{acset} / V_{dacc}) \cdot (0.1 / PR56) = 4.04A$
 $V_{acset} = 3.3 \cdot (50K / (50K + 64.9K)) = 1.436V$
 $CP\ POINT = (1.436V / 3.3V) \cdot (0.1 / 0.015) = 2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz



VBATT	Calibrate#	VDAC=3.3
4.0V	L=0	
4.2V	1.8755V	
4.3V	2.8132V	
4.35V	H=3.3	

LI-4S : 18.0V---BATT-OVP=2.001V
BATT-OVP=0.1112*VMB(18)
LI-3S : 13.5V---BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB(13.5)
Per cell=4.5V



Icharge Setting
 For 2200mA, $I_{charge} = 0.8C = 0.8 \cdot 2.2 = 3.52A$
 For 2400mA, $I_{charge} = 0.8C = 0.8 \cdot 2.4 = 3.84A$
 $I_{charge} = (V_{srset} / V_{dacc}) \cdot (0.1 / PR64)$
 $IREF = ((100k / (100k + 17.4k)) / 3.3) \cdot (0.1 / 0.02) = I_{charge}$
IREF=0.7748*Icharge

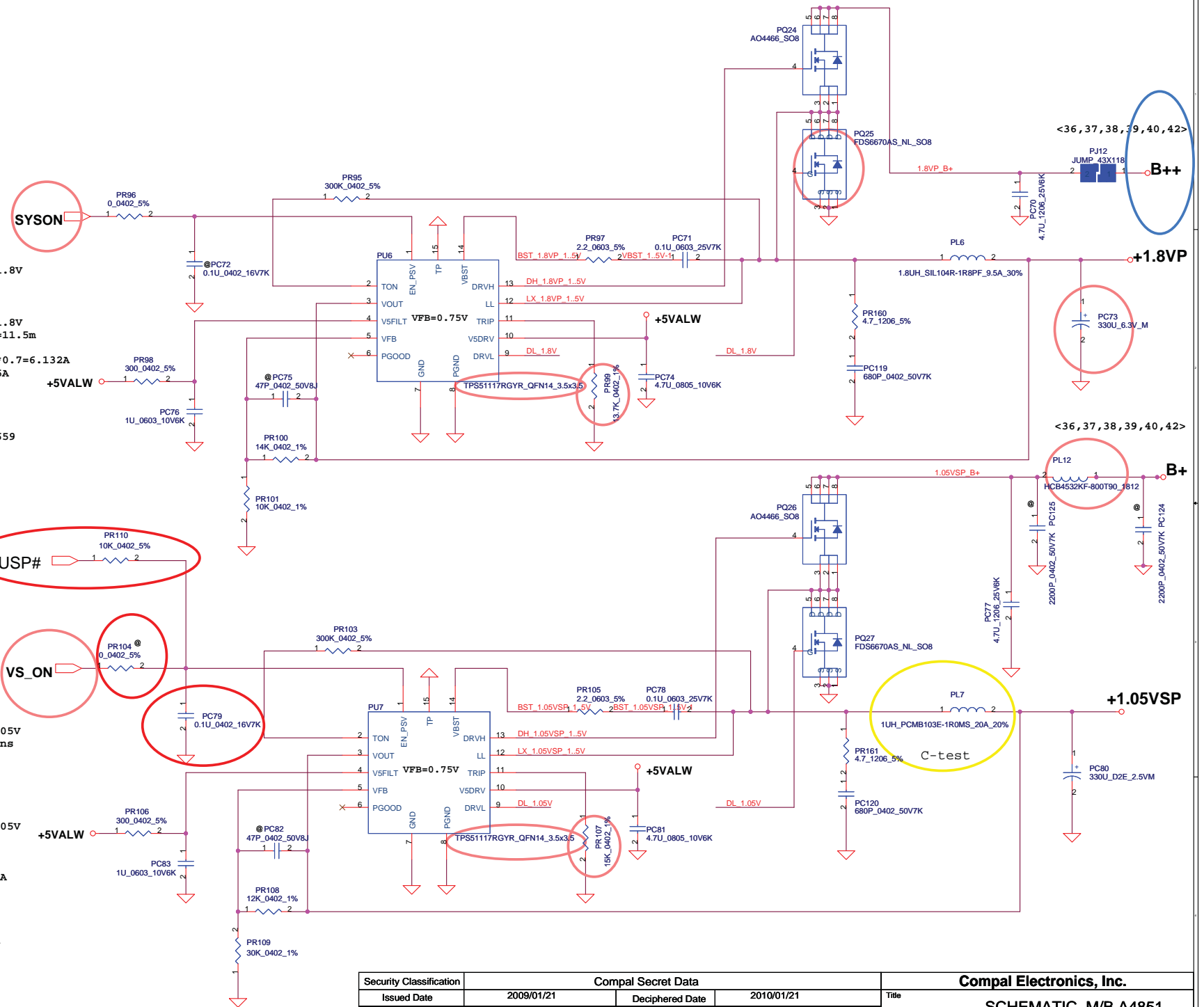
VFB=0.75V
 $V_o = VFB * (1 + PR100 / PR101) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $F_{sw} = 262KHz$ (by Calculation Tool)

<V_o=1.8V> VFB=0.75V
 $V_o = VFB * (1 + PR100 / PR101) = 0.75 * (1 + 14K / 10K) = 1.8V$
 $F_{sw} = 262KHz$ C_{out} ESR=15m ohm R_{dson}(max)=11.5m
 R_{dson}(min)=9m
 I_{peak}=8.76A (by power budget), I_{max}=I_{peak}*0.7=6.132A
 $\Delta I = ((19-1.8) * (1.8/19)) / (L * F_{sw}) = 3.455A$
 $\Rightarrow 1/2 \Delta I = 1.7275A$
 $V_{trip} = R_{trip} * I_{0uA} = 13.7K * 10uA = 0.137V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.3 + 1.7275 = 10.8914A$
 $I_{ocpmax} = (0.137 / (0.009 * 1.1)) + 1.7275A = 15.5659$
 $I_{ocp} = 10.8914 - 15.5659A$

note: Reference AO4712&TPS51117 spec

VFB=0.75V
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$
 $T_{on} = 19 * e^{-12 * 143000} * ((2/3) * V_o + 100mV / 19) + 50ns$
 $= 2.645e-7$ us
 $\Rightarrow V_o / V_{in} = D = T_{on} / T_s \Rightarrow T_s = 3.35us$
 $F_{sw} = 261KHz$ (by calculation tool)

<V_o=1.05V> VFB=0.75V
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$
 $F_{sw} = 261KHz$ C_{out} ESR=15m ohm
 R_{dson}(max.)=11.5m R_{dson}(min)=9m
 I_{peak}=9A, I_{max}=I_{peak}*0.7=6.3A
 $\Delta I = ((19-1.05) * (1.05/19)) / (L * F_{sw}) = 2.11A$
 $\Rightarrow 1/2 \Delta I = 1.055A$
 $V_{trip} = R_{trip} * I_{0uA} = 15K * 10uA = 0.15V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.3 + 1.055 = 11.0892A$
 $I_{ocpmax} = (0.15 / (0.009 * 1.1)) + 1.055A = 16.2073A$
 $I_{ocp} = 11.0892A - 16.2073A$

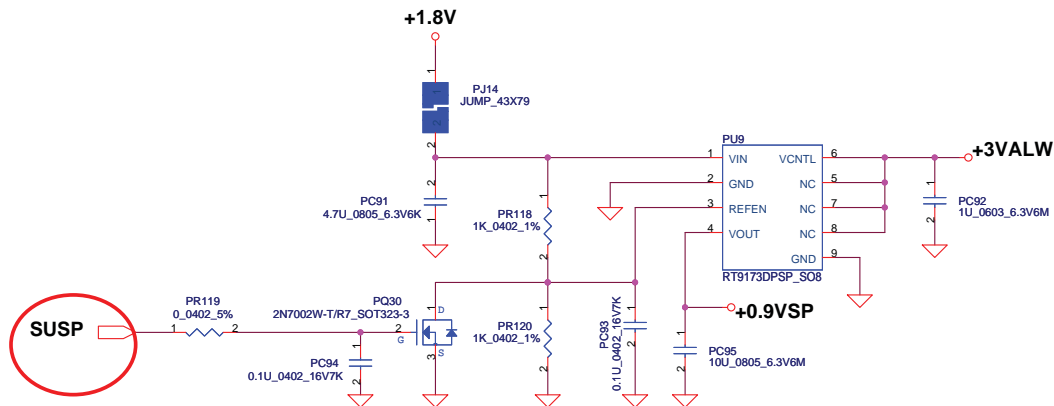
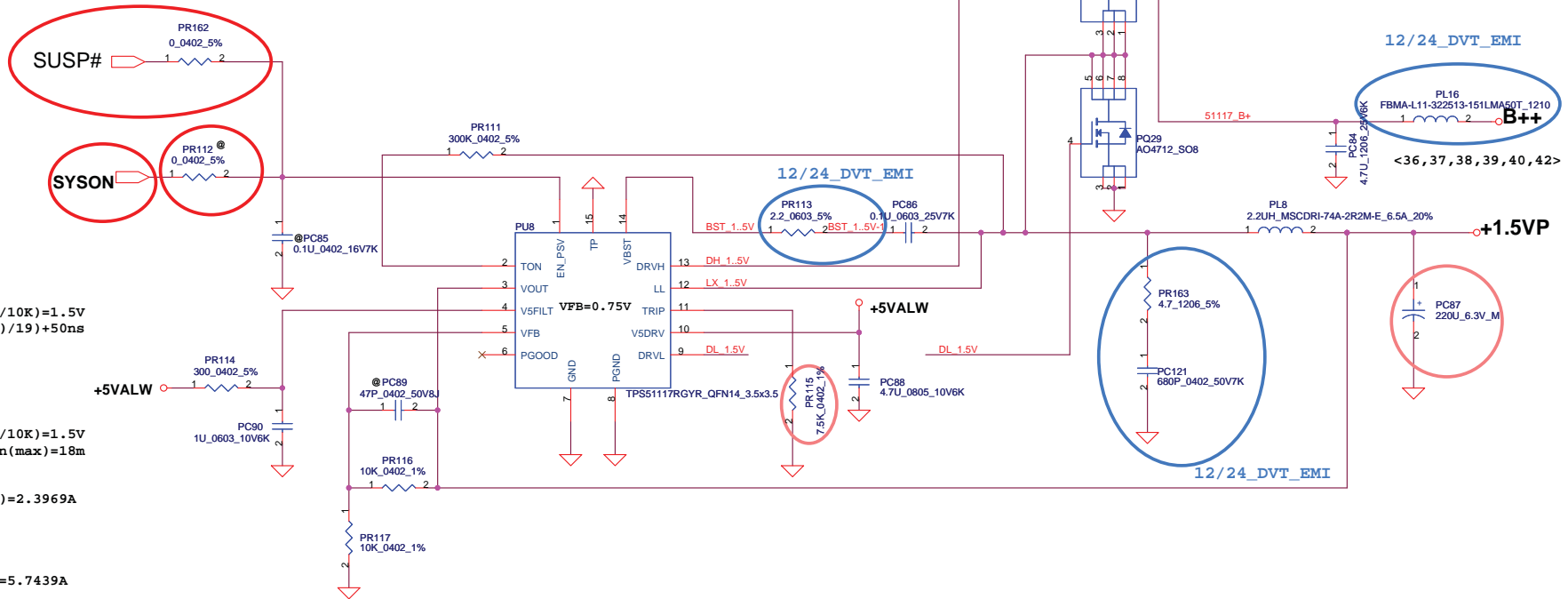


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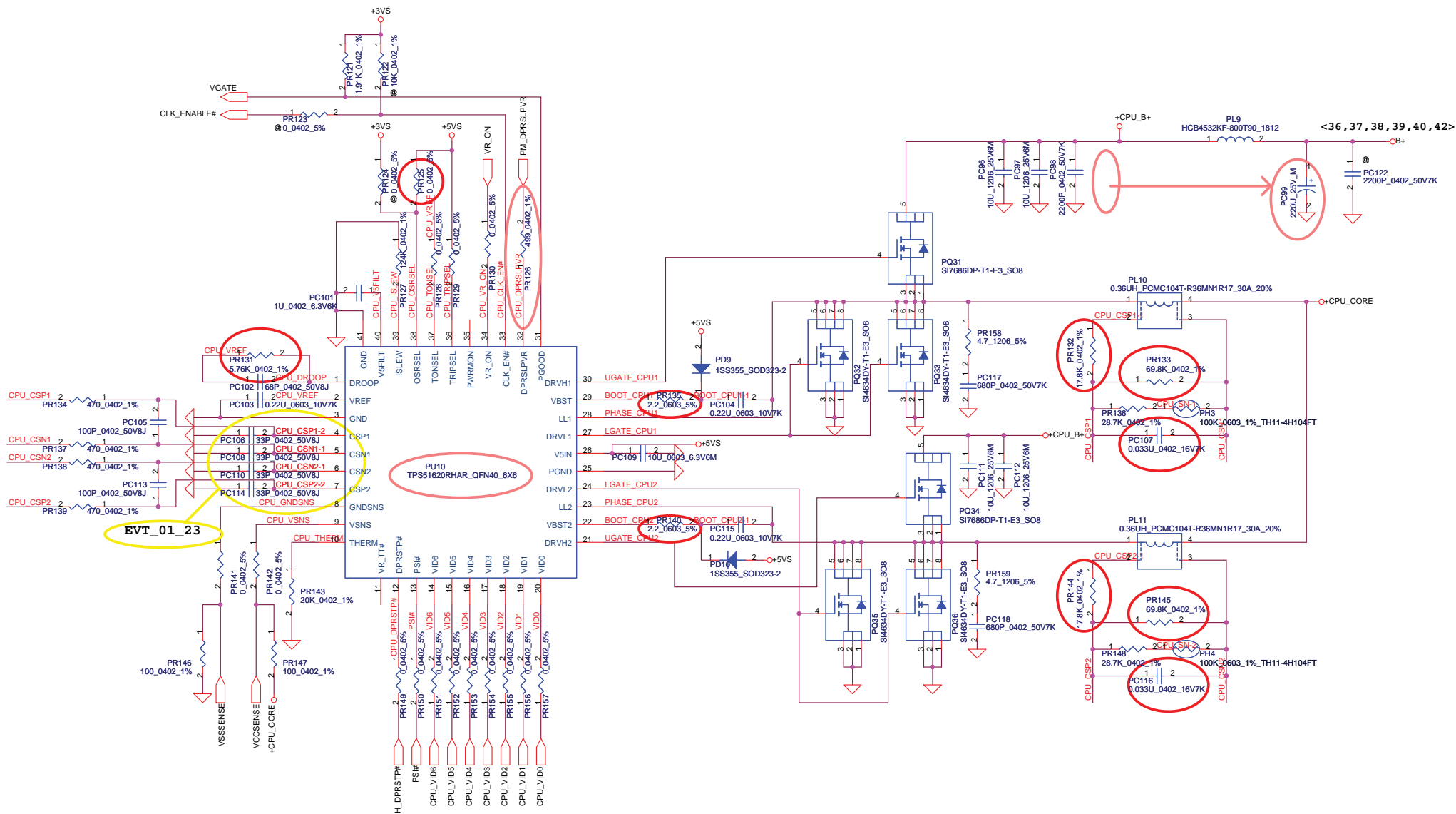
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$V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR116/PR117)=0.75 \cdot (1+10K/10K)=1.5V$
 $Ton=19 \cdot e^{-12 \cdot 143000 \cdot ((2/3) \cdot V_o + 100mV) / 19} + 50ns$
 $= 2.645e-7 \text{ us}$
 $\Rightarrow V_o/V_{in}=D=Ton/Ts \Rightarrow Ts=3.35us$
 $Fsw=262KHz$

$<V_o=1.5V> \quad V_{FB}=0.75V$
 $V_o=V_{FB} \cdot (1+PR116/PR117)=0.75 \cdot (1+10K/10K)=1.5V$
 $Fsw=262KHz \quad C_{out} ESR=15m \text{ ohm} \quad R_{dson(max)}=18m$
 $R_{dson(min)}=15m$
 $I_{peak}=3.51A, \quad I_{max}=2.457A$
 $\Delta I = ((19-1.5) \cdot (1.5/19)) / (L \cdot Fsw) = 2.3969A$
 $\Rightarrow 1/2 \Delta I = 1.198A$
 $V_{trip} = R_{trip} \cdot I_{peak} = 7.5K \cdot 10uA = 0.075V$
 $I_{ocpmin} = V_{trip} / R_{dsonmax} \cdot 1.2 + 1.198$
 $= 0.075 / (0.018 \cdot 1.3) + 1.198 = 4.4035A$
 $I_{ocpmax} = (0.075 / (0.015 \cdot 1.1)) + 1.198A = 5.7439A$
 $I_{ocp} = 4.4035A - 5.7439A$



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1% +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%	0.2	38 39 40	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1% +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K +1.5VP PR112: Reserve(@) 0_0402_5%	20081124	DVT
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35 40	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT
20	POWER Solution	+3VALWP/+5VALWP RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT

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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 (HCB4532KF-800T90_1812) Add PL 14 (FBMA-L11-322513-151LMA50T_1210) Add PL 15 (FBMA-L11-322513-151LMA50T_1210) Add PC126 (100P_0402_50V8J) Add PC128 (100P_0402_50V8J) Add PC129 (1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 (100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT

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11/11

1. Page 17;Un-POP R412,Q35
2. Page 32;Un-POP R340,POP R339
3. Page 32;Un-POP D3
4. Change C13,C269,C282,C482 P/N to SGA1933D10 (ESR From 15 to 9 ohm)
5. DEL HDMI Schematic (del HDMI@/NHDMI@)

11/19

1. Change C538,C539 to B size 150U
2. POP D11,D12,D29 and change P/N to SCA00000A00

11/24

- 1.Add LAN_CLKREQ# on CLK Gen and AR8132

11/25

- 1.Add C563~C568 for EMI request
- 2.Add L44 for EMI request
- 3.Add +3VS and +3V for SB HDA bus
- 4.Add 0 ohm resistor for Audio DVDD_IO bus
- 5.Add 0 ohm between +1.5V and +1.5VS
- 6.Add 3VS_GATE schematic on +3VALW to +3VS
- 7.remove c318 and D16
- 8.add R400 and C439 for soft-off
- 9.add R244 to connect +1.5v to +1.5vs

11/25

1. Change R325,R311 Form 11ohm to 22 ohm
2. Change D21,D24,D28 from RB751 to CH751
3. Reserve C485,C282

12/18

1. Change R299 to 47K,ADD R470 (100K)

1/20

1. Change R299 to 22K and R470 to 120K
2. Add R570 (150U) in pgae 23
- 3.change board ID R273 to 33K

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