

# Compal Confidential

## HCW51 Schematics Document

AMD/Sempron/ATI RS485MC/SB460

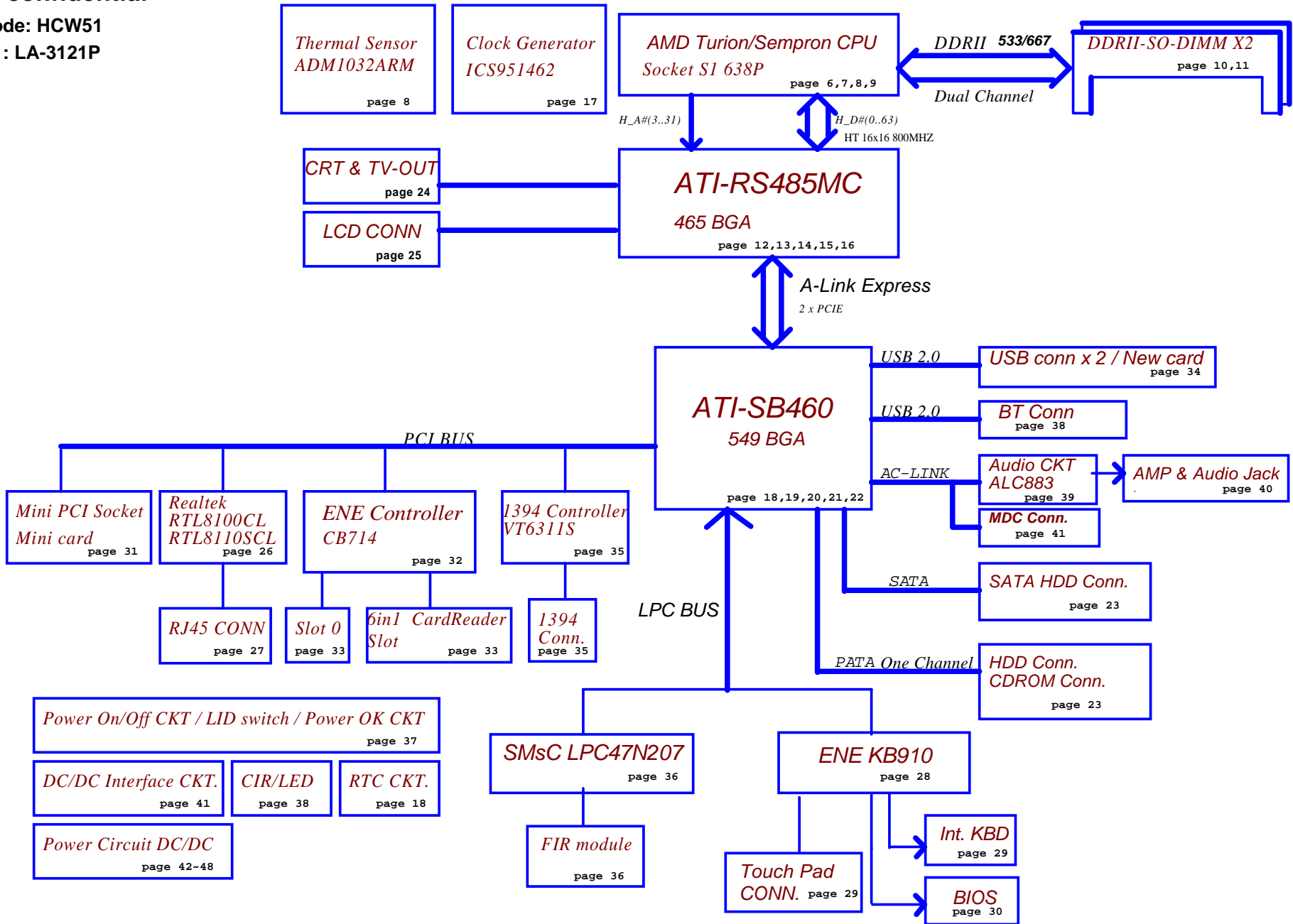
2006 / 04 / 27      Rev:1.0      FOR MP

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Project Code: HCW51

File Name : LA-3121P



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.2VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQE/PIRQH
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		
(24C04)	1011 000X b		

## SB460 SM Bus address

Device	Address
Clock Generator (ICS951462)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	UMA
1	DISCRETE
2	
3	
4	
5	
6	
7	

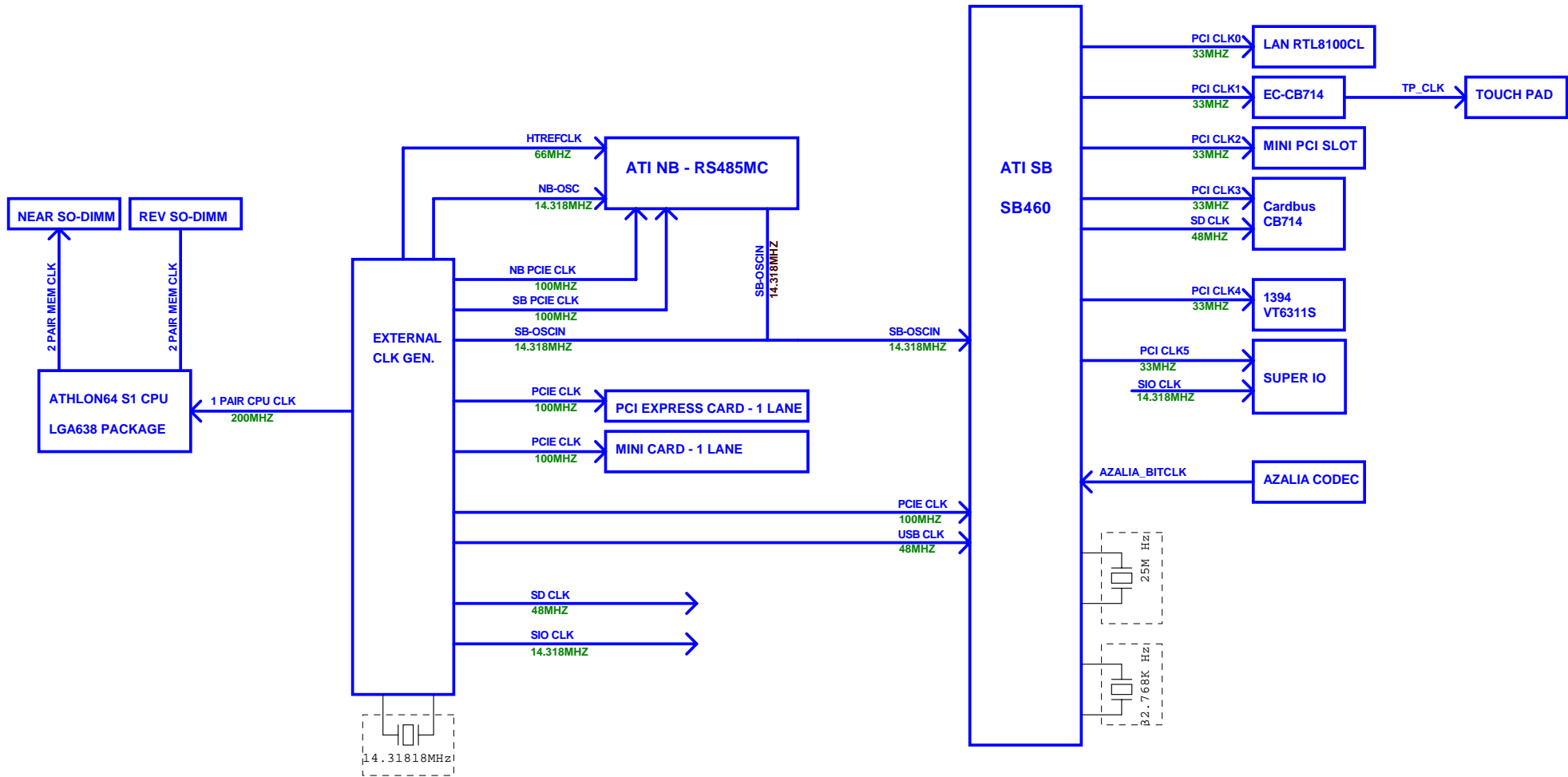
## SKU ID Table

SKU ID	SKU
0	W/O SATA
1	WITH SATA
2	
3	
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
WITH TV-OUT	TV@
WITH FIR	FIR@
WITH CARD READER	61@
WITH 1394	1394@
WITH EXPRESS CARD	EXPRESS@
WITH CIR	CIR@
WITH LAN(10/100)	100@
WITH LAN(10/100/1000)	GIGA@
WITH GIGA LAN(8110SBL)	8110SB@
WITH GIGA LAN(8110SCL)	8110SC@
WITH PATA HDD	PATA@
WITH SATA HDD	SATA@
WITH BLUETOOTH	BT@
WITH USBx2	USB2@
WITH LPC47N207	SIO1@
WITH SIO1036	SIO2@
WITH SIO BOTH	SIOALL@
WITH SSC	SPREAD@
W/O SSC	NOSPREAD@
DIP CAP	45@

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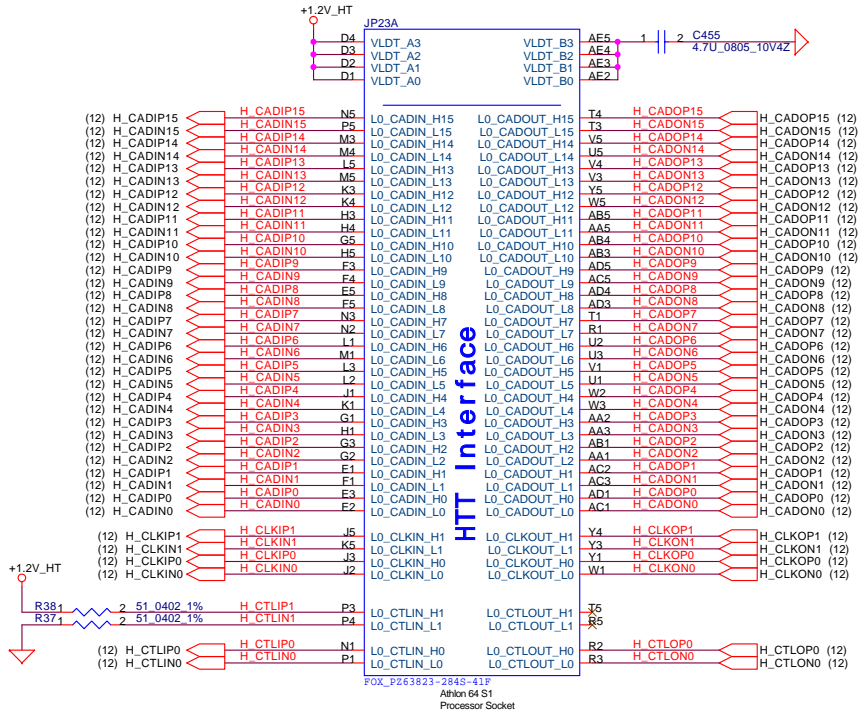
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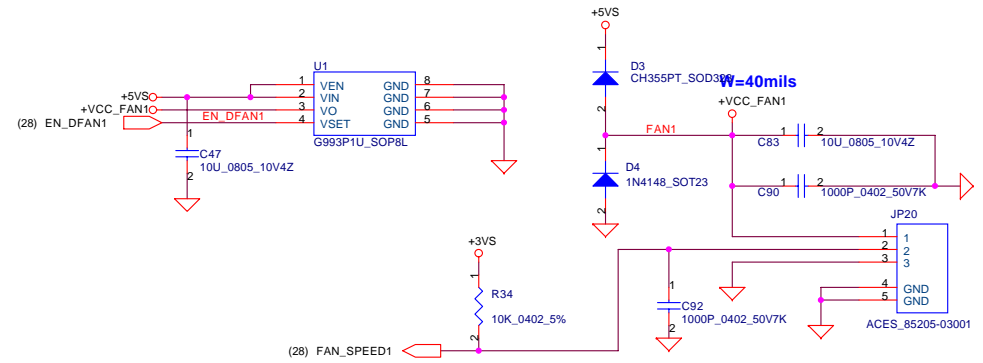
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## PROCESSOR HYPERTRANSPORT INTERFACE

VLDT\_Ax AND VLDT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

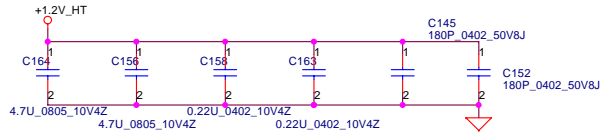


## FAN Conn



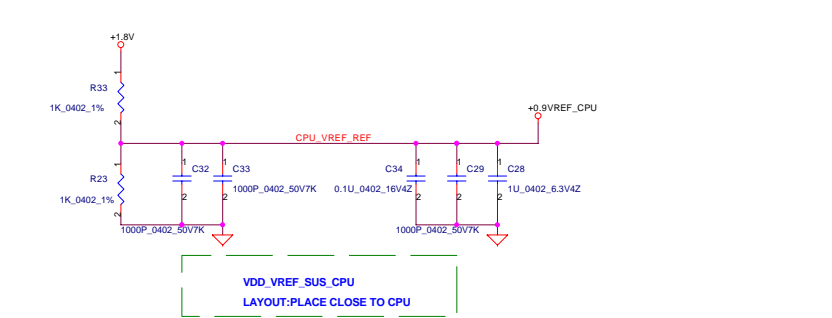
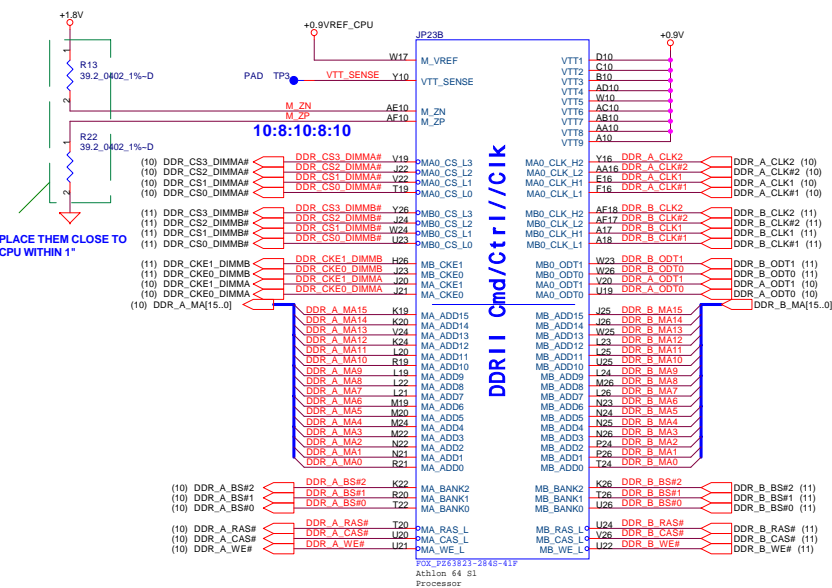
## LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
PLACE CLOSE TO VLDTO POWER PINS

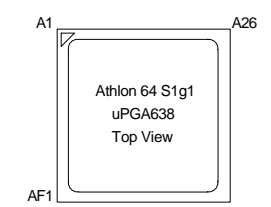
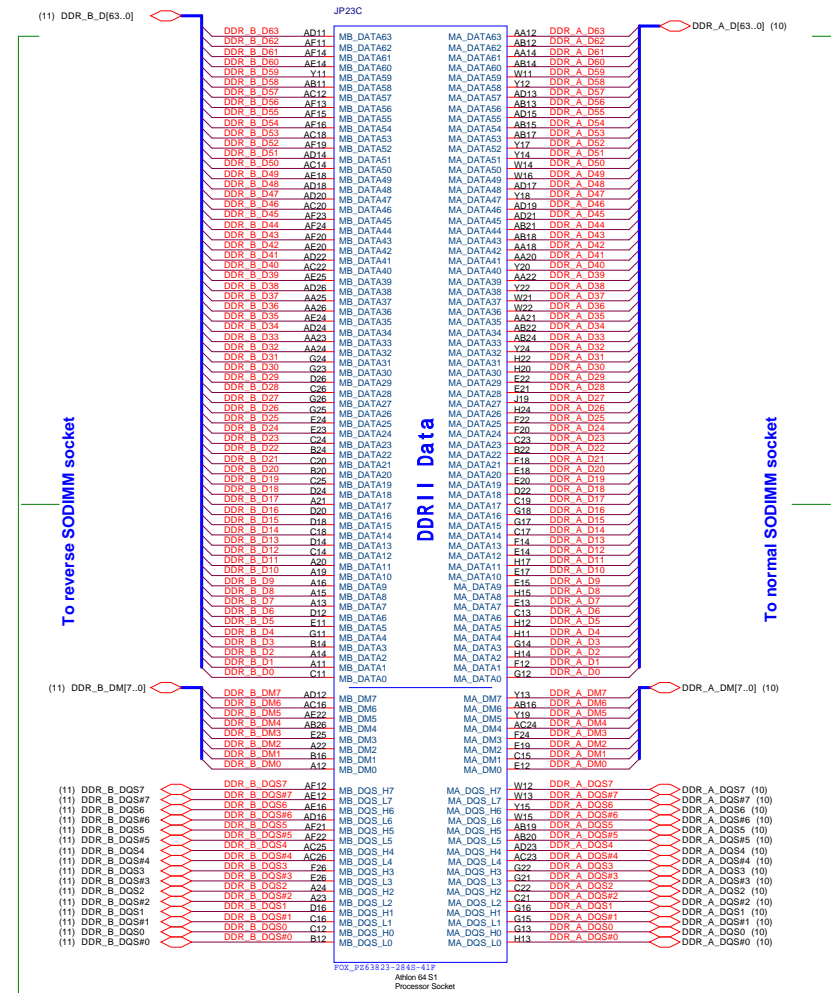


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VDD VTT SUS\_CPU IS CONNECTED TO THE VDD VTT SUS\_POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE.IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE.



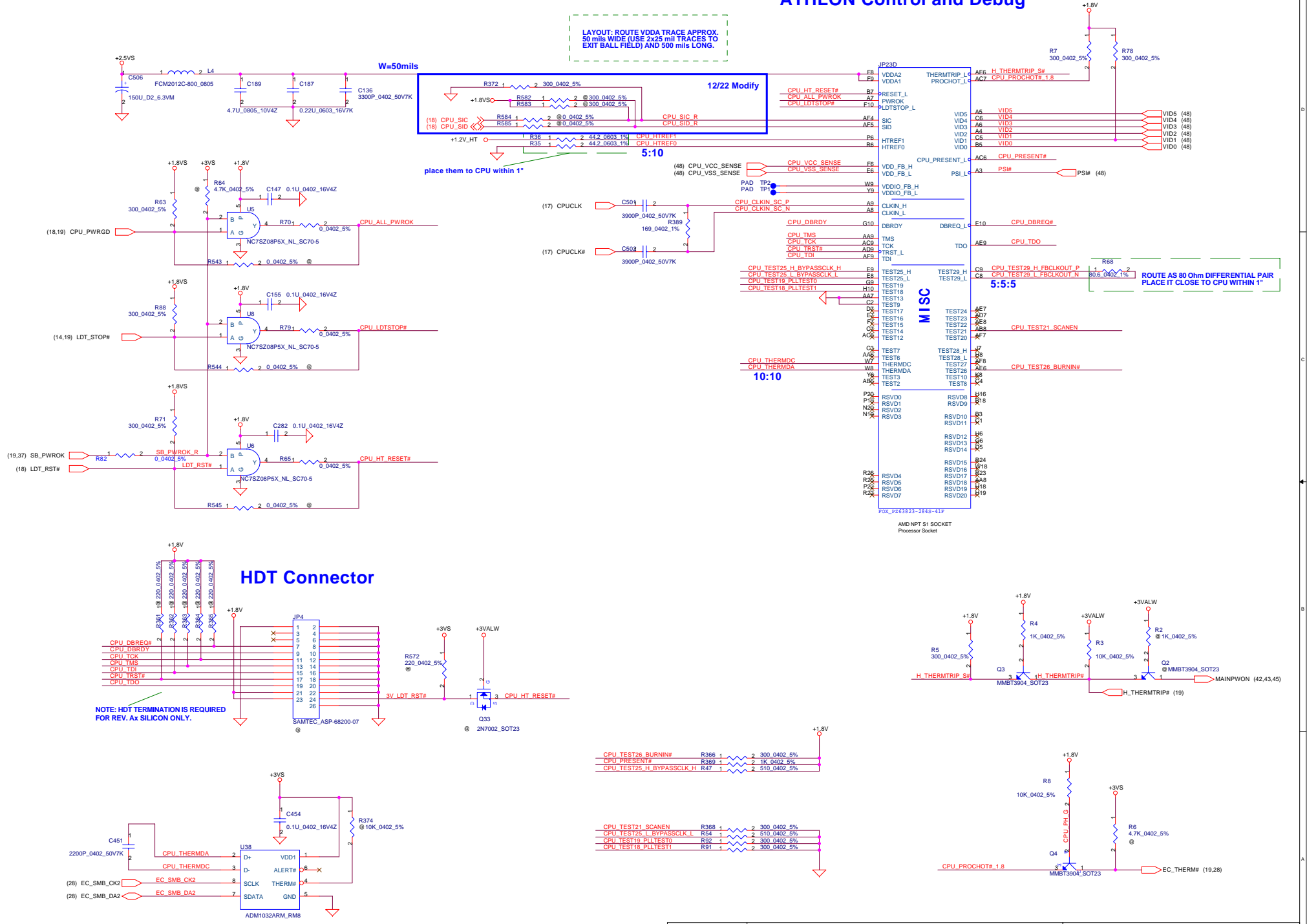
## Processor DDR2 Memory Interface



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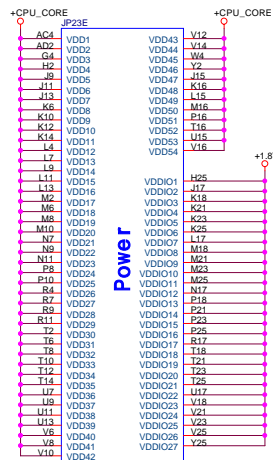
# ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXT BALL FIELD) AND 500 mils LONG.

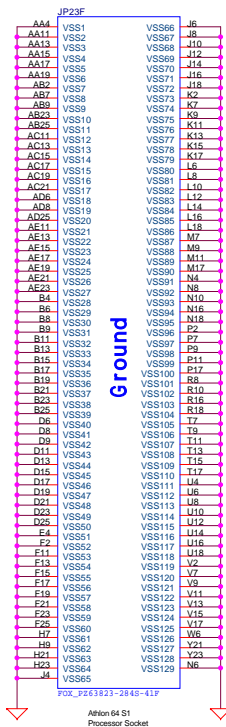


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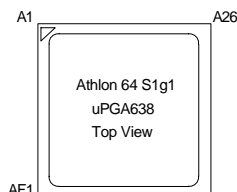


Athlon 64 S1 Processor Socket

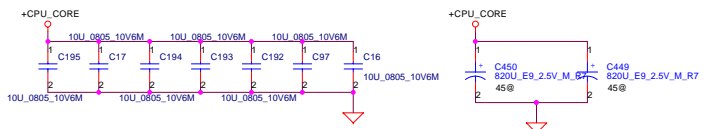
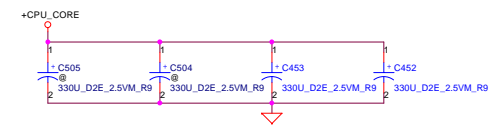


Ground

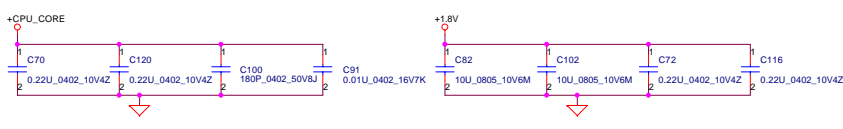
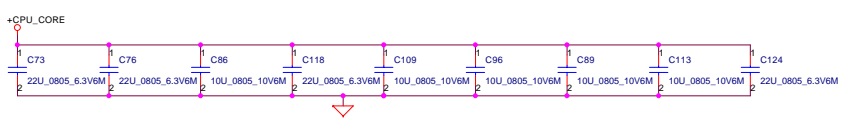
Athlon 64 S1 Processor Socket



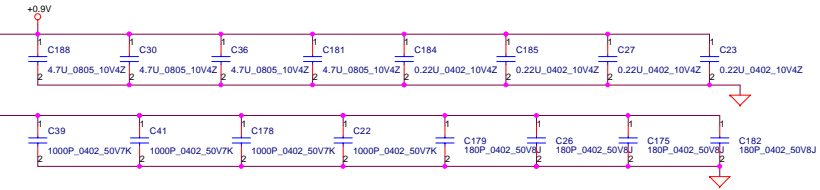
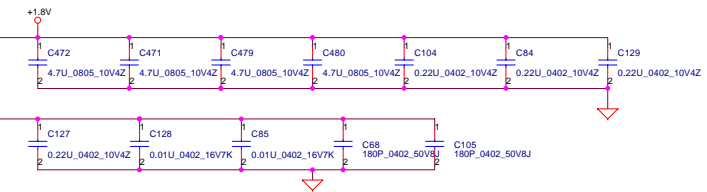
Athlon 64 S1g1 uPGA638 Top View



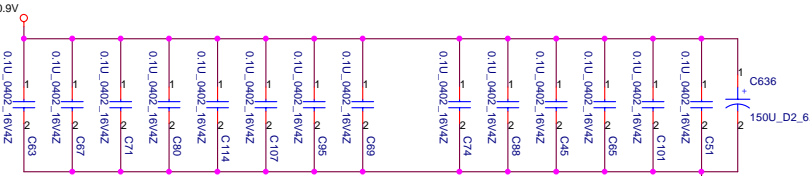
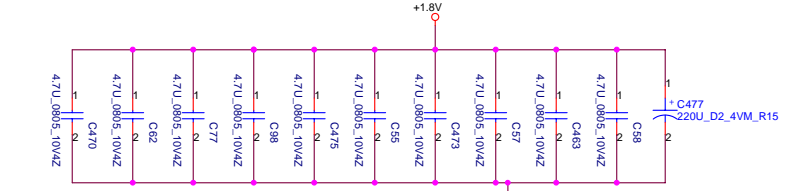
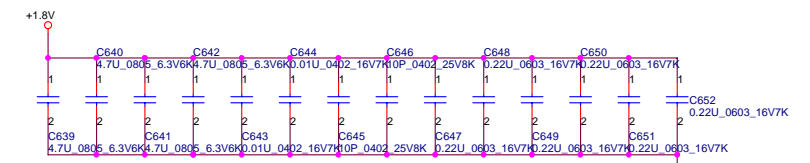
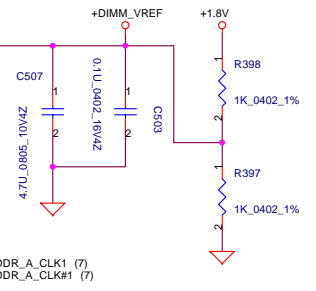
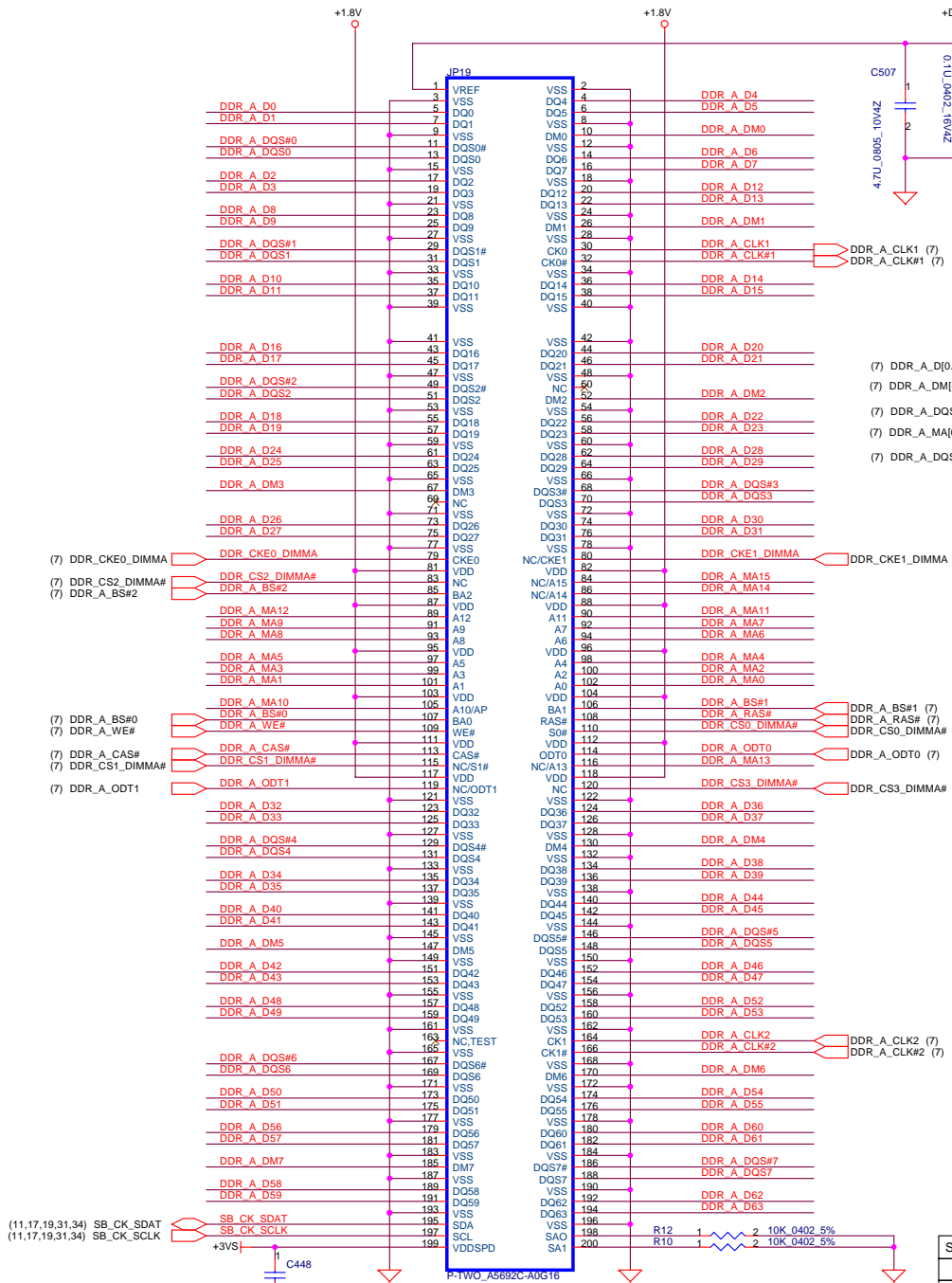
CPU SOCKET S1 DECOUPLING



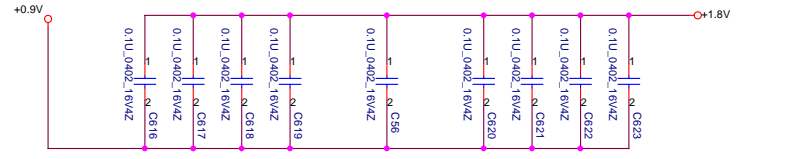
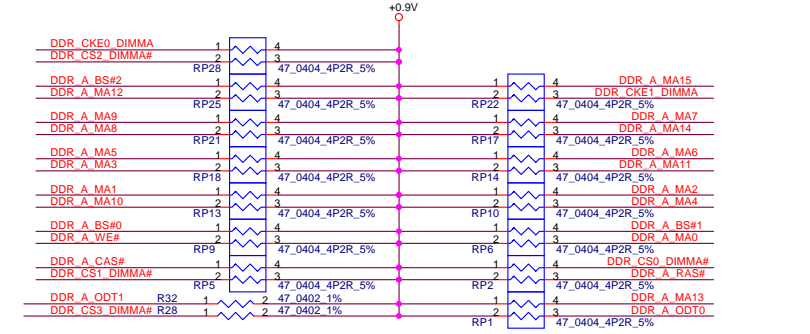
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



PROCESSOR POWER AND GROUND

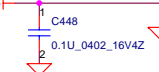


**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



**Layout Note:**  
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

(11,17,19,31,34) SB\_CK\_SDAT  
(11,17,19,31,34) SB\_CK\_SCLK

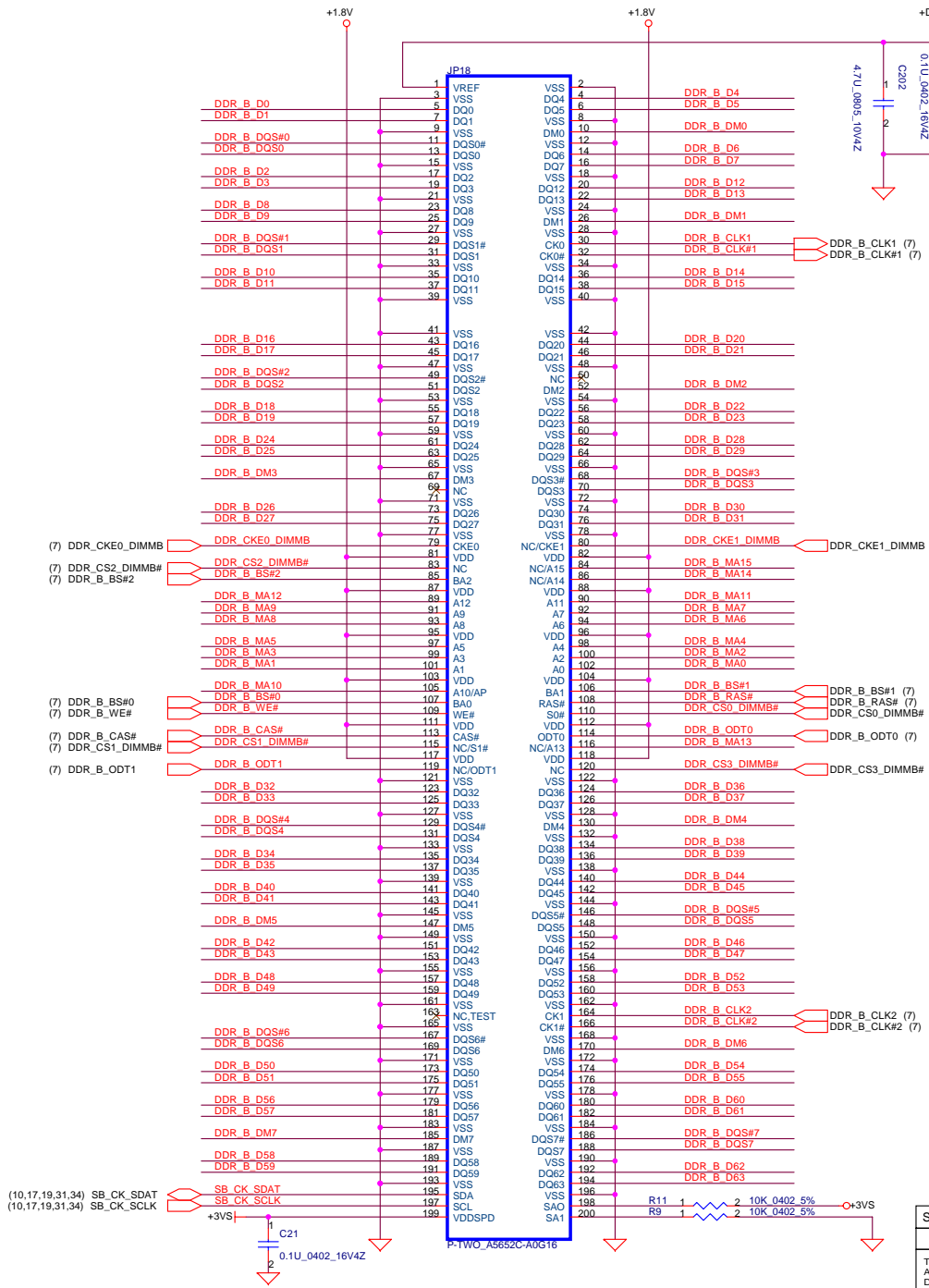


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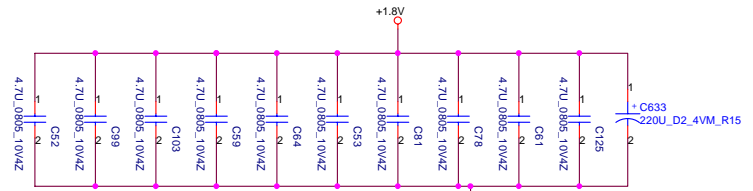
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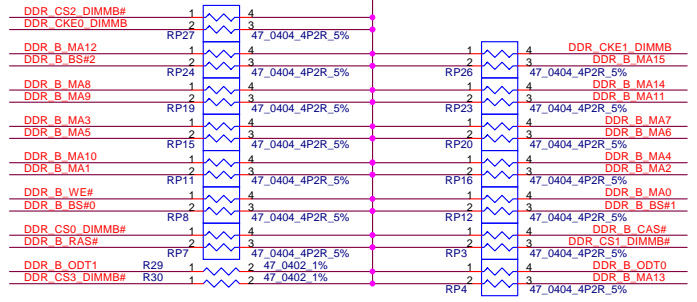
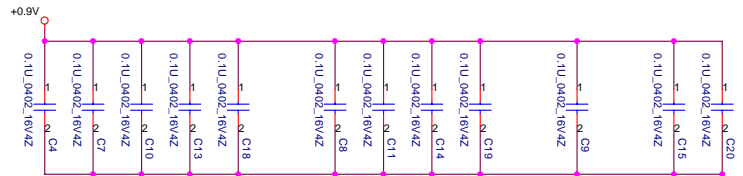
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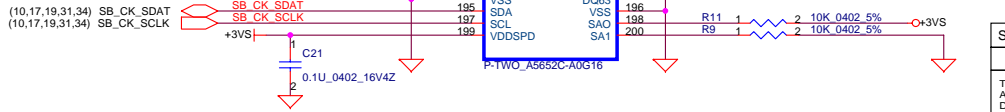
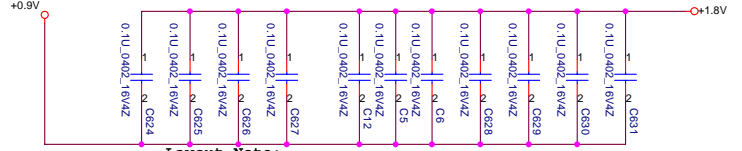
- (7) DDR\_B\_D[0..63]
- (7) DDR\_B\_DM[0..7]
- (7) DDR\_B\_DQS[0..7]
- (7) DDR\_B\_MA[0..15]
- (7) DDR\_B\_DQS#[0..7]



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9V



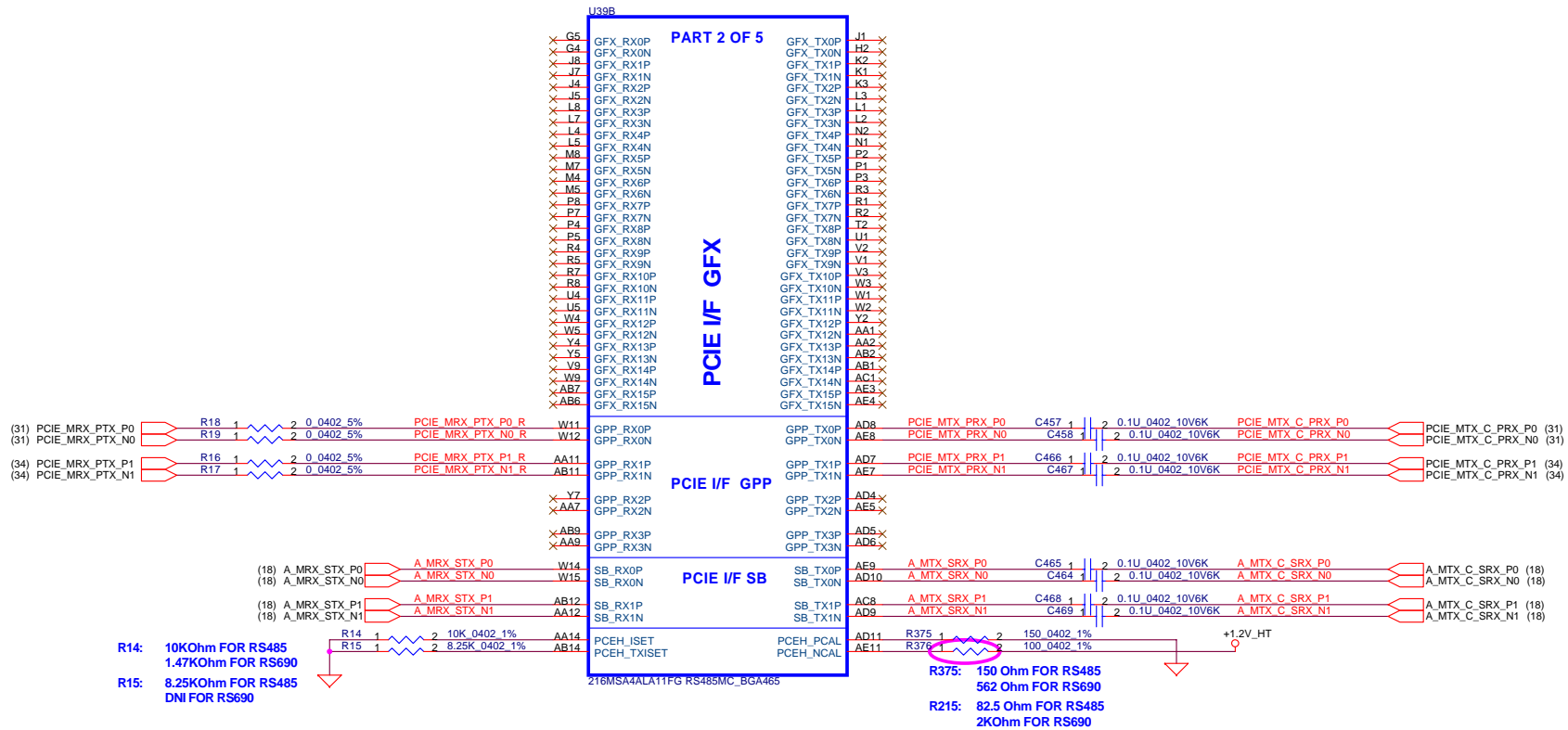
**Layout Note:**  
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V



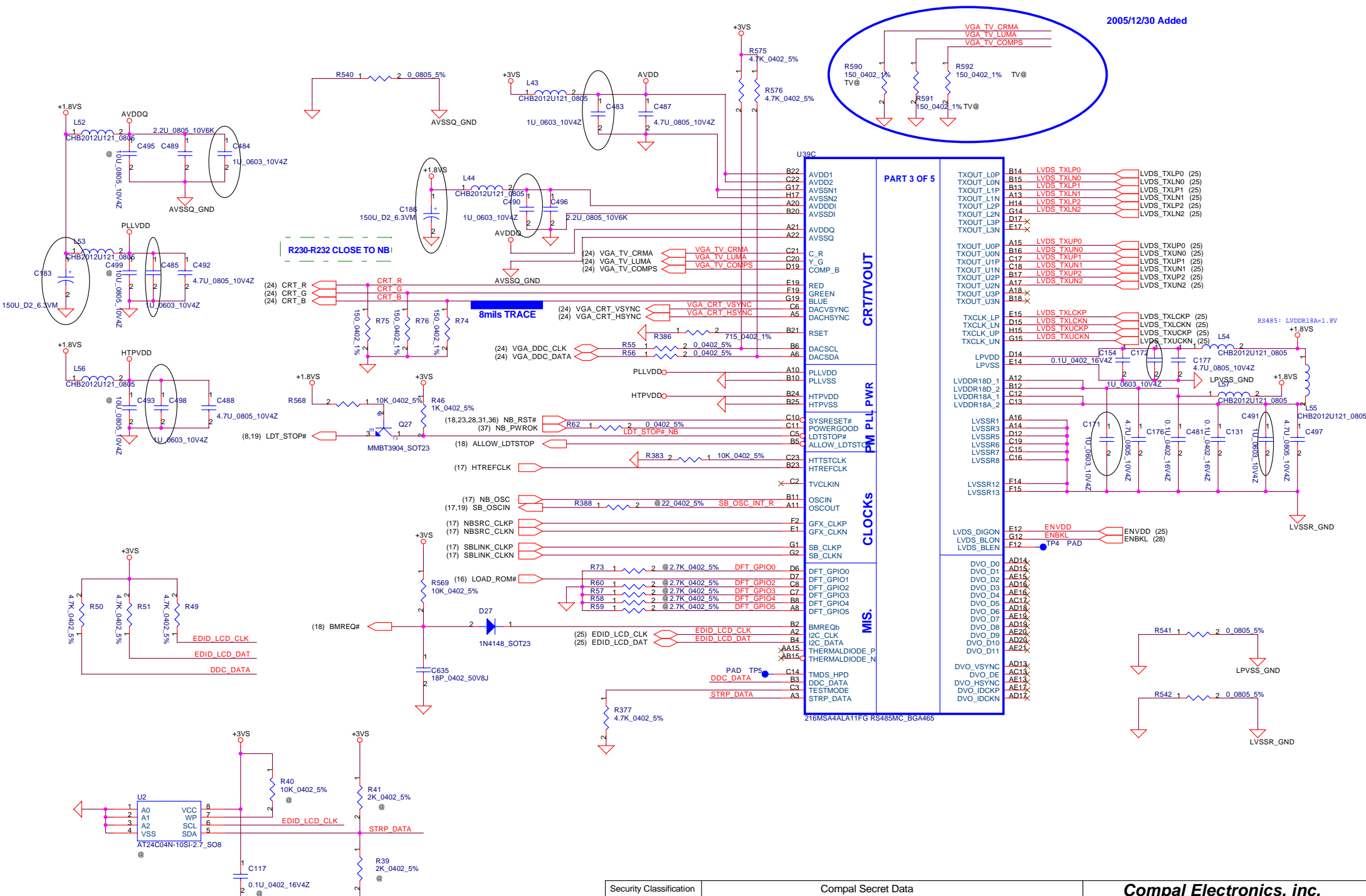
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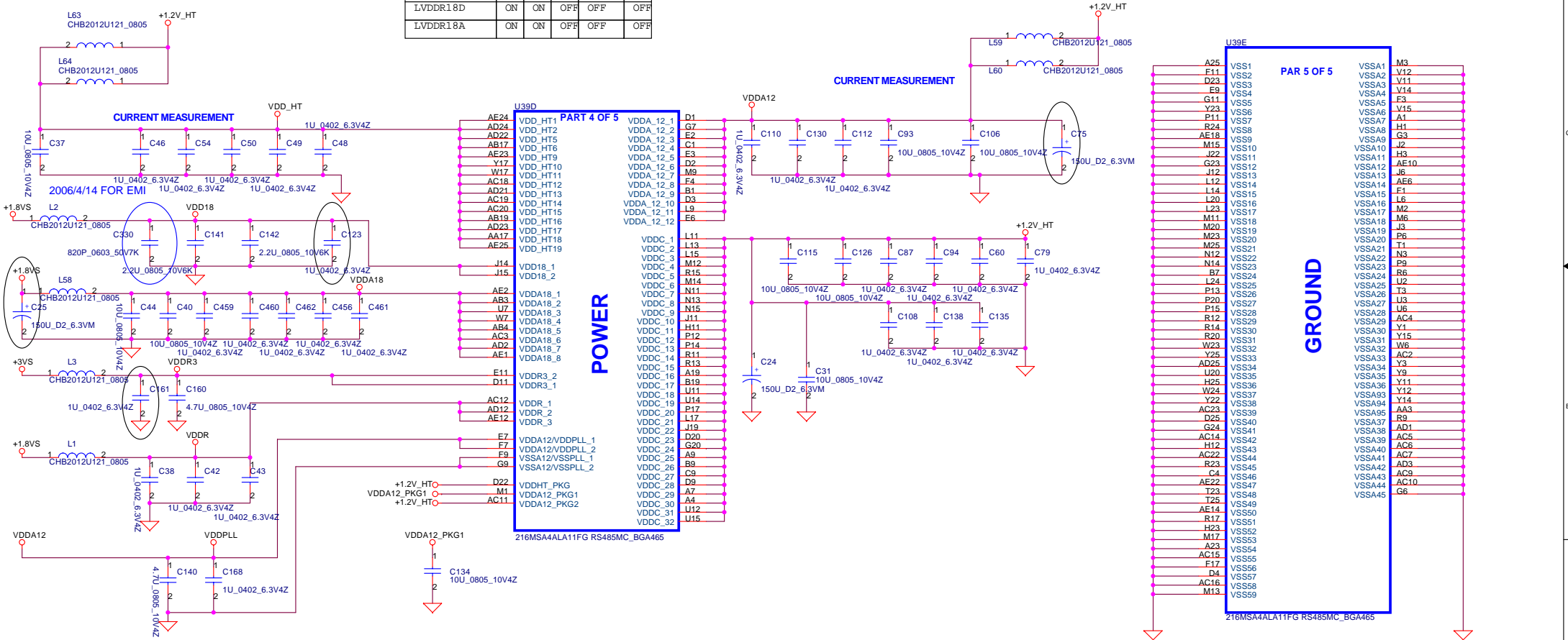
NOTE: ACCESS TO STRAP\_DATA and I2C\_CLK PIN IS MANDATORY.

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**NB RS485 POWER STATES**

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF



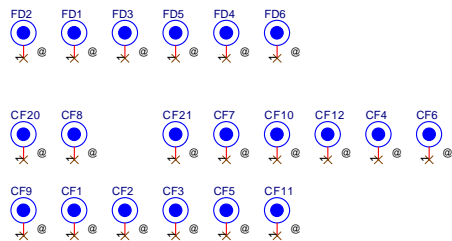
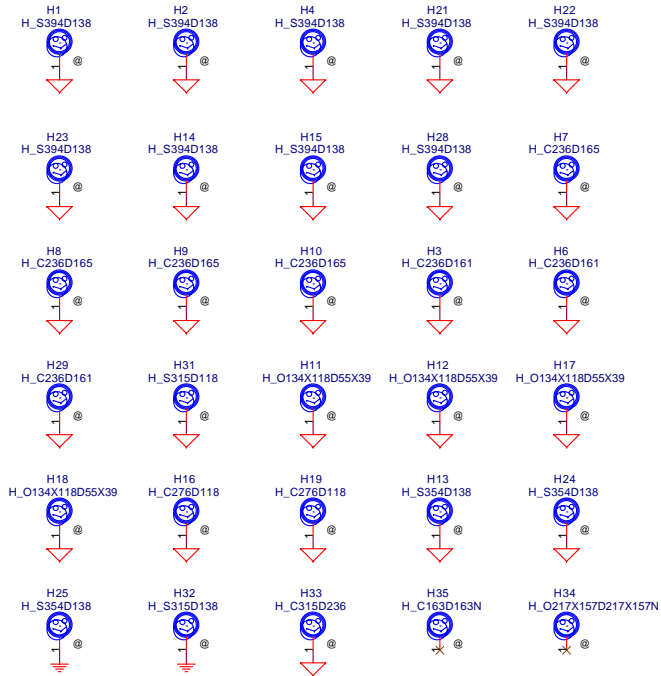
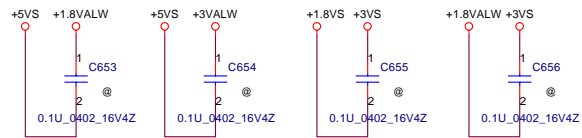
RS485: 0 Ohm RESISTOR  
RS690: 220 Ohm 500mA FERRITE BEAD

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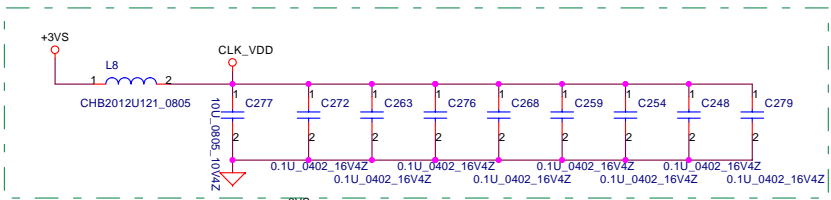
LOAD\_ROM#: LOAD ROM STRAP ENABLE

High, LOAD ROM STRAP DISABLE  
Low, LOAD ROM STRAP ENABLE

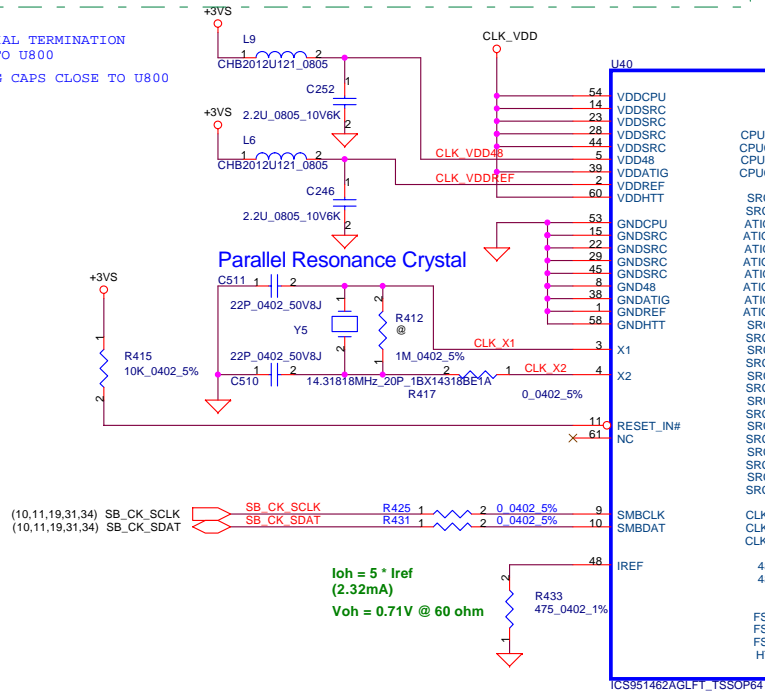


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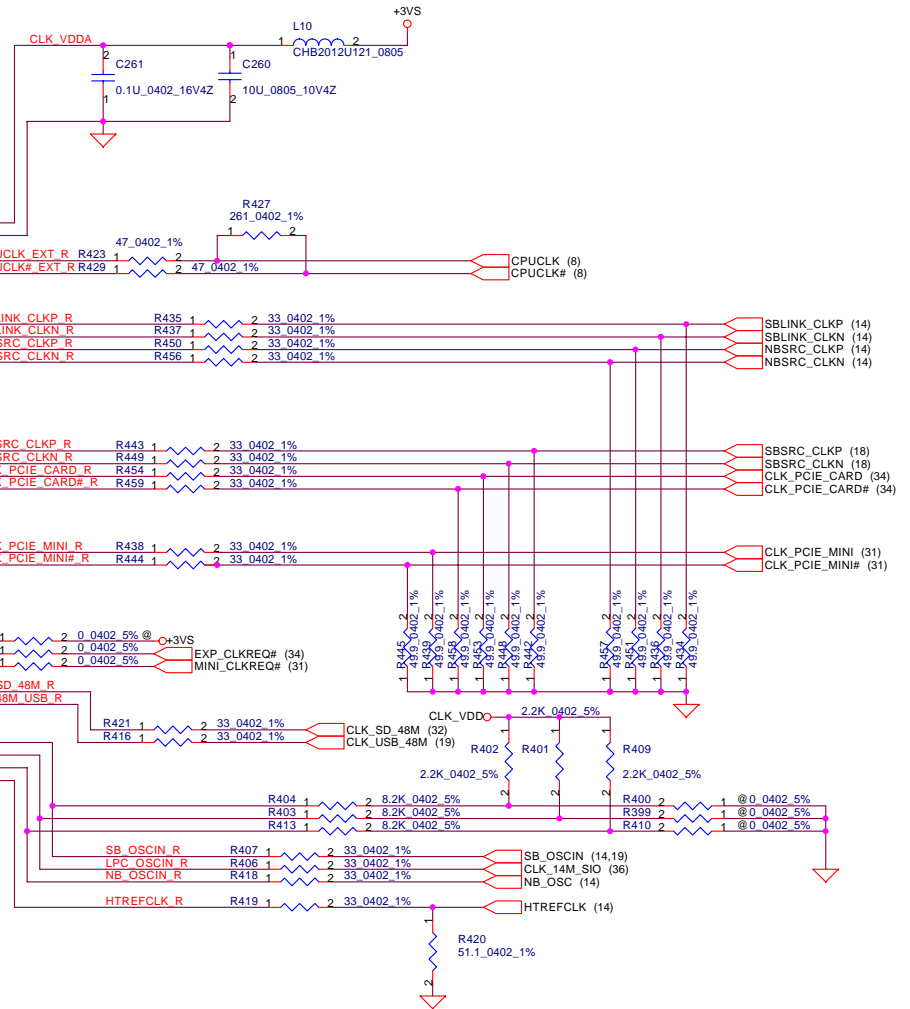




- 1- PLACE ALL SERIAL TERMINATION RESISTORS CLOSE TO U800
- 2- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



$I_{oh} = 5 * I_{ref}$   
 (2.32mA)  
 $V_{oh} = 0.71V @ 60 \text{ ohm}$

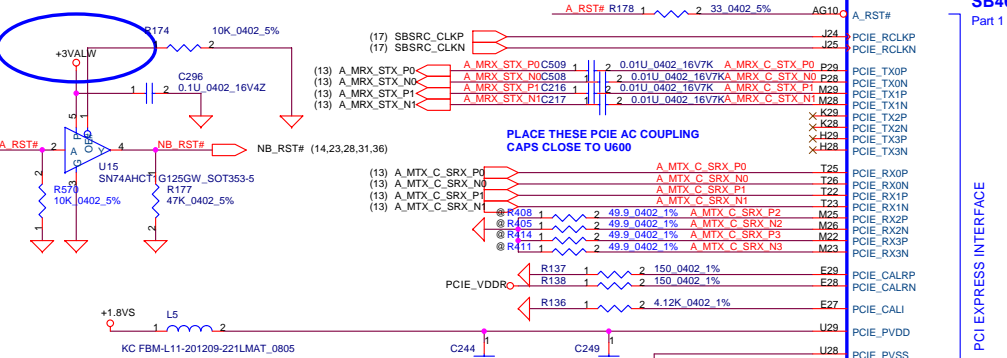


EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HIT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

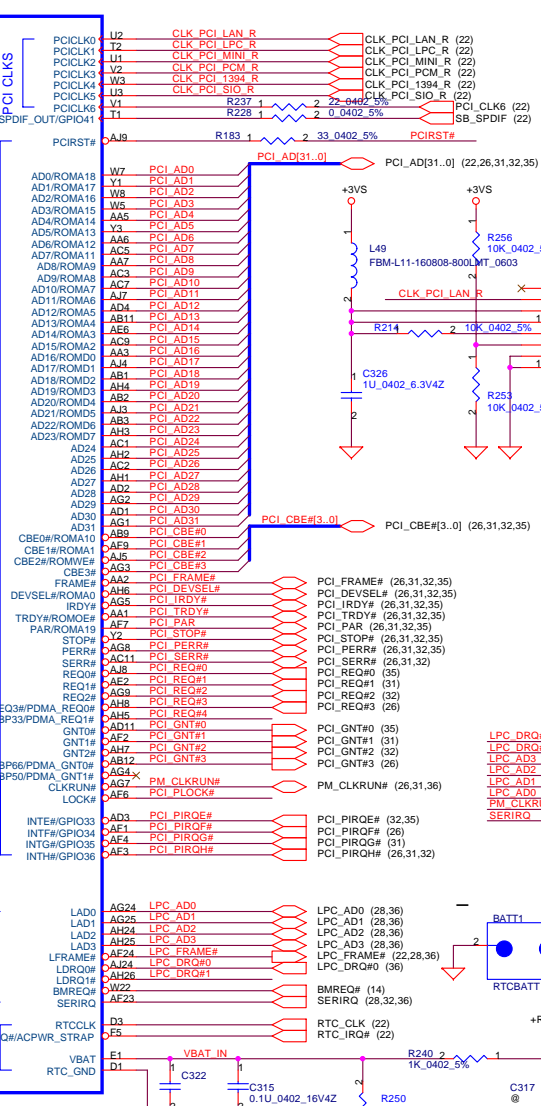
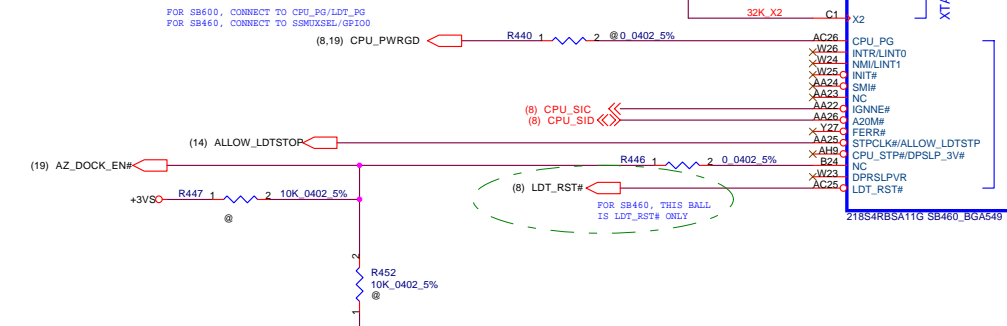
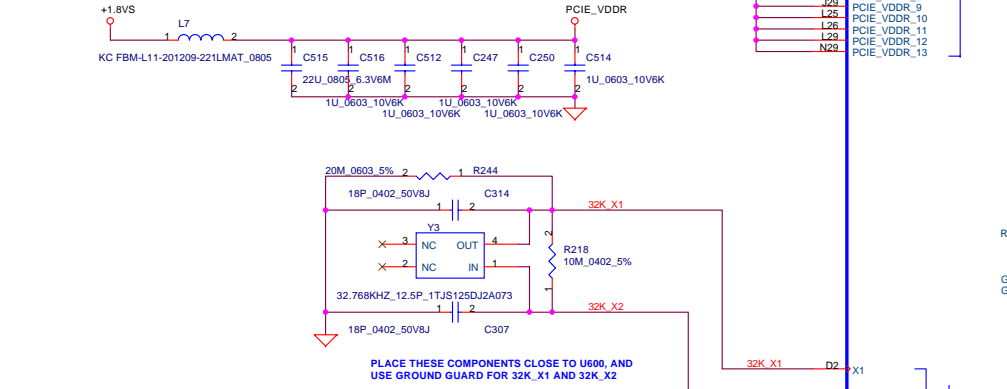
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2005/12/30 Change net to +3VALW

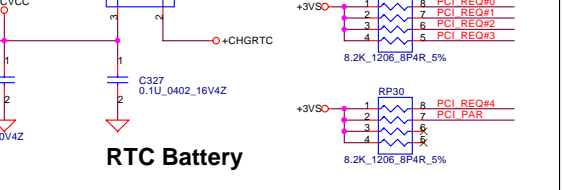
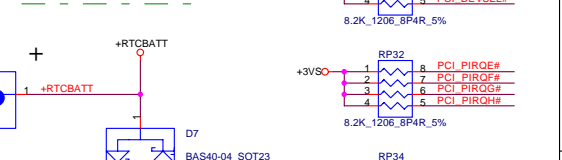
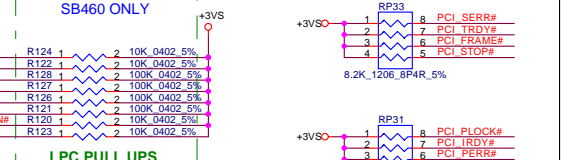
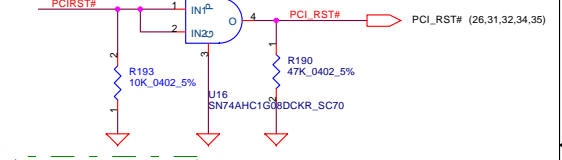
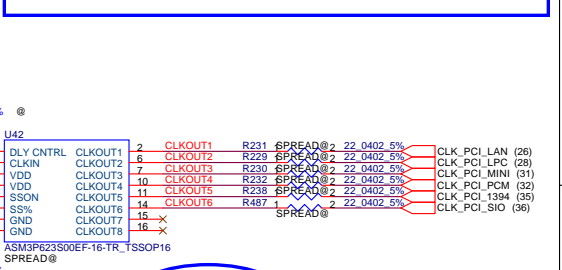
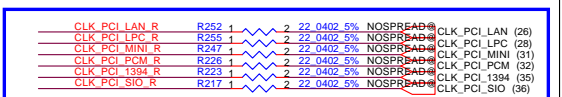


FOR SB600 VCC\_SB=1.2V  
 FOR SB460 VCC\_SB=1.8V

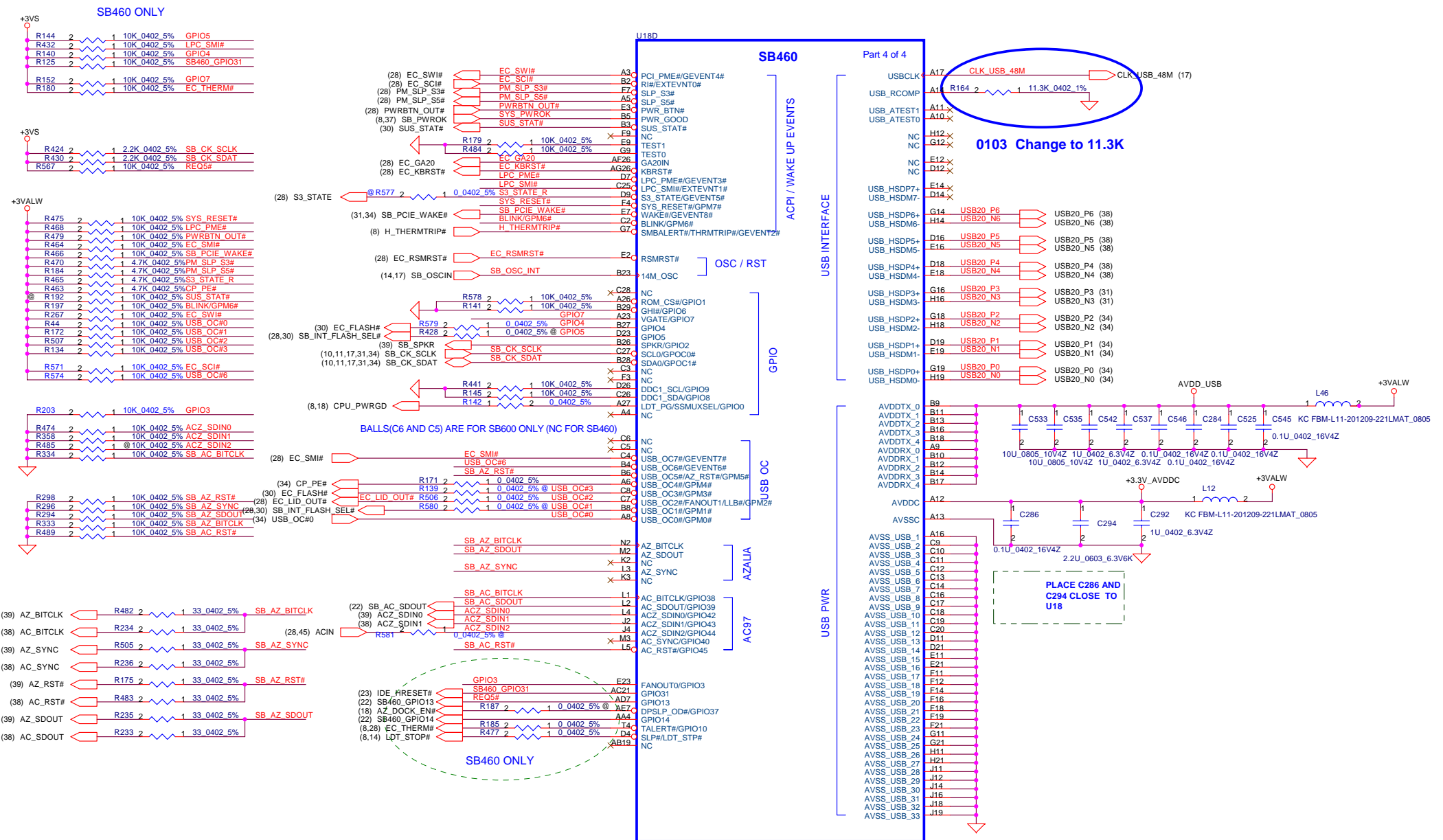
R601 CALRP: SB600=562R 1%, SB460=150R 1%  
 R603 CALRN: SB600=2.05K 1%, SB460=150R 1%  
 R603 CALRN: SB600=0R 1%, SB460=4.12K 1%



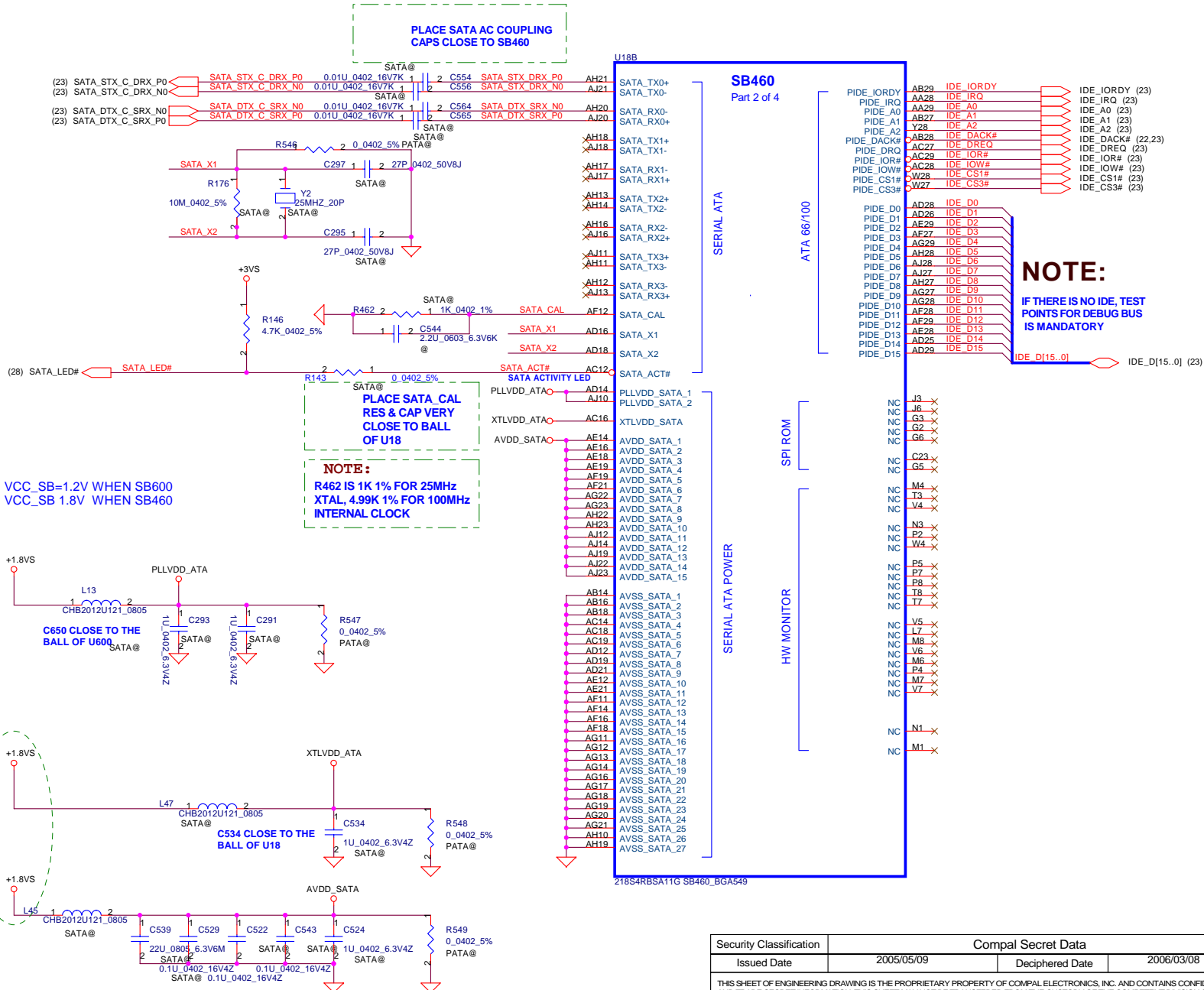
2005/10/27 Added, Near U4520, Need equal length



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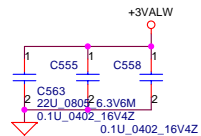
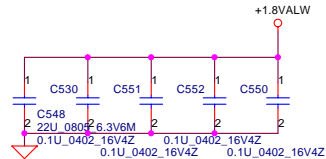
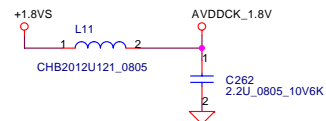
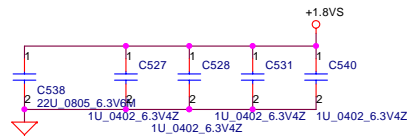
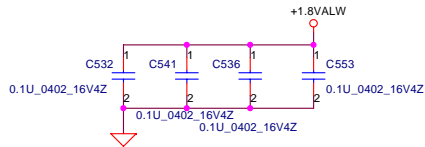
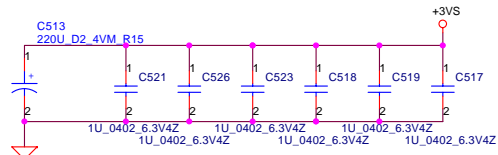
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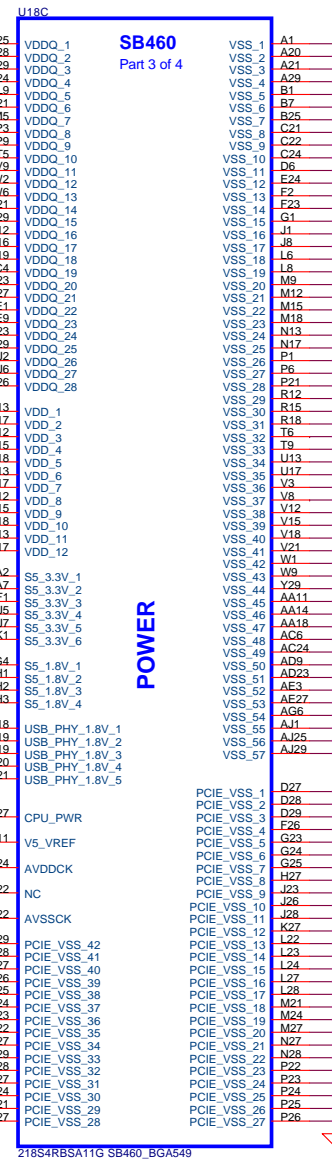
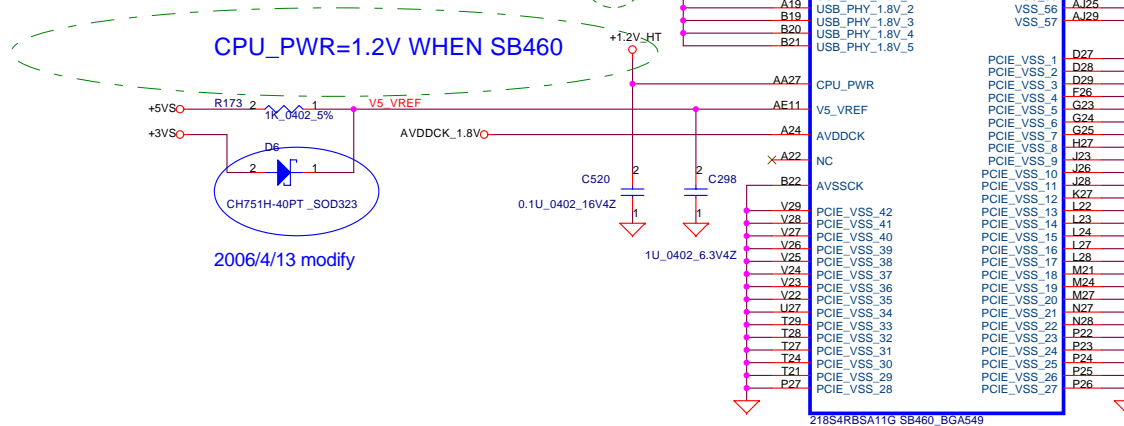
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



VCC\_SB=1.8V WHEN SB460

VCC\_SB=1.8V WHEN SB460

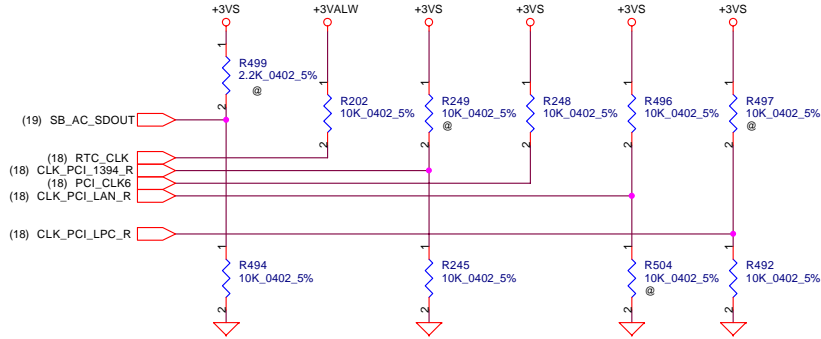
CPU\_PWR=1.2V WHEN SB460



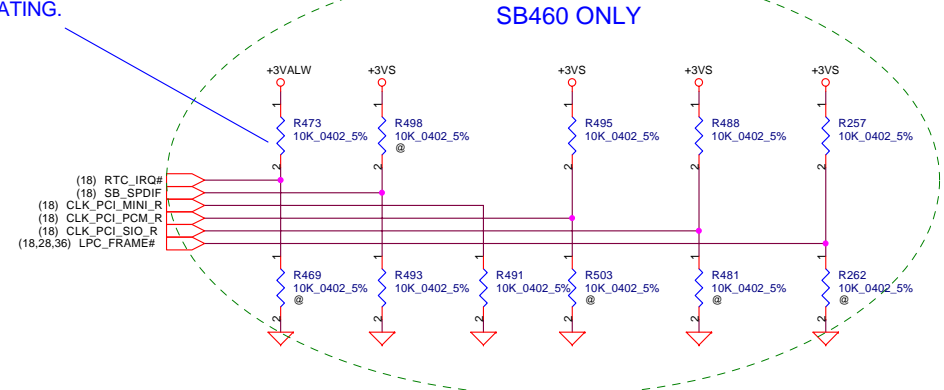
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# REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC\_SDATA\_OUT, 15K PU FOR RTC\_CLK, EXTERNAL PU/PD IS NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE REQUIRED



NOTE: R751 PU RESISTOR FOR RTC\_IRQ# IS REQUIRED FOR SB600 TO KEEP THE INPUT FROM FLOATING.



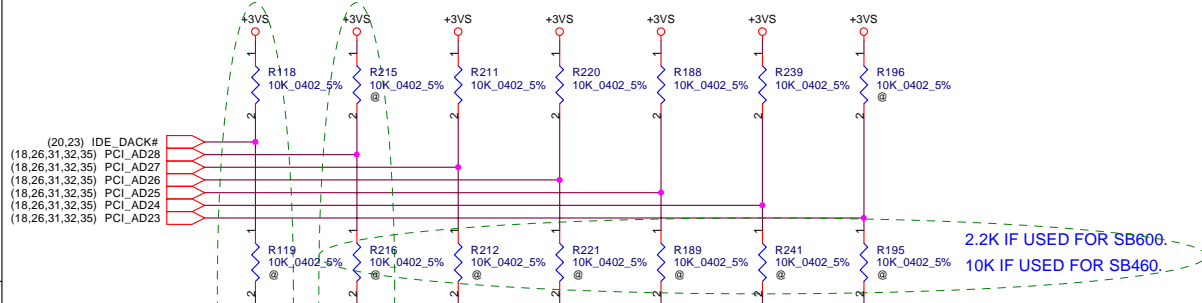
		SB600				SB460	
		AC_SDOUT	RTC_CLK	PCI_1394_R	PCI_CLK6	PCI_LAN_R	PCI_LPC_R
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM L, H = LPC II ROM L, L = FWH ROM	
	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4			
PULL LOW	USE DEBUG STRAPS	INTERNAL RTC	USE INT. PLL48	CPU IF=K8			
	IGNORE DEBUG STRAPS	EXTERNAL RTC	USE EXT. 48MHZ	CPU IF=P4			

NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK1[0]

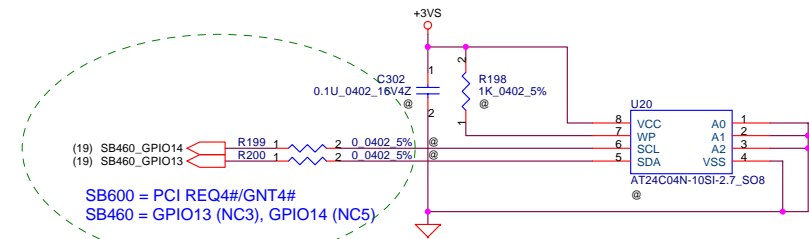
	ACPWON	SPDIF_OUT	PCI_MINI_R	PCI_PCM_R	PCI_SIO_R	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHZ	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHZ DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

# DEBUG STRAPS

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

SB600 ONLY

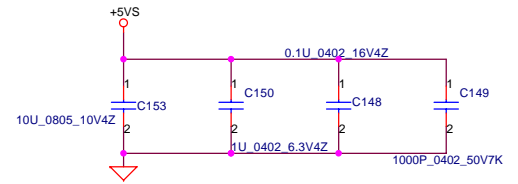
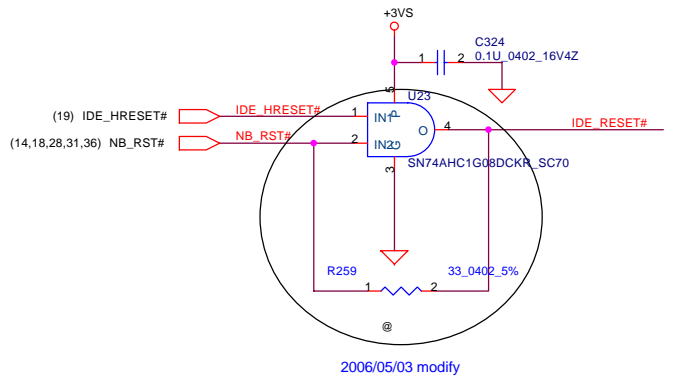
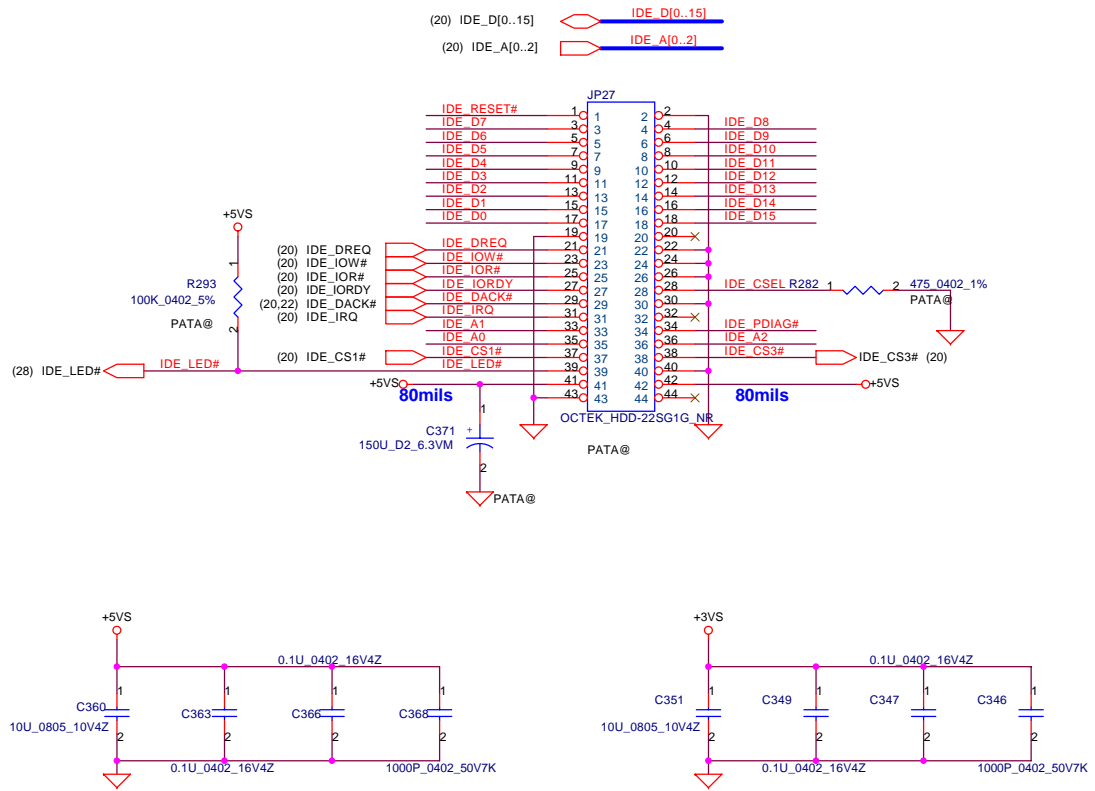
NOTE: FOR SB460, PCI\_AD23 IS RESERVED

SB PCIE EEPROM STRAPS

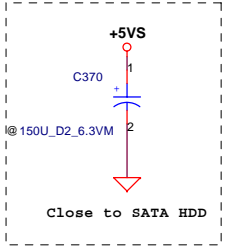
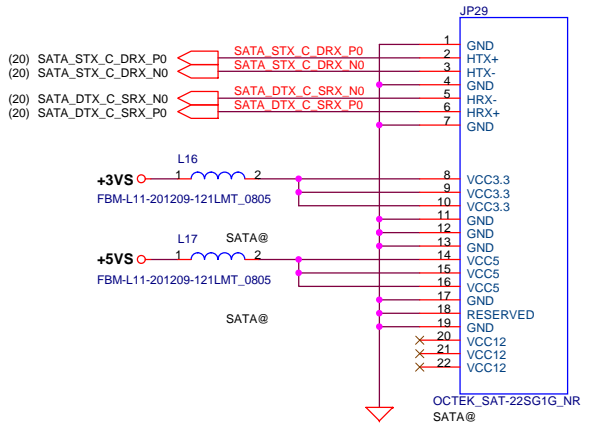
SB460 ONLY

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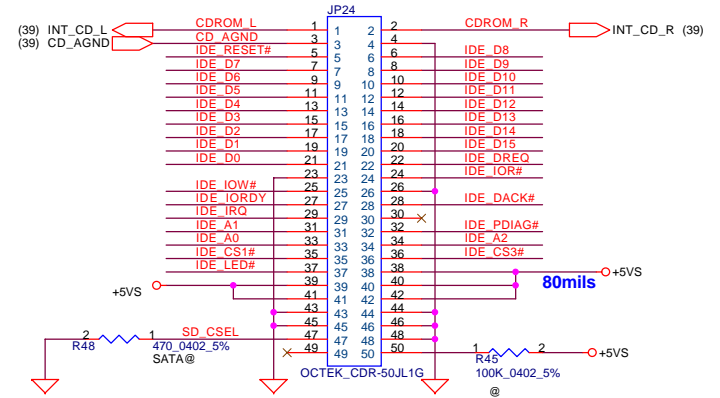
# HDD CONN



# SATA HDD CONN



# CDROM CONN

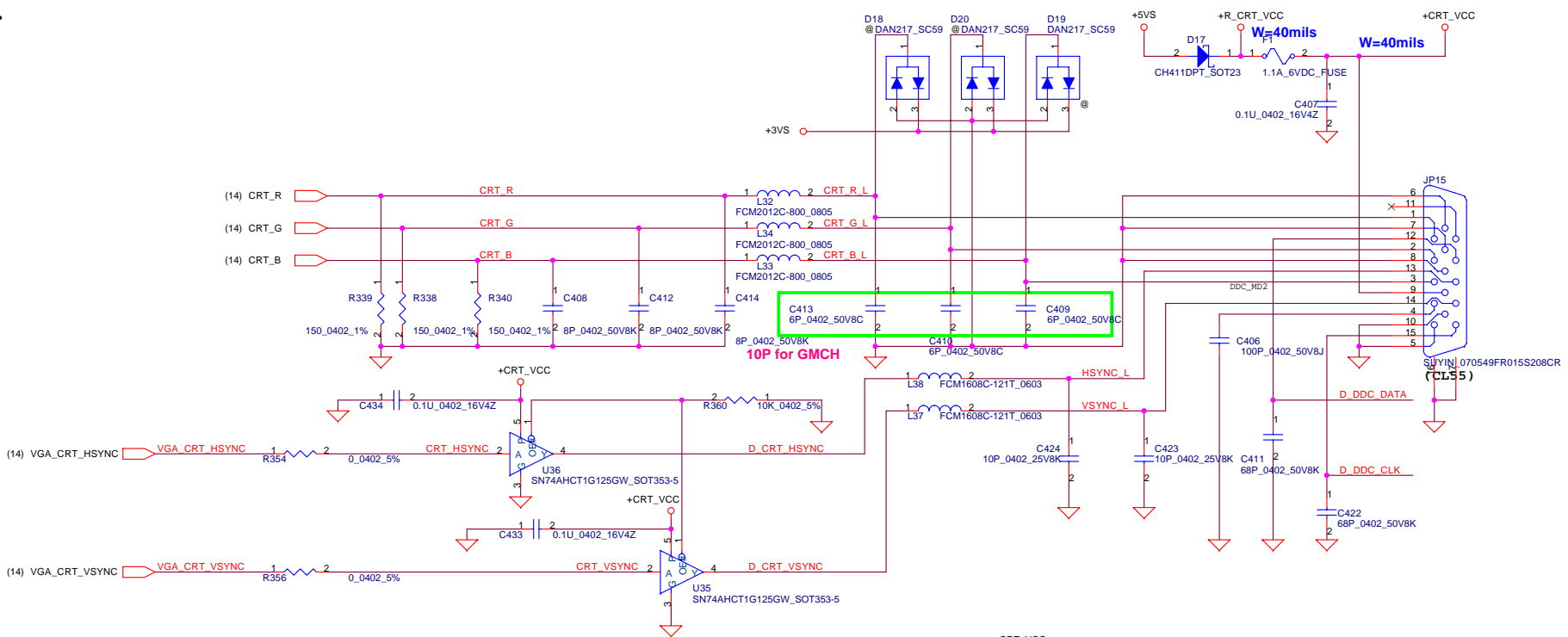


If CDROM is Slave  
then SD\_CSEL= Floating  
else SD\_CSEL= Low

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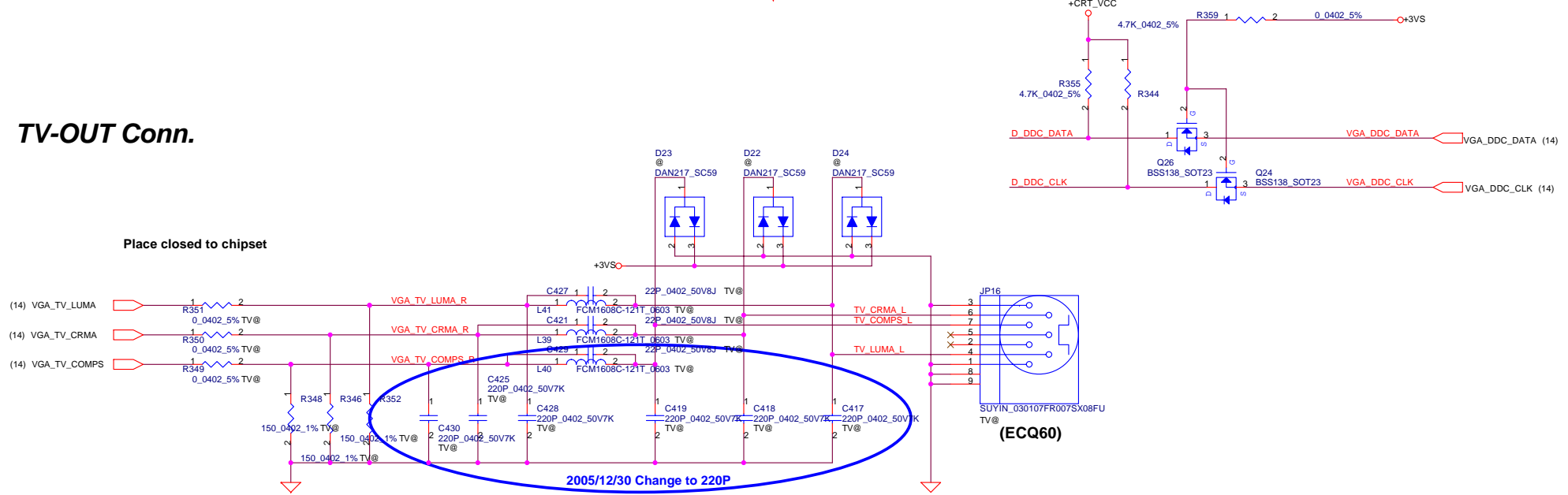
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# CRT Connector



# TV-OUT Conn.

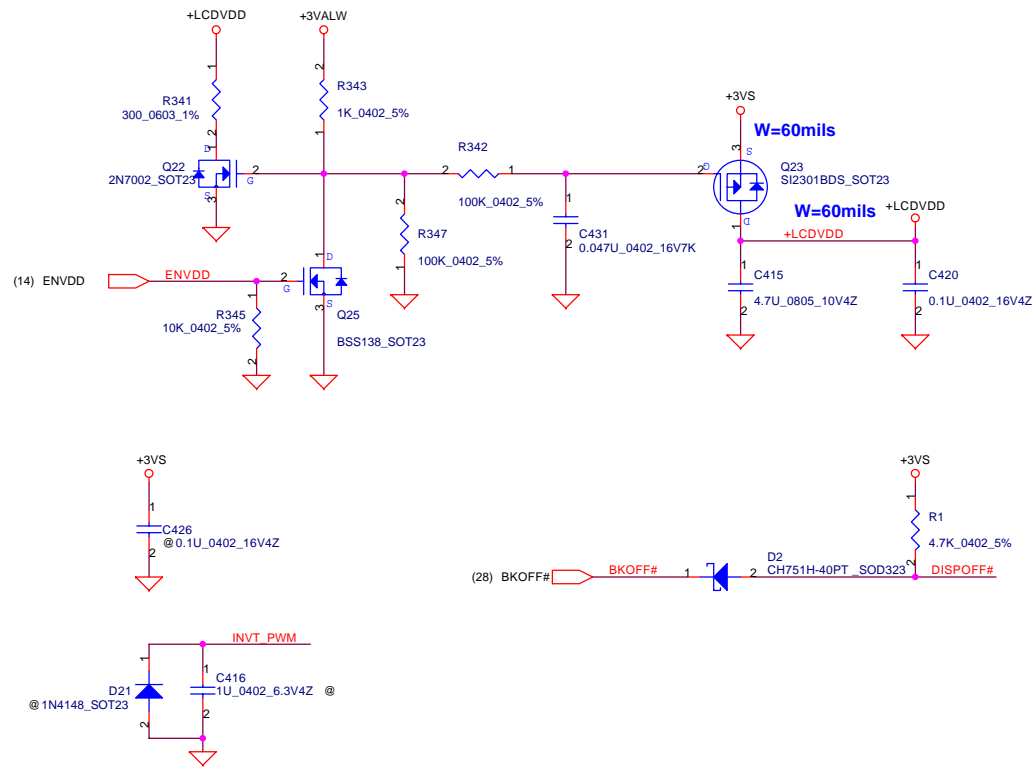
Place closed to to chipset



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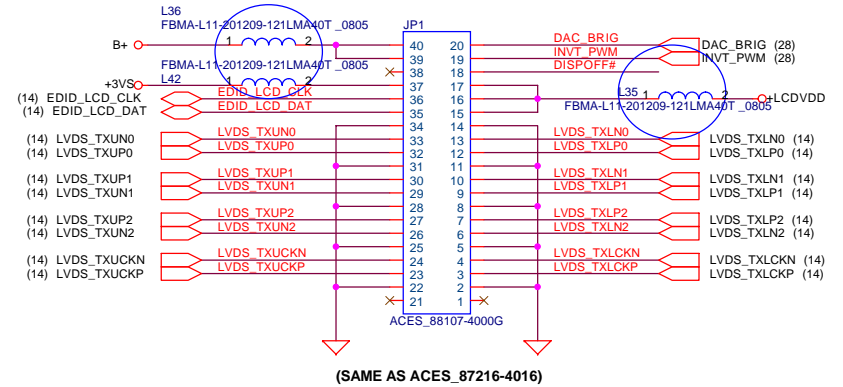


# LCD POWER CIRCUIT



# LCD/PANEL CONN.

04/17 modify



(SAME AS ACES\_87216-4016)

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(18,22,31,32,35) PCI\_AD[0..31] PCI\_AD[0..31]

PCI AD0	104	AD0
PCI AD1	103	AD1
PCI AD2	102	AD2
PCI AD3	98	AD3
PCI AD4	96	AD4
PCI AD5	97	AD5
PCI AD6	95	AD6
PCI AD7	93	AD7
PCI AD8	90	AD8
PCI AD9	89	AD9
PCI AD10	87	AD10
PCI AD11	86	AD11
PCI AD12	85	AD12
PCI AD13	83	AD13
PCI AD14	82	AD14
PCI AD15	79	AD15
PCI AD16	59	AD16
PCI AD17	58	AD17
PCI AD18	57	AD18
PCI AD19	55	AD19
PCI AD20	53	AD20
PCI AD21	50	AD21
PCI AD22	49	AD22
PCI AD23	47	AD23
PCI AD24	43	AD24
PCI AD25	42	AD25
PCI AD26	40	AD26
PCI AD27	39	AD27
PCI AD28	37	AD28
PCI AD29	36	AD29
PCI AD30	34	AD30
PCI AD31	33	AD31

(18,31,32,35) PCI_CBE#0	92	CBE#0
(18,31,32,35) PCI_CBE#1	77	CBE#1
(18,31,32,35) PCI_CBE#2	60	CBE#2
(18,31,32,35) PCI_CBE#3	44	CBE#3

PCI_AD17	1	LAN_IDSEL	46
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(18,31,32,35) PCI_PAR	76	PAR_FRAME#
(18,31,32,35) PCI_FRAME#	61	IRDY#
(18,31,32,35) PCI_IRDY#	63	TRDY#
(18,31,32,35) PCI_TRDY#	67	DEVSEL#
(18,31,32,35) PCI_DEVSEL#	68	STOP#
(18,31,32,35) PCI_STOP#	69	

(18,31,32,35) PCI_PERR#	70	PERR#
(18,31,32) PCI_SERR#	75	SERR#

(18) PCI_REQ#3	30	REQ#
(18) PCI_GNT#3	29	GNT#

(18,31,32) PCI_PIRQ#	25	INTA#
(18,31,32) PCI_PIRQH#	25	INTA#

(28) LAN_PME#	31	PME#
---------------	----	------

(18,31,32,34,35) PCI_RST#	27	RST#
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(18) CLK_PCI_LAN	28	CLK_CLKRUN#
(18,31,36) PM_CLKRUN#	65	CLK_CLKRUN#

4	GND/VSS	
17	GND/VSS	
128	GND/VSS	

21	GND/VSSPST	
38	GND/VSSPST	
51	GND/VSSPST	
81	GND/VSSPST	
91	GND/VSSPST	
101	GND/VSSPST	
119	GND/VSSPST	

35	GND	
52	GND	
80	GND	
100	GND	

24	NC/VDD12	
45	NC/VDD12	
64	NC/VDD12	
110	NC/VDD12	
116	NC/VDD12	

12	NC	
----	----	--

100@	RTL8110SBL_LQFP128	
------	--------------------	--

100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
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100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

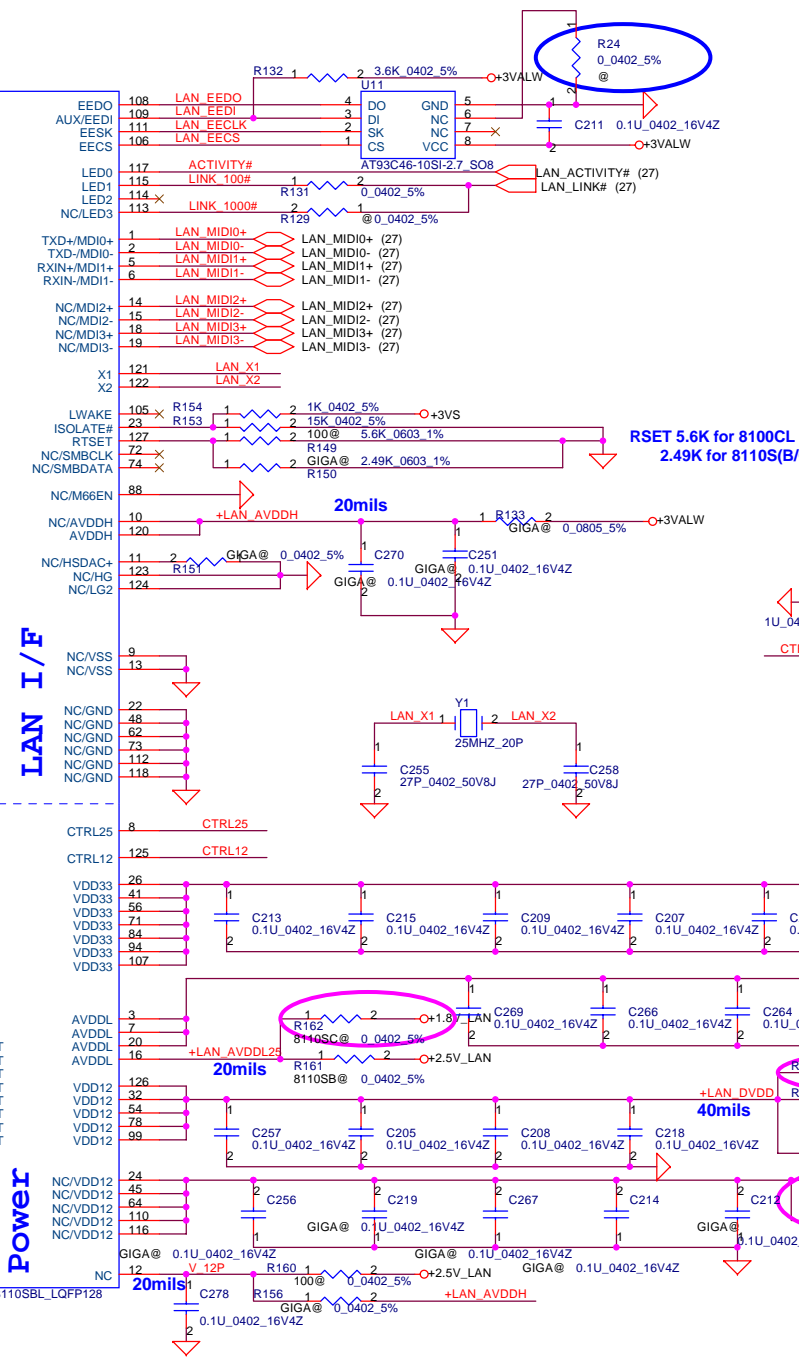
100@	RTL8110SBL change to Ver.D	
------	----------------------------	--

100@	RTL8110SBL change to Ver.D	
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100@	RTL8110SBL change to Ver.D	
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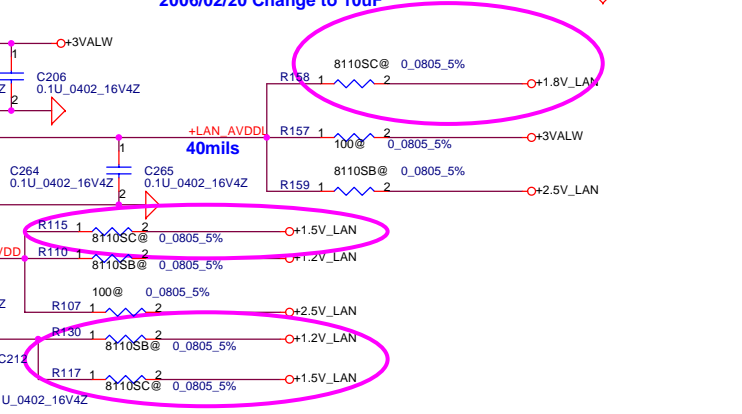
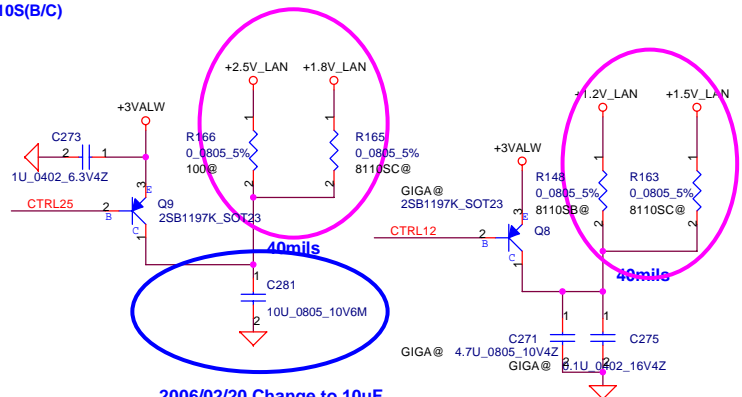
100@	RTL8110SBL change to Ver.D	
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100@	RTL8110SBL change to Ver.D	
------	----------------------------	--



FN	8100CL(10/100 LAN)	8110SB/CL(10/100/1000 LAN)
RSET	5.6K	2.49K

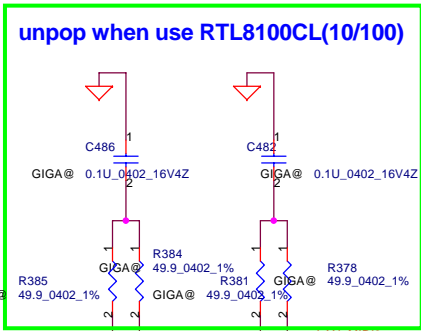
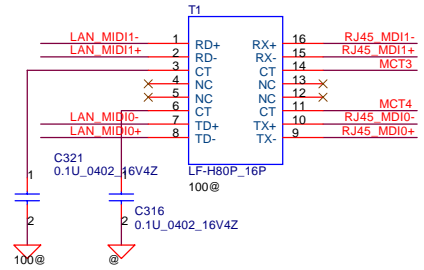
BOM structure	8100CL(10/100 LAN)		8110SB/CL(10/100/1000 LAN)	
	100@	Stuff	No_Stuff	No_Stuff
8110SB@	No_Stuff	Stuff	No_Stuff	No_Stuff
8110SC@	No_Stuff	No_Stuff	No_Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff	No_Stuff



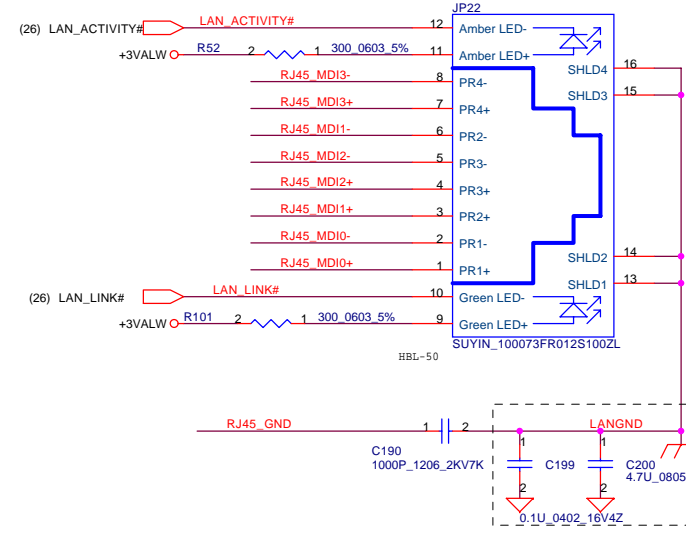
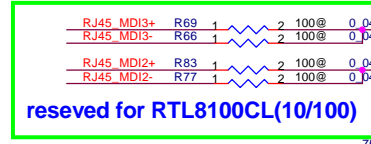
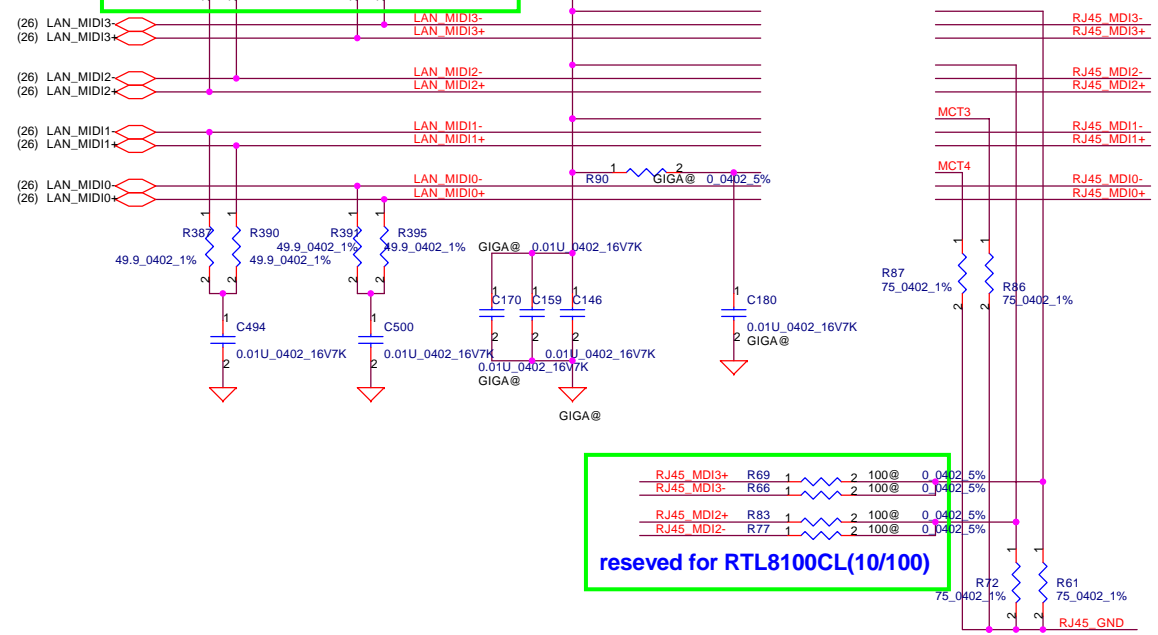
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Issued Date	2005/05/09	Deciphered Date	2006/07/29
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Title		
SCHEMATIC, M/B LA-3121P		
Size	Document Number	Rev
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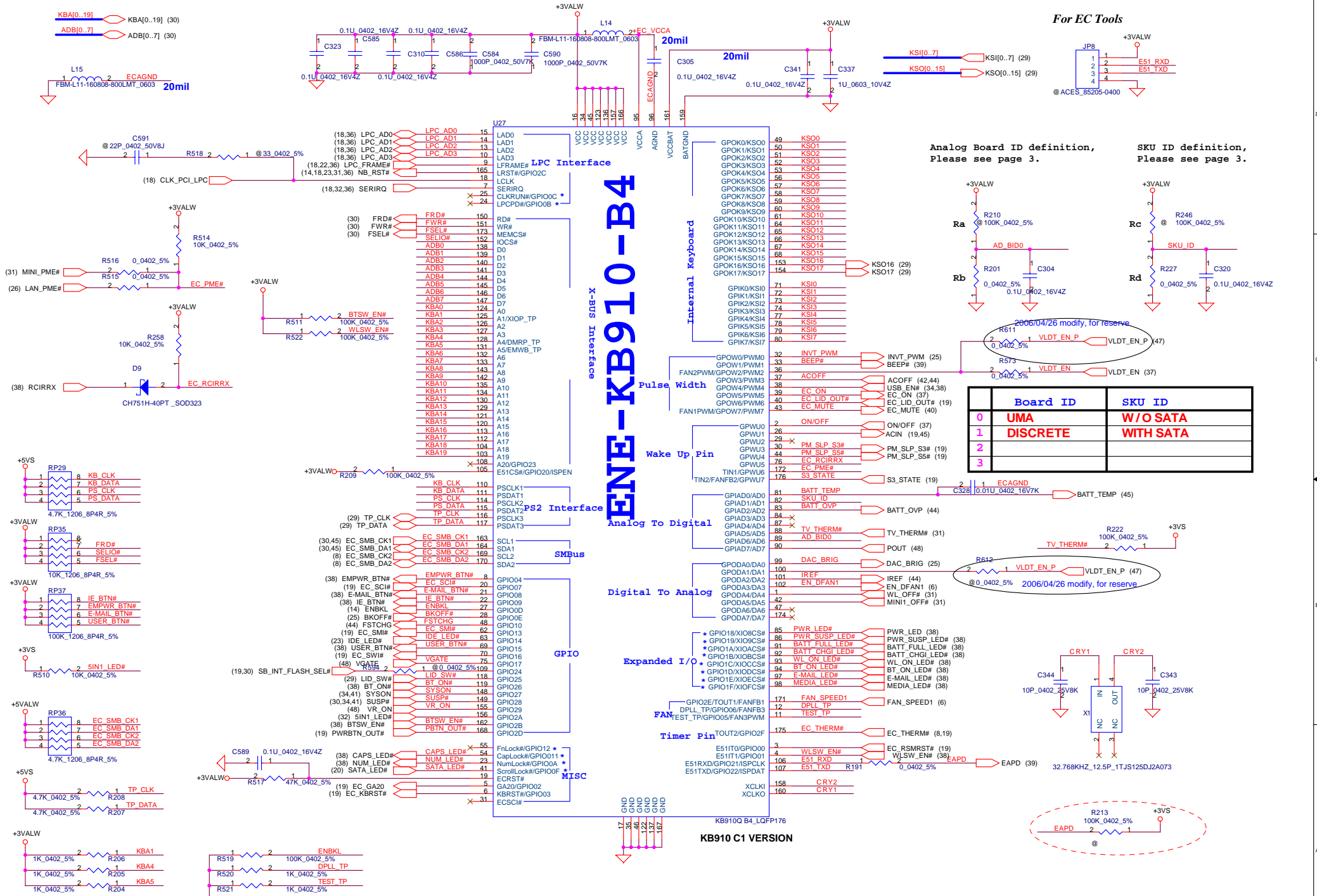
# LAN RTL8110SB/C & RTL8100CL



**24HST1041A-3(SP050002110) for RTL8110SB/CL(GbE)**  
**TST1284-LF (SP050001X10) for RTL8100CL(10/100)**  
**24ST0023-3: Half port(TD[3:4], MX[3:4])**



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Size		Document Number			Rev	
B		401411			D	
Date:	星期一, 五月 08, 2006			Sheet	27 of 51	

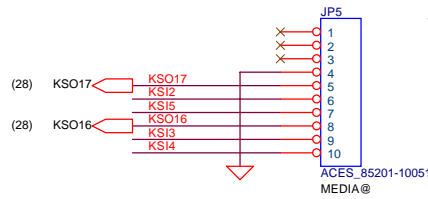
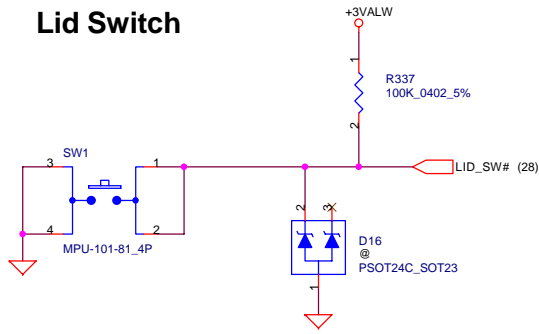


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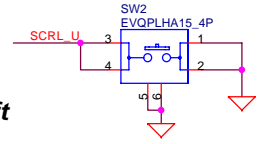
Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-3121P			
Size	Document Number	Rev D	
	401411		
Date:	星期一, 五月 08, 2006	Sheet	28 of 51

### Lid Switch

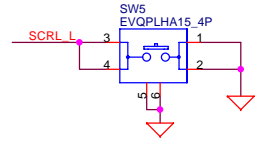


	KSO16	KSO17
KSI2	PLAY	VOL_UP
KSI3	STOP	VOL_DOWN
KSI4	NEXT	ARCADE_TV
KSI5	REV	

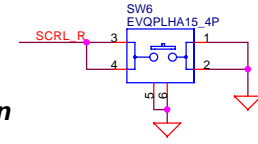
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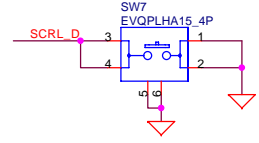
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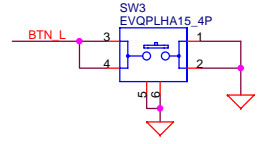
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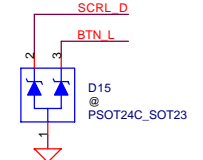
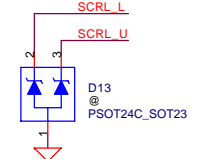
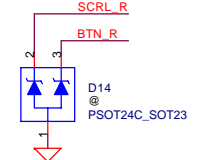
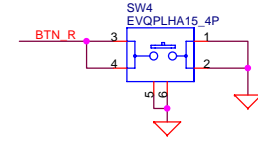
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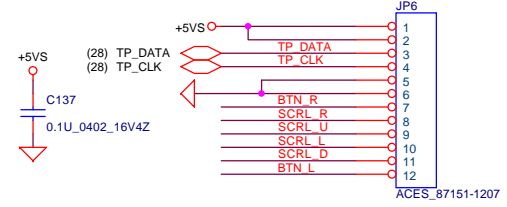
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### Right

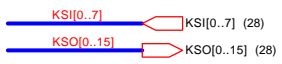
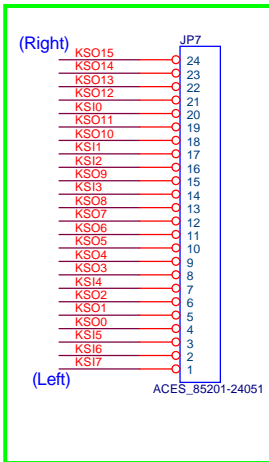
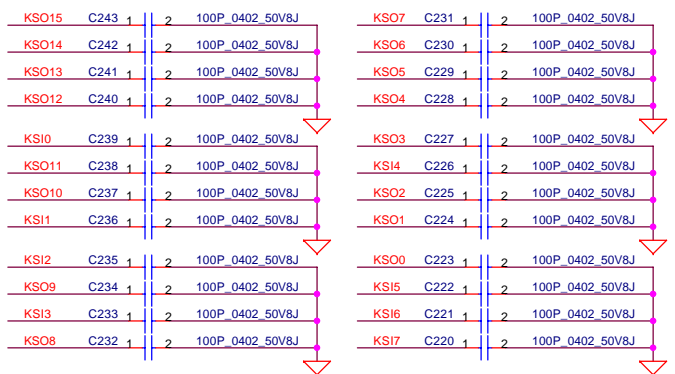


### To TP/B Conn.





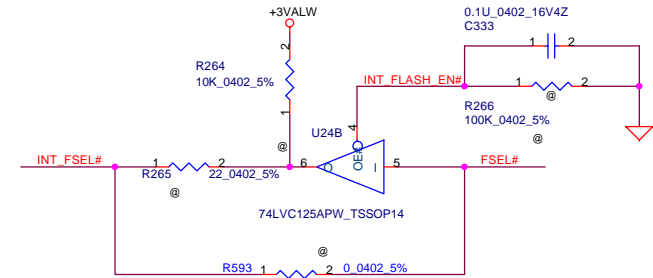
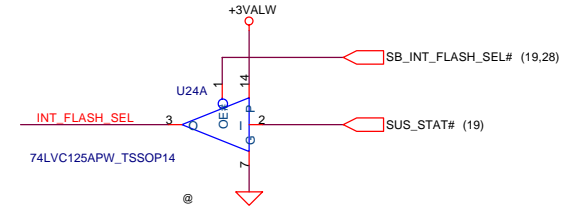
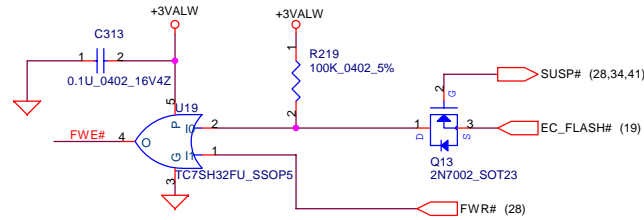
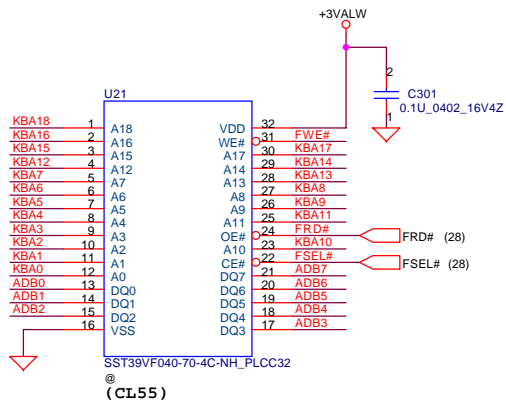
BTN_R	C139	1	2	100P_0402_50V8J
SCRL_R	C157	1	2	100P_0402_50V8J
SCRL_U	C162	1	2	100P_0402_50V8J
SCRL_L	C151	1	2	100P_0402_50V8J
SCRL_D	C167	1	2	100P_0402_50V8J
BTN_L	C144	1	2	100P_0402_50V8J
TP_DATA	C169	1	2	100P_0402_50V8J
TP_CLK	C174	1	2	100P_0402_50V8J

### INT\_KBD Conn.

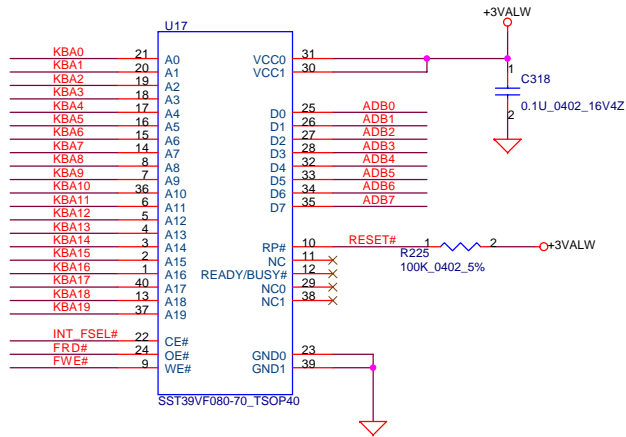


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(28) KBA[0..19]  KBA[0..19]  
 (28) ADB[0..7]  ADB[0..7]

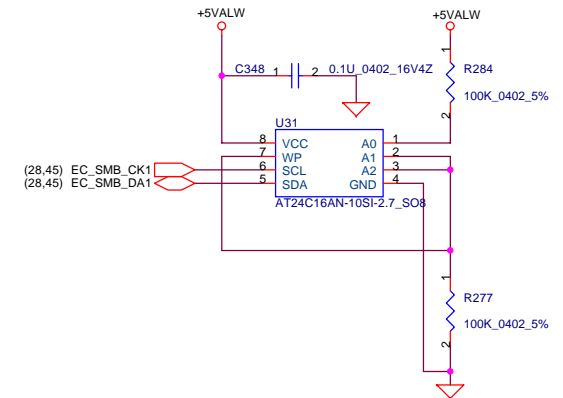
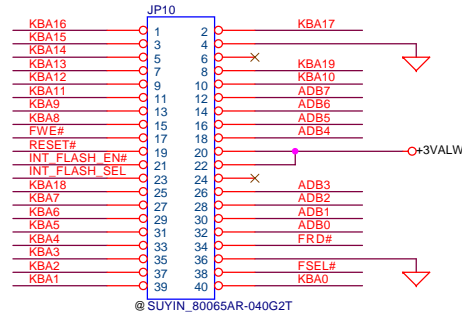


### 1MB Flash ROM

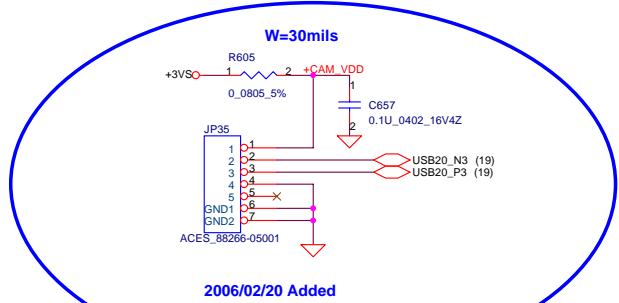
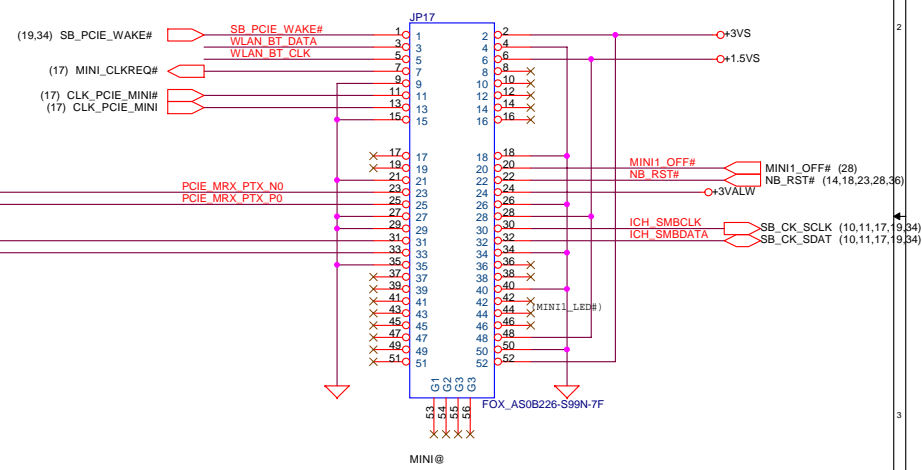
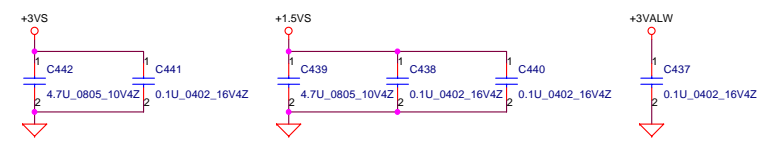
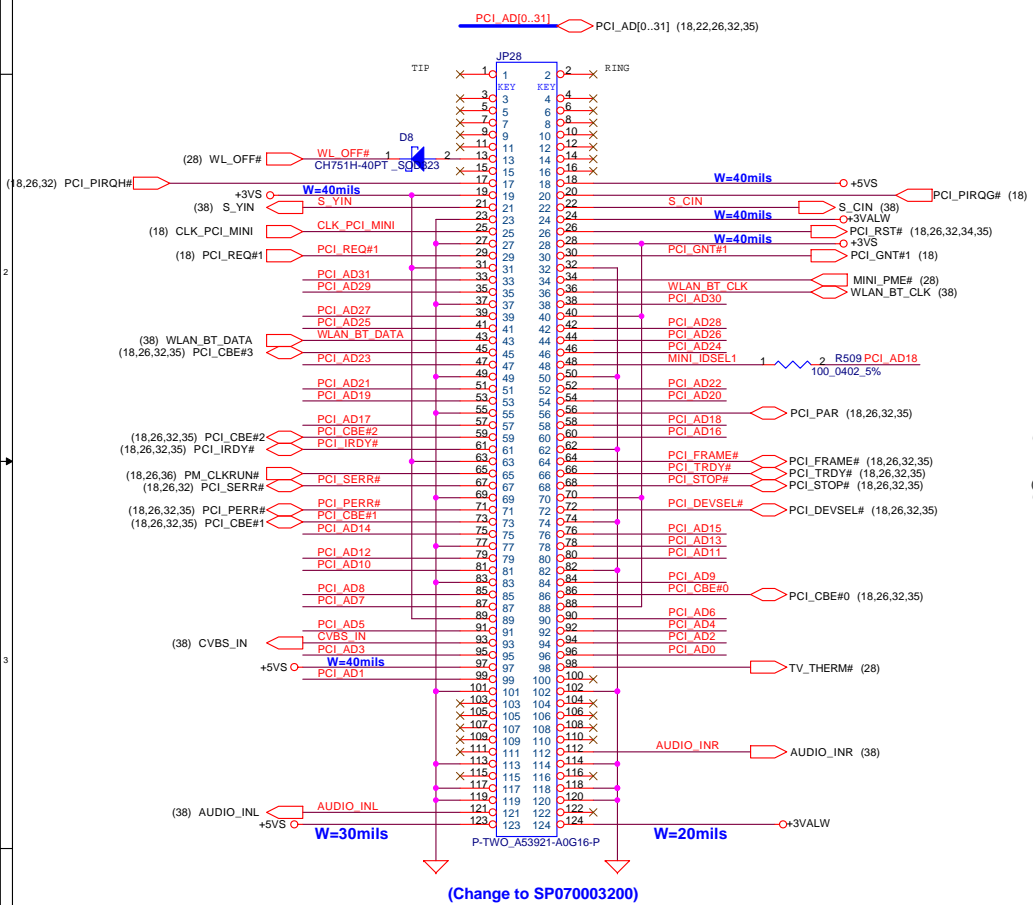
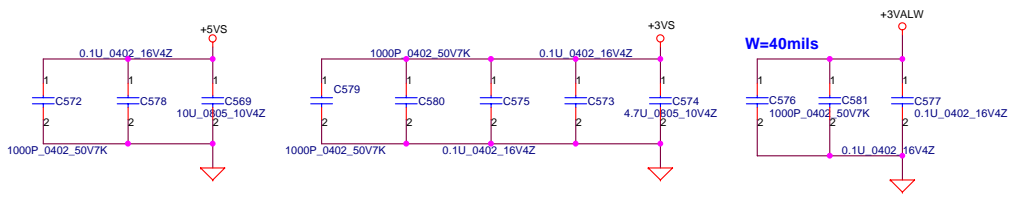


SST part : SA39080000  
 MXIC part : SA290080120

### 1MB ROM Socket

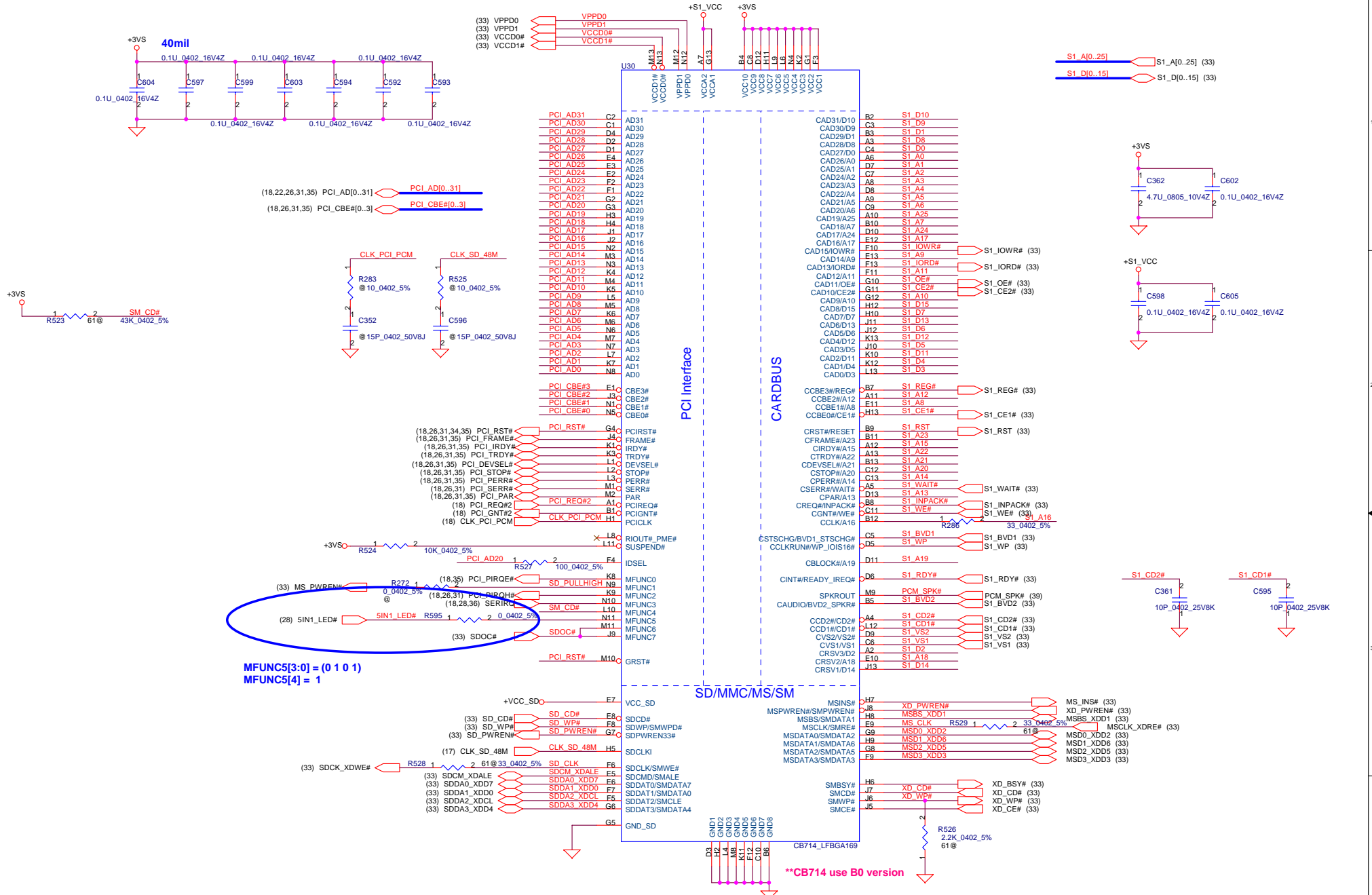


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			Document Number 401411
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**Mini Card Power Rating**

Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



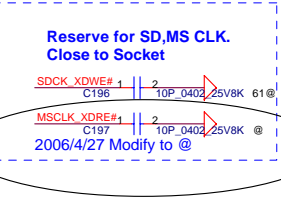
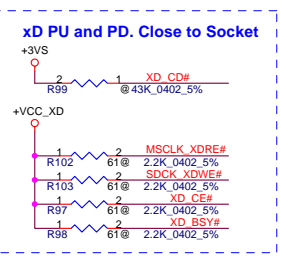
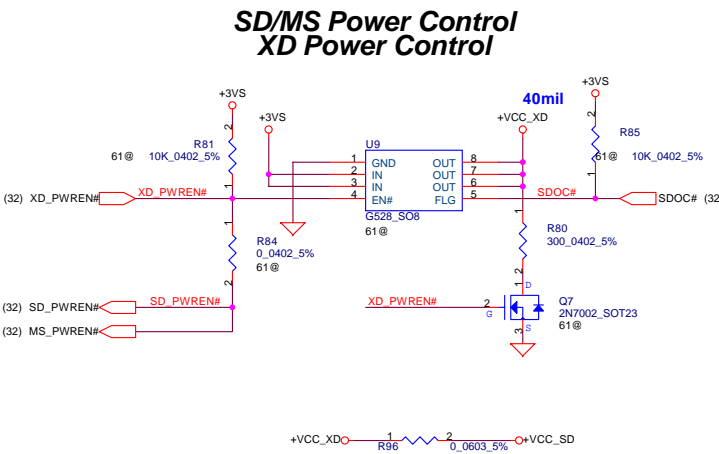
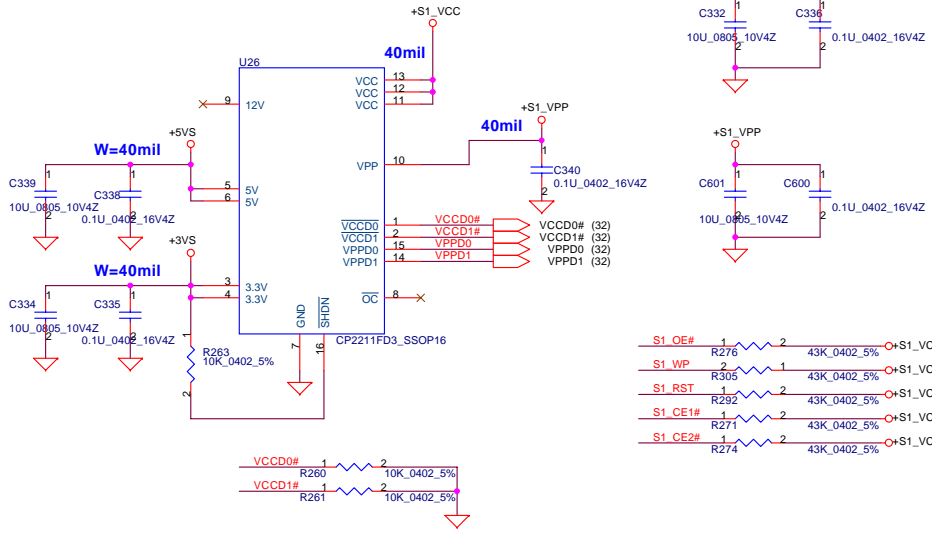
MFUNC5[3:0] = (0 1 0 1)  
MFUNC5[4] = 1

\*\*CB714 use B0 version

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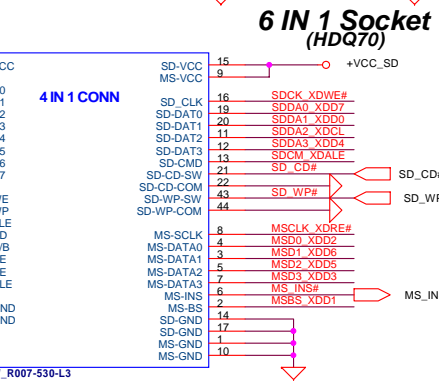
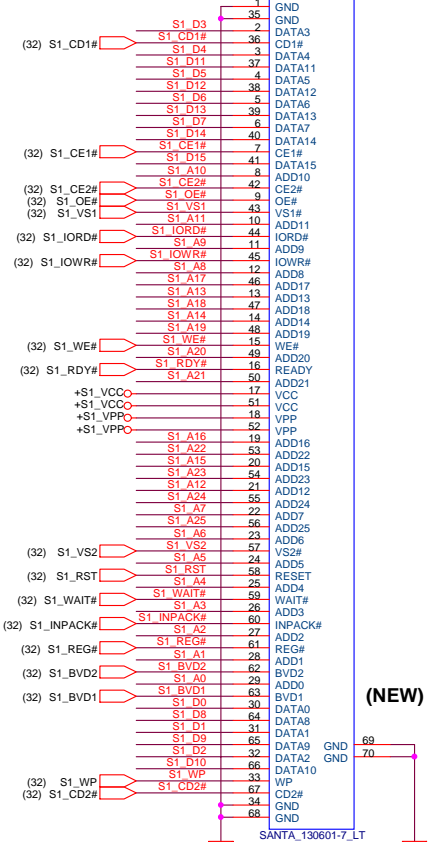


### PCMCIA Power Control



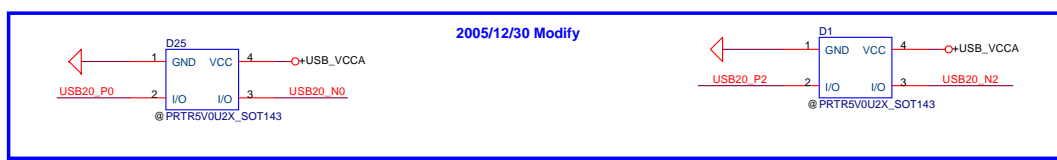
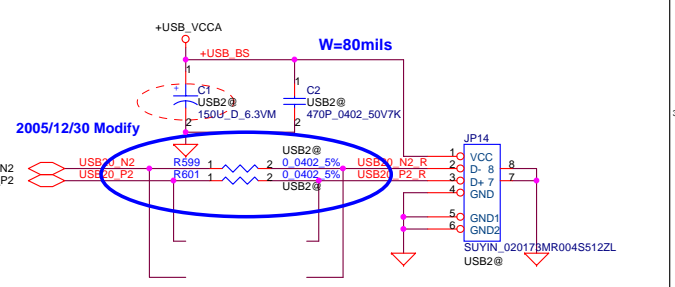
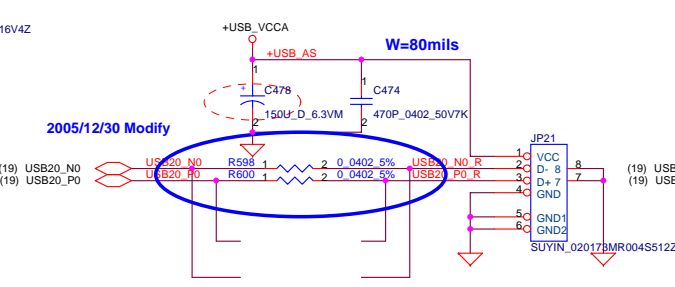
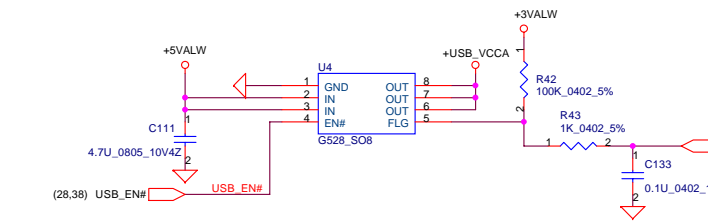
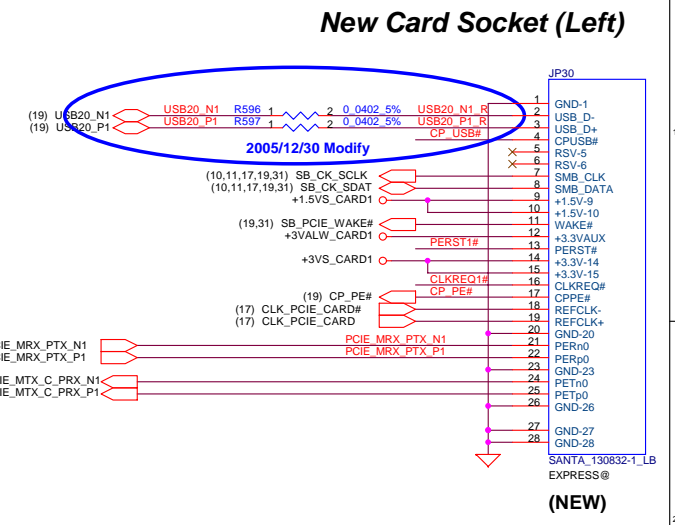
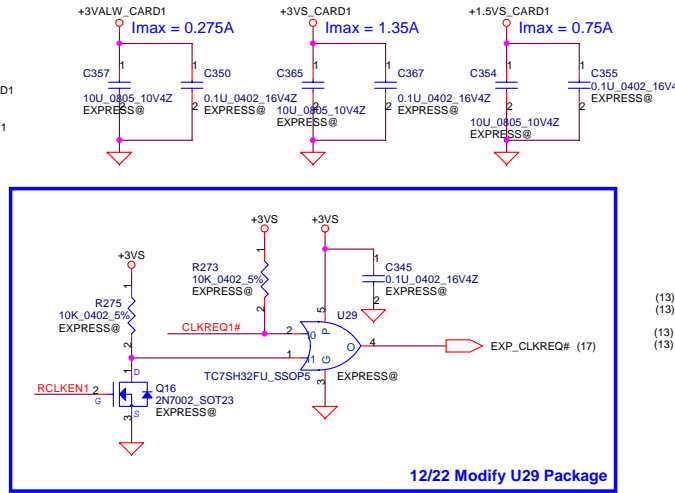
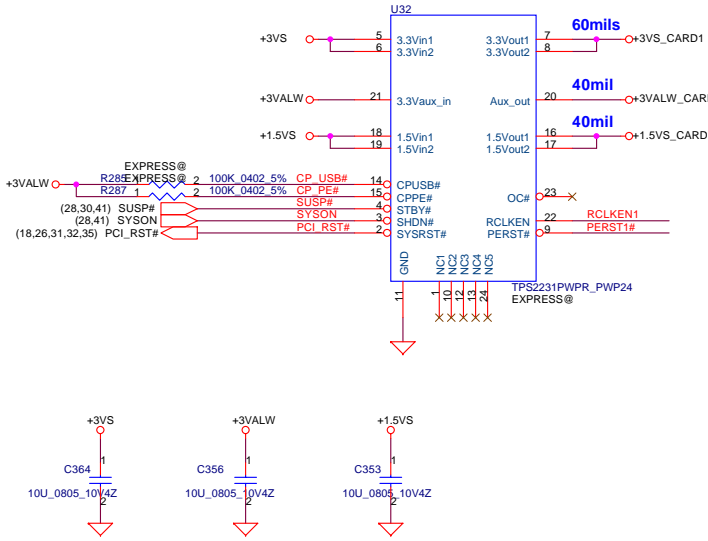
2006/4/13 modify

### PCMCIA Socket

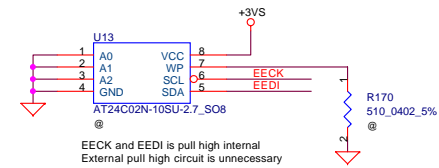
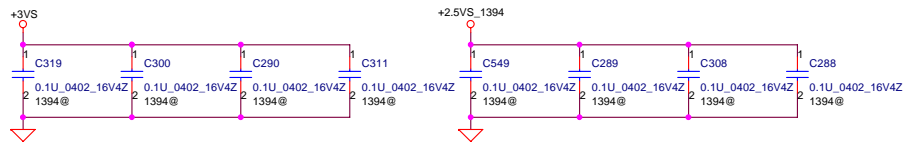


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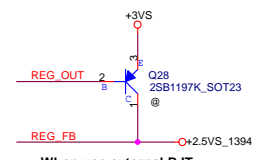
# New Card Power Switch



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Size	B	Document Number	401411	Rev	D
Date:	星期一, 五月 08, 2006	Sheet	34	of	51



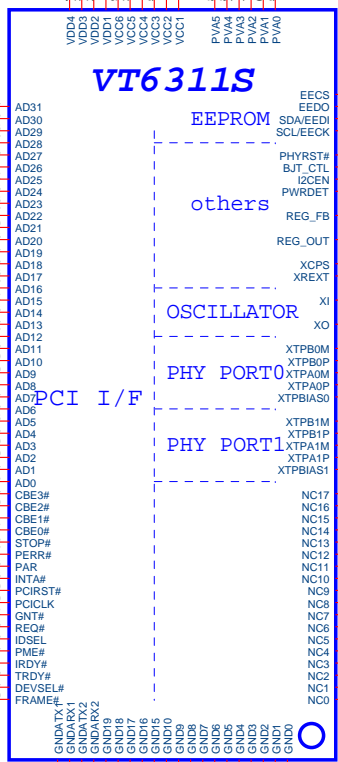
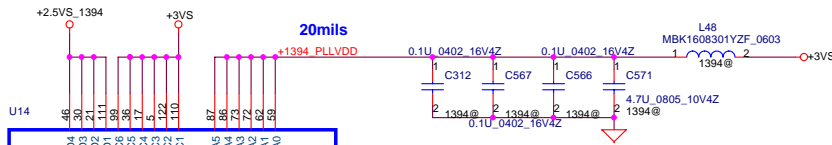
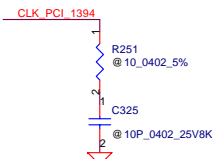
When use external EEPROM  
Populate U13, R170, R186  
Un-populate R169



(18,26,31,32) PCI\_AD[0..31] PCI\_AD10..31

IDSEL:PCI\_AD16  
PCI\_AD16 1 1394 IDSEL  
R194 1394@100\_0402\_5%

- (18,26,31,32) PCI\_CBE#3
- (18,26,31,32) PCI\_CBE#2
- (18,26,31,32) PCI\_CBE#1
- (18,26,31,32) PCI\_CBE#0
- (18,26,31,32) PCI\_STOP#
- (18,26,31,32) PCI\_PERR#
- (18,26,31,32) PCI\_PAR
- (18,32) PCI\_PIRQE#
- (18,26,31,32,34) PCI\_RST#
- (18) CLK\_PCI\_1394
- (18) PCI\_GNT#0
- (18) PCI\_REQ#0
- (18,26,31,32) PCI\_IRDY#
- (18,26,31,32) PCI\_TRDY#
- (18,26,31,32) PCI\_DEVSEL#
- (18,26,31,32) PCI\_FRAME#



**VT6311S**

EEPROM

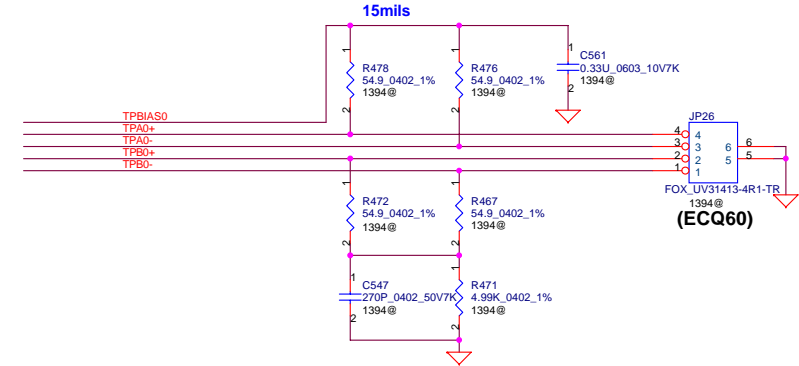
others

OSCILLATOR

PHY PORT0

PHY PORT1

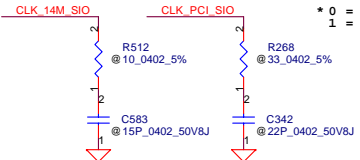
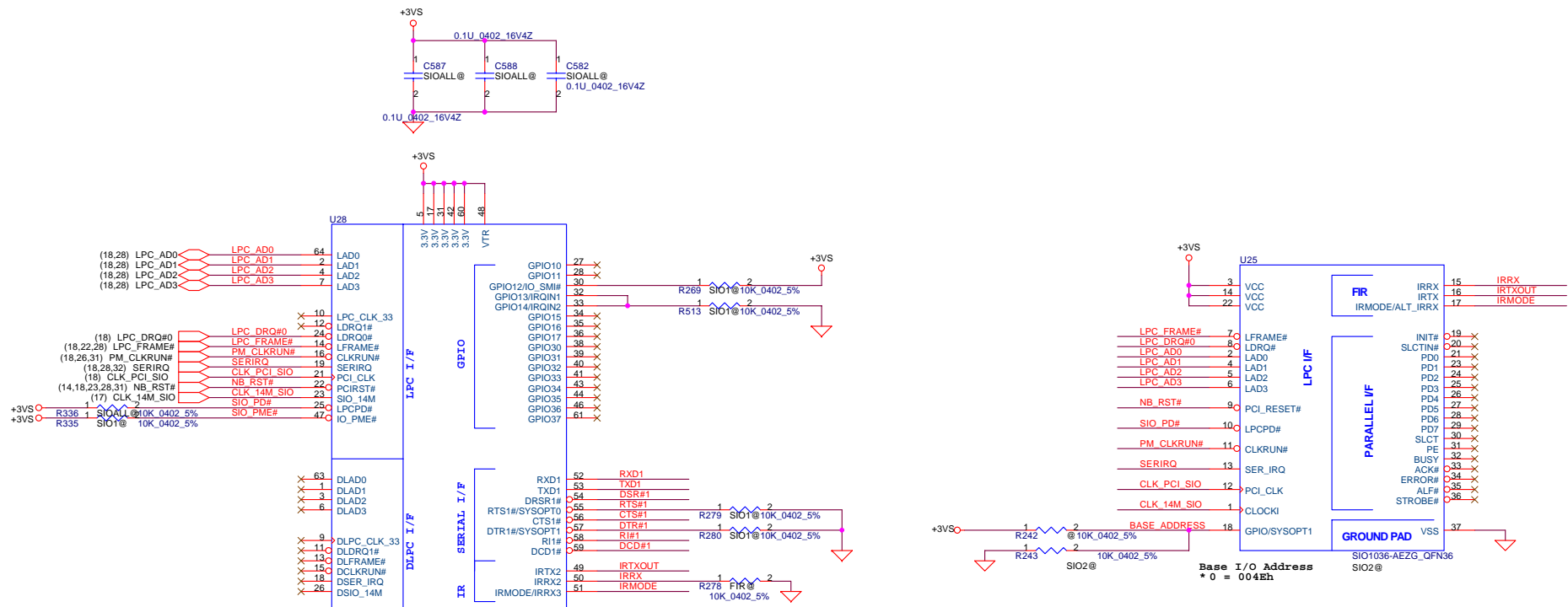
VIA 1394 with Sn-Bi part : SA00000P510



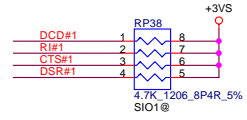
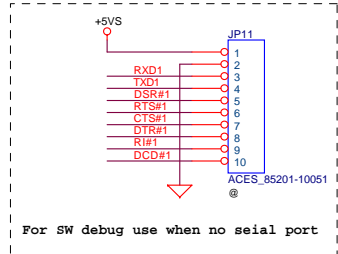
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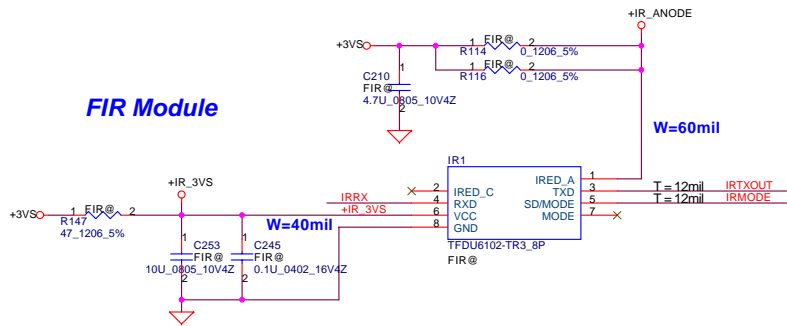
# SUPER I/O SMsC LPC47N207



Place on the BOT side (near MINIPCI conn.)

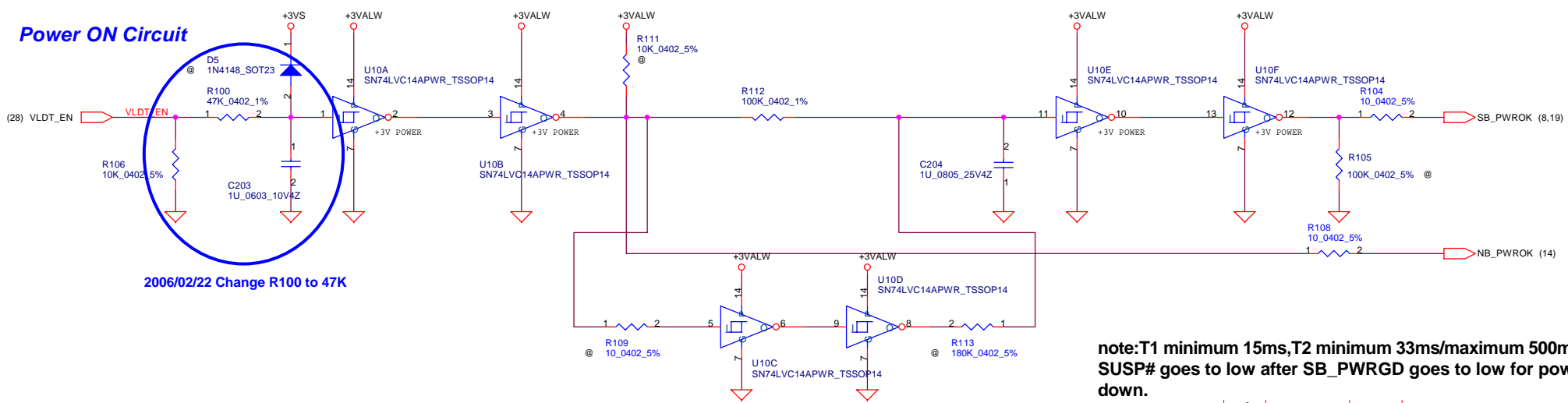


## FIR Module

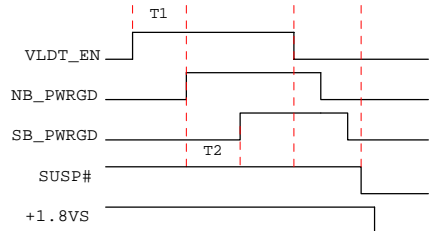


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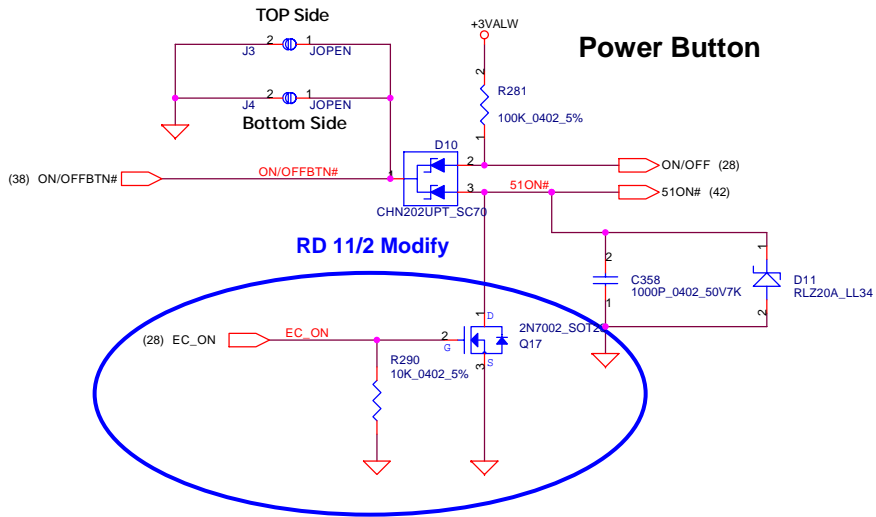
**Power ON Circuit**



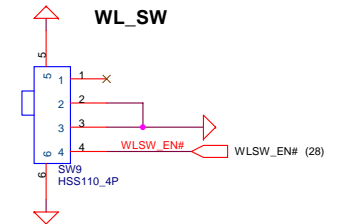
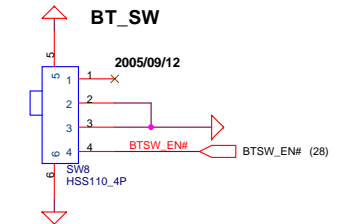
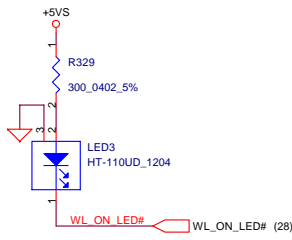
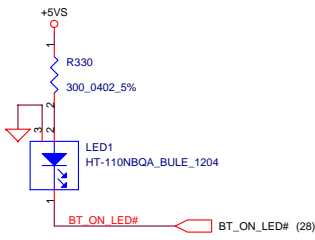
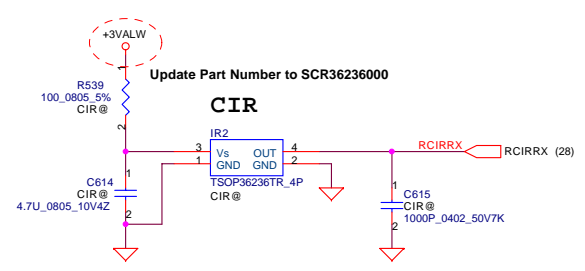
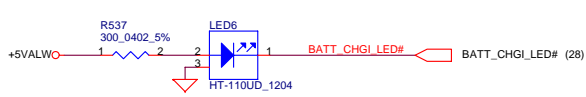
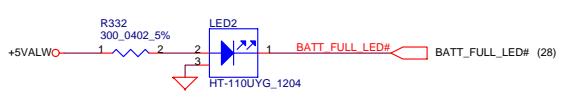
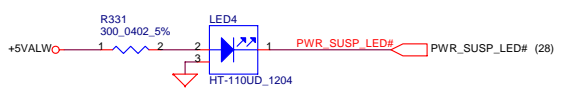
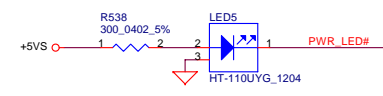
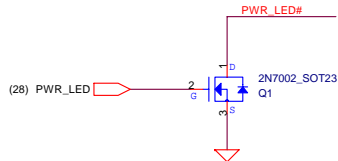
**note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB\_PWRGD goes to low for power down.**



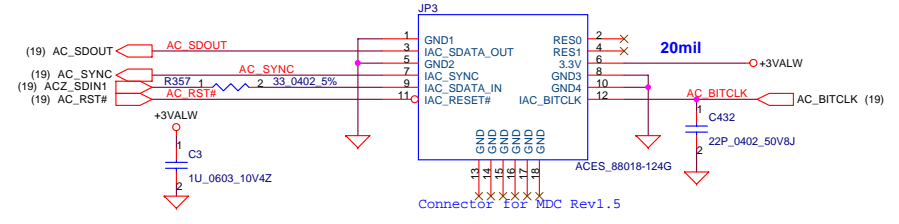
**Power Button**



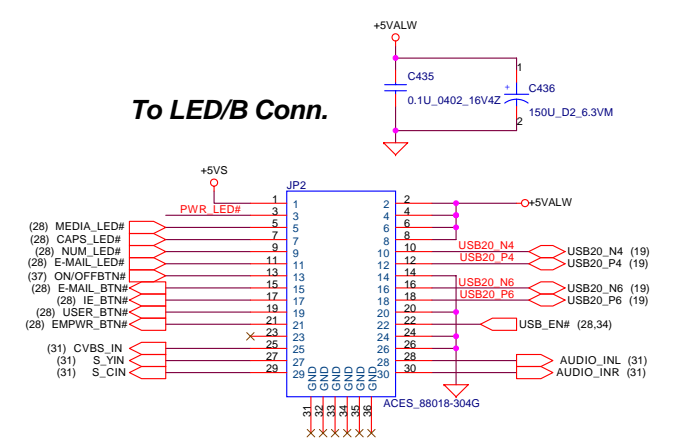
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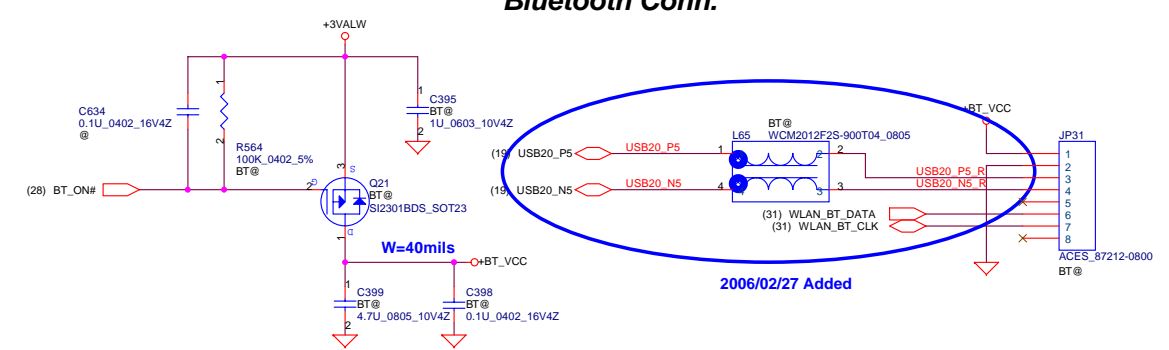
### MDC Conn.



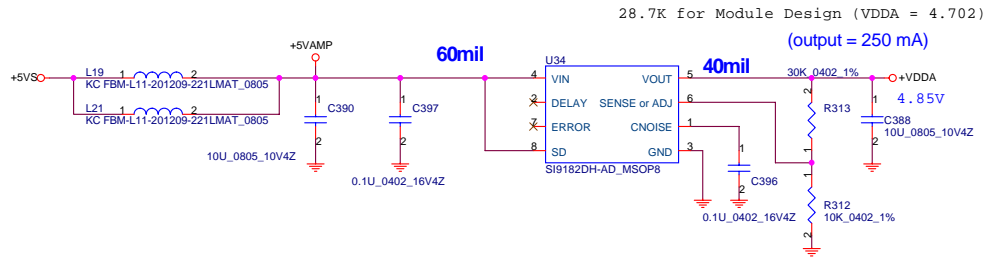
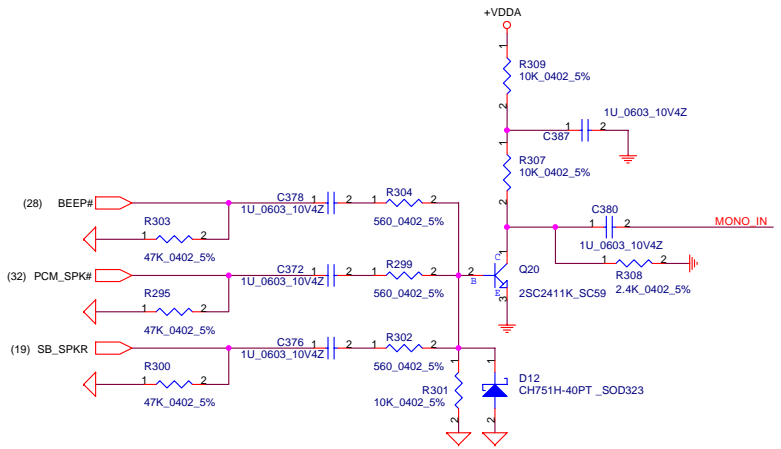
### To LED/B Conn.



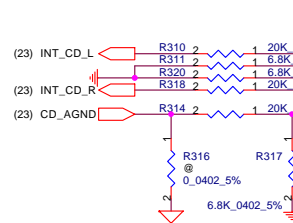
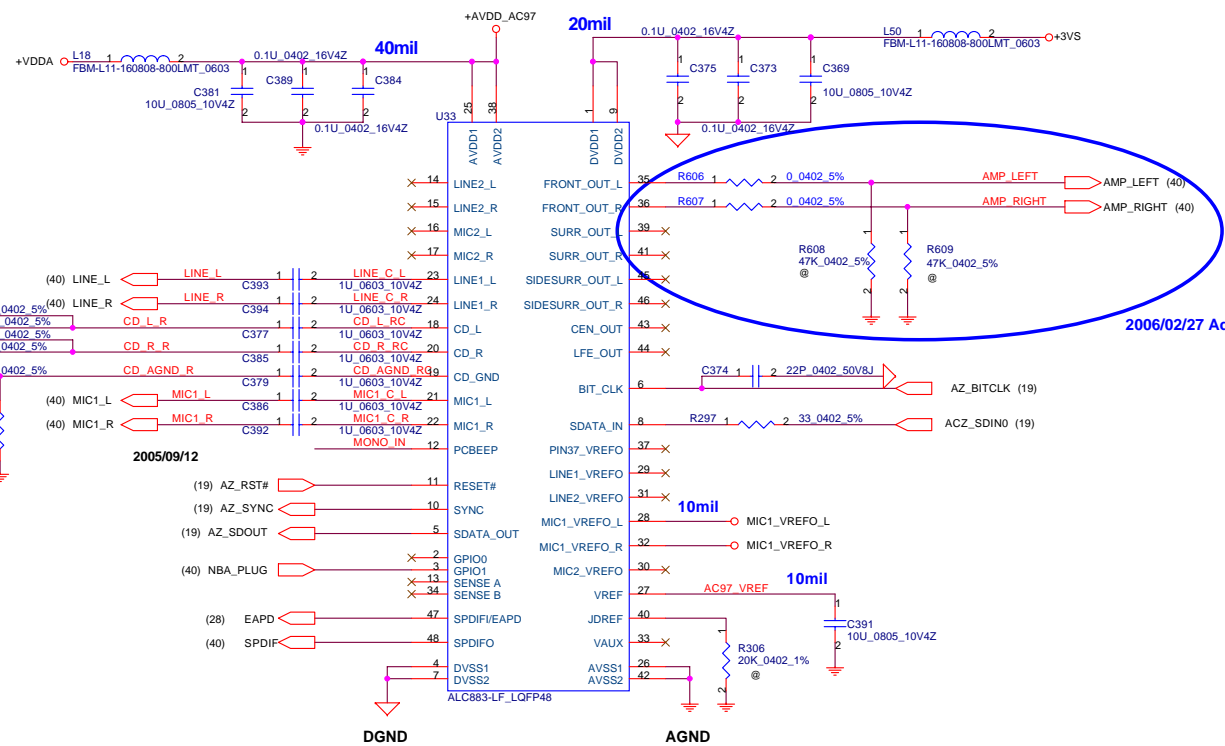
### Bluetooth Conn.



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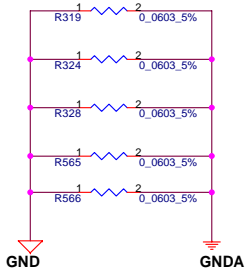


### HD Audio Codec



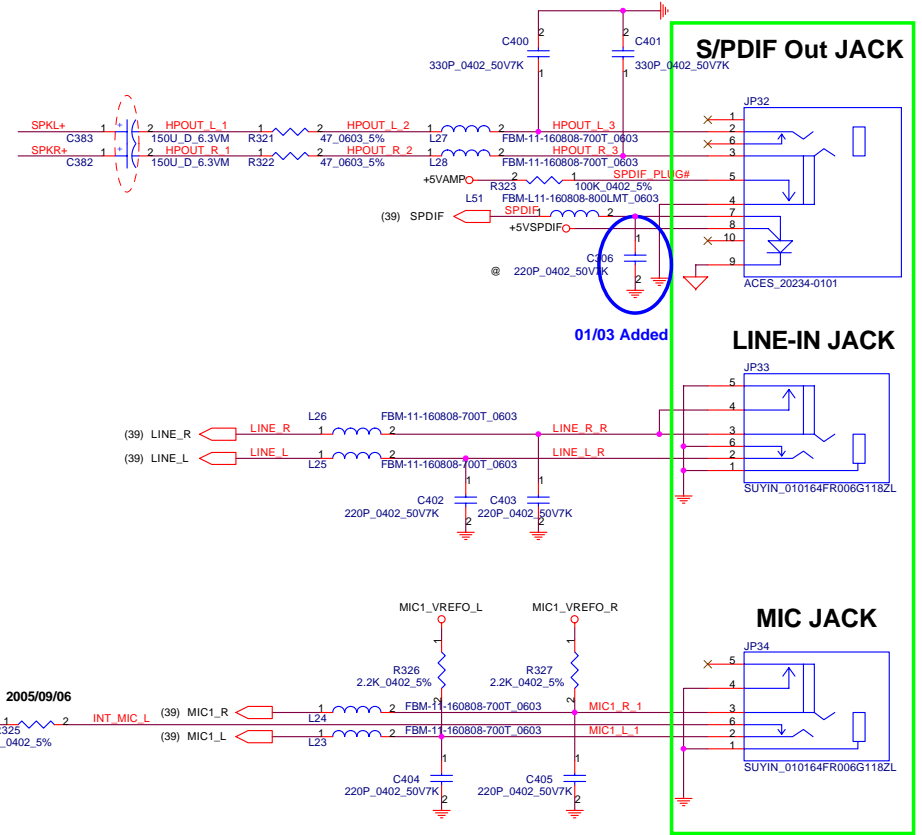
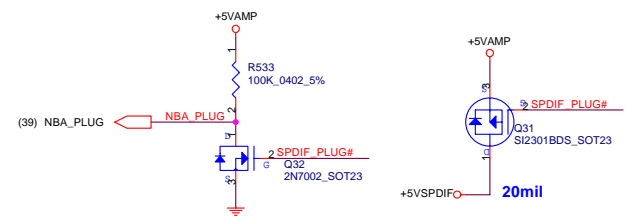
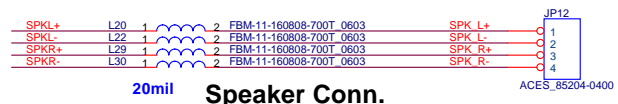
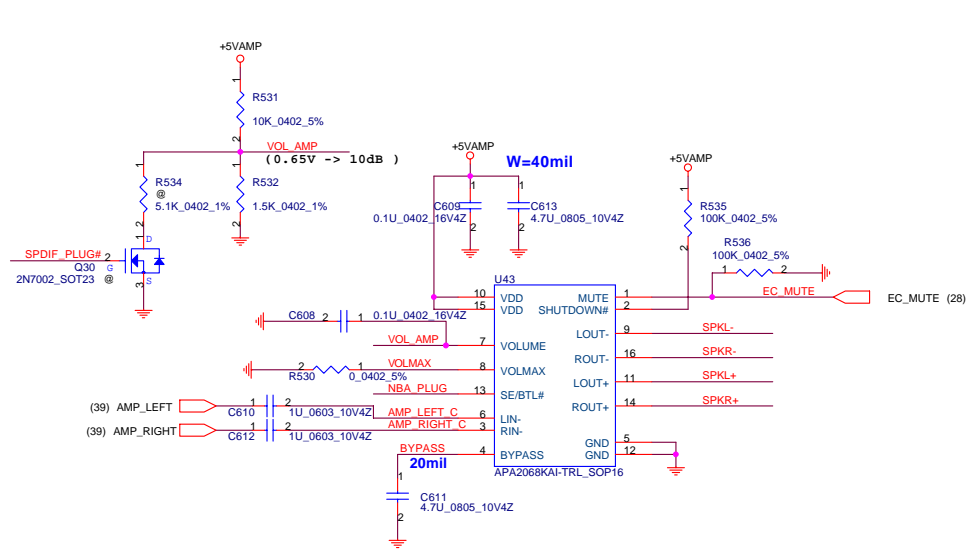
2005/09/12

2006/02/27 Added

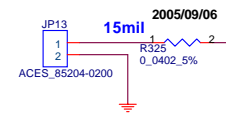


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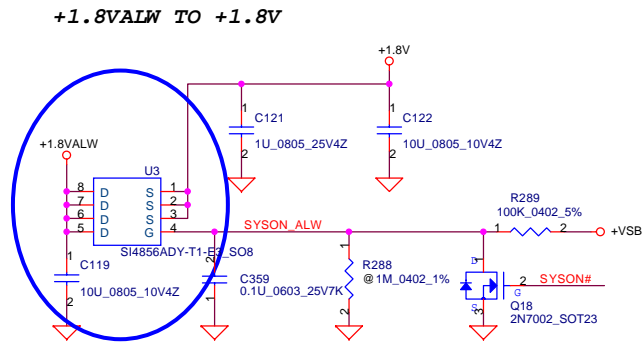
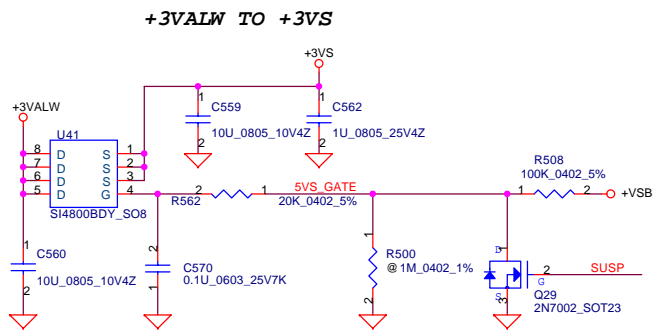
**Int MIC Conn.**



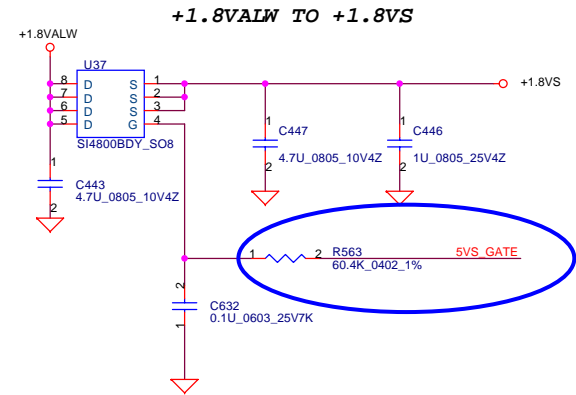
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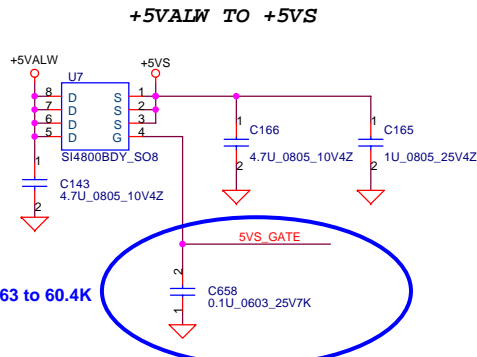




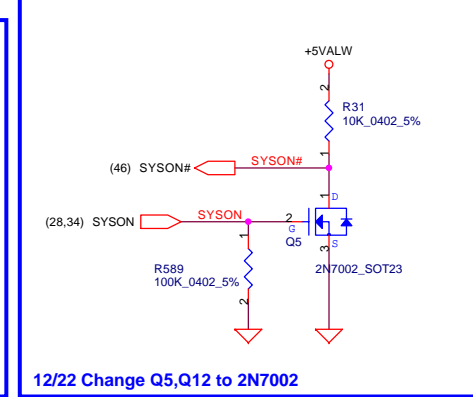
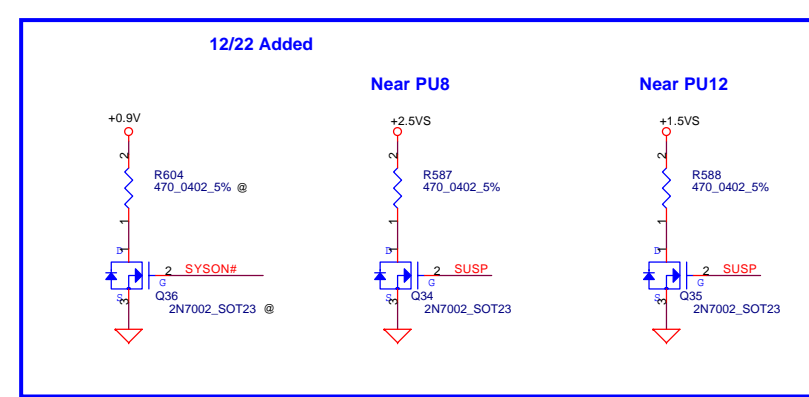
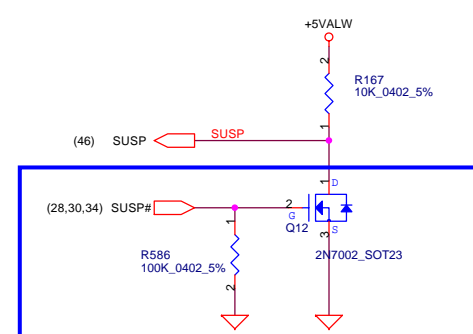
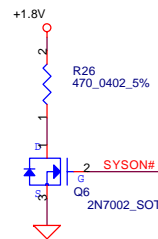
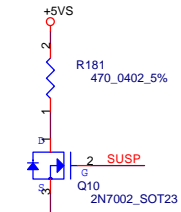
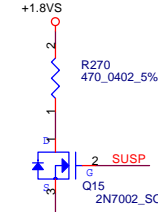
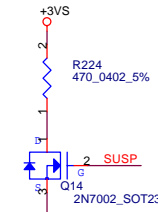
12/30 Change U3 to SI4856ADY



12/30 Change R563 to 60.4K

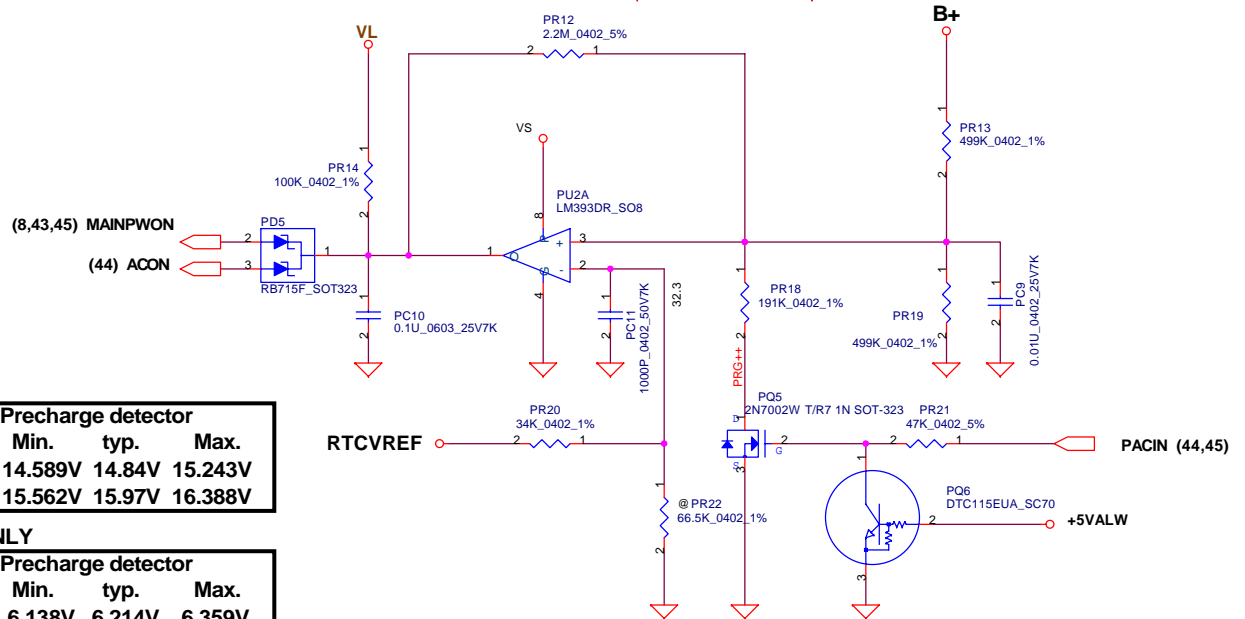
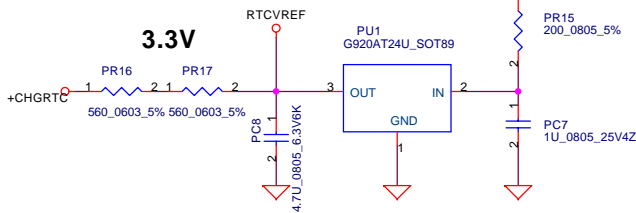
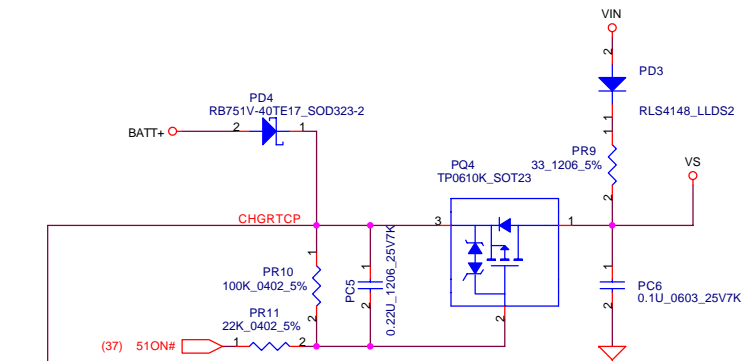
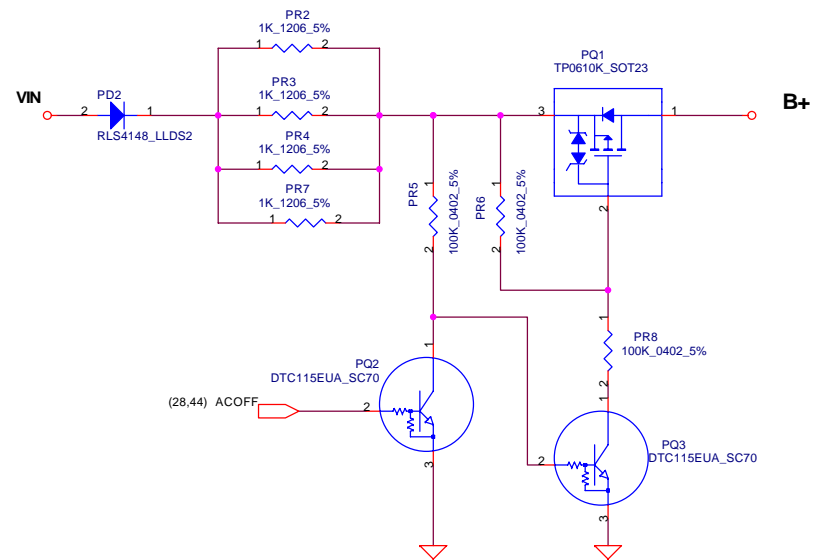
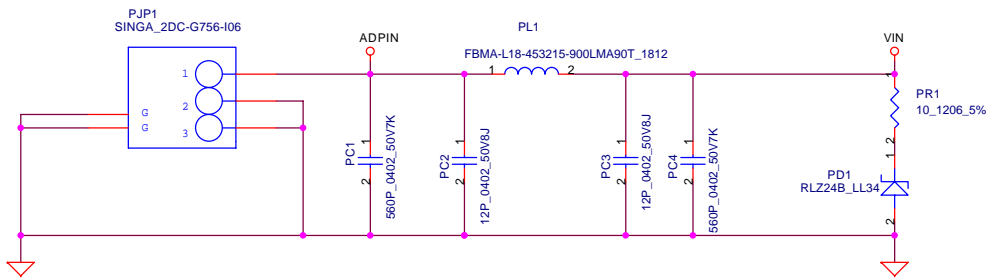


2006/2/22 Add C658 0.1uF  
2006/4/13 modify package for lead-free part



12/22 Change Q5,Q12 to 2N7002

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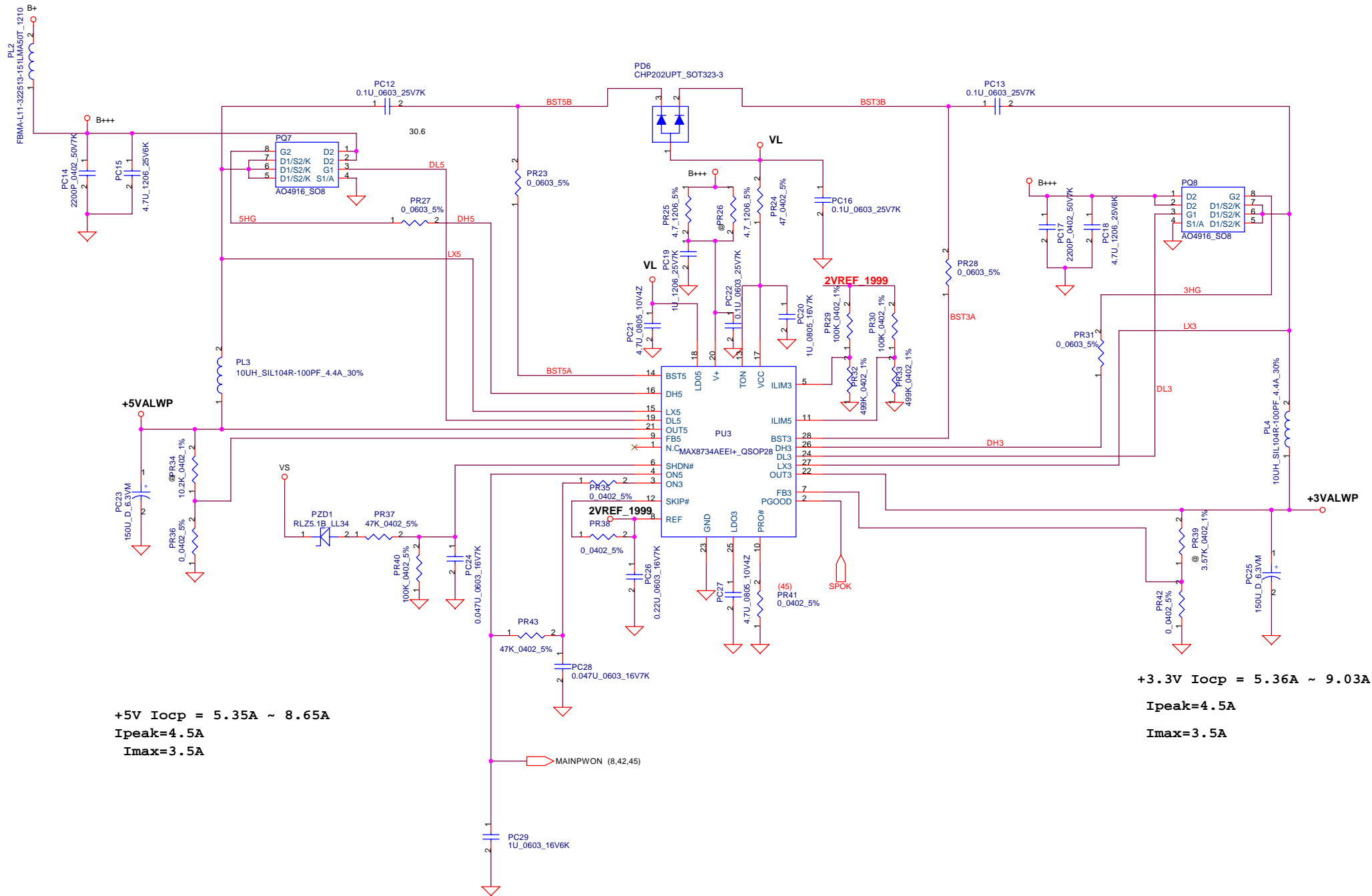


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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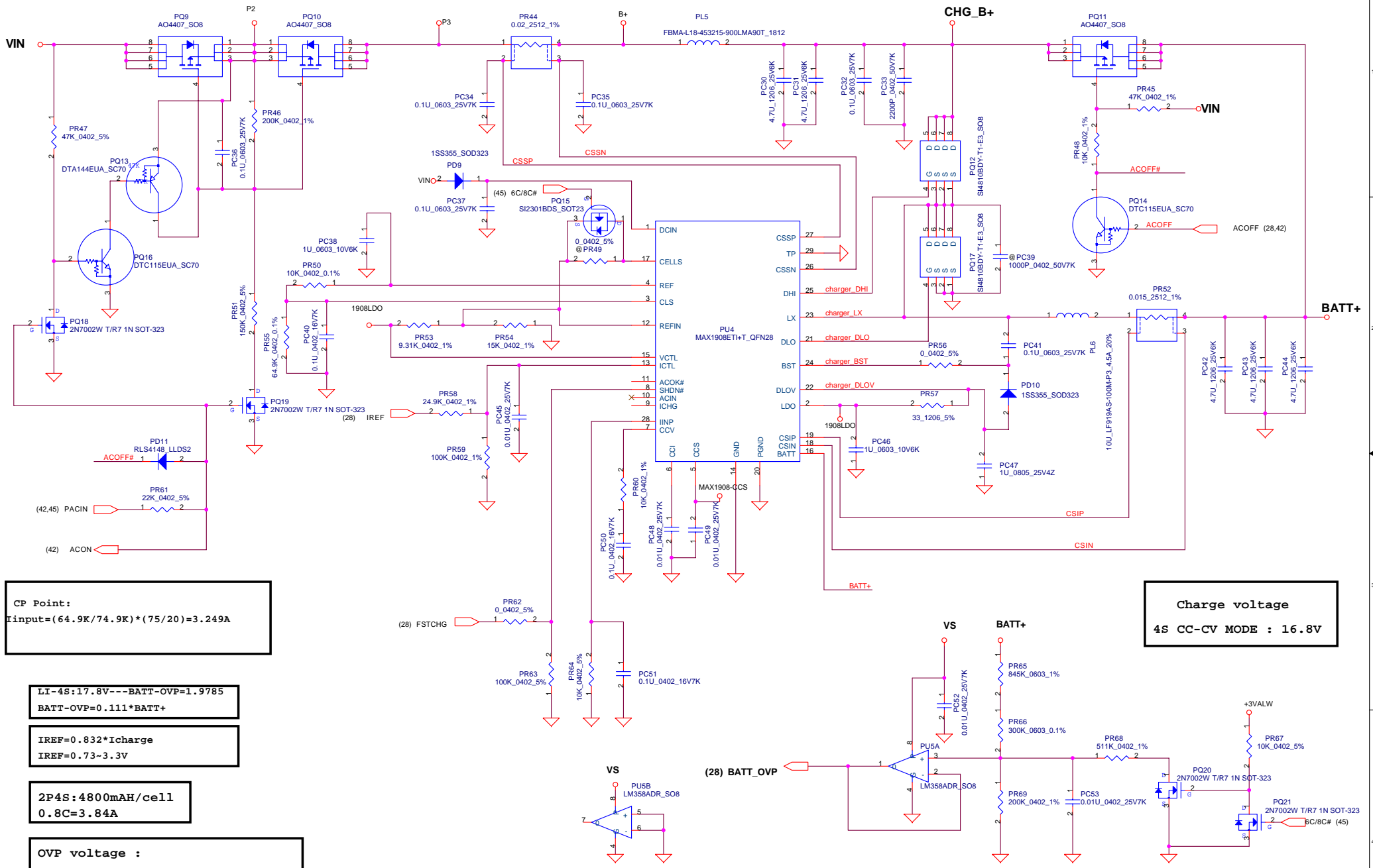


**+5V Iocp = 5.35A ~ 8.65A**  
**Ipeak=4.5A**  
**Imax=3.5A**

**+3.3V Iocp = 5.36A ~ 9.03A**  
**Ipeak=4.5A**  
**Imax=3.5A**

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I<sub>adp</sub>=0~3.25A(65W)



CP Point:  
 $I_{in} = (64.9K / 74.9K) * (75 / 20) = 3.249A$

LI-4S: 17.8V --- BATT-OVP = 1.9785  
 BATT-OVP = 0.111 \* BATT+

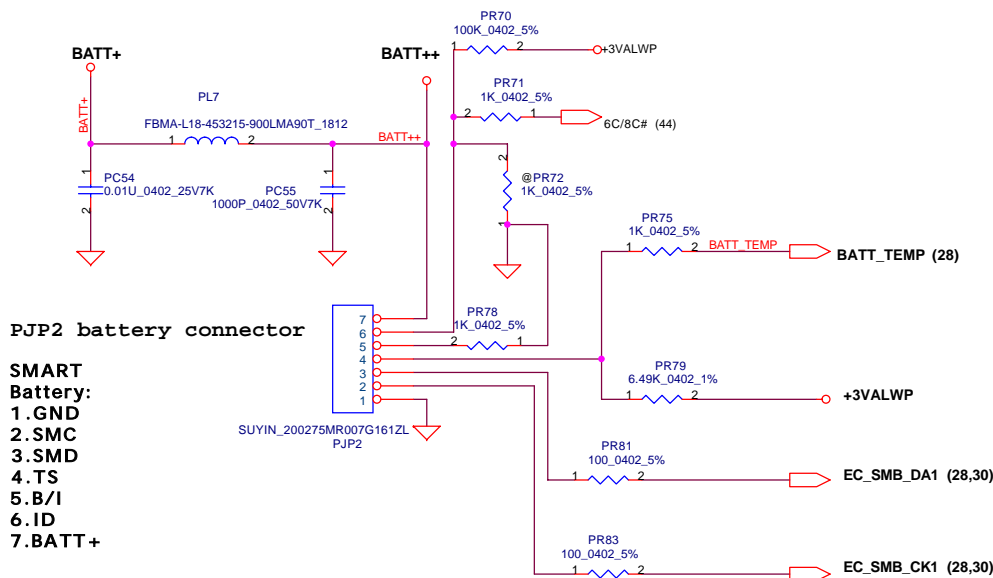
IREF = 0.832 \* Icharge  
 IREF = 0.73 ~ 3.3V

2P4S: 4800mAh/cell  
 0.8C = 3.84A

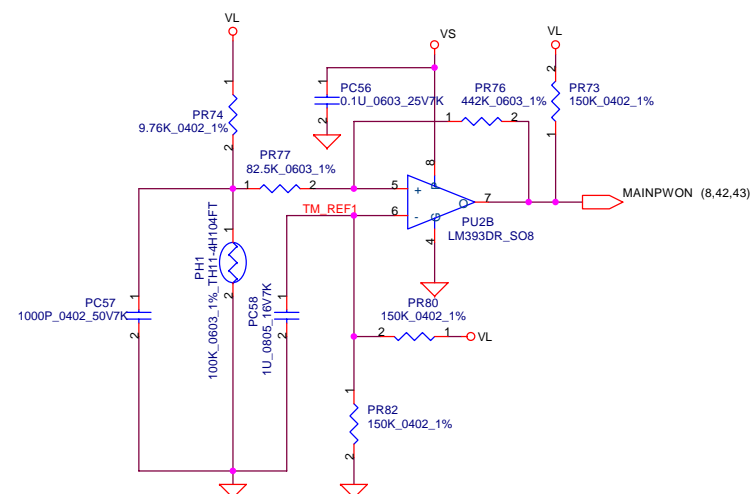
OVP voltage :  
 LI-3S : 17.8V --- BATT-OVP = 1.9758V  
 BATT-OVP = 0.111 \* BATT+

Charge voltage  
 4S CC-CV MODE : 16.8V

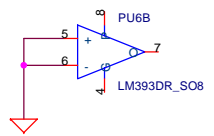
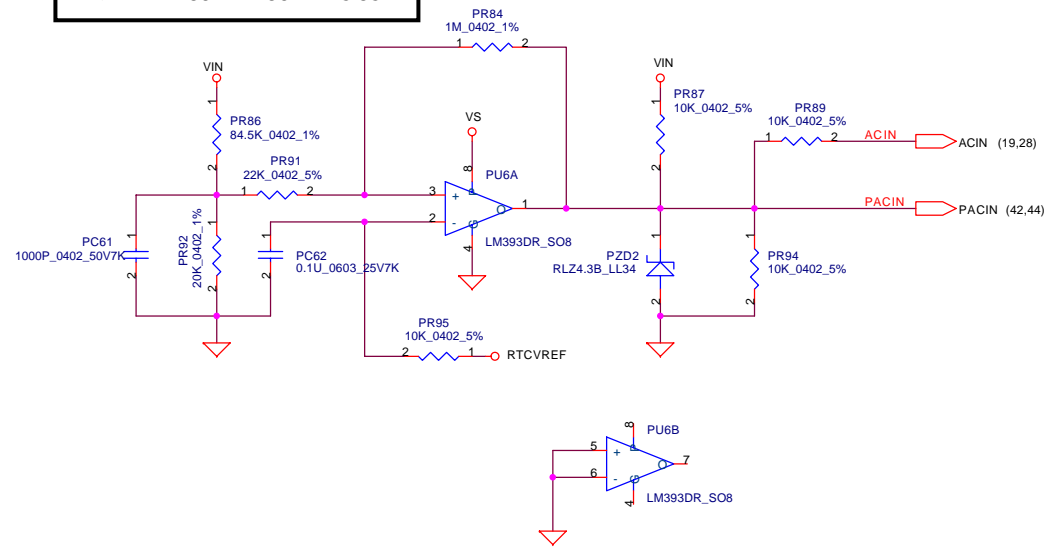
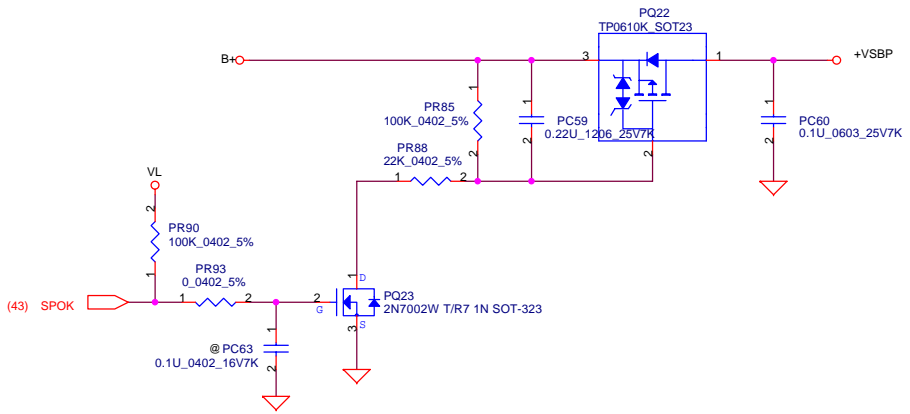
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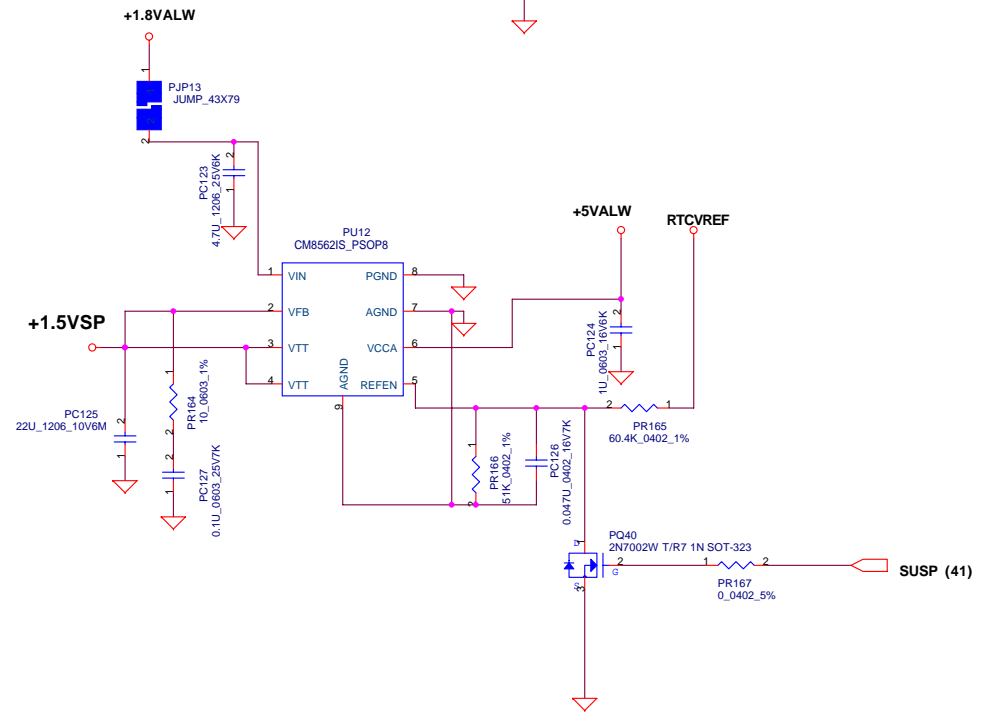
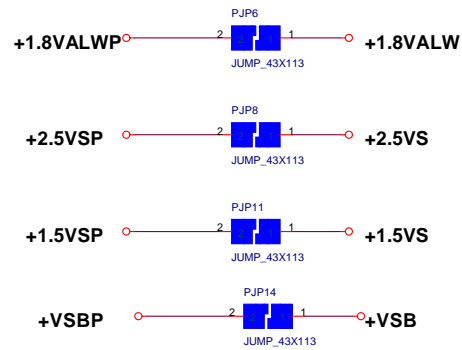
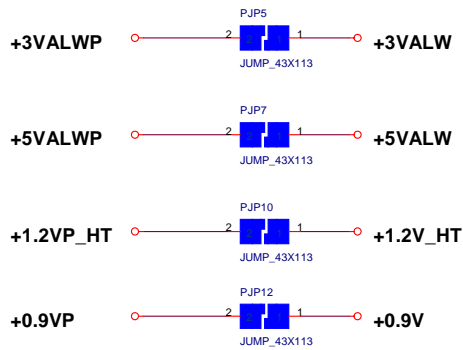
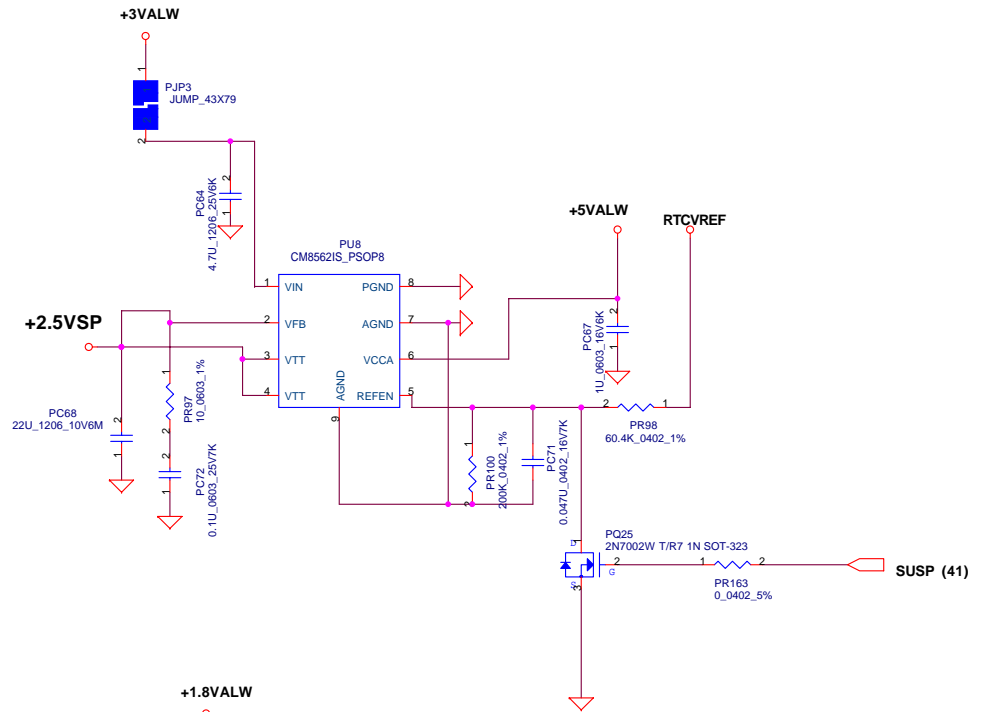
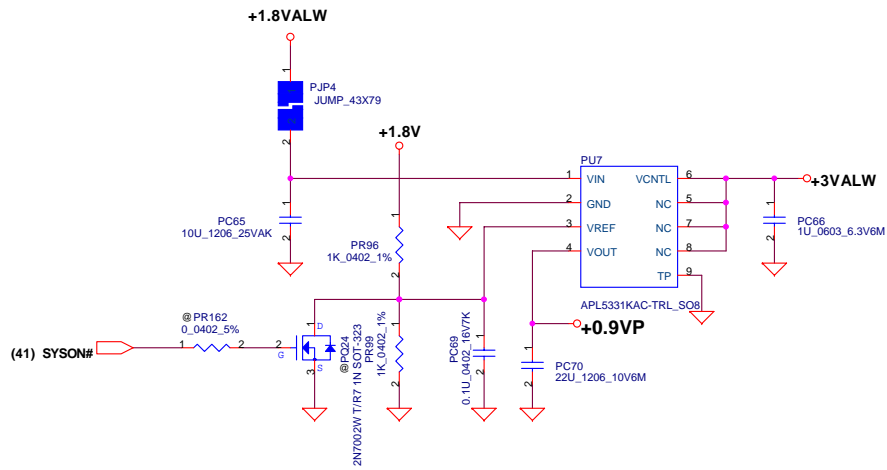
PH1 under CPU bottom side :  
 CPU thermal protection at 90 degree C  
 Recovery at 70 degree C



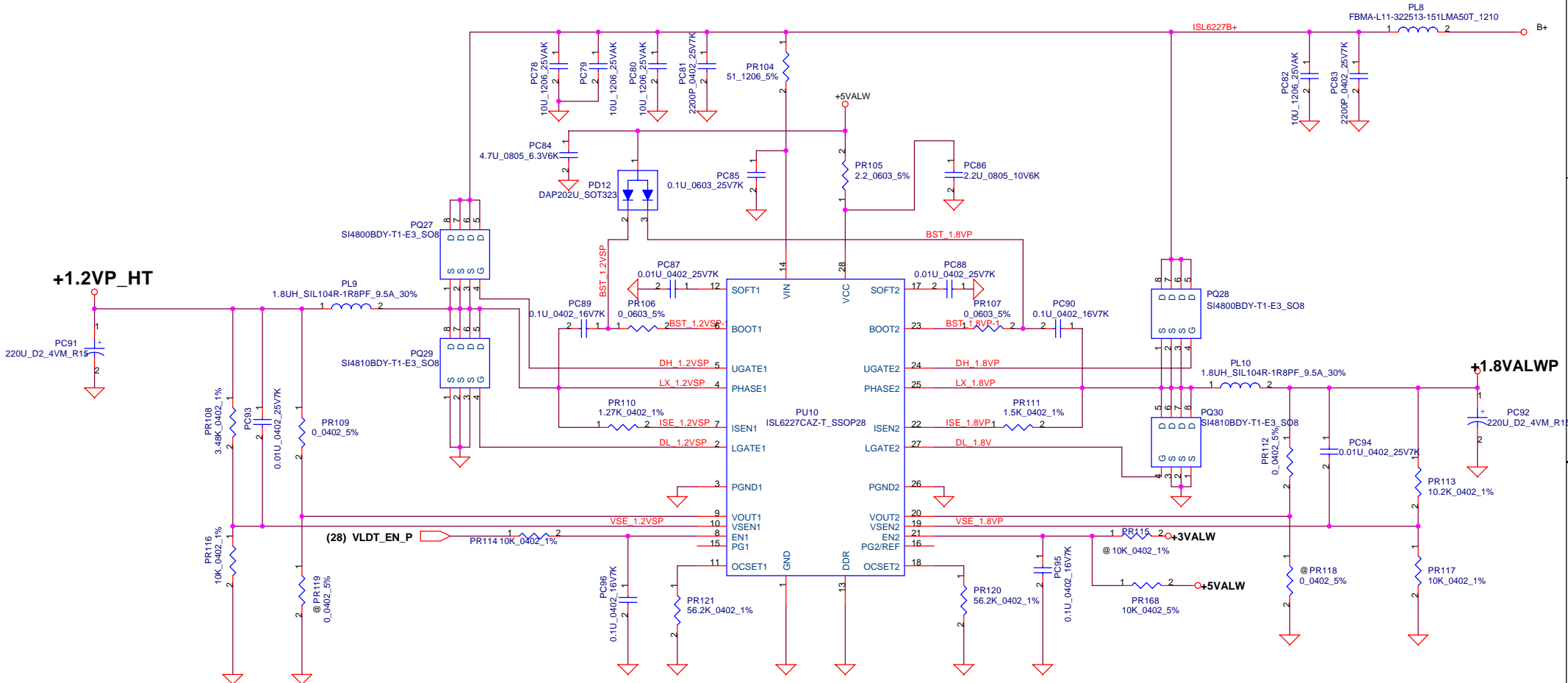
**Vin Detector**  
 Min. typ. Max.  
 H->L 16.976V 17.257V 17.728V  
 L->H 17.430V 17.901V 18.384V



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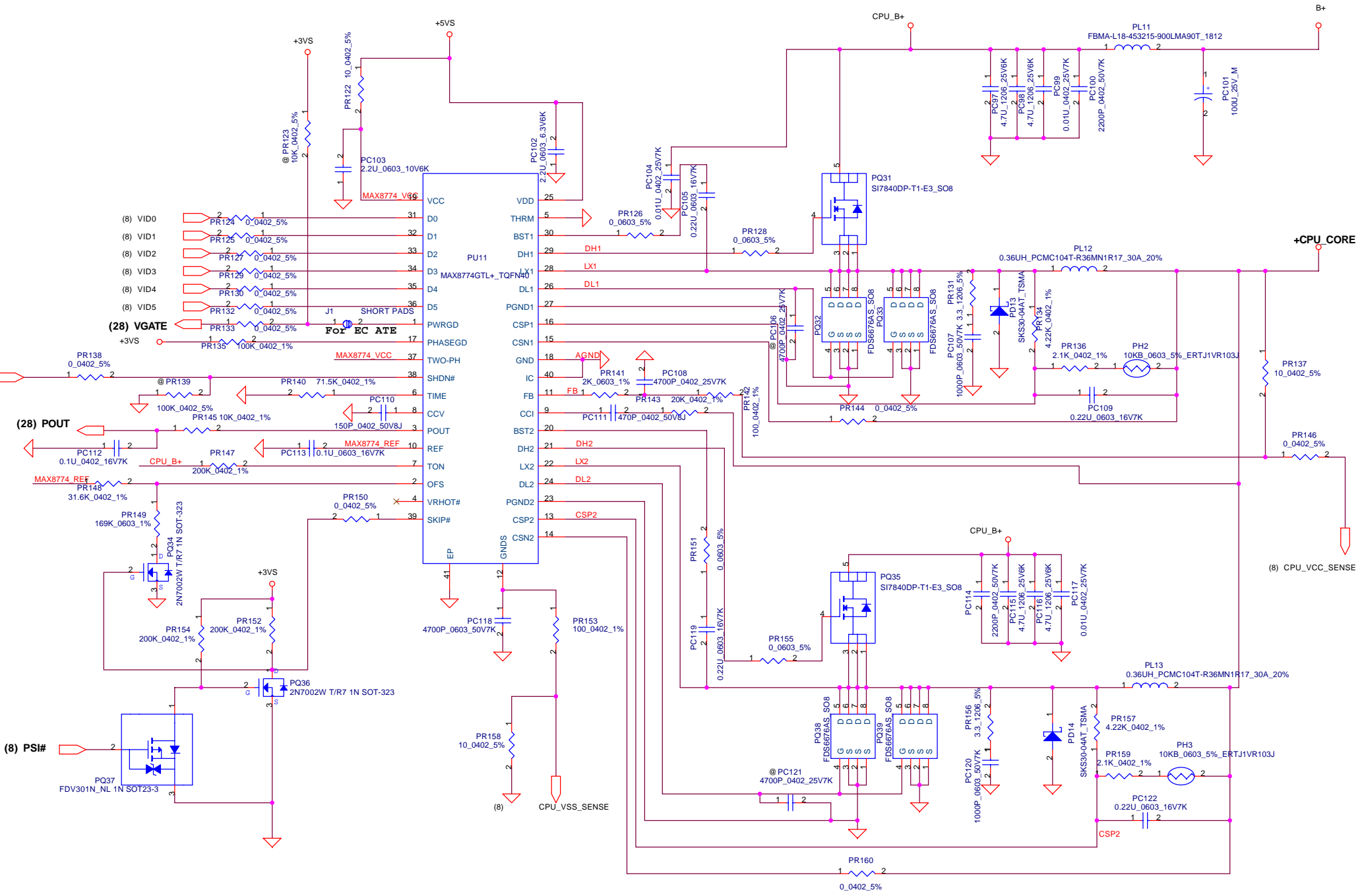
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$I_{peak} = 6.47A$ ,  $I_{max} = 6.47 * 0.7 = 4.53A$   
 $I_{ocpmin} = 7.79A$   
 $I_{ocpmax} = 11.83A$

$I_{peak} = 8.5A$ ,  $I_{max} = 6A$   
 $I_{ocpmin} = 8.76A$   
 $I_{ocpmax} = 13.46A$

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1	Schematic update.	Because schematic update, we don't need this two parts.	0.1	46	Delete PQ24 SB000005M10.	0.1	EVT
2	Schematic update.	Because schematic update, we don't need this two parts.	0.1	46	Delete PR162 SD028000080.	0.1	EVT
3	BOM error	BOM error	0.1	44	Change PQ15 from SB923010010 to SB923010020.	0.1	EVT
4	BOM error	BOM error	0.1	48	Change PQ37 from SB503010004 to SB503010010	0.1	EVT
5	MOSFET thermal issue	Because we need to reduce MOSFET teperature of high side mos.	0.1	48	Change PQ31 and PQ35 from SB562940000 to SB578400080.	0.1	EVT
6	BOM error	BOM error	0.1	42	Change PL1,PL5,PL7 and PL11 form SM010018210 to SM010020720.	0.1	EVT
7	BOM error	BOM error	0.1	47	Change PR121 from SD000001500 to SD000001580.	0.1	EVT
8	BOM error	BOM error	0.1	48	Change PR149 from SD014169300 to SD014169380.	0.1	EVT
9	BOM error	BOM error	0.1	44	Change PR55 from SD034100380 to SD034100280.	0.1	EVT
10	BOM error	BOM error	0.1	44	Change PR50 from SD034576280 to SD034140280.	0.1	EVT
11	BOM error	BOM error	0.1	48	Change PR148 from SD034316200 to SD034316280.	0.1	EVT
12	BOM error	BOM error	0.1	44	Change PC52,PC53,PC54,PC87,PC88,PC93 and PC94 from SE075103Z00 to SE075103K80.	0.1	EVT
13	BOM error	BOM error	0.1	46	Change PC70 from SE153106K80 to SE116226M80.	0.1	EVT
14	High limit issue.	Because the high is limited, we need to reduce space.	0.1	48	Change PC101 from SF22004M210 to SF10004M080.	0.1	EVT
15	BOM error	BOM error	0.1	48	Add PR137 and PR158 SD028100A80.	0.1	EVT
16	Power sequence adjust.	Power sequence adjust.	0.1	47	Add PR168 SD034100280.	0.1	EVT
17	Power sequence adjust.	Power sequence adjust.	0.1	47	Delete PR115 SD034100280.	0.1	EVT
18	BOM cost issue.	BOM cost issue.	0.1	42	Change PQ5,PQ18,PQ19,PQ20,PQ21,PQ23,PQ25,PQ34,PQ36,PQ40 from SB000005M10 to SB000006800.	0.1	EVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1	Charger accuracy issue.	Increase charger accuracy to meet customer request.	0.2	44	Change PR44 from SE000001E00 to SE000001F00.	0.1	EVT
2	Charger accuracy issue.	Increase charger accuracy to meet customer request.	0.2	44	Change PR50 form SD034140280 to SD000008B00.	0.1	EVT
3	Charger accuracy issue.	Increase charger accuracy to meet customer request.	0.2	44	Change PR55 from SD034100280 to SD000000CL80.	0.1	EVT
4	Improve IC risk.	Improve IC risk.	0.2	44	Change PR60 from SD034100180 to SD034100280.	0.1	EVT
5	Improve OCP point.	Improve OCP point.	0.3	43	Change PR29 and PR30 from SD034200380 to SD034100380	0.1	EVT
6	Improve OCP point.	Improve OCP point.	0.3	47	Change PR120 from SD034499280 to SD000001580.	0.1	EVT
7	Improve ripple voltage.	Improve ripple voltage.	0.4	46	Change PC68 and PC125 from SE142475K80 to SE116226M80.	0.2	DVT
8	Incesr +1.2VP_HT voltage.	Incesr +1.2VP_HT voltage.	0.4	47	Change PR108 from SD034340180 to SH034348180.	0.2	DVT
9	Incesr +1.8VALWP voltage.	Incesr +1.8VALWP voltage.	0.4	47	Change PR113 from SD034100280 to SD028102280.	0.2	DVT
10	Improve thermal issue.	Improve thermal issue.	0.4	48	Change PQ32, PQ33, 38, PQ39 from SB000003W00 to SB578320010	0.2	DVT
11	Improve thermal issue.	Improve thermal issue.	0.4	48	Change PL12, PL13 from SH12056BM00 to SH000005680.	0.2	DVT
12	Improve +CPU_CORE OCP point.	Improve +CPU_CORE OCP point.	0.4	48	Change PR134, PR157 from SD034150280 to SD034422180	0.2	DVT
13	Improve +CPU_CORE OCP point.	Improve +CPU_CORE OCP point.	0.4	48	Change PR136 and PR159 from SD034150280 to SH034210180.	0.2	DVT
14	Improve +CPU_CORE OCP point.	Improve +CPU_CORE OCP point.	0.4	48	Change PC109 and PC122 from SE042333K80 to SE026224K80	0.2	DVT
15	Improve CPU load line	Improve CPU load line	0.4	48	Change PR141 from SD014255180 to SD014200180	0.2	DVT
16	Improve CPU load line	Improve CPU load line	0.4	48	Change PR142 and PR153 from SD034100A80 to SD034100080.	0.2	DVT
17							
18							

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Item	Fixed Issue	PG#	Modify List	VER	Phase
1	ATI Reccommand.	13	Change R376 82.5 ohm to 100 ohm.	0.2	DVT
2	TV-OUT 阻抗匹配.	14	Increase R590,R591,R592 150 ohm pull down resister.	0.2	DVT
3	解決PCI_RST# 漏電問題.	18	Change U15,U16 voltage source +3VS to +3VALW.	0.2	DVT
4	Fixed USB2.0 EYE Diagram .	19	Change R164 11.8K ohm to 11.3K ohm.	0.2	DVT
5	IMPROVE TV-OUT SIGNAL QUALITY.	24	Change C417,C418,C419,C425,C428,C430 to 220P.	0.2	DVT
6	SB_INT_FLASH_SEL# 改為EC可以控制.	28	Add R594.	0.2	DVT
7	解 M插AC電源, LED會閃一下的問題.	41	Add R586,R589,Q5,Q12 change to 2N7002.	0.2	DVT
8	增加+1.5VS, +2.5VS, +0.9V 放電線路.	41	Add R587,Q34(+2.5VS),R588,Q35(+1.5VS),R604,Q36(+0.9V).	0.2	DVT
9	1w窗.	41	Add C658 0.1uF	0.3	PVT
10	Sometimes run S3 test program will interrupt .	37	Change R100 to 47K(ori : 100K)	0.3	PVT
11	改 ?+2.5V_LAN Power.	26	C281 change to 10uF	0.3	PVT
12	改善 LAN 訊號品質 ?	27	Change R387,R390,R391,R395,C494,C500 placement to near Transformer.	0.3	PVT
13	減少 Speaker 訊號增益(預留).	39	Add R606(0 ohm),R607(0 ohm),R608(47K未上),R609(47K未上)	0.3	PVT
14	Add Camera Connect.	31	Add R605,C657,JP35	0.3	PVT
15	Bluetooth 加 chock.	38	Add L65	0.3	PVT
16	For EMI request	15	Add C330	0.4	PVT2
17	JP25 5-in-1 connector Spec update (Pin18 from NC to SD-GND)	33	Add R610	0.4	PVT2
18	Modify Package for Lead-free part	41	Modify C658 package from 0402 to 0603	0.4	PVT2
19	Reserve	28	Add R611, R612, EC_Pin-100	1.0	MP
20	for solve MS detect issue	33	Remove C197	1.0	MP

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