SECTION 9.2: PC BOARD DESIGN ISSUES

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Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Comprised of a sandwich of insulating layer (or layers) and one or more copper conductor patterns, they can introduce various forms of errors into a circuit, particularly if the circuit is operating at either high precision or high speed. PCBs then, act as "unseen" components, wherever they are used in precision circuit designs. Since designers don't always consider the PCB electrical characteristics as additional components of their circuit, overall performance can easily end up worse than predicted. This general topic, manifested in many forms, is the focus of this section.

PCB effects that are harmful to precision circuit performance include leakage resistances; spurious voltage drops in trace foils, vias, and ground planes; the influence of stray capacitance, dielectric absorption (DA), and the related "hook." In addition, the tendency of PCBs to absorb atmospheric moisture, *hygroscopicity,* means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories— those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog designs, and it can be said that implementing a PCB based circuit doesn't change that fact. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB based analog designs, and an appreciable amount of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques enables control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. This topic is the subject of many application calls, and it is certainly true that interfacing with ADCs (or DACs) is a major part of the system design, and thus it shouldn't be overlooked. Indeed, the single issue of quality grounding can drive the entire layout philosophy of a high performance mixed signal PCB design— as it well should.

Resistance of Conductors

Every engineer is familiar with resistors, although perhaps fewer are aware of their idiosyncrasies, as generally covered in Section 9.1. But far too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors. In higher precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is *not* a superconductor—and too many engineers appear to think it is!

Figure 9.16 illustrates a method of calculating the sheet resistance R of a copper square, given the length Z, the width X, and the thickness Y.

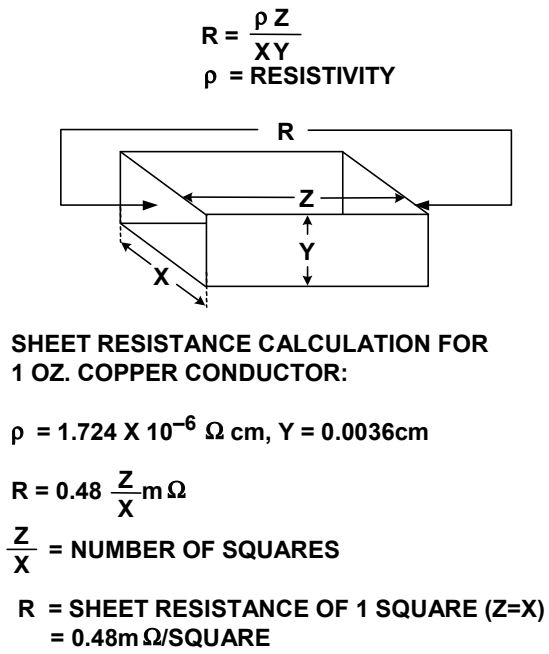


Figure 9.16: *Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors*

At 25°C the resistivity of pure copper is 1.724×10^{-6} Ωcm. The thickness of standard 1 ounce PCB copper foil is 0.036 mm (0.0014"). Using the relations shown, the resistance of such a standard copper element is therefore 0.48 mΩ /square. One can readily calculate the resistance of a linear trace, by effectively "stacking" a series of such squares end-end, to make up the line's length. The line length is Z and the width is X, so the line resistance R is simply a product of Z/X and the resistance of a single square, as noted in the figure.

For a given copper weight and trace width, a resistance/length calculation can be made. For example, the 0.25-mm (10-mil) wide traces frequently used in PCB designs equates to a resistance/length of about 19 mΩ/cm (48 mΩ /inch), which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4% /°C around room temperature. This is a factor that shouldn't be ignored, in particular within low impedance precision circuits, where the TC can shift the net impedance over temperature.

As shown in Figure 9.17, PCB trace resistance can be a serious error when conditions aren't favorable. Consider a 16-bit ADC with a 5-kΩ input resistance, driven through 5 cm of 0.25-mm wide 1-oz PCB track between it and its signal source. The track resistance of nearly 0.1 Ω forms a divider with the 5-kΩ load, creating an error. The resulting voltage drop is a gain error of 0.1/5000 (~0.0019%), well over 1 LSB (0.0015% for 16 bits).

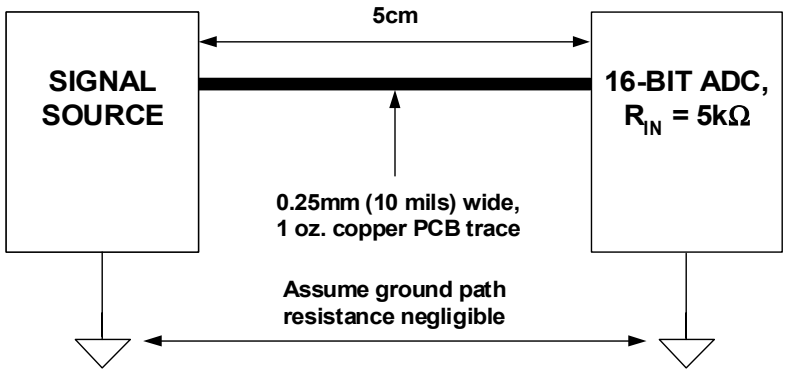


Figure 9.17: *Ohm's Law Predicts >1 LSB of Error due to Drop In PCB Conductor*

So, when dealing with precision circuits, the point is made that even simple design items such as PCB trace resistance cannot be dealt with casually. There are various solutions that can address this issue, such as wider traces (which may take up excessive space), the use of heavier copper (which may be too expensive), or simply choosing a high impedance converter. But, the most important thing is to think it all through, avoiding any tendency to overlook items appearing innocuous on the surface.

Voltage Drop in Signal Leads—"Kelvin" Feedback

The gain error resulting from resistive voltage drop in PCB signal leads is important only with high precision and/or at high resolutions (the Figure 9.17 example), or where large signal currents flow. Where load impedance is constant and resistive, adjusting overall system gain can compensate for the error. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback, as shown in Figure 9.18.

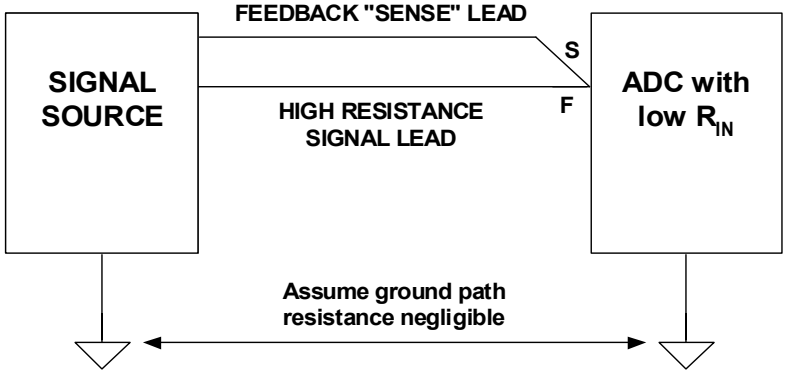


Figure 9.18: *Use of a Sense Connection Moves Accuracy to the Load Point*

In this modification to the case of Figure 9.17, a long resistive PCB trace is still used to drive the input of a high resolution ADC, with low input impedance. In this case however, the voltage drop in the signal lead does *not* give rise to an error, as feedback is taken directly from the input pin of the ADC, and returned to the driving source. This scheme allows full accuracy to be achieved in the signal presented to the ADC, despite any voltage drop across the signal trace.

The use of separate force (F) and sense (S) connections at the load removes any errors resulting from voltage drops in the force lead, but, of course, may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point. Also, in this much-simplified system, errors in the common lead source/load path are ignored, the assumption being that ground path voltages are negligible. In many systems this may not necessarily be the case, and additional steps may be needed, as noted below.

Signal Return Currents

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit, as is illustrated in Figure 9.19 (see References 7 and 8).

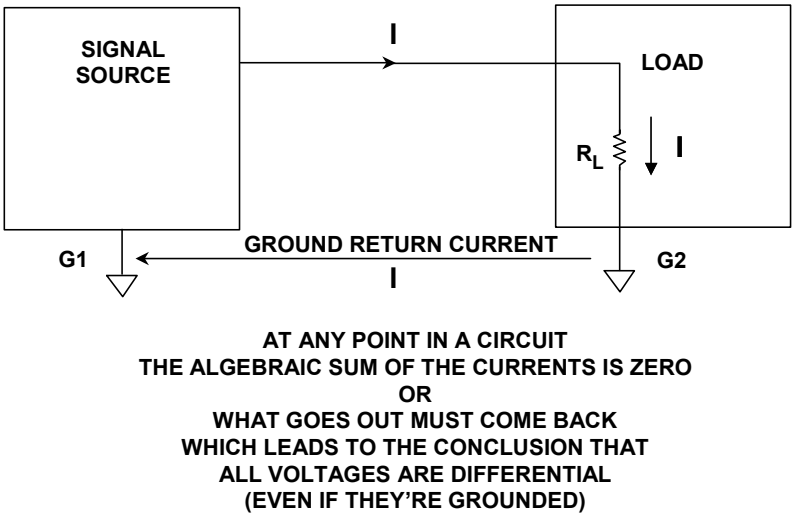


Figure 9.19: *Kirchoff's Law Helps in Analyzing Voltage Drops Around a Complete Source/Load Coupled Circuit*

In dealing with grounding issues, common human tendencies provide some insight into how the correct thinking about the circuit can be helpful towards analysis. Most engineers readily consider the ground return current, "I", *when they are considering a fully differential circuit*.

However, when considering the more usual circuit case, where a single-ended signal is referred to "ground", it is common to assume that all the points on the circuit diagram

where ground symbols are found are at the same potential. Unfortunately, this happy circumstance just ain't necessarily so!

This overly optimistic approach is illustrated in Figure 9.20, where, if it really should exist, "infinite ground conductivity" would lead to zero ground voltage difference between source ground G1 and load ground G2. Unfortunately this approach isn't a wise practice, and when dealing with high precision circuits, it can lead to disasters.

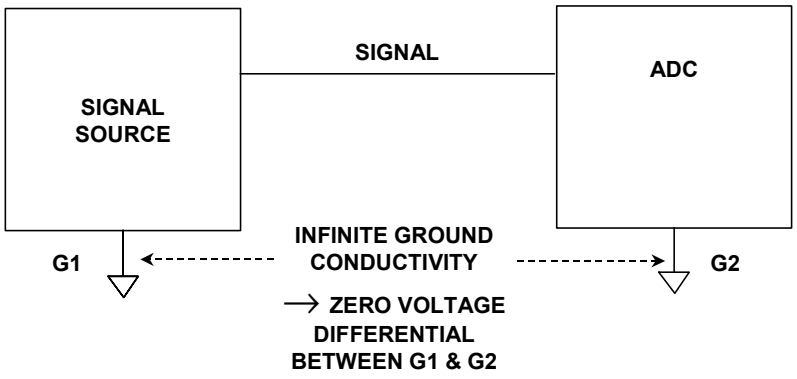


Figure 9.20: *Unlike This Optimistic Diagram, it is Unrealistic to Assume Infinite Conductivity Between Source/Load Grounds in a Real-World System*

A more realistic approach to ground conductor integrity includes analysis of the impedance(s) involved, and careful attention to minimizing spurious noise voltages.

A more realistic model of a ground system is shown in Figure 9.21. The signal return current flows in the complex impedance existing between ground points G1 and G2 as shown, giving rise to a voltage drop ΔV in this path. But it is important to note that additional *external* currents, such as I_{EXT}, may also flow in this same path. It is critical to understand that such currents may generate uncorrelated noise voltages between G1 and G2 (dependent upon the current magnitude and relative ground impedance).

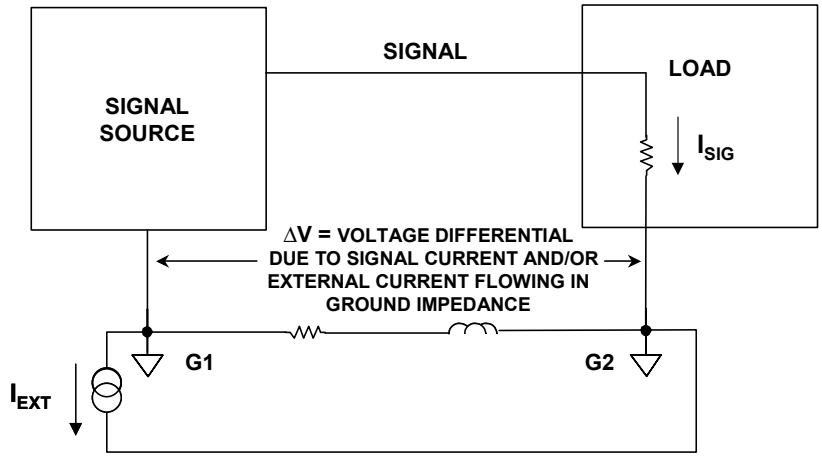


Figure 9.21: *A More Realistic Source-to-Load Grounding System View Includes Consideration of the Impedance Between G1-G2, Plus the Effect of Any Non-Signal-Related Currents*

Some portion of these undesired voltages may end up being seen at the signal's load end, and they can have the potential to corrupt the signal being transmitted.

Grounding in Mixed Analog/Digital Systems

Walt Kester, James Bryant, Mike Byrne

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques including proper signal routing, decoupling, and grounding.

In the past, "high precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high-speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, a medium-speed 12-bit successive approximation (SAR) ADC may operate on a 10-MHz internal clock, while the sampling rate is only 500 kSPS.

Sigma-delta (Σ-Δ) ADCs also require high speed clocks because of their high oversampling ratios. Even high resolution, so-called "low frequency" Σ-Δ industrial measurement ADCs (having throughputs of 10 Hz to 7.5 kHz) operate on 5-MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD77xx-series).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

Ground and Power Planes

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for

decoupling high frequency currents (caused by fast digital logic) but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20 nH/inch inductance. A transient current having a slew rate of 10 mA/ns created by a logic signal would develop an unwanted voltage drop of 200 mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20\ \text{nH} \times \frac{10\ \text{mA}}{\text{ns}} = 200\ \text{mV}. \qquad \text{Eq. 9.1}$$

For a signal having a 2-V peak-to-peak range, this translates into an error of about 200 mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 9.22 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

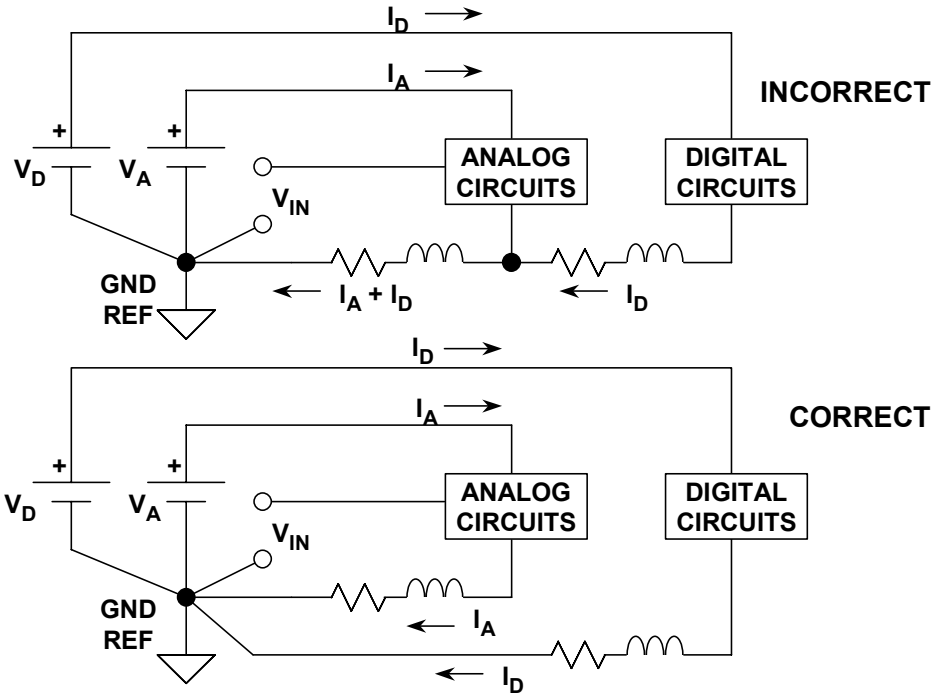


Figure 9.22: *Digital Currents Flowing in Analog Return Path Create Error Voltages*

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1 mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

Double-Sided vs. Multilayer Printed Circuit Boards

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands," because IC ground pins located in a ground "island" have no current return path to the ground plane. Also, the ground plane should be checked for "skinny" connections between adjacent large areas which may significantly reduce the effectiveness of the ground plane. Needless to say, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. A simple 4-layer board would have internal ground and power plane layers with the outer two layers used for interconnections

between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply. In most systems, 4-layers are not enough, and additional layers are required for routing signals as well as power. Figure 9.23 summarizes the key issues relating to ground planes.

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
  - **Avoid High-Density Interconnection Crossovers and Vias Which Reduce Ground Plane Area**
  - **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards: Mandatory for Dense Systems**
  - **Dedicate at Least One Layer for the Ground Plane**
  - **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

Figure 9.23: *Ground Planes Are Mandatory!*

Multicard Mixed-Signal Systems

The best way of minimizing ground impedance in a multicard system is to use a "motherboard" PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

1. The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a "multipoint" grounding system and is shown in Figure 9.24.

2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

The first approach is most often used in all-digital systems, but can be used in mixed-signal systems provided the ground currents due to digital circuits are sufficiently low and diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. However, it is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

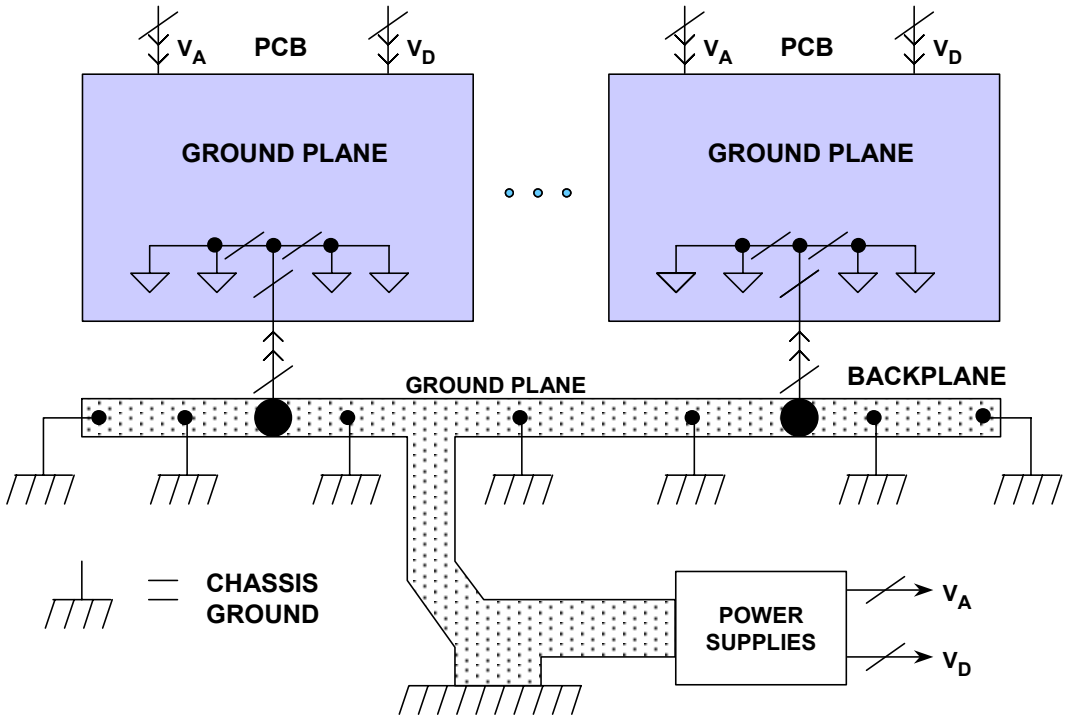


Figure 9.24: *Multipoint Ground Concept*

The second approach ("star ground") is often used in high speed mixed-signal systems having separate analog and digital ground systems and warrants further discussion.

Separating Analog and Digital Grounds

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to *physically* separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 9.25 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper braids for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental dc voltage from developing between the two ground systems when cards are plugged and unplugged. This voltage should be kept less than 300 mV to prevent damage to ICs which have connections to both the analog and digital ground planes. Schottky diodes are preferable because of their low capacitance and low forward voltage drop. The low capacitance prevents ac coupling between the analog and digital ground planes. Schottky diodes begin to conduct at about 300 mV, and several parallel diodes in parallel may be required if high currents are expected. In some cases, ferrite beads can be used instead of Schottky diodes, however they introduce dc ground loops which can be troublesome in precision systems.

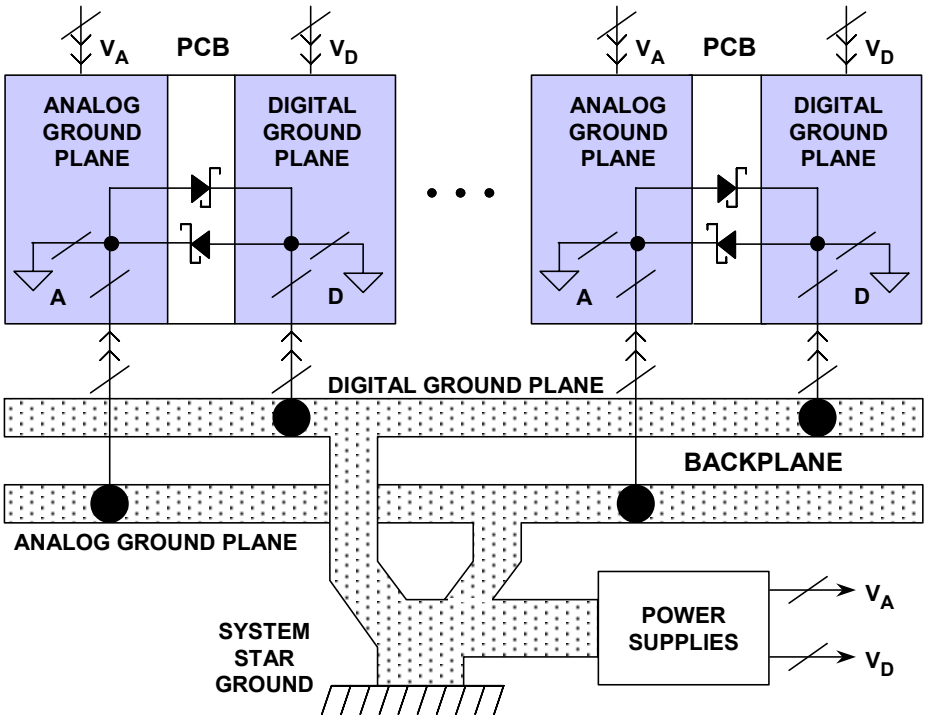


Figure 9.25: *Separating Analog and Digital Ground Planes*

It is mandatory that the impedance of the ground planes be kept as low as possible, all the way back to the system star ground. DC or ac voltages of more than 300 mV between the two ground planes can not only damage ICs but cause false triggering of logic gates and possible latchup.

Grounding and Decoupling Mixed-Signal ICs with Low Digital Currents

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane*. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually has pins designated as *analog ground* (AGND) and *digital ground* (DGND). The diagram shown in Figure 9.26 will help to explain this seeming dilemma.

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 9.26 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2-pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together

externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins and invites disaster!*

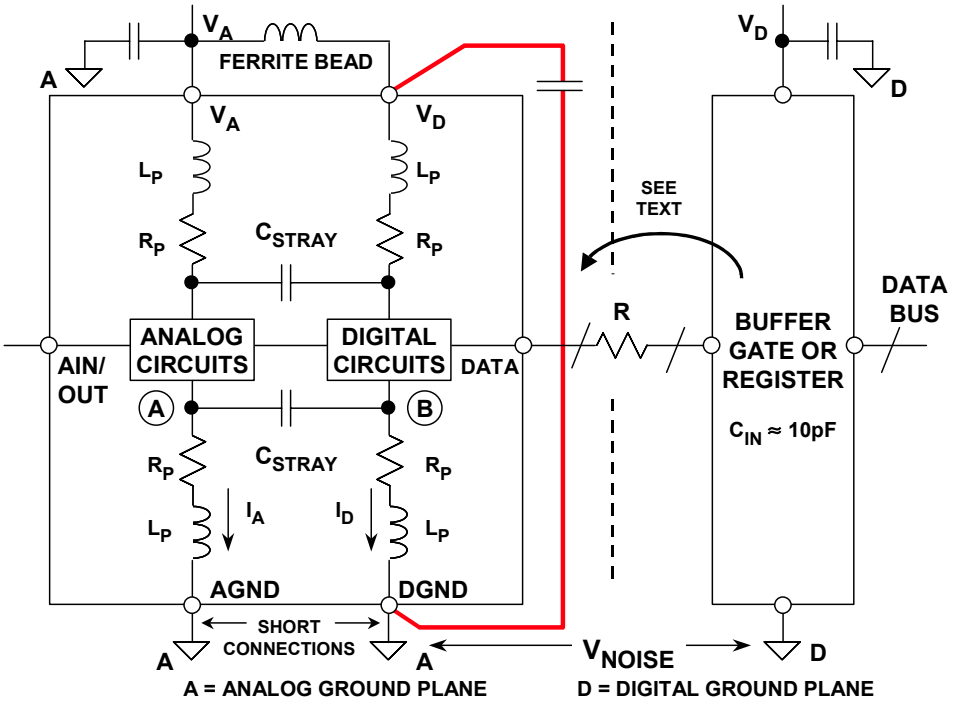


Figure 9.26: *Proper Grounding of Mixed-signal ICs With Low Internal Digital Currents*

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement may inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally can't, by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 9.26. The internal transient digital currents of the converter will flow in the small loop from V_D through the decoupling capacitor and to DGND (this path is shown with a heavy line on the diagram). The transient digital currents will therefore not appear on the external analog ground plane, but are confined to the loop. The V_D pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. These decoupling capacitors should be low inductance ceramic types, typically between 0.01 µF and 0.1 µF.

Treat the ADC Digital Outputs with Care

It is always a good idea (as shown in Figure 9.26) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus. Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice. In some cases it may be desirable to add an additional buffer register on the analog ground plane next to the converter output to provide greater isolation.

The series resistors (labeled "R" in Figure 9.26) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and a through-hole will create a load of approximately 10 pF. A logic output slew rate of 1 V/ns will produce 10 mA of dynamic current if there is no isolation resistor:

$$\Delta I = C\frac{\Delta v}{\Delta t} = 10\ \text{pF} \times \frac{1\ \text{V}}{\text{ns}} = 10\ \text{mA}\,. \qquad \text{Eq. 9.2}$$

A 500Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \cdot C = 2.2 \times 500\ \Omega \times 10\ \text{pF} = 11\ \text{ns}. \qquad \text{Eq. 9.3}$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital ground plane impedance, thereby maintaining the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300 mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable, even if the voltages are the same. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane as shown in Figure 9.27.

In some cases it may not be possible to connect V_D to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5 V, but the digital interface powered by +3 V to interface to 3-V logic. In this case, the +3-V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the +3-V digital logic supply.

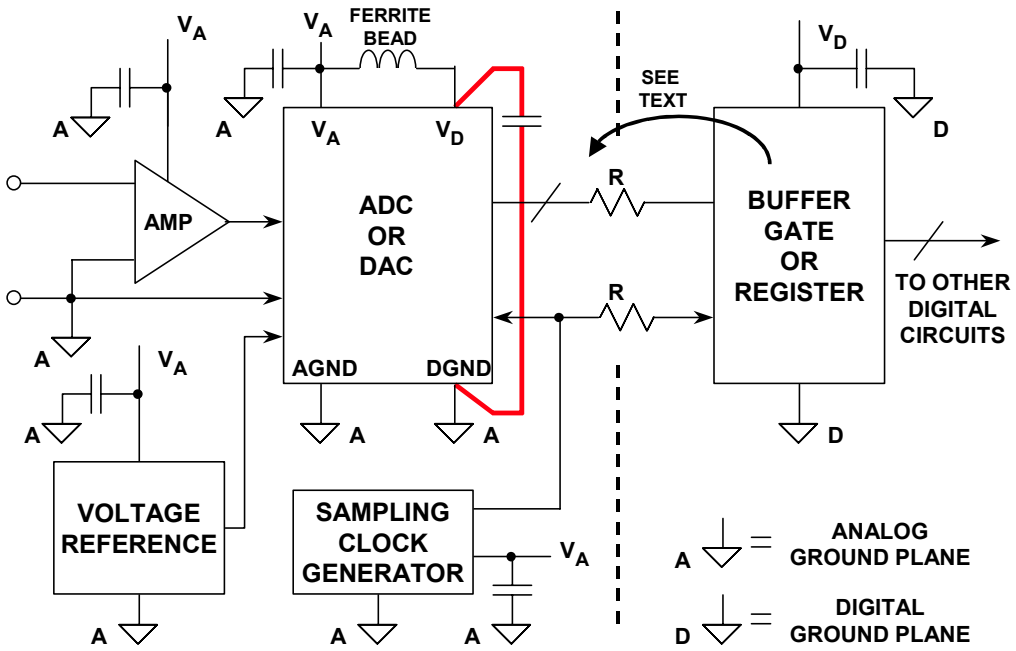


Figure 9.27: *Grounding and Decoupling Points*

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

Sampling Clock Considerations

In a high performance sampled data system a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC signal-to-soise ratio (SNR) is given approximately by the equation:

$$SNR = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right], \qquad \text{Eq. 9.4}$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the rms sampling clock jitter, t_j. Note that f in the above equation is the analog input frequency. Just working through a simple example, if t_j = 50 ps rms, f = 100 kHz, then SNR = 90 dB, equivalent to about 15-bit dynamic range.

It should be noted that t_j in the above example is the root-sum-square (rss) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5-ps rms) CMOS compatible outputs. (For example, MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801, Tel. 914-576-6570 and Wenzel Associates, Inc., 2215 Kramer Lane, Austin, Texas 78758 Tel. 512- 835-2038).

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics.

This can be remedied somewhat by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in Figure 9.28 or a high speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single +5-V supply system, ECL logic can be connected between ground and +5 V (PECL), and the outputs ac coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low phase noise crystal oscillator, and not the clock output of a DSP, microprocessor, or microcontroller.

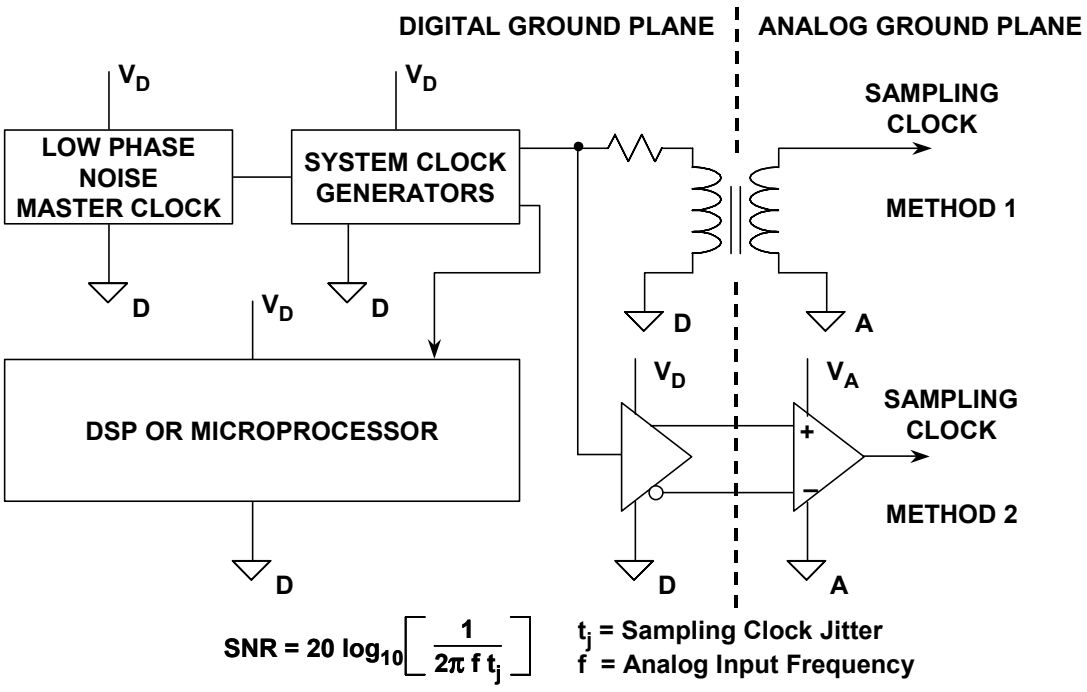


Figure 9.28: *Sampling Clock Distribution From Digital to Analog Ground Planes*

The Origins of the Confusion about Mixed-Signal Grounding: Applying Single-Card Grounding Concepts to Multicard Systems

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point as shown in Figure 9.29. This essentially creates the system "star" ground at the mixed-signal device.

All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. For these reasons, this grounding approach is not recommended for multicard systems, and the approach previously discussed should be used for mixed signal ICs with low digital currents.

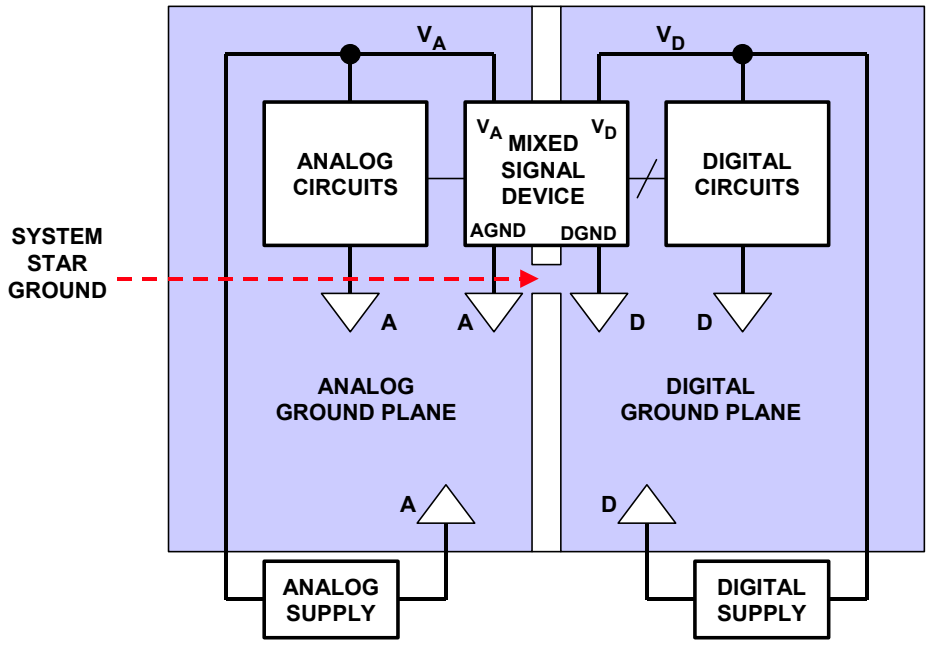


Figure 9.29: *Grounding Mixed Signal ICs : Single PC Board (Typical Evaluation/Test Board)*

Summary: Grounding Mixed Signal Devices with Low Digital Currents in a Multicard System

Figure 9.30 summarizes the approach previously described for grounding a mixed signal device which has low digital currents. The analog ground plane is not corrupted because the small digital transient currents flow in the small loop between V_D, the decoupling capacitor, and DGND (shown as a heavy line). The mixed signal device is for all intents and purposes treated as an analog component. The noise V_N between the ground planes reduces the noise margin at the digital interface but is generally not harmful if kept less than 300 mV by using a low impedance digital ground plane all the way back to the system star ground.

However, mixed signal devices such as sigma-delta ADCs, codecs, and DSPs with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC or DAC contains a complex digital filter which adds considerably to the digital current in the device. The method previously discussed depends on the decoupling capacitor between V_D and DGND to keep the digital transient currents isolated in a small loop. However, if the digital currents are significant enough and have components at dc or low frequencies, the decoupling capacitor may have to be so large that it is impractical. Any digital current which flows outside the loop between V_D and DGND must flow through the analog ground plane. This may degrade performance, especially in high resolution systems.

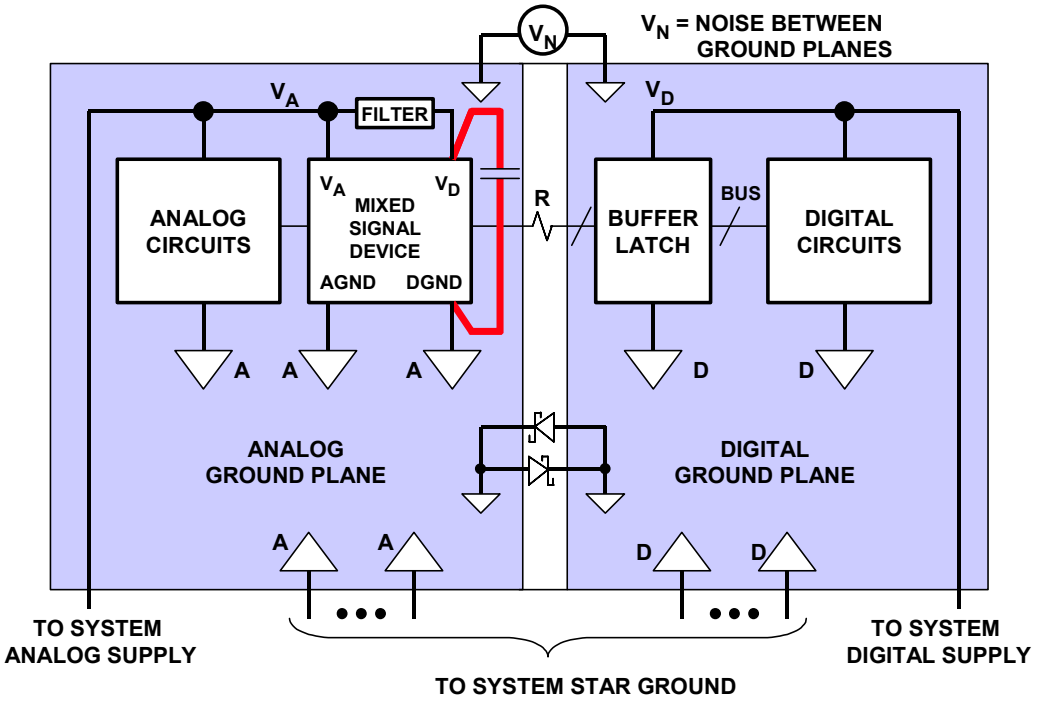


Figure 9.30: *Grounding Mixed Signal ICs with Low Internal Digital Currents: Multiple PC Boards*

It is difficult to predict what level of digital current flowing into the analog ground plane will become unacceptable in a system. All we can do at this point is to suggest an alternative grounding method which may yield better performance.

Summary: Grounding Mixed Signal Devices with High Digital Currents in a Multicard System

An alternative grounding method for a mixed signal device with high levels of digital currents is shown in Figure 9.31. The AGND of the mixed signal device is connected to the analog ground plane, and the DGND of the device is connected to the digital ground plane. The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the AGND and DGND pins of the device. For this method to be successful, the analog and digital circuits within the mixed signal device must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

Figure 9.31 shows optional Schottky diodes (back-to-back) or a ferrite bead connecting the analog and digital ground planes. The Schottky diodes prevent large dc voltages or low frequency voltage spikes from developing across the two planes. These voltages can potentially damage the mixed signal IC if they exceed 300 mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a dc connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive. This protects the IC from dc voltages between AGND and DGND, but the dc connection

provided by the ferrite bead can introduce unwanted dc ground loops and may not be suitable for high resolution systems.

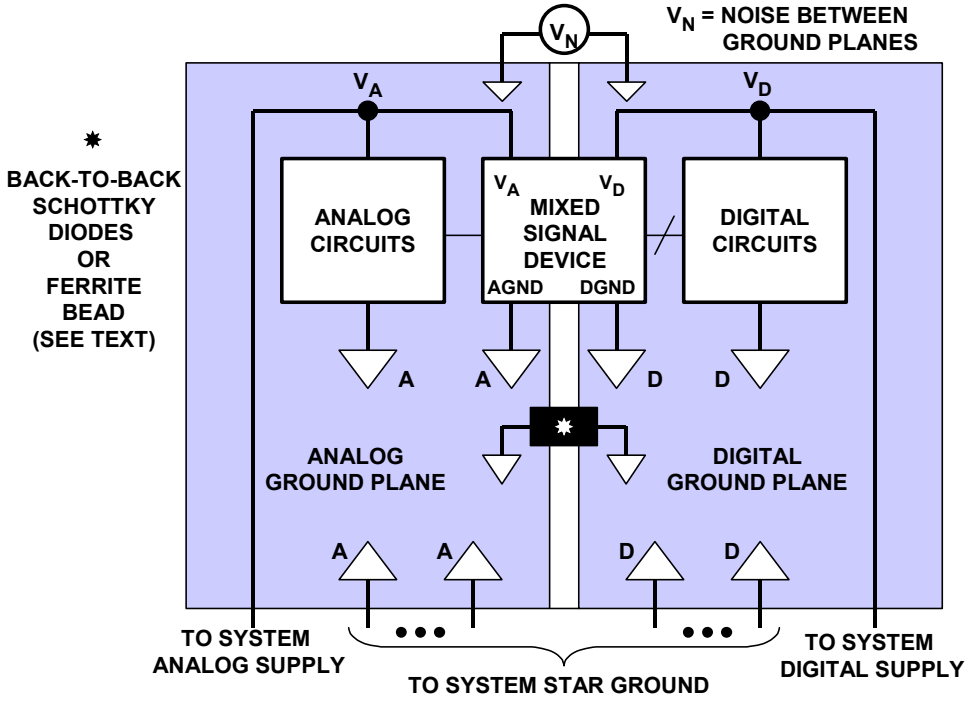


Figure 9.31: *Grounding Alternative for Mixed-Signal ICs with High Digital Currents: Multiple PC Boards*

Grounding DSPs with Internal Phase-Locked Loops

As if dealing with mixed-signal ICs with AGND and DGNDs wasn't enough, DSPs such as the ADSP-21160 SHARC with internal phase-locked-loops (PLLs) raise issues with respect to proper grounding. The ADSP-21160 PLL allows the internal core clock (determines the instruction cycle time) to operate at a user-selectable ratio of 2, 3, or 4 times the external clock frequency, CLKIN. The CLKIN rate is the rate at which the synchronous external ports operate. Although this allows using a lower frequency external clock, care must be taken with the power and ground connections to the internal PLL as shown in Figure 9.32.

In order to prevent internal coupling between digital currents and the PLL, the power and ground connections to the PLL are brought out separately on pins labeled AV_{DD} and AGND, respectively. The AV_{DD} +2.5-V supply should be derived from the $V_{DD\ INT}$ +2.5-V supply using the filter network as shown. This ensures a relatively noise-free supply for the internal PLL. The AGND pin of the PLL should be connected to the digital ground plane of the PC board using a short trace. The decoupling capacitors should be routed between the AV_{DD} pin and AGND pin using short traces.

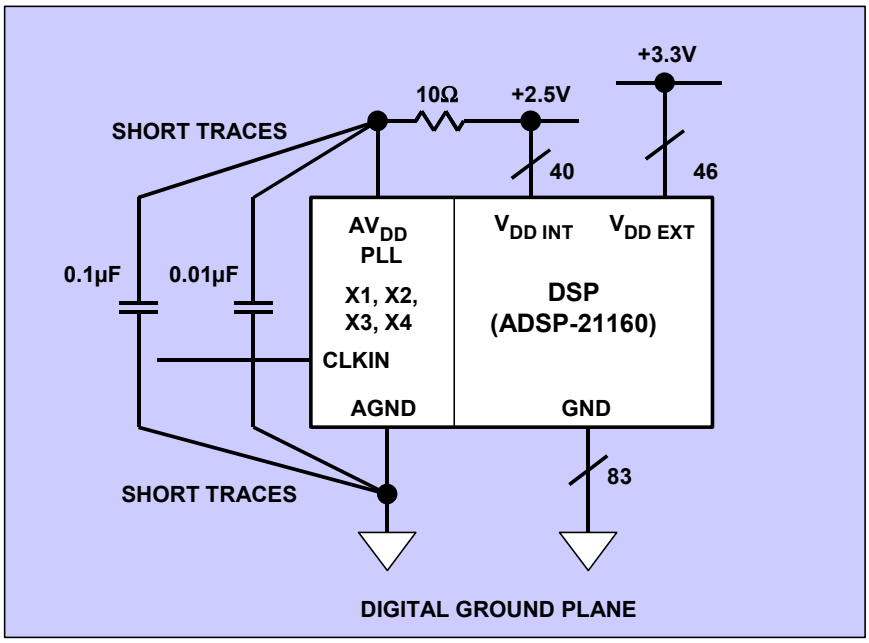


Figure 9.32: *Grounding DSPs with Internal Phase-Locked-Loops (PLLs)*

Grounding Summary

There is no single grounding method which will guarantee optimum performance 100% of the time! This section has presented a number of possible options depending upon the characteristics of the particular mixed signal devices in question. It is helpful, however, to provide for as many options as possible when laying out the initial PC board.

It is mandatory that at least one layer of the PC board be dedicated to ground plane! The initial board layout should provide for non-overlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required. Pads and vias should also be provided so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should in general always be connected to the analog ground plane. An exception to this are DSPs which have internal phase-locked-loops (PLLs), such as the ADSP-21160 SHARC. The ground pin for the PLL is labeled AGND, but should be connected directly to the digital ground plane for the DSP. See Figure 9.33 for a general summary of grounding philosophy.

- **There is no single grounding method which is guaranteed to work 100% of the time!**
- **Different methods may or may not give the same levels of performance.**
- **At least one layer on each PC board MUST be dedicated to ground plane!**
- **Do initial layout with split analog and digital ground planes.**
- **Provide pads and vias on each PC board for back-to-back Schottky diodes and optional ferrite beads to connect the two planes.**
- **Provide "jumpers" so that DGND pins of mixed-signal devices can be connected to AGND pins (analog ground plane) or to digital ground plane. (AGND of PLLs in DSPs should be connected to digital ground plane).**
- **Provide pads and vias for "jumpers" so that analog and digital ground planes can be joined together at several points on each PC board.**
- **Follow recommendations on mixed signal device data sheet.**

Figure 9.33: *Grounding Philosophy Summary*

Some General PC Board Layout Guidelines for Mixed-Signal Systems

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems. If clock driver packages are used in clock distribution, only one frequency clock should be passed through a single package. Sharing drivers between clocks of different frequencies in the same package will produce excess jitter and crosstalk and degrade performance.

The ground plane can act as a shield where sensitive signals cross. Figure 9.34 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel—it is therefore imperative to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mΩ) when the board is new—as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins

on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

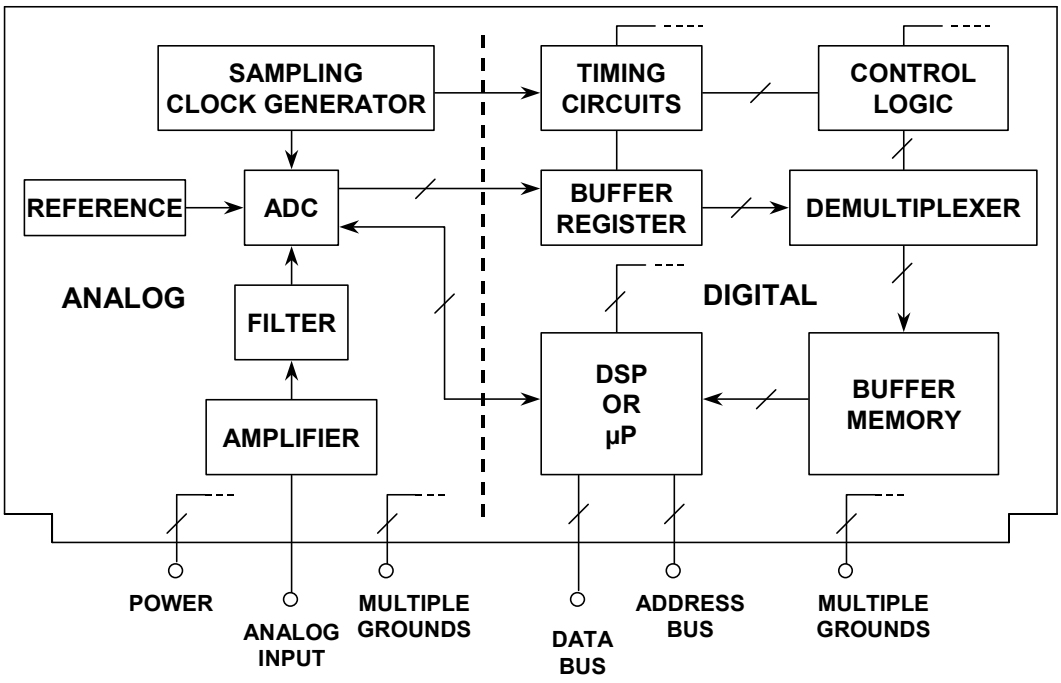


Figure 9.34: *Analog and Digital Circuits Should be Partitioned on PCB Layout*

Analog Devices and other manufacturers of high performance mixed-signal ICs offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device.

Skin Effect

At high frequencies, also consider *skin effect*, where inductive effects cause currents to flow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions of this section on dc resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this discussion. However, a good approximation for copper is that the skin depth in centimeters is $6.61/\sqrt{f}$, (f in Hz).

A summary of the skin effect within a typical PCB conductor foil is shown in Figure 9.35. Note that this copper conductor cross-sectional view assumes looking into the *side* of the conducting trace.

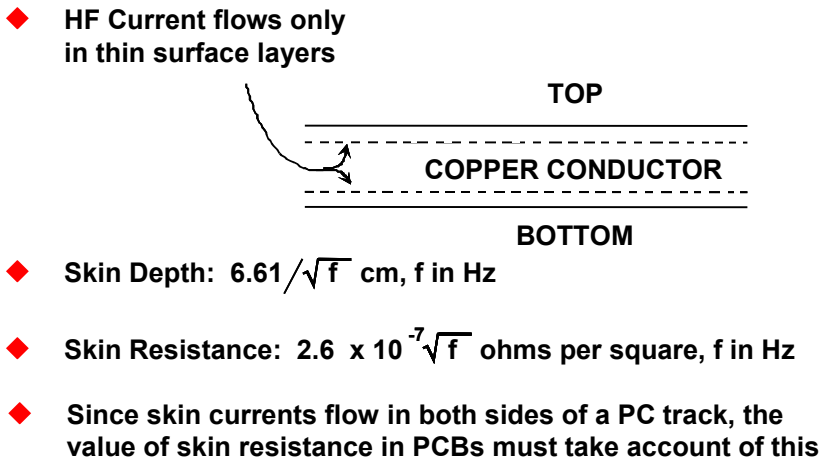


Figure 9.35: *Skin Depth in a PC Conductor*

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the conductor, this tells us that for a typical PC foil, we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance for copper is $2.6 \times 10^{-7} \sqrt{f}$ ohms per square, (f in Hz). This formula is invalid if the skin thickness is greater than the conductor thickness (i.e. at dc or low frequencies).

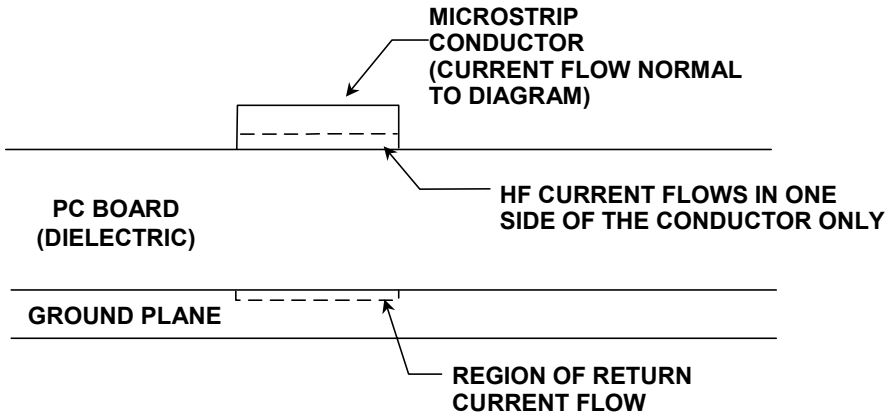


Figure 9.36: *Skin Effect with PC Conductor and Ground Plane*

Figure 9.36 illustrates a case of a PCB conductor with current flow, as separated from the ground plane underneath.

In this diagram, note the (dotted) regions of high frequency current flow, as reduced by the skin effect. When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines, see below), so the resistance per square of PC foil may be half the above value.

Transmission Lines

We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As shown previously in Figure 9.36, when a high frequency signal flows in a PC track running over a ground plane, the arrangement functions as a *microstrip* transmission line, and the majority of the return current flows in the ground plane underneath the line.

Figure 9.37 shows the general parameters for a microstrip transmission line, given the conductor width, w, dielectric thickness, h, and the dielectric constant, E_r.

The characteristic impedance of such a microstrip line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. Designs of microstrip lines are covered in more detail later in this chapter.

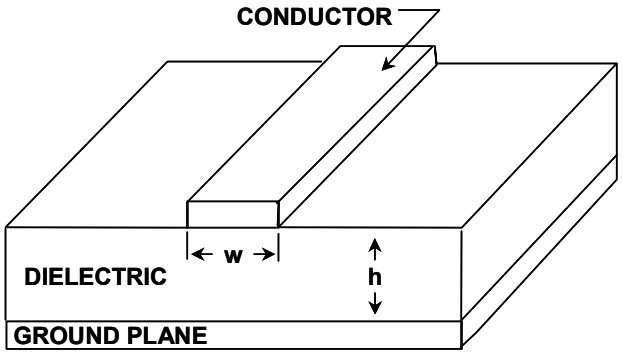


Figure 9.37: *A PCB Microstrip Transmission Line is an Example of a Controlled Impedance Conductor Pair*

For most dc and lower frequency applications, the characteristic impedance of PCB traces will be relatively unimportant. Even at frequencies where a track over a ground plane behaves as a transmission line, it is not necessary to worry about its characteristic impedance or proper termination if the free space wavelengths of the frequencies of interest are greater than ten times the length of the line.

However, at VHF and higher frequencies it is possible to use PCB tracks as microstrip lines within properly terminated transmission systems. Typically the microstrip will be designed to match standard coaxial cable impedances, such as 50, 75 or 100 Ω, simplifying interfacing.

Note that if losses in such systems are to be minimized, the PCB material must be chosen for low high-frequency losses. This usually means the use of Teflon or some other comparably low-loss PCB material. Often, though, the losses in short lines on cheap glass-fiber board are small enough to be quite acceptable.

Be Careful With Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in Figure 9.38, where conductors A and B must cross one another.

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire or a resistor. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to trouble-shoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

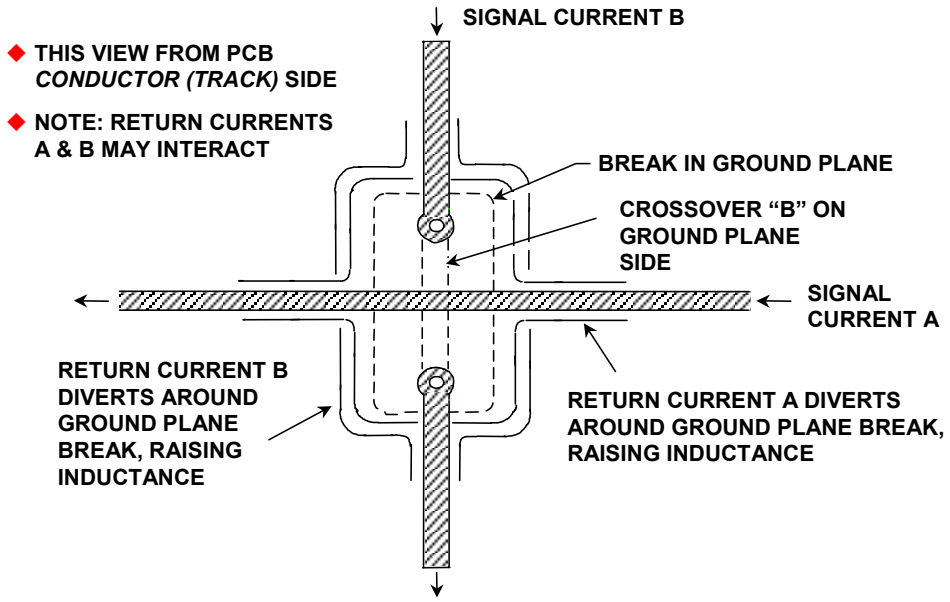


Figure 9.38: *A Ground Plane Break Raises Circuit Inductance, and Increases Vulnerability to External Fields*

The use of double-sided or multi-layer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high performance mixed signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

Ground Isolation Techniques

While the use of ground planes does lower impedance and helps greatly in lowering ground noise, there may still be situations where a prohibitive level of noise exists. In such cases, the use of ground error minimization and isolation techniques can be helpful.

Another illustration of a common-ground impedance coupling problem is shown in Figure 9.39. In this circuit a precision gain-of-100 preamp amplifies a low-level signal V_{IN}, using an AD8551 chopper-stabilized amplifier for best dc accuracy. At the load end, the signal V_{OUT} is measured with respect to G2, the local ground. Because of the small 700-µA I_{SUPPLY} of the AD8551 flowing between G1 and G2, there is a 7-µV ground error—about 7 times the typical input offset expected from the op amp!

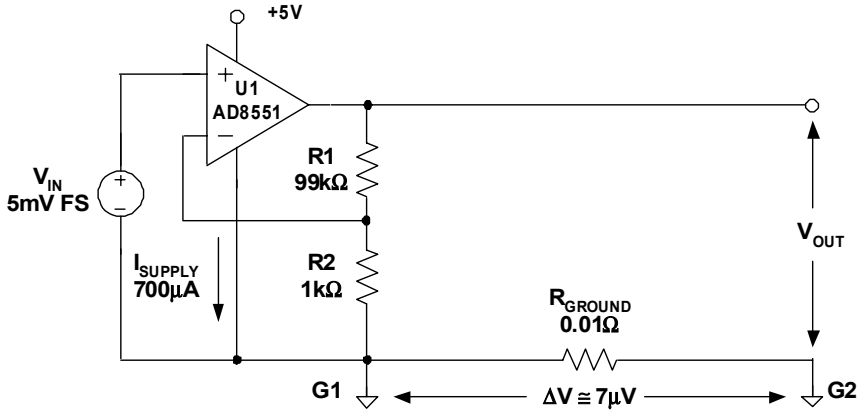


Figure 9.39: *Unless Care is Taken, Even Small Common Ground Currents can Degrade Precision Amplifier Accuracy*

This error can be avoided by routing the negative supply pin current of the op amp back to star ground G2 as opposed to ground G1, by using a separate trace. This step eliminates the G1-G2 path power supply current, and so minimizes the ground leg voltage error. Note that there will be little error developed in the "hot" V_{OUT} lead, so long as the current drain at the load end is small.

In some cases, there may be simply unavoidable ground voltage differences between a source signal and the load point where it is to be measured. Within the context of this "same-board" discussion, this might require rejecting ground error voltages of several tens-of-mV. Or, should the source signal originate from an "off-board" source, then the magnitude of the common-mode voltages to be rejected can easily rise into a several volt range (or even tens-of-volts).

Fortunately, full signal transmission accuracy can still be accomplished in the face of such high noise voltages, by employing a principle discussed earlier. This is the use of a differential-input, *ground isolation* amplifier. The ground isolation amplifier minimizes the effect of ground error voltages between stages by processing the signal in differential fashion, thereby rejecting common-mode voltages by a substantial margin (typically 60 dB or more). Note that this approach is only effective for very low frequency signals, however.

Two ground isolation amplifier solutions are shown in Figure 9.40. This diagram can alternately employ either the AD629 to handle CM voltages up to ±270 V, or the AMP03, which is suitable for CM voltages up to ±20 V.

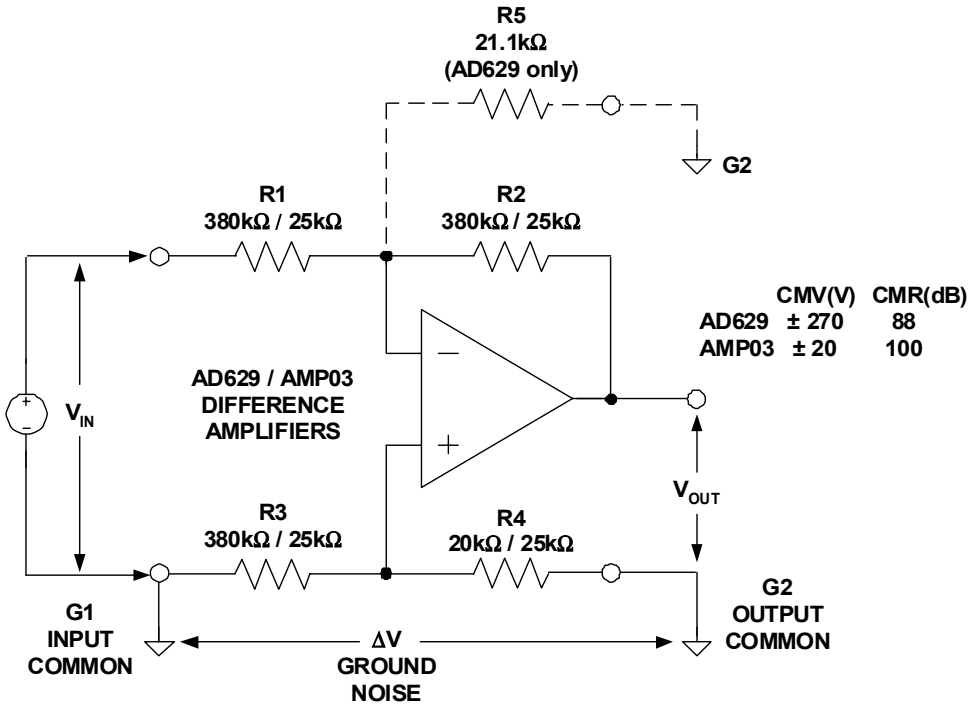


Figure 9.40: *A Differential Input Ground Isolating Amplifier Allows High Transmission Accuracy by Rejecting Ground Noise Voltage Between Source (G1) and Measurement (G2) Grounds*

In the circuit, input voltage V_{IN} is referred to G1, but must be measured with respect to G2. With the use of a high CMR unity-gain difference amplifier, the noise voltage ΔV existing between these two grounds is easily rejected. The AD629 offers a typical CMR of 88 dB, while the AMP03 typically achieves 100 dB. In the AD629, the high CMV rating is done by a combination of high CM attenuation, followed by differential gain, realizing a net differential gain of unity. The AD629 uses the first listed value resistors noted in the figure for R1-R5. The AMP03 operates as a precision four-resistor differential amplifier, using the 25-kΩ value R1-R4 resistors noted. Both devices are complete, one package solutions to the ground-isolation amplifier.

This scheme allows relative freedom from tightly controlling ground drop voltages, or running additional and/or larger PCB traces to minimize such error voltages. Note that it can be implemented either with the fixed gain difference amplifiers shown, or also with a

standard in-amp IC, configured for unity gain. The AD623, for example, also allows single-supply use. In any case, signal polarity is also controllable, by simple reversal of the difference amplifier inputs.

In general terms, transmitting a signal from one point on a PCB to another for measurement or further processing can be optimized by two key interrelated techniques. These are the use of high-impedance, differential signal-handling techniques. The high impedance loading of an in-amp minimizes voltage drops, and differential sensing of the remote voltage minimizes sensitivity to ground noise.

When the further signal processing is A/D conversion, these transmission criteria can be implemented *without* adding a differential ground isolation amplifier stage. Simply select an ADC which operates differentially. The high input impedance of the ADC minimizes load sensitivity to the PCB wiring resistance. In addition, the differential input feature allows the output of the source to be sensed directly at the source output terminals (even if single-ended). The CMR of the ADC then eliminates sensitivity to noise voltages between the ADC and source grounds.

An illustration of this concept using an ADC with high impedance differential inputs is shown in Figure 9.41. Note that the general concept can be extended to virtually any signal source, driving any load. All loads, even single-ended ones, become differential-input by adding an appropriate differential input stage.

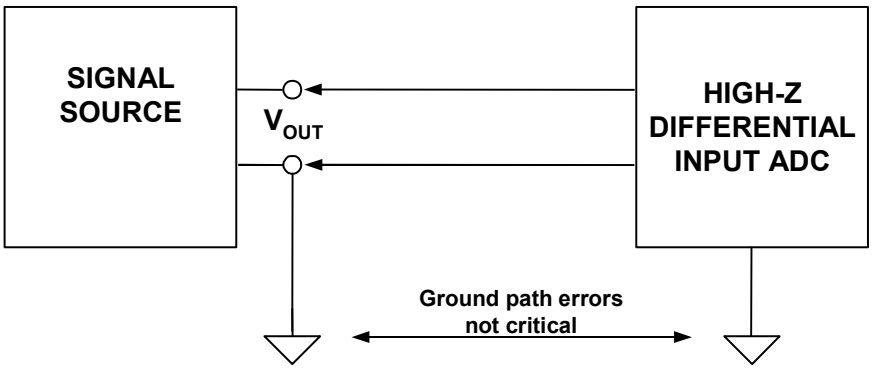


Figure 9.41: *A High-Impedance Differential Input ADC Also Allows High Transmission Accuracy Between Source and Load*

The differential input can be provided by either a fully developed high-Z in-amp, or in many cases it can be a simple subtractor stage op amp, such as Figure 9.40.

Static PCB Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the PCB surface by flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well-cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15-V supply rails. Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10-MΩ resistance causes a 0.1-V error. Unfortunately, the standard op amp pinout

places the $-V_S$ supply pin next to the + input, which is often hoped to be at high impedance! To help identify nodes sensitive to the effects of leakage currents ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, you can localize moisture sensitivity to a suspect node with a classic test. While observing circuit operation, blow on potential trouble spots through a simple soda straw. The straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact. There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by thorough washing with deionized water and an 85°C bakeout for a few hours. Be careful when selecting board-washing solvents, though. When cleaned with certain solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon handling, or exposure to foul atmospheres, and high humidity. Some additional means must be sought to stabilize circuit behavior, such as conformal surface coating.

Fortunately, there is an answer to this, namely *guarding*, which offers a fairly reliable and permanent solution to the problem of surface leakage. Well-designed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments. Two schematics illustrate the basic guarding principle, as applied to typical inverting and non-inverting op amp circuits.

Figure 9.42 illustrates an inverting mode guard application. In this case, the op amp reference input is grounded, so the guard is a grounded ring surrounding all leads to the inverting input, as noted by the dotted line.

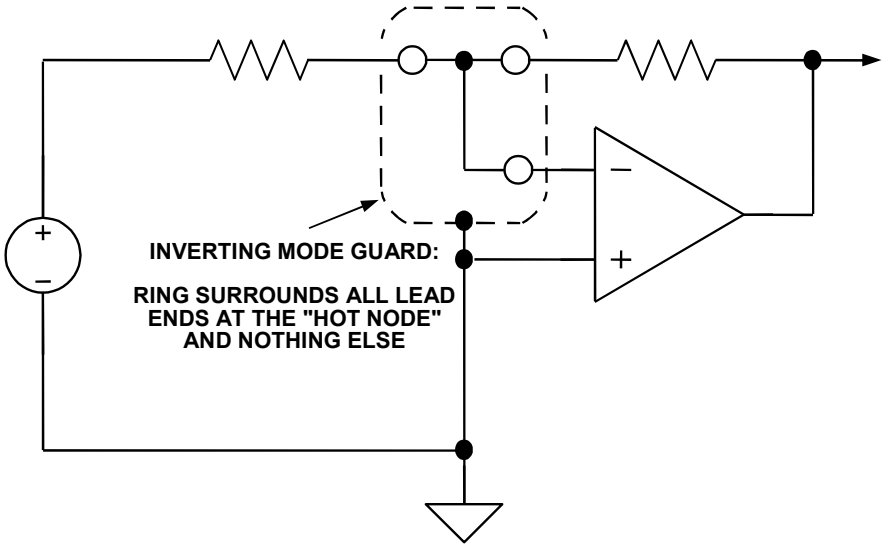


Figure 9.42: *Inverting Mode Guard Encloses All Op Amp Inverting Input Connections Within a Grounded Guard Ring*

Basic guarding principles are simple: *Completely* surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node (as otherwise the guard will serve as a leakage source rather than a leakage sink). For example, to keep leakage into a node below 1 pA (assuming 1000-MΩ leakage resistance) the guard and guarded node must be within 1 mV. Generally, the low offset of a modern op amp is sufficient to meet this criterion.

There are important caveats to be noted with implementing a true high-quality guard. For traditional through-hole PCB connections, the guard pattern should appear on *both* sides of the circuit board, to be most effective. And, it should also be connected along its length by several vias. Finally, when either justified or required by the system design parameters, do make an effort to include guards in the PCB design process from the outset—there is little likelihood that a proper guard can be added as an afterthought.

Figure 9.43 illustrates the case for a non-inverting guard. In this instance the op amp reference input is directly driven by the source, which complicates matters considerably. Again, the guard ring completely surrounds all of the input nodal connections. In this instance however, the guard is driven from the low impedance feedback divider connected to the inverting input.

Usually the guard-to-divider junction will be a direct connection, but in some cases a unity gain buffer might be used at "X" to drive a cable shield, or also to maintain the lowest possible impedance at the guard ring.

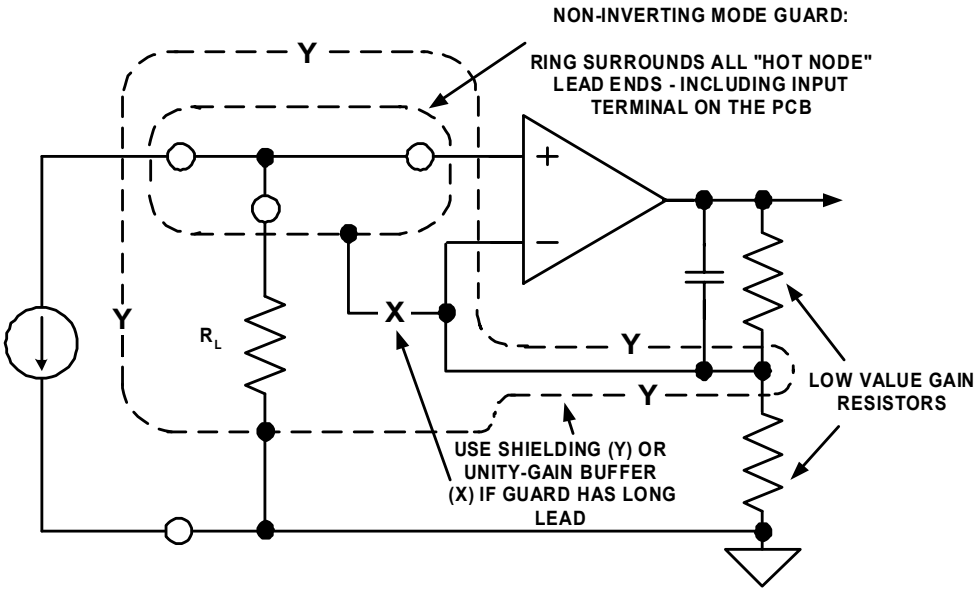


Figure 9.43: *Non-Inverting Mode Guard Encloses All Op Amp Non-Inverting Input Connections Within a Low Impedance, Driven Guard Ring*

In lieu of the buffer, another useful step is to use an additional, directly grounded screen ring, "Y", which surrounds the inner guard and the feedback nodes as shown. This step

costs nothing except some added layout time, and will greatly help buffer leakage effects into the higher impedance inner guard ring.

Of course what hasn't been addressed to this point is just how the op amp itself gets connected into these guarded islands without compromising performance. The traditional method using a TO-99 metal can package device was to employ double-sided PCB guard rings, with both op amp inputs terminated within the guarded ring.

Many high impedance sensors use the above-described method. The section immediately following illustrates how more modern IC packages can be mounted to PCB patterns, and take advantage of guarding and low-leakage operation.

Sample MINIDIP and SOIC Op Amp PCB Guard Layouts

Modern assembly practices have favored smaller plastic packages such as 8-pin MINIDIP and SOIC types. Some suggested partial layouts for guard circuits using these packages is shown in the next two figures. While guard traces may also be possible with even more tiny op amp footprints, such as SOT23, SC70, etc., the required trace separations become even more confining, challenging the layout designer as well as the manufacturing processes.

For the ADI "N" style MINIDIP package, Figure 9.44 illustrates how guarding can be accomplished for inverting (left) and non-inverting (right) operating modes. This setup would also be applicable to other op amp devices where relatively high voltages occur at pin 1 or 4. Using a standard 8-pin DIP outline for a single op amp, it can be noted that this package's 0.1" pin spacing allows a PC trace (here, the guard trace) to pass between adjacent pins. This is the key to implementing effective DIP package guarding, as it can adequately prevent a leakage path from the $-V_S$ supply at pin 4, or from similar high potentials at pin 1.

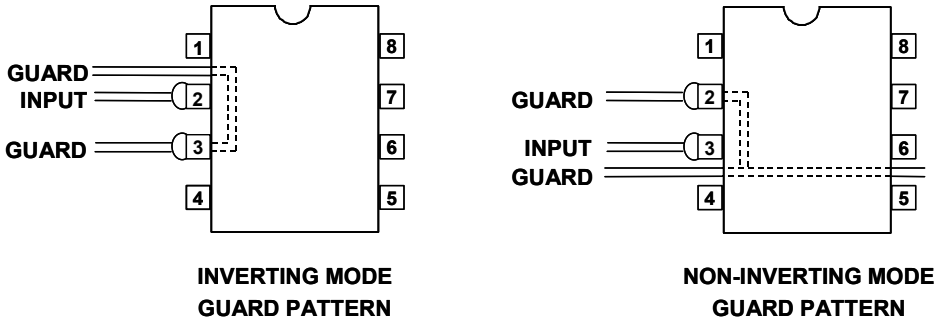


Figure 9.44: *PCB Guard Patterns for Inverting and Non-Inverting Mode Op Amps Using 8 Pin MINIDIP (N) Package*

For the left-side inverting mode, note that the grounded guard traces connected to pin 3 surround the op amp inverting input (pin 2), and run parallel to the input trace. This guard would be continued out to and around the source and feedback connections of Figure 9.42 (or other similar circuit), including an input pad in the case of a cable. In the

right-side non-inverting mode, the guard voltage is the feedback divider voltage to pin 2. This corresponds to the inverting input node of the amplifier, from Figure 9.43.

Note that in both of the cases of Figure 9.44, the guard physical connections shown are only partial—an actual layout would include all sensitive nodes within the circuit. In both the inverting and the non-inverting modes using the MINIDIP or other through-hole style package, the PCB guard traces should be located on both sides of the board, with top and bottom traces connected with several vias.

Things become slightly more complicated when using guarding techniques with the SOIC surface mount ("R") package, as the 0.05" pin spacing doesn't easily allow routing of PCB traces between the pins. But, there is still an effective guarding answer, at least for the inverting case. Figure 9.45 shows guards for the ADI "R" style SOIC package.

Note that for many single op amp devices in this SOIC "R" package, pins 1, 5, and 8 are "no connect" pins. For such instances, this means that these locations can be employed in the layout to route guard traces. In the case of the inverting mode (left), the guarding is still completely effective, with the dummy pin 1 and pin 3 serving as the grounded guard trace. This is a fully effective guard without compromise. Also, with SOIC op amps, much of the circuitry around the device will not use through-hole components. So, the guard ring may only be necessary on the op amp PCB side.

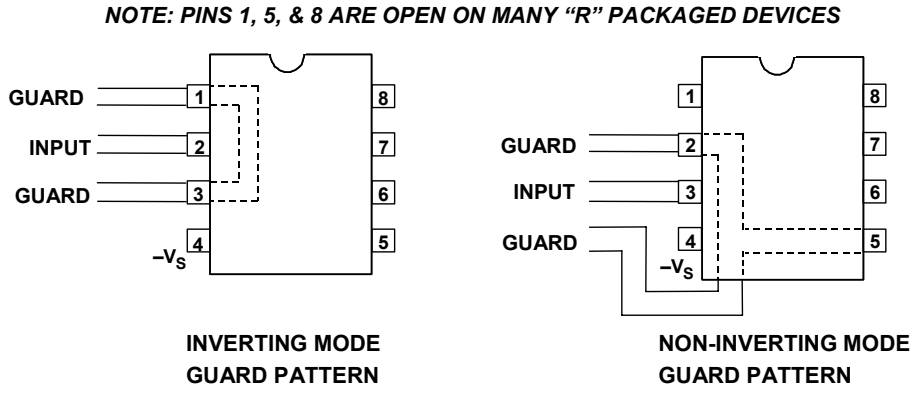


Figure 9.45: *PCB Guard Patterns for Inverting and Non-Inverting Mode Op Amps Using 8 Pin SOIC (R) Package*

In the case of the follower stage (right), the guard trace must be routed around the negative supply at pin 4, and thus pin 4 to pin 3 leakage isn't fully guarded. For this reason, a precision high impedance follower stage using an SOIC package op amp isn't generally recommended, as guarding isn't as effective for dual supply connected devices.

However, an exception to this caveat does apply to the use of a *single-supply* op amp as a non-inverting stage. For example, if the AD8551 is used, pin 4 becomes ground, and some degree of intrinsic guarding is then established by default.

Dynamic PCB Effects

Although static PCB effects can come and go with changes in humidity or board contamination, problems that most noticeably affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, washing or any other simple fixes can't fix them. As such, they can permanently and adversely affect a design's specifications and performance. The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads optimally.

Dielectric absorption (DA), on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in Figure 9.46, the RC model for this effective capacitance ranges from 0.1 to 2.0 pF, with the resistance ranging from 50 to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board DA interacts most strongly with high-impedance circuits.

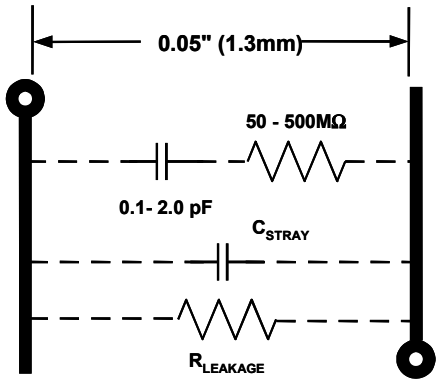


Figure 9.46: *DA Plagues Dynamic Response of PCB-Based Circuits*

PCB DA most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects aren't usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties. The chemistry involved in producing plated-through holes seems to exacerbate the problem. If your circuits don't meet expected transient response specs, you should consider PCB DA as a possible cause.

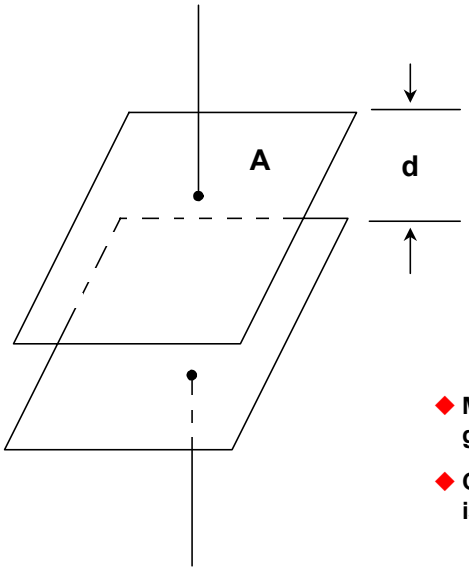
Fortunately, there are solutions. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem (note that these guards should be duplicated on both sides of the board, in cases of through-hole components). As noted previously, low-loss PCB dielectrics are also available at higher costs.

PCB "hook", similar if not identical to DA, is characterized by variation in effective circuit-board capacitance with frequency (see Reference 1). In general, it affects high-impedance circuit transient response where board capacitance is an appreciable portion of the total in the circuit. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit board DA, the board's chemical makeup very much influences its effects.

Stray Capacitance

When two conductors aren't short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. So, on any PCB, there will be a large number of capacitors associated with any circuit (which may or may not be considered in models of the circuit). Where high frequency performance matters (and even dc and VLF circuits may use devices with high F_t and therefore be vulnerable to high frequency instability), it is very important to consider the effects of this stray capacitance.

Any basic textbook will provide formulas for the capacitance of parallel wires and other geometric configurations (see References 9 and 10). The example we need consider in this discussion is the parallel plate capacitor, often formed by conductors on opposite sides of a PCB. The basic diagram describing this capacitance is shown in Figure 9.47.



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm^2

d = plate separation in mm

E_r = dielectric constant relative to air

- **Most common PCB type uses 1.5mm glass-fiber epoxy material with $E_r = 4.7$**
- **Capacity of PC track over ground plane is roughly 2.8pF/cm^2**

Figure 9.47: *Capacitance of Two Parallel Plates*

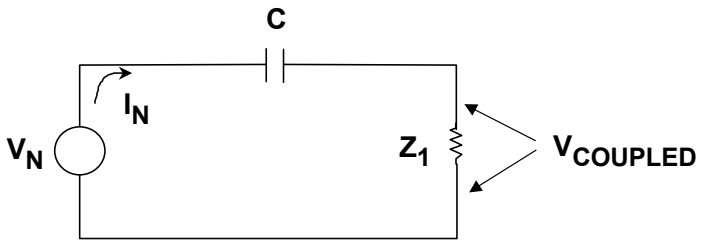
Neglecting edge effects, the capacitance of two parallel plates of area A mm^2 and separation d mm in a medium of dielectric constant E_r relative to air is $0.00885\ E_r\ A/d$ pF.

From this formula, we can calculate that for general purpose PCB material ($E_r = 4.7$, d = 1.5 mm), the capacitance between conductors on opposite sides of the board is just under 3 pF/cm^2. In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance.

While it is possible to use PCB capacitance in place of small discrete capacitors, the dielectric properties of common PCB substrate materials cause such capacitors to behave poorly. They have a rather high temperature coefficient and poor Q at high frequencies, which makes them unsuitable for many applications. Boards made with lower-loss dielectrics such as Teflon are expensive exceptions to this rule.

Capacitive Noise and Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a change of voltage on one, there will be a movement of charge on the other. A basic model for this is shown in Figure 9.48.



Z_1 = CIRCUIT IMPEDANCE
$Z_2 = 1/j\omega C$

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

Figure 9.48: *Capacitive Coupling Equivalent Circuit Model*

It is evident that the noise voltage, $V_{COUPLED}$ appearing across Z_1, may be reduced by several means, all of which reduce noise current in Z_1. They are reduction of the signal voltage V_N, reduction of the frequency involved, reduction of the capacitance, or reduction of Z_1 itself. Unfortunately however, often none of these circuit parameters can be freely changed, and an alternate method is needed to minimize the interference. The best solution towards reducing the noise coupling effect of C is to insert a grounded conductor, also known as a *Faraday shield*, between the noise source and the affected circuit. This has the desirable effect of reducing Z_1 noise current, thus reducing $V_{COUPLED}$.

A Faraday shield model is shown by Figure 9.49. In the left picture, the function of the shield is noted by how it effectively divides the coupling capacitance, C. In the right picture the net effect on the coupled voltage across Z_1 is shown. Although the noise current I_N still flows in the shield, most of it is now diverted away from Z_1. As a result, the coupled noise voltage $V_{COUPLED}$ across Z_1 is reduced.

A Faraday shield is easily implemented and almost always successful. Thus capacitively coupled noise is rarely an intractable problem. However, to be fully effective, a Faraday shield must completely block the electric field between the noise source and the shielded circuit. It must also be connected so that the displacement current returns to its source, without flowing in any part of the circuit where it can introduce conducted noise.

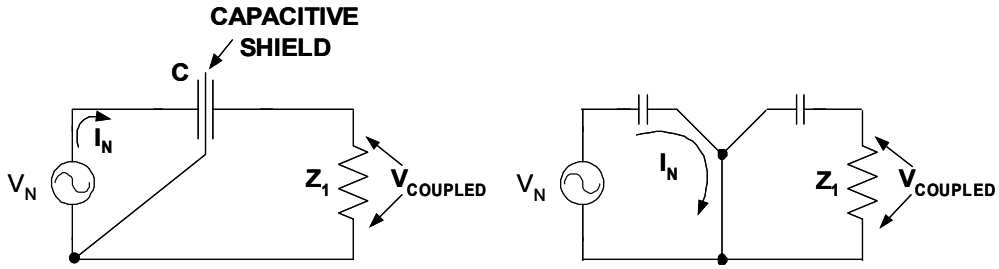


Figure 9.49: *An Operational Model of a Faraday Shield*

The Floating Shield Problem

And, it is quite important to note here—*a conductor that is intended to function as a Faraday shield must never be left floating, as this almost always increases capacity and exacerbates the noise problem*!

An example of this "floating shield" problem is seen in side-brazed ceramic IC packages. These DIP packages have a small square conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected.

Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Alas, many analog circuits don't have a ground pin at a package corner, and the lid is left floating—acting as an antenna for noise. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is completely unshielded.

Whenever practical, it is good practice for the user to ground the lid of any side brazed ceramic IC where the lid is not grounded by the manufacturer, thus implementing an *effective* Faraday shield. This can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip or conductive paint from the lid to the ground pin may be used to make the ground connection,.

A safety note is appropriate at this point. Never attempt to ground such a lid without first verifying that it is unconnected. Occasionally device types are found with the lid connected to a power supply rather than to ground!

A case where a Faraday shield is impractical is between IC chip bondwires. This can have important consequences, as the stray capacitance between chip bondwires and associated leadframes is typically ≈ 0.2 pF, with observed values generally between 0.05 and 0.6 pF.

Buffering ADCs Against Logic Noise

If we have a high resolution data converter (ADC or DAC) connected to a high speed data bus which carries logic noise with a 2-5 V/ns edge rate, this noise is easily connected

to the converter analog port via stray capacitance across the device. Whenever the data bus is active, intolerable amounts of noise are capacitively coupled into the analog port, thus seriously degrading performance.

This particular effect is illustrated by the diagram of Figure 9.50, where multiple package capacitors couple noisy edge signals from the data bus into the analog input of an ADC.

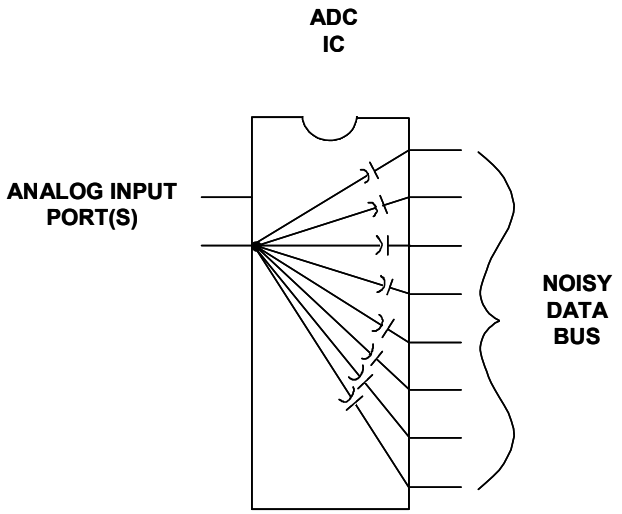
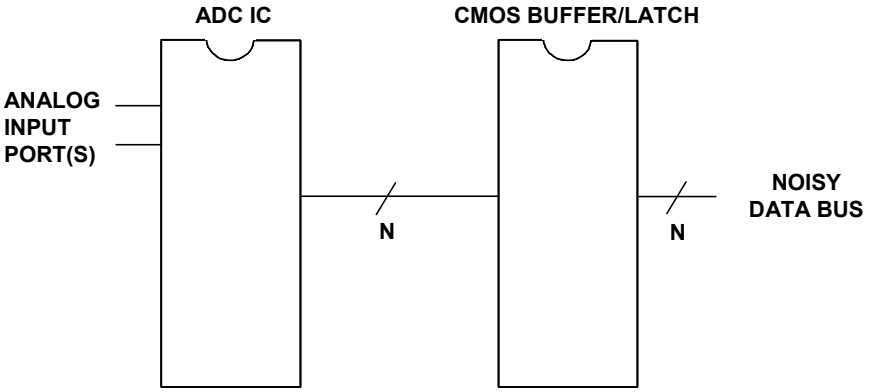


Figure 9.50: *A High Speed ADC IC Sitting on a Fast Data Bus Couples Digital Noise into the Analog Port, Thus Limiting Performance*

Present technology offers no cure for this problem, within the affected IC device itself. The problem also limits performance possible from other broadband monolithic mixed signal ICs with single-chip analog and digital circuits. Fortunately, this coupled noise problem can be simply avoided, by *not* connecting the data bus directly to the converter.

Instead, *use a CMOS latched buffer as a converter-to-bus interface*, as shown by Figure 9.51. Now the CMOS buffer IC acts as a Faraday shield, and dramatically reduces noise coupling from the digital bus. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power, and it complicates the design—but it does improve the signal-to-noise ratio of the converter! The designer must decide whether it is worthwhile for individual cases, but in general it is highly recommended.

Bus switches can also be utilized to isolate data lines from buses as described later in this chapter.



- THE OUTPUT BUFFER/LATCH ACTS AS A FARADAY SHIELD BETWEEN "N" LINES OF A FAST, NOISY DATA BUS AND A HIGH PERFORMANCE ADC.
- THIS MEASURE ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY, AND MOST IMPORTANTLY, *IMPROVED PERFORMANCE!*

Figure 9.51: *A High Speed ADC IC Using a CMOS Buffer/Latch at the Output Shows Enhanced Immunity of Digital Data Bus Noise*

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ACKNOWLEDGEMENTS:

Portions of this section were adapted from Doug Grant and Scott Wurcer, "Avoiding Passive Component Pitfalls", originally published in **Analog Dialogue 17-2**, 1983.