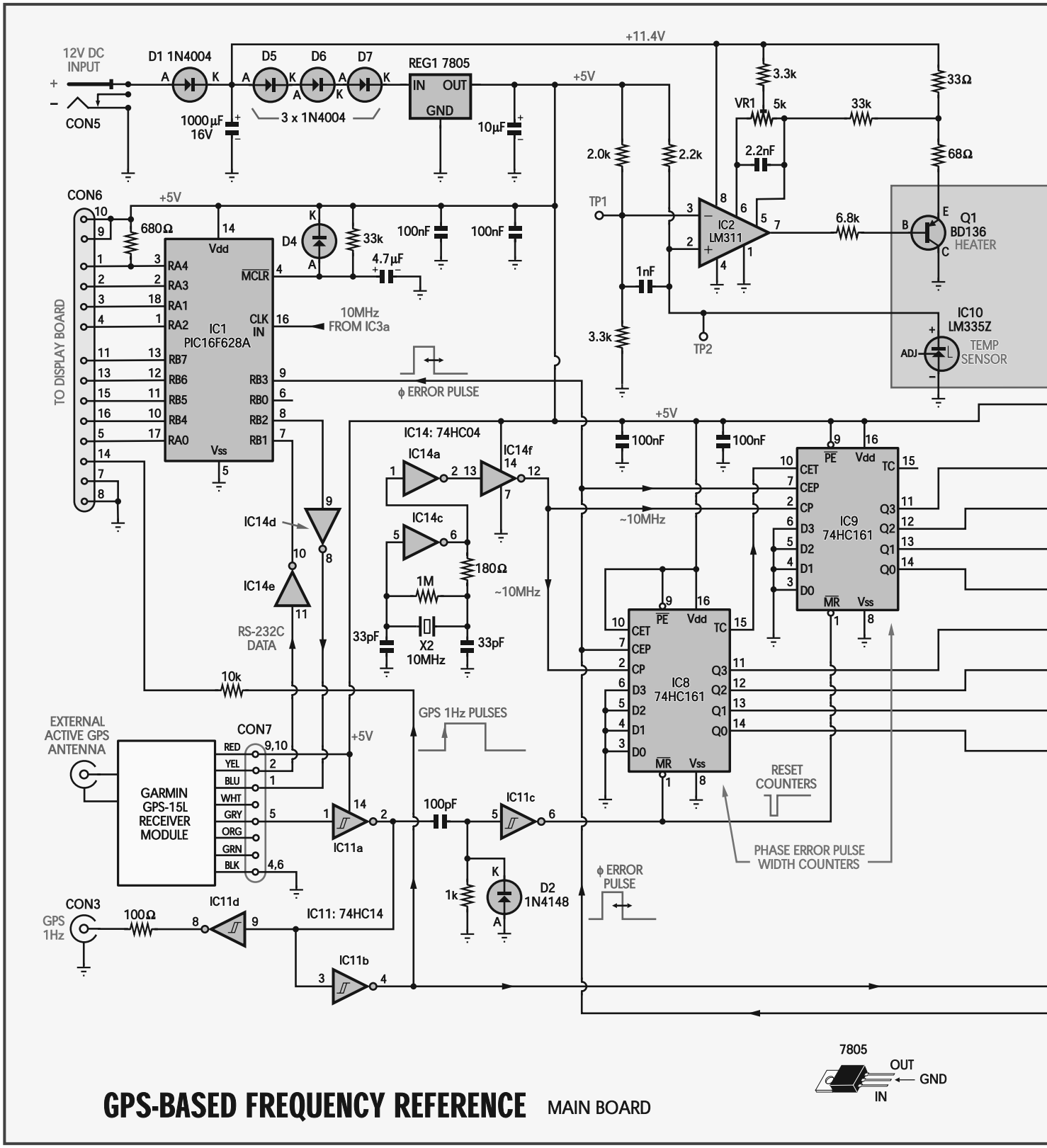

which act as buffer stages. The resulting 5V peak-to-peak pulses from IC11b are then fed directly to pin 14 of IC7, which is the phase comparator.

The 10MHz crystal oscillator that's phase-locked to the GPS pulses is based on inverter IC3f and crystal X1, plus varicap diode VC1 and several low-value capacitors. Its 10MHz output is fed via inverting buffer stage IC3b to CON1 and also via IC3c to divider stage IC4. This stage divides the signal by 10 and provides two 1MHz outputs, at pins 12 and 15. Pin 12 output is then fed via inverter IC3d to CON2, to provide the 1MHz output signal at BNC connector CON2.

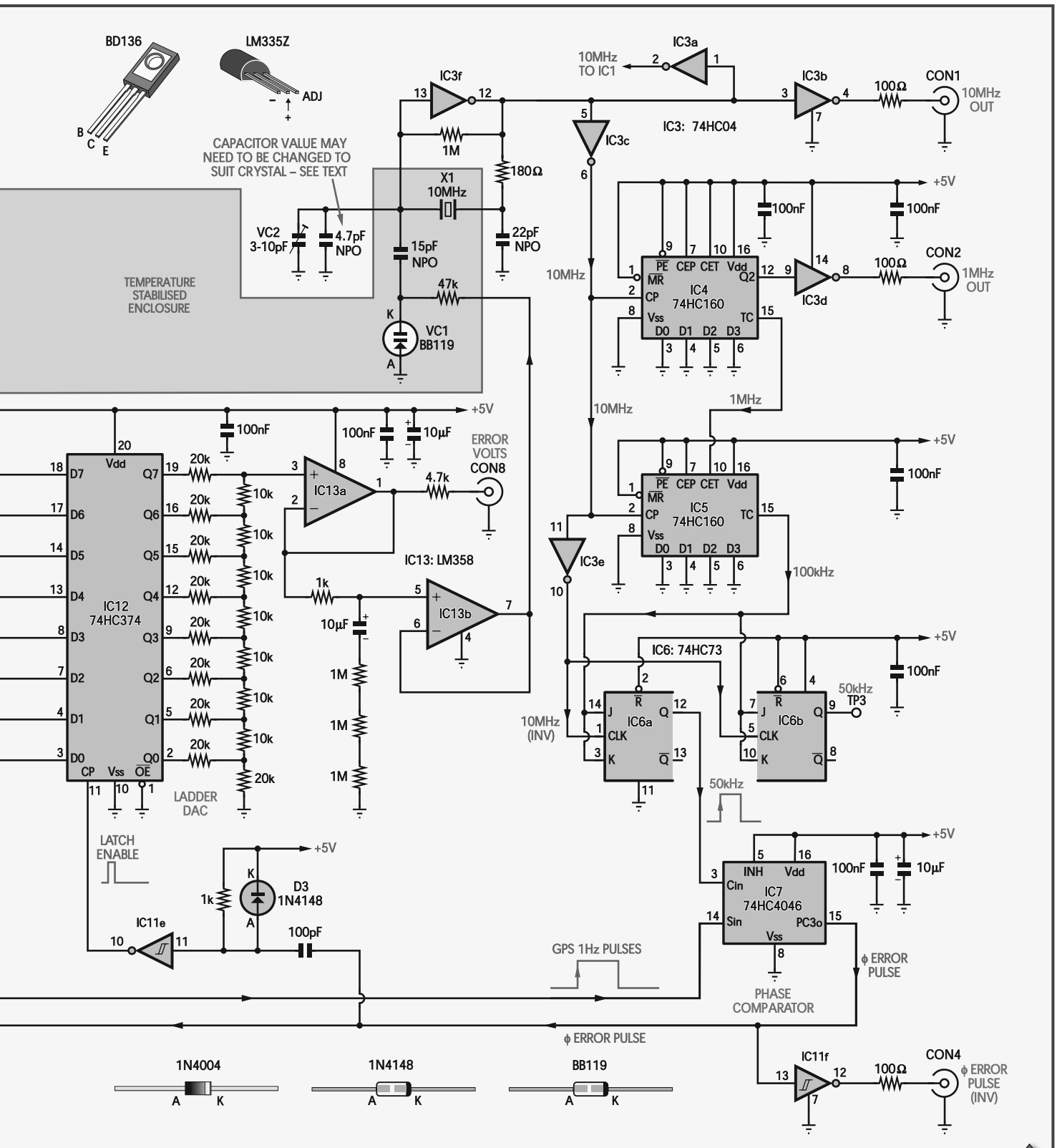

Fig.2 (above): the complete circuit for the GPS-Based Frequency Reference except the display circuitry (LCD and LED indicators). The PLL-controlled 10MHz oscillator is built into a small temperature-controlled oven to ensure stability, with power transistor Q1 acting as the oven heater.

By contrast, the 1MHz pulse output from pin 15 is fed to a second divide-by-10 stage based on IC5 (ie, to the CET input at pin 10). The resulting 100kHz pulse output from pin 15 of IC5 is then fed to the J and K inputs of flip-flops IC6a and IC6b. Note that the 10MHz output from IC3c is used to clock IC5, IC6a and IC6b, the latter two stages via inverter IC3e. This ensures that the counter and divider outputs are correctly synchronised.