Green-Mode PWM Controller with HV Start-Up Circuit and Soft Start time Adjustment

REV. 00

General Description

The LD7752B brings high performance, highly integrated functions, protections and EMI-improve solution. It's an ideal solution for those cost-sensitive system, reducing component count and overall system cost.

The LD7752B features high voltage startup circuit, minimum loss and green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. They also consist of more protections of OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent the circuit from damage under abnormal conditions.

Furthermore, the proprietary frequency swapping function can reduce the noise and help the power circuit designers to enhance EMI performance with fewer components and less developing time.

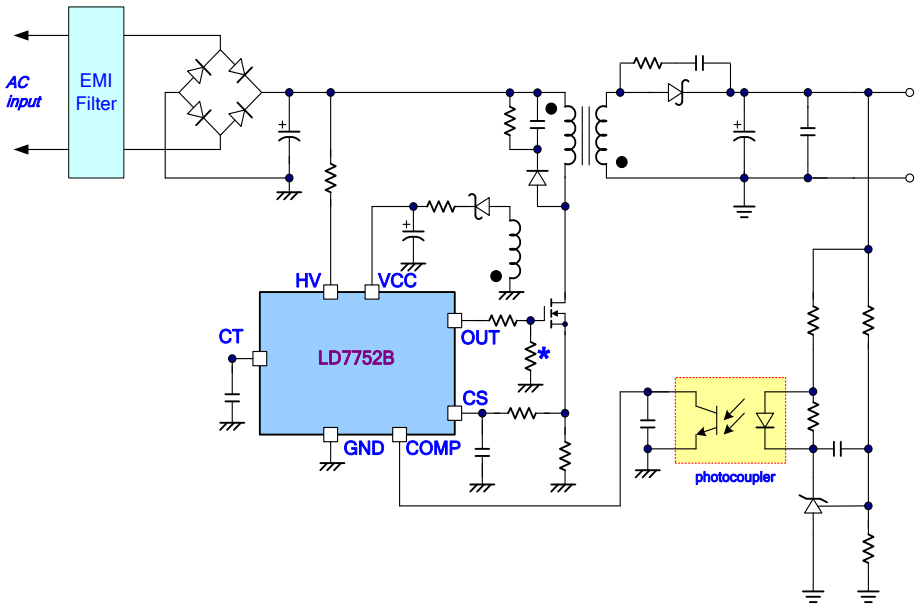
Features

- High-Voltage Startup Circuit
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency swapping
- Internal Slope Compensation
- Internal OCP Compensation
- OVP (Over Voltage Protection) on Vcc Pin
- OLP (Over Load Protection)
- +250mA/-500mA Driving Capability
- Soft-Driving
- Soft Start Time and Grouping Frequency Adjustment

Applications

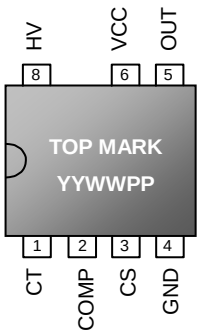
- LCD Monitor/TV Power
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application

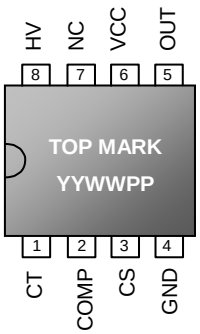


Pin Configuration

SOP-7 (TOP VIEW)



SOP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

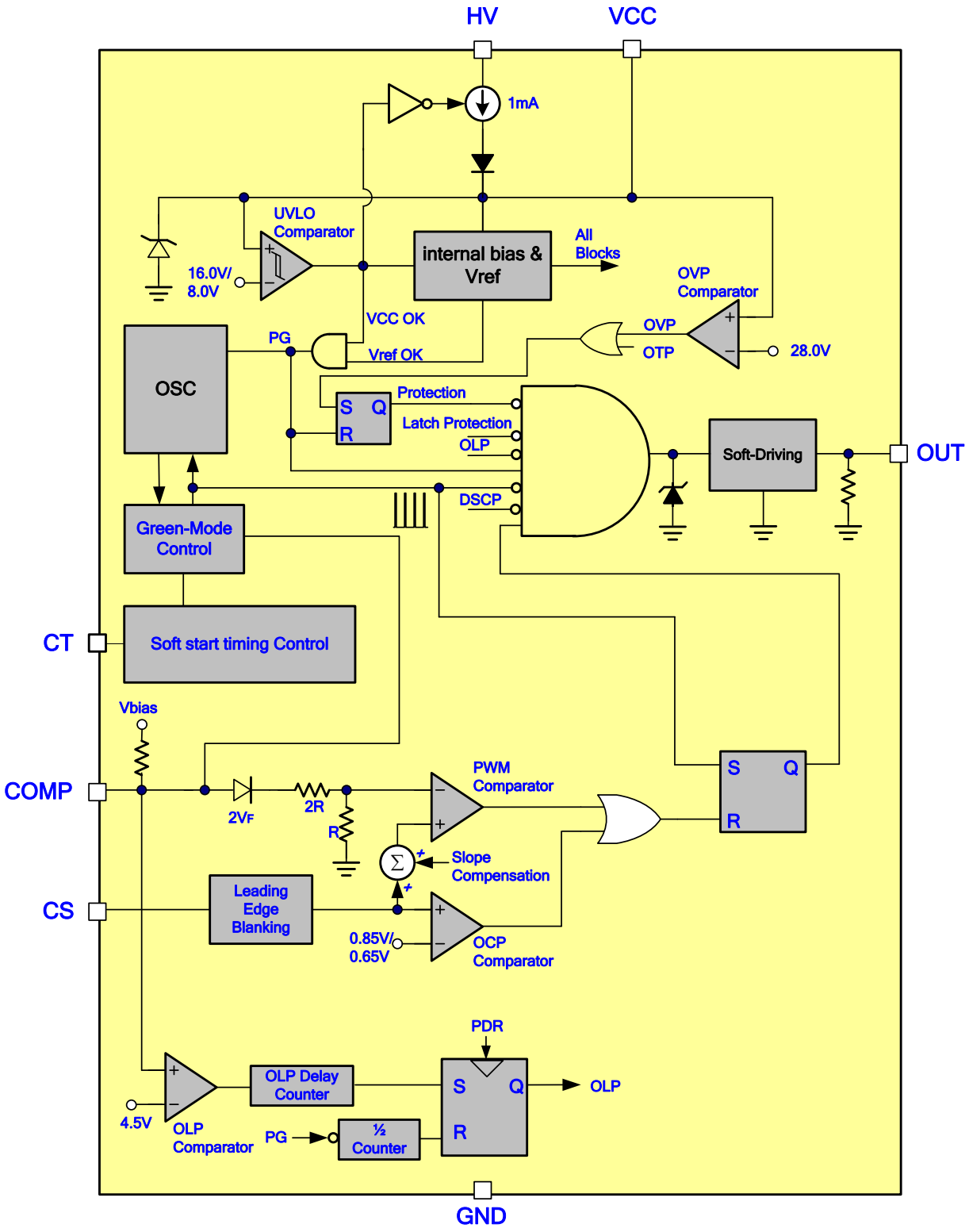
Part number	Switching Freq.	Package	Top Mark	Shipping
LD7752B GS	100kHz	SOP-8	LD7752B GS	2500 /tape & reel
LD7752B GR	100kHz	SOP-7	LD7752B GR	2500 /tape & reel

The LD7752B is ROHS compliant/ Green Packaged.

Pin Descriptions

PIN	NAME	FUNCTION
1	CT	Soft start time adjustment.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve regulation.
3	CS	Current sense pin, connect it to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin with positive terminal of bulk capacitor to provide startup current for the controller. As Vcc voltage trips to UVLO (on), this HV loop will be disabled to minimize power loss through the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V~30V
High-Voltage Pin, HV	-0.3V~500V
COMP, OTP, CS	-0.3 ~6V
OUT	-0.3 ~VCC+0.3V
Maximum Junction Temperature	150°C
Operating Junction Temperature Range	-40°C to 125°C
Operating Ambient Temperature	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8/ SOP-7, θ_{JA})	160°C/W
Power Dissipation, PD@85°C (SOP-8/ SOP-7)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	2.5KV
ESD Voltage Protection, Machine Model (except HV Pin)	250V
ESD Voltage Protection, Human Body Model (HV Pin)	1KV
ESD Voltage Protection, Machine Model (HV pin)	250V
Gate Output Current	250mA/-500mA

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Supply Voltage Vcc	9.5V to 26V
VCC Capacitor	10 to 47μF
COMP Capacitor Value	1~100nF
CT Capacitor Value	22~330nF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin, HV MOS process)					
High-Voltage Current Source	V_{CC} < UVLO(on)	1.1	1.3	1.5	mA
Off-State Leakage Current	V_{CC} > UVLO(off), HV=500V			15	μA
Supply Voltage (VCC Pin)					
Startup Current	V_{CC}=15V, HV=500V	100	150	200	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		0.55		mA
	V_{COMP}=3V		2.0		mA
	OLP tripped		230		μA
	OVP tripped, VCC=OVP		230		μA
UVLO (OFF)		7.0	8.0	9.0	V
UVLO (ON)		15.0	16.0	17.0	V
OVP Level	.	27.0	28.0	29.0	V
Voltage Feedback (COMP Pin)					
Short Circuit Current	V_{COMP}=0V	0.14	0.17	0.20	mA
Open Loop Voltage	COMP pin open	5.10	5.30	5.50	V
Fixed Frequency Mode Threshold VCOMP(*)			2.5		V
Green Mode Threshold VCOMP(*)	25kHz		2.1		V
Burst Mode Threshold VCOMP			1.60		V
Current Sensing (CS Pin)					
V_{CS-OFF}		0.80	0.85	0.90	V
V_{CS-MIN}		0.60	0.65	0.7	V
Leading Edge Blanking Time			250		ns
Delay to Output			100		ns
Oscillator for Switching Frequency					
Frequency		94.0	100	106	kHz
Temp. Stability(*)			5		%
Voltage Stability(*)	(V_{CC} =11V-25V)		1		%
Green Mode Frequency	100kHz		25		kHz
Frequency Swapping	100kHz		± 6.0		kHz
Maximum Duty			75		%

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output (OUT Pin)					
Output Low Level	V_{CC} =15V, Io=20mA			1	V
Output High Level	V_{CC} =15V, Io=20mA	9			V
Rising Time(*)	Load Capacitance=1000pF		50	160	ns
Falling Time(*)	Load Capacitance=1000pF		30	60	ns
OLP (Over Load Protection)					
OLP Trip Level		4.3	4.5	4.7	V
OLP Delay Time			84		ms
Soft start (CT Pin)					
Soft Start duration	CT pin = 0.033μF		3.8		ms
On Chip OTP (Over Temperature)					
OTP Level(*)			140		°C
OTP Hysteresis(*)			30		°C

Notes:

*Guaranteed by design.

Typical Performance Characteristics

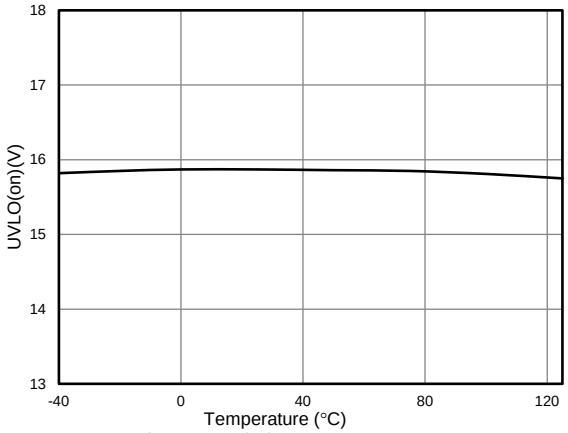


Fig. 1 UVLO(on) vs. Temperature

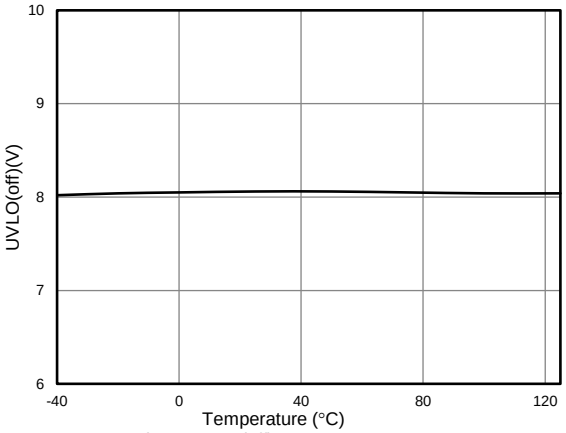


Fig. 2 UVLO(off) vs. Temperature

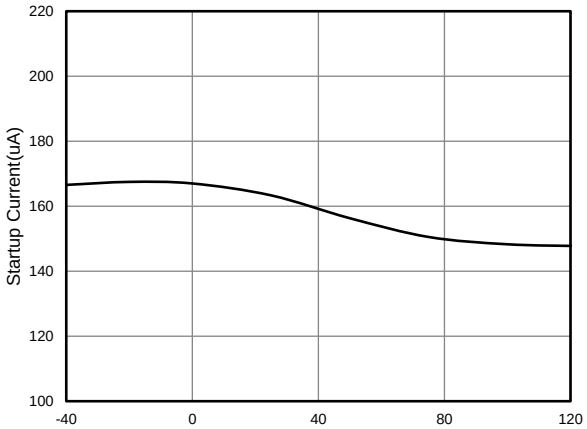


Fig. 3 Startup Current Ivcc vs.Temperature

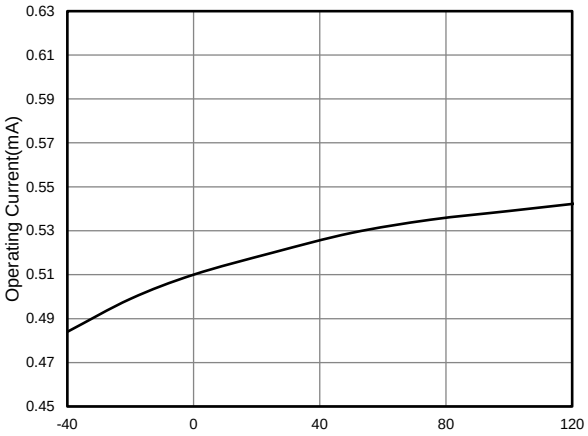


Fig. 4 Operating Current v.s.Temperature

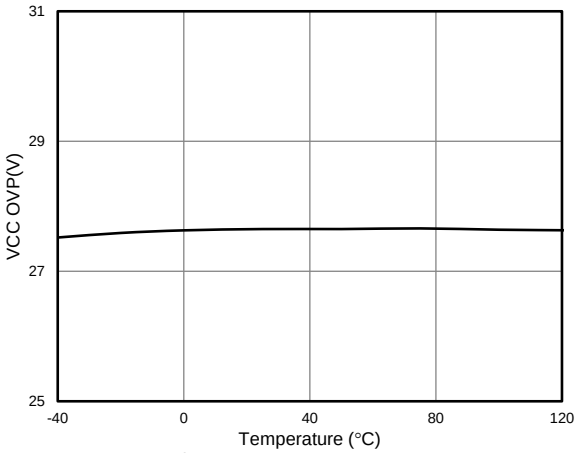


Fig. 5 VCC OVP vs.Temperature

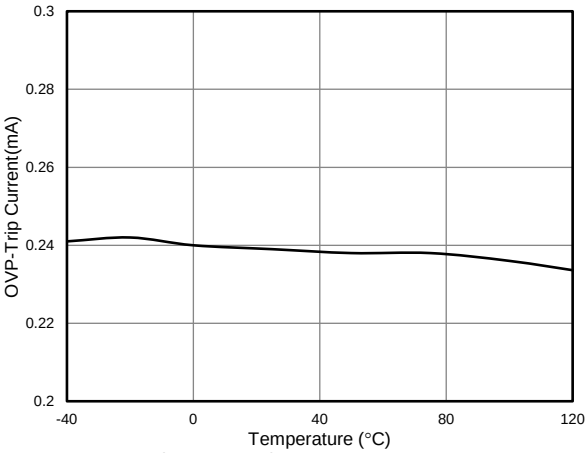


Fig. 6 OVP-Trip Current vs.Temperature

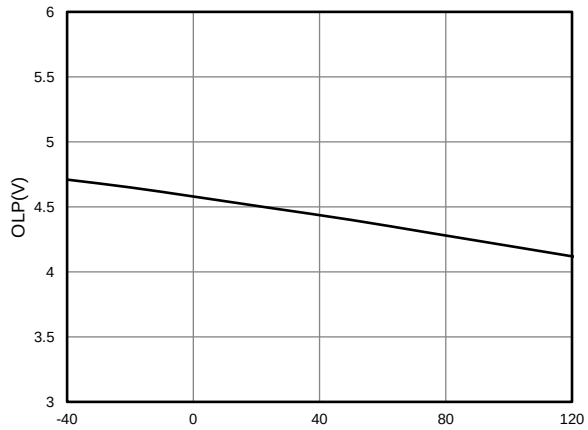


Fig. 7 OLP-Trip Level vs.Temperature

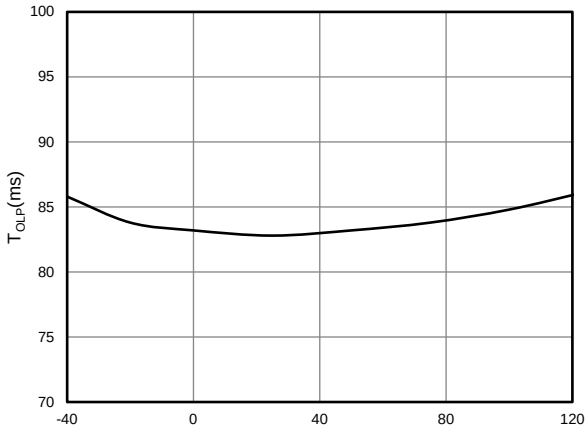


Fig. 8 OLP Delay Time vs.Temperature

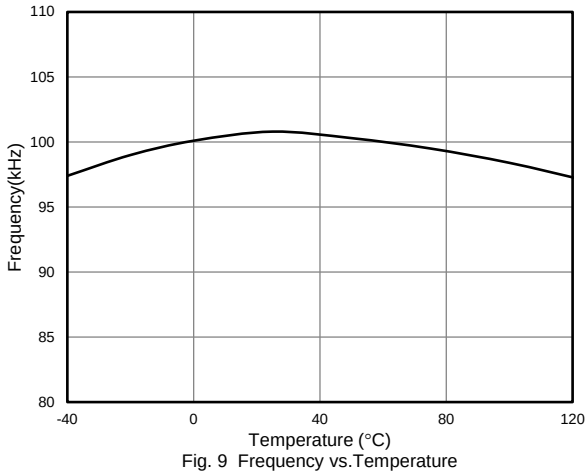


Fig. 9 Frequency vs.Temperature

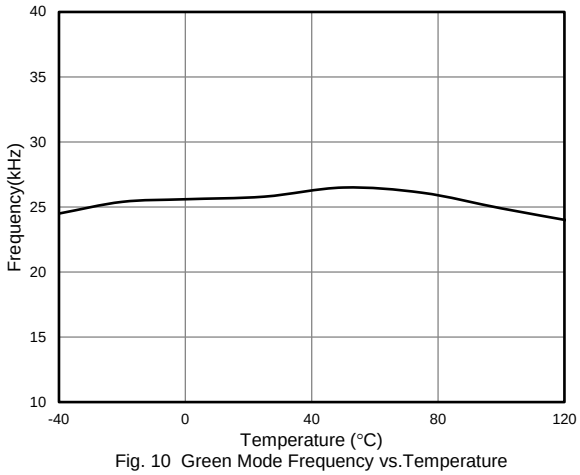


Fig. 10 Green Mode Frequency vs.Temperature

Application Information

Operation Overview

The LD7752B meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

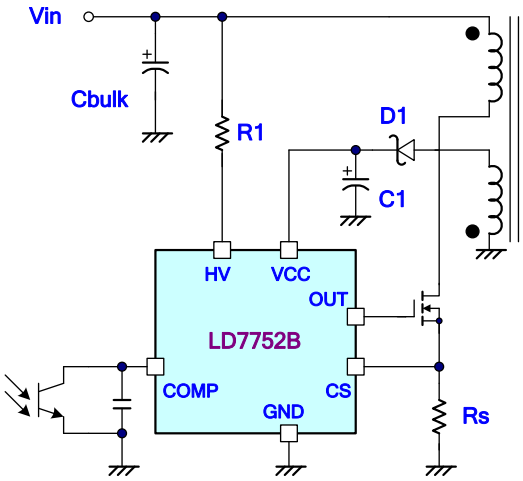


Fig. 7

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power. In most cases, startup resistors carry large resistance. And larger resistance spends more time to startup.

To achieve optimized topology, as shown in Fig. 7, LD7752B is designed with high-voltage startup circuit for it. At startup transient, the high-voltage current source sinks through the bulk capacitor to provide the startup current to charge the Vcc capacitor C1. During initialization, the Vcc drops below UVLO threshold to enable the current source to supply 1mA current. Since there's only 150μA required for startup, most of the HV current is reserved to charge the Vcc capacitor. With such configuration, it spends almost same time for turn-on delay either under low-line or high-line conditions.

As VCC trips UVLO(ON), HV pin would no longer charge the capacitor and instead, send a gate drive signal to draw supply current for VCC from the auxiliary winding of the transformer. That minimizes the power loss on the start-up circuit successfully.

An UVLO comparator is embedded to detect the voltage across the Vcc pin to monitor if the supply voltage is enough to power on the LD7752B and in addition to drive the power MOSFET. As shown in Fig. 8, a hysteresis is provided to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 8V, respectively.

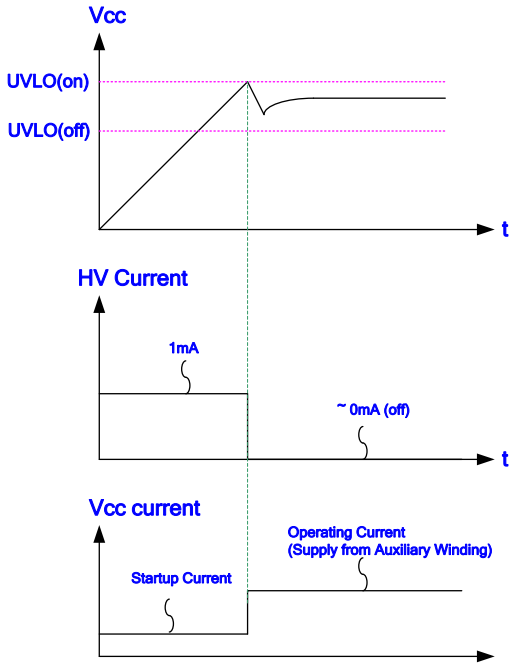


Fig. 8

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the

control loop and achieve regulation. The LD7752B detects the primary MOSFET current over CS pin for the peak current mode control and also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. Thus the MOSFET peak current is calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 250nS leading-edge blanking (LEB) time is programed in the input of CS pin to prevent false-triggering from the current spike. For most low power applications, the R-C filter (as shown in Fig.9) is eliminable if the total pulse width of the turn-on spikes is less than 250nS and the negative spike on the CS pin does not exceed -0.3V.

However, the total pulse width of the turn-on spike is subject to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in Fig. 10) for larger power applications to avoid the CS pin from being damaged by the negative turn-on spike.

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer with typical 250mA source and 500mA sink driving capability is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7752B is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is delivered from the TL431 on the secondary side through the photo-coupler to the COMP pin. The input stage of LD7752B, as UC384X, consists of 2 diodes voltage offset to feed the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit.

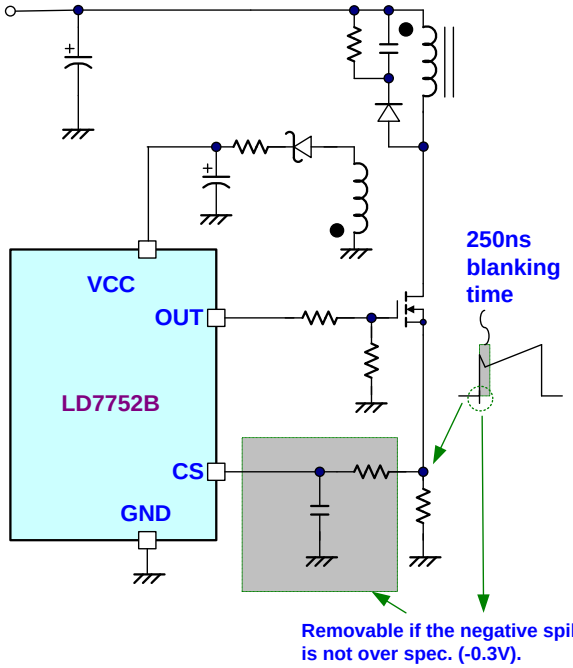


Fig. 9

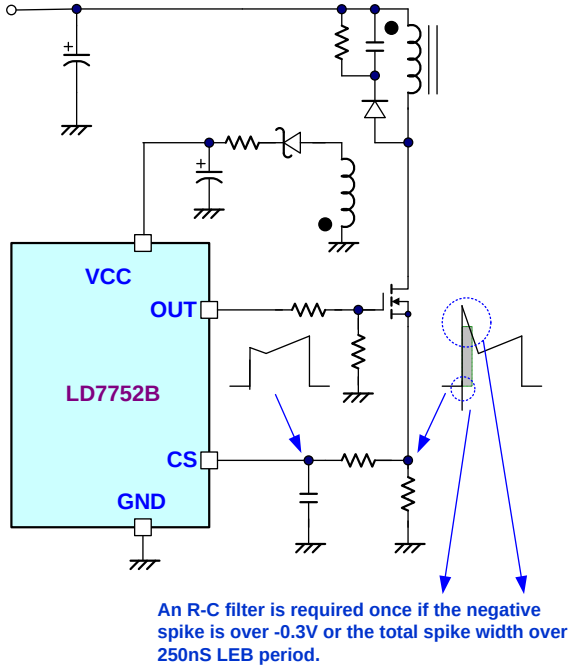


Fig. 10

Oscillator and Switching Frequency

The switching frequency of LD7752B is fixed at 100kHz internally to optimize the operation in consideration of the EMI performance, thermal treatment, component sizes and transformer design.

Adjustable Grouping Frequency and Soft Start on CT Pin

In order to prevent the acoustic noise from grouping frequency Fg, adjust the external capacitance of CT pin and the soft start time for it according to the below table. The grouping frequency is limited from 600Hz to 1.80KHz

C_{CT} (nF)	Grouping frequency Fg (KHz)	Soft start time Tss (mS)
22nF	1.2~1.8	≈ 3.0
33nF	0.8~1.3	≈ 3.8
47nF	0.6~1.0	≈ 6.0

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, slope compensation is required in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. Well, LD7752B requires none of it since there's a built-in slope compensation circuit to simplify the external circuit design.

On/Off Control

Pulling COMP pin below 1.6V will disable the gate output pin of LD7752B immediately. The off mode will be released soon as the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are various topologies for chips to meet green-mode or power saving requirements, such as "burst-mode control", "skipping-cycle mode", "variable off-time control "…etc. The basic operation theory of all these approaches intends to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

With LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from being damaged in over-load, short or open loop condition, the LD7752B is implemented with smart OLP function. It also features auto recovery function; see Fig. 11 for the waveform. If in fault condition, the feedback system will force the voltage loop enter toward the saturation and then pull the voltage high over COMP pin (V_{COMP}). When the V_{COMP} ramps up over OLP threshold of 4.5V and stays for more than OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

A divide-2 counter is implemented to reduce the average power under OLP behavior. As soon as OLP is activated, the output will be latched off and the divide-2 counter starts to count the numbers of UVLO(off). The latch will be released when the 2nd UVLO(off) point is tripped, then the output will recover to switch again.

With the protection mechanism, it minimizes the average input power to control the component's temperature and stress within the safe operating area.

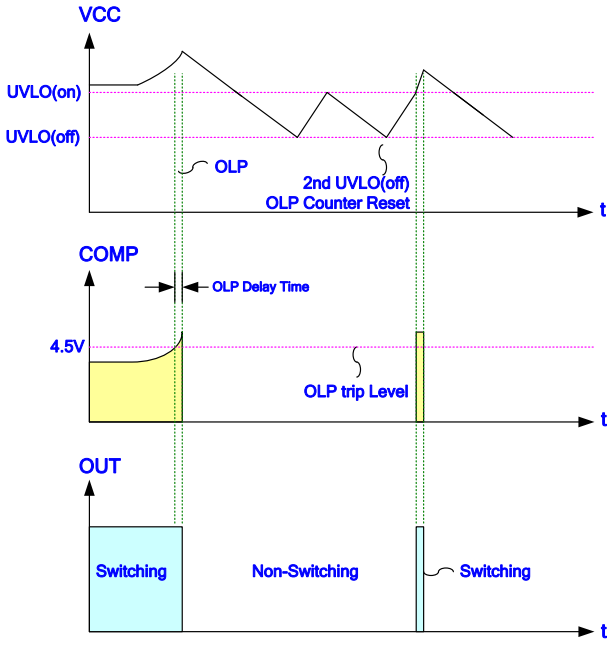


Fig. 11

OVP (Over Voltage Protection) on Vcc - Auto Recovery

The maximum V_{GS} ratings of the power MOSFETs are mostly set at 30V. To prevent the V_{GS} from damage in fault condition, LD7752B is embedded with OVP function on Vcc. Once the Vcc voltage rises above OVP threshold, it shuts down output gate drive circuit simultaneously and disable the switching of the power MOSFET until the next UVLO(on) is reached.

The LD7752B possess auto-recoverable Vcc OVP functions. The OVP condition usually comes with open-loop of feedback. Before it's released, the Vcc will trip to OVP level and shutdown the output again. The Vcc works in hiccup mode. Fig. 12 shows its operation.

Otherwise, soon as the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

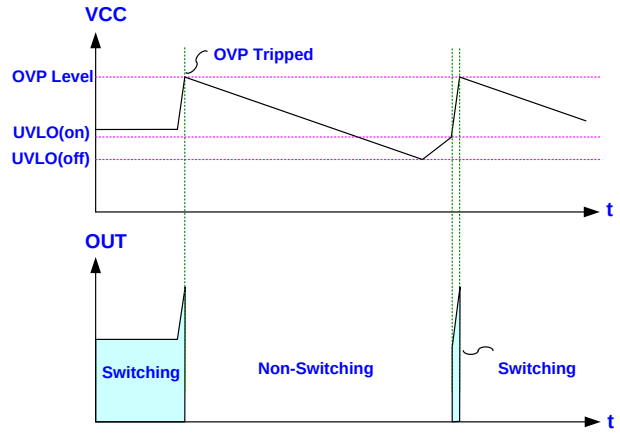


Fig. 12

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7752B consists of an anti-floating resistor on the OUT pin to protect the output from abnormally operation or false triggering of MOSFET. Even so, we still recommend adding an external one at the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In single-fault condition, as shown in Fig. 13, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET is always pulled low and placed in the off-state either as the gate resistor is disconnected or opened.

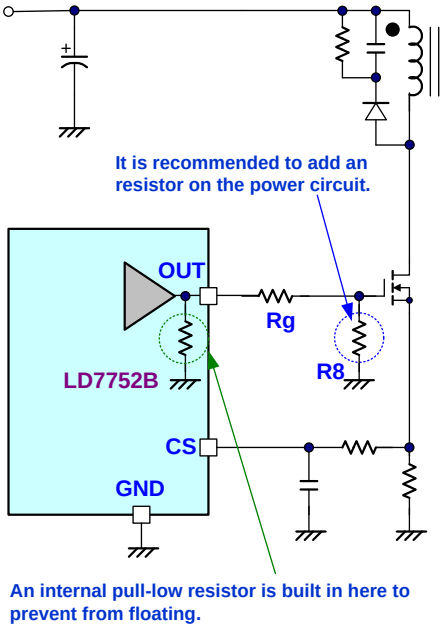


Fig. 13

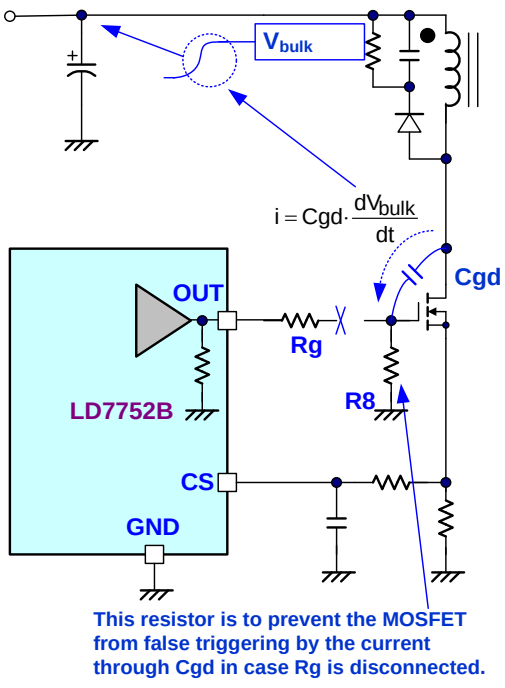


Fig. 14

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, Vcc and GND. As shown in Fig. 15, any small negative spike on the HV pin may trigger this parasitic SCR and cause latch-up between Vcc and GND. It will damage the chip because of the equivalent short-circuit induced by the latch-up behavior.

With Leadtrend's proprietary of Hi-V technology, the LD7752B is free from parasitic SCR. Fig. 10 shows the equivalent circuit for it. The LD7752B is stronger to sustain negative voltage than the other similar products. However, a 10KΩ resistor is recommended to add on the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

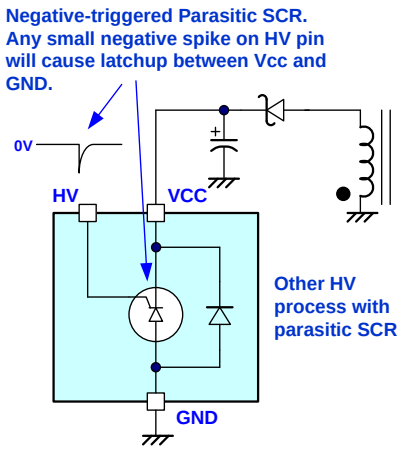


Fig. 15

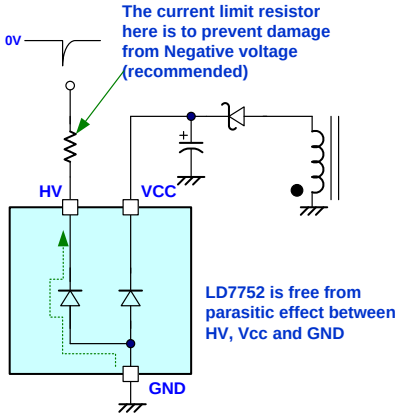


Fig. 16

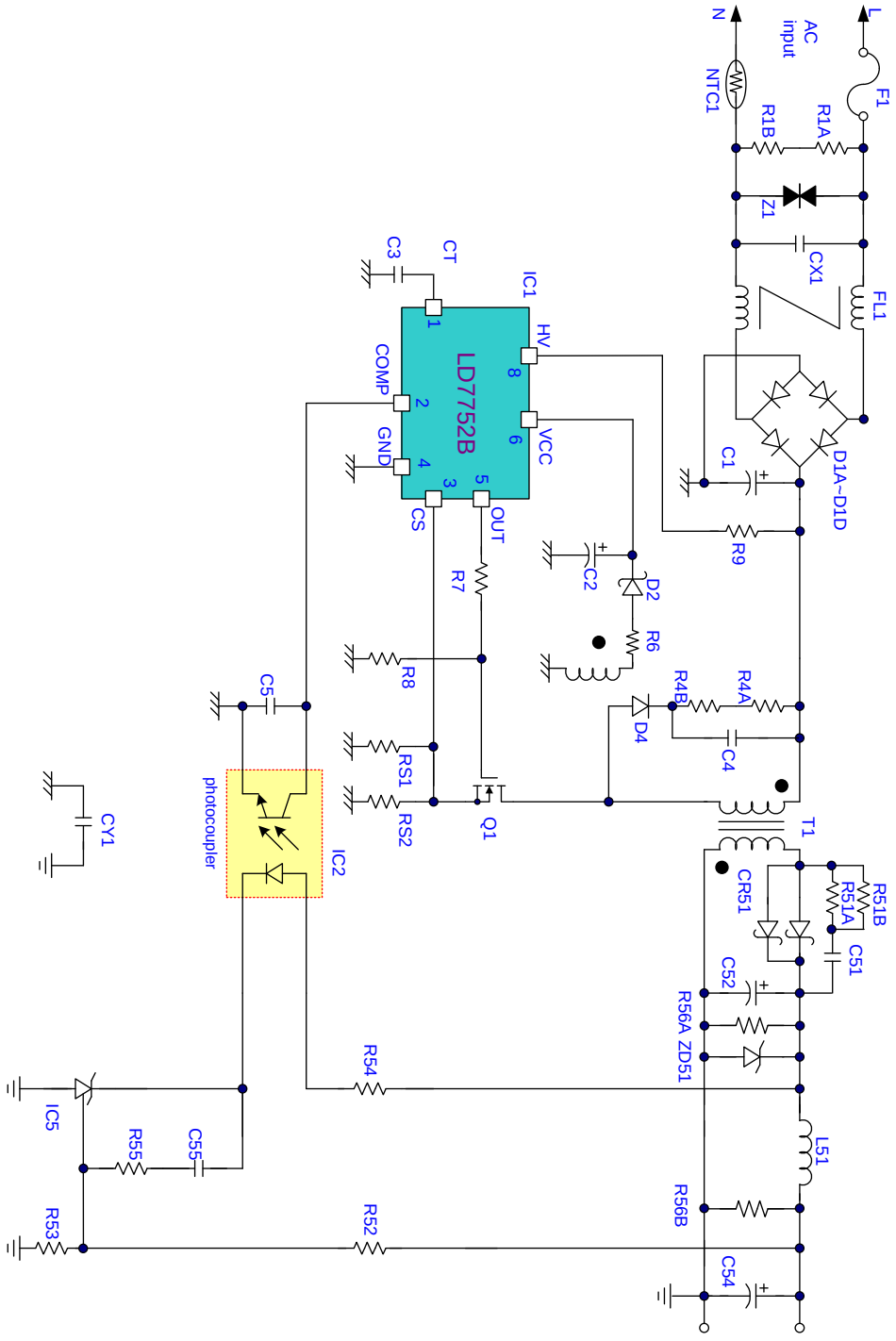
Frequency Swapping

The LD7752B is built-in with programmable frequency swapping function. It enables the power supply designers to optimize EMI performance and system cost. The Frequency Swapping was internally set at ±4KHz when incorporating with 100KHz switching frequency.

On-Chip OTP – Auto Recovery

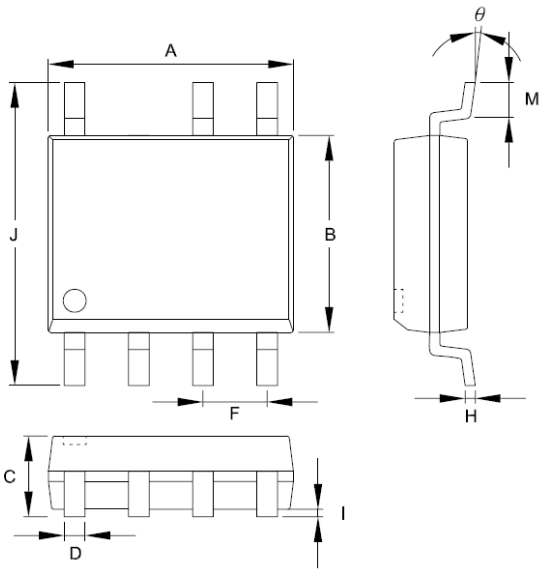
An internal OTP circuit is embedded to provide the worst-case protection for this controller. If the chip temperature rises over the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

Reference Application Circuit --- 10W (5V/2A) Adapter



Package Information

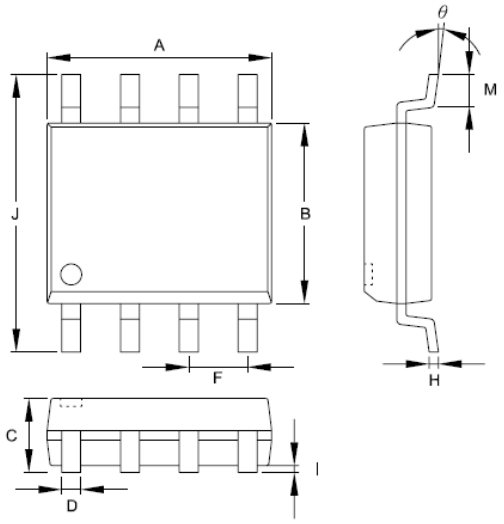
SOP-7



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

Rev.	Date	Change Notice
00	6/11/2013	Original Specification