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 some parametric limits are subject to change.

MITSUBISHI SOUND PROCESSORS

# M62463AFP

Dolby Pro Logic Surround Decoder

## Description

The M62463AFP is a Single Chip Dolby Pro Logic Surround Decoder. This LSI has all of required functions for Dolby Pro Logic Surround.

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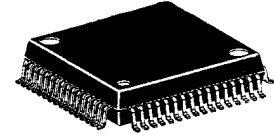
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Licensing and application information may be obtained from Dolby Lab.

## Features

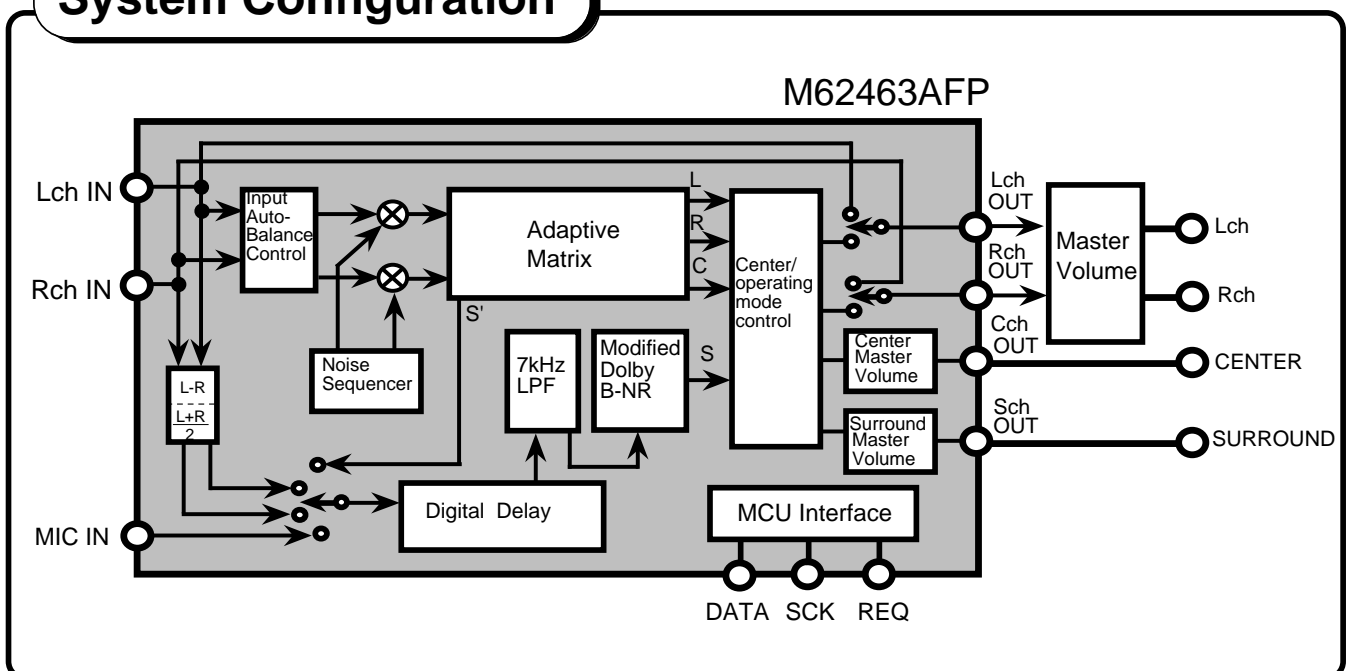
- Includes all functions necessary for Dolby Pro Logic Surround
  - Adaptive Matrix
  - Input Auto-Balance
  - Noise Sequencer
  - Center Mode Control ON/OFF, WIDE/NORMAL/PHANTOM
  - Modified Dolby B type Noise Reduction
  - 4 channel (Lch/Rch/Cch/Sch) / 3 channel (Lch/Rch/Cch)
  - Digital delay Delay time: 15.4 to 51.2msec
- Cch/Sch Master Volume 0 to -87dB/1dB step, -
- 3-lines MCU control
- Space Surround such as Disco, Hall and Live
- Digital Echo for Karaoke Function Delay time 123,184msec
- Current control oscillation circuit for system clock

## Outline



Outline 64P6N  
 0.8mm pitch QFP  
 (14.0mmx14.0mmx2.8mm)

## System Configuration



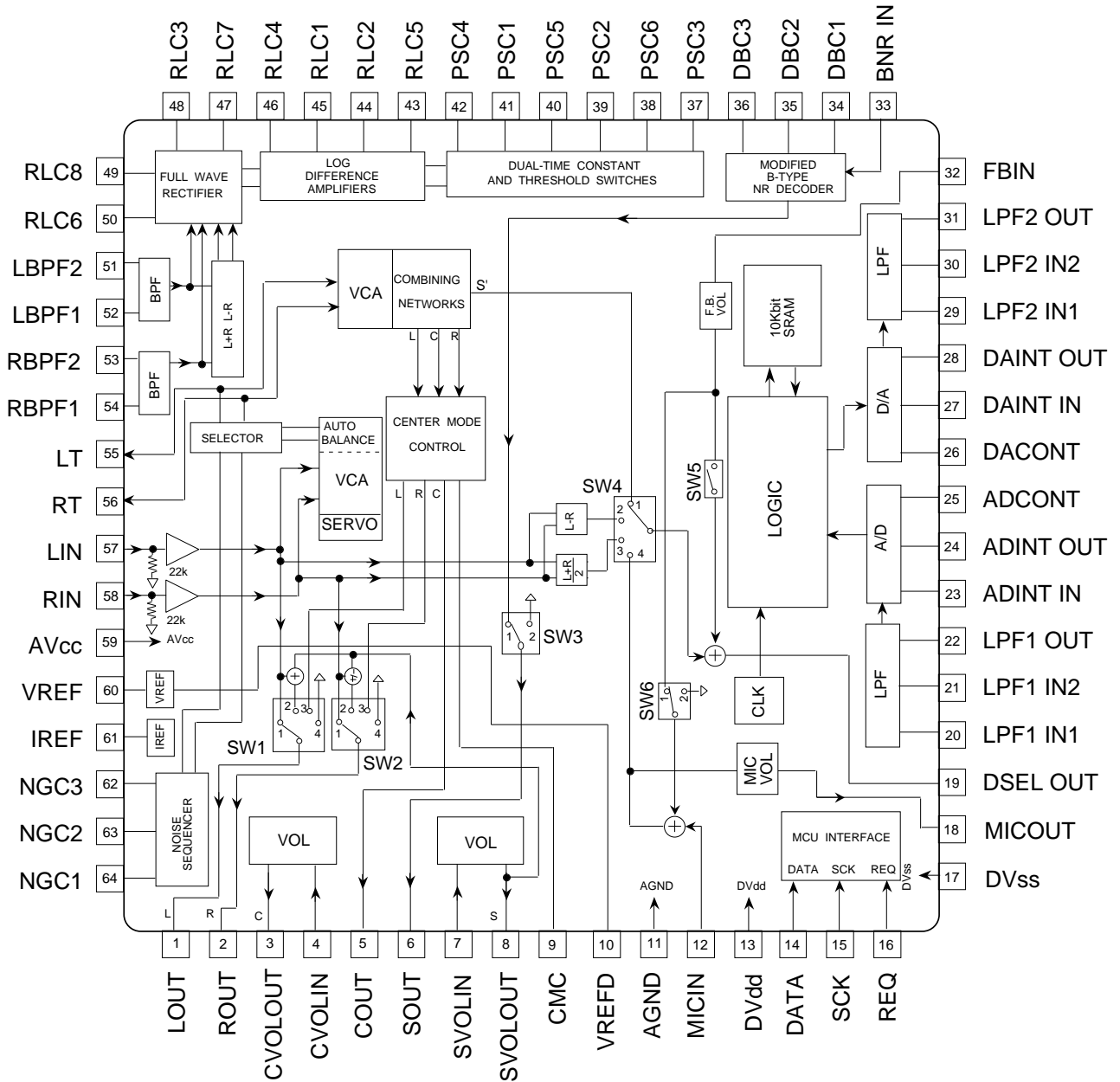
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## Pin Configuration



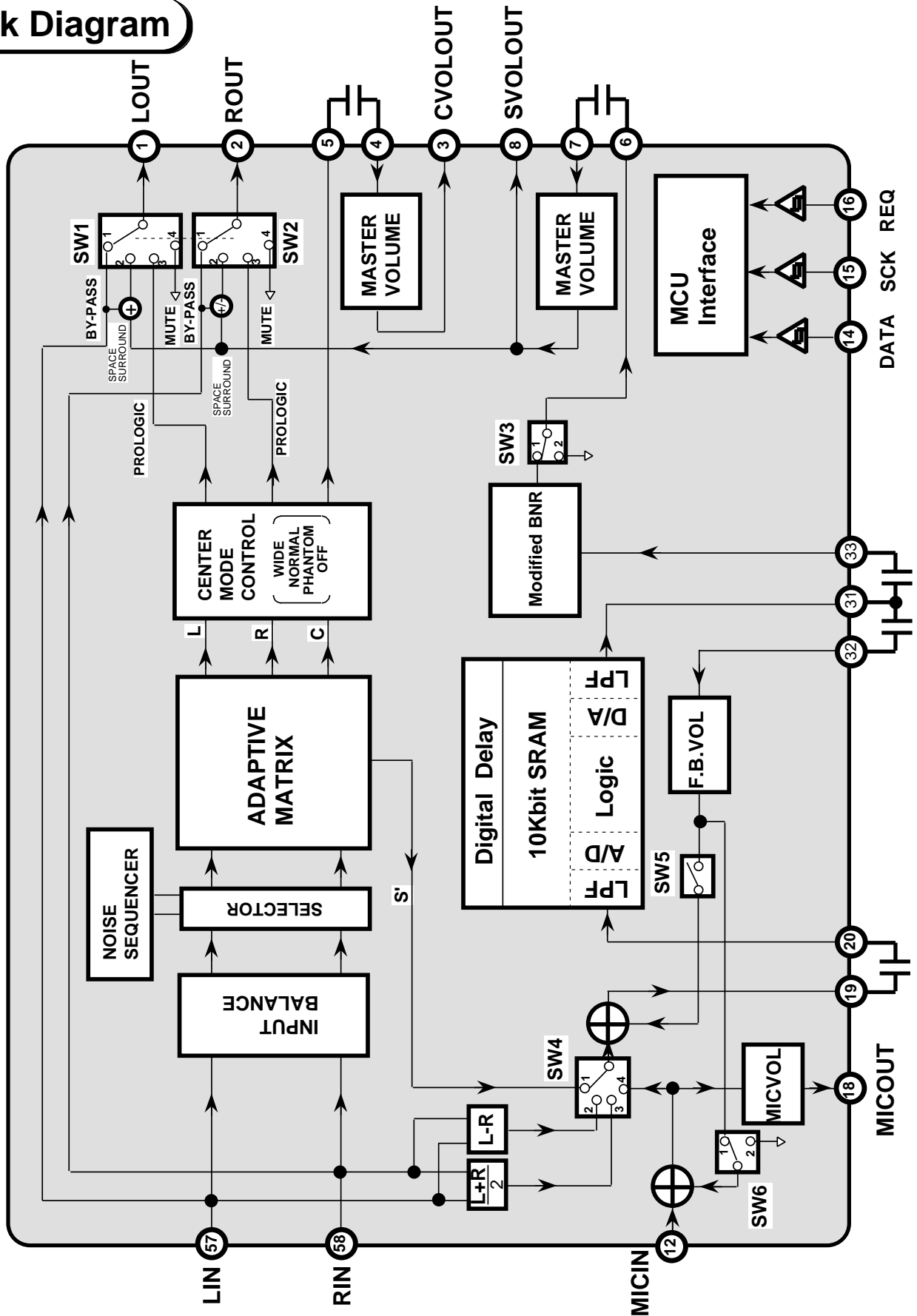
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## Block Diagram



**FUNCTIONAL DESCRIPTION**

FUNCTION		DESCRIPTION
1	Fundamental function for Dolby Pro Logic Surround Decoder	-Adaptive Matrix -Input Auto-Balance -Noise Sequencer -Center Mode Control ON/OFF WIDE/NORMAL/PHANTOM -Modified Dolby B type Noise Reduction -4ch(L,R,C,S), 3ch(L,R,C) Mode Switch
2	RAM for Digital Delay	10K-bit RAM
3	Surround Delay Time	15.4, 20.5, 25.6, 29.2msec (for Dolby Pro Logic Surround) 51.2msec (for Space Surround)
4	Circuit for Space Surround	Digital delay circuit can be used for Space Surround such as a Disco, Hall or Live, and Karaoke echo.
5	Echo delay time	123,184 msec
6	Feedback Volume	Delay Signal Feedback Volume -3 to -21 dB/3dB step, and -∞
7	Microphone Volume	Internal Microphone Volume 0 to -18 dB/3dB step, and -∞
8	Cch/Sch Master Volume	0 to -87dB/1dB step, and -∞
9	Bypass Switch	Bypass the decode circuit
10	Output Mute	Mute the Lch and Rch output
11	MCU Interface	Controlled by 3-lines serial data from MCU Including the Chip Address (2 bit)
12	Current control oscillation circuit	Including the oscillation circuit without external parts.

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## ABSOLUTE MAXIMUM RATINGS

(Ta=25°C Unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply Voltage		10.5	V
Vdd			6.5	V
Pd	Power Dissipation		1	W
Topr	Operating Temperature		-20 to +75	°C
Tstg	Storage Temperature		-40 to +125	°C

## RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Condition	Limits			Units
			Min	Typ	Max	
Vcc	Supply Voltage		8	9	10	V
Vdd			4.5	5	5.5	V
VIL	Input Voltage(L)	14,15,16pin	0	—	0.8	V
VIH	Input Voltage(H)	14,15,16pin	Vdd-1	—	Vdd	V

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## ELECTRICAL CHARACTERISTICS

(Ta=25°C, Vcc=9V, Vdd=5V, Cch volume=0dB, at C-OUT 0dBd=300mVrms, f=1kHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
<b>Total</b>						
Icc	Circuit current	No signal	—	25	40	mA
IDD	Circuit current	No signal	—	13	25	mA
<b>Auto-Balance</b>						
CPR	Capture range		—	5	—	dB
CER	Error collection		—	4	—	dB
<b>Adaptive Matrix</b>						
$\Delta$ VoL	Output level accuracy relative to Cch	L, R, Sch output	-0.5	0	0.5	dB
MR	Matrix rejection	L, R, C, Sch output	25	40	—	dB
HRAM	Head room	L, R, C, Sch output	15	17	—	dB
THDAM	Total harmonic distortion	L, R, Cch output 30kHzLPF	—	0.05	0.2	%
SNAM	S/N ratio	Rg=0, weighted CCIR/ARM 4ch mode	70	80	—	dB
<b>Noise Sequencer</b>						
Vno	Output noise level	L, R, C, Sch output	-15	-12.5	-10	dB
$\Delta$ Vno	Noise level accuracy relative to Cch	L, R, Sch output	-0.5	0	0.5	dB
<b>Modified B Noise Reduction (Sch Volume=0dB, 0dB reference is 300mVrms/100Hz at S-Out)</b>						
VGNR	Gain between input and output	Vin=0dBd, f=100Hz	—	5.1	—	dB
DEC1	Decode character 1	Vin=0dBd, f=1.0kHz	-1.6	-0.1	1.4	dB
DEC2	Decode character 2	Vin=-15dBd, f=1.4kHz	-3.0	-1.5	0	
DEC3	Decode character 3	Vin=-20dBd, f=1.4kHz	-4.9	-3.4	-1.9	
DEC4	Decode character 4	Vin=-40dBd, f=5.0kHz	-6.8	-5.3	-3.8	
THDNR	Total harmonic distortion	Vin=0dBd, f=1kHz 30kHzLPF	—	0.07	0.3	%
HRNR	Head room	THD=1%	15	17	—	dB
SNNR	S/N ratio	Rg=0, weighted CCIR/ARM	68	78	—	dB
<b>Cch/Sch Master Volume</b>						
ATTmax	Maximum attenuator	ATT=-, Vi=2Vrms	—	-95	-87	dB
ATTmin	Minimum attenuator	ATT=0dB	-3.0	0	3.0	dB
VOLS1	Volume step	ATT=0 to -40dB	0.5	1.0	1.5	dB
VOLS2	Volume step	ATT=-40 to -87dB	0.2	1.0	1.8	dB
CTVOL	Volume cross-talk	R input/CVOL, SVOL output	68	83	—	dB
VnoVOL	Output noise voltage	ATT=-	—	2.6	5.2	$\mu$ Vrms
<b>Line(Bypass mode)</b>						
THDLN	Total harmonic distortion	L, Rch output 30kHzLPF	—	0.002	0.05	%
SNLN	S/N ratio	L, Rch output	95	100	—	dB
CTLN	Line cross-talk	L input/R output, R input/L output	70	80	—	dB
Zi	Input impedance		11	22	44	k

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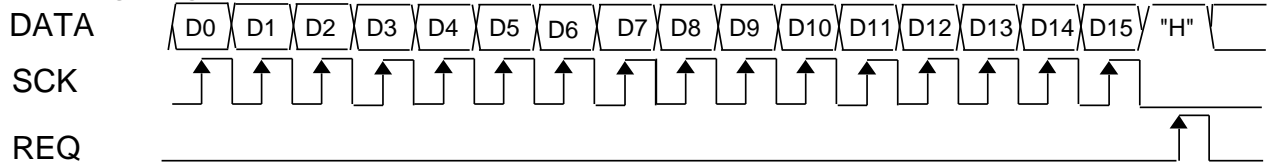
(Ta=25 °C, Vcc=9V, Vdd=5V, Vin=200mVrms, f=1kHz unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Units	
			Min	Typ	Max		
<b>Digital Delay</b>							
GvD	Input/output voltage gain	LIN-LPF2OUT,surround L-R	-8.1	-5.1	-2.1	dB	
Td	Delay time	Td=20.5ms	17.4	20.5	23.6	ms	
THDD	Total harmonic distortion	30kHzLPF	Td=20.5ms	—	0.5	0.9	%
			Td=51.2ms	—	1.2	2.2	
			Td=184ms	—	3.0	5.6	
NoD	Output noise voltage	Vin=0Vrms JIS-A	Td=20.5ms	—	-92	-80	dBV
			Td=51.2ms	—	-84	-70	
			Td=184ms	—	-80	-65	
Vomax	Maximum output voltage	THD=10%	0.7	1.0	—	Vrms	
LPFfc	LPF cut-off frequency	Td=15.4 to 51.2ms Gv=-3dB (Dolby Pro Logic mode)	6.0	7.0	8.0	kHz	
		Td=123, 184ms(Echo mode) Gv=-3dB	—	3.0	—	kHz	
<b>Feedback Volume</b>							
FBATT <sub>max</sub>	Maximum attenuation	ATT=-	—	-70	-60	dB	
FBATT <sub>min</sub>	Minimum attenuation	ATT=-3dB	-6.0	-3.0	0	dB	
FBVOLS	Volume step		—	3.0	—	dB	
<b>Microphone Volume</b>							
MICATT <sub>max</sub>	Maximum attenuation	ATT=-	—	-70	-60	dB	
MICATT <sub>min</sub>	Minimum attenuation	ATT=0dB	-3.0	0	3.0	dB	
MICVOLS	Volume step		—	3.0	—	dB	
VnoMIC	Output noise voltage	ATT=-	—	2.0	4.0	μVrms	

**SERIAL DATA CONTROL FORMAT**

(1)Data Input Format

DATA is read at the rising edge of SCK, and loaded last 16 bits at the rising edge of REQ.



	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15		
L	L	Mode Set		Pro Logic Mode	Center Mode		Sch Volume								L	H		
	H	Delay Time			Auto-Balance	set to "L"	Cch Volume								Chip Address			
H	L	Noise Sequencer			Surround / Echo Mode													
	H	Test Mode (user inhibit)																

(2)Control condition

	Control Mode	Contents
1	Mode Set	Normal Stereo / Dolby Pro Logic / Space Surround or Echo/ Mute
2	Pro Logic Mode	4ch Pro Logic / 3ch stereo
3	Center Mode	Wide / Normal / Phantom / OFF
4	Delay Time	15.4, 20.5, 25.6, 29.2, 51.2 ms (for Surround) 123,184 ms (for Echo)
5	Auto-Balance	Input Auto-Balance ON / OFF
6	Noise Sequencer	ON / OFF Lch / Rch / Cch / Sch
7	Surround /Echo mode	Delay input L-R/ (L+R)/2 /MICin Feedback volume , Microphone volume Delay output mixing
8	Cch/Sch Volume	0 to -87dB / 1dB step and $-\infty$
9	Chip Address	Input data effect or not



(3)Set Conditions

Mode Setting (D0="L",D1="L")

D2	D3	Condition
L	L	Normal stereo (bypass)
L	H	Dolby Pro Logic Surround
H	L	Space surround / Echo
H	H	Output Mute

Pro Logic Mode Setting(D0="L",D1="L")

D4	Condition
L	4ch Pro Logic
H	3ch Stereo

Center Mode Setting (D0="L",D1="L")

D5	D6	Condition
L	L	Wide
L	H	Normal
H	L	Phantom
H	H	OFF

Delay Time Setting (D0="L,D1="H")

D2	D3	D4	Delay time	Sampling frequency	LPF cutoff frequency
L	L	L	15.4msec	500kHz	7kHz
L	L	H	20.5msec	500kHz	
L	H	L	25.6msec	400kHz	
L	H	H	29.2msec	333kHz	
H	L	L	51.2msec	200kHz	3kHz
H	L	H	123msec	83.3kHz	
H	H	L	184msec	55.6kHz	

Auto-Balance Setting (D0="L",D1="H")

D5	Condition
L	Auto-Balance OFF
H	Auto-Balance ON

Noise Sequencer (D0="H",D1="L")

D2	D3	D4	Condition	
L	-	-	Noise Sequencer OFF	
H	L	L	Noise Sequencer ON	Lch
	L	H		Rch
	H	L		Cch
	H	H		Sch

Surround / Echo mode (D0="H",D1="L")

Surround / Echo mode switch

D5	Condition
L	Surround
H	Echo

Delay input

D6	Delay input
L	L-R
H	$(L+R)/2$

Delay Mixing polarity

D7	Mixing polarity
L	L+Delay signal/R+Delay signal
H	L+Delay signal/R-Delay signal

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## Feedback Volume

D8	D9	D10	Volume
L	L	L	-3dB
L	L	H	-6dB
L	H	L	-9dB
L	H	H	-12dB
H	L	L	-15dB
H	L	H	-18dB
H	H	L	-21dB
H	H	H	-

## Microphone Volume

D11	D12	D13	volume
L	L	L	0dB
L	L	H	-3dB
L	H	L	-6dB
L	H	H	-9dB
H	L	L	-12dB
H	L	H	-15dB
H	H	L	-18dB
H	H	H	-

## Relation between mode setting and switch condition

Mode Setting	Pro Logic Mode (D0=L,D1=L) D4	Surround/Echo Mode (D0=H,D1=L)		Switch Condition					
		D5	D6	SW1	SW2	SW3	SW4	SW5	SW6
Normal stereo (bypass)	X	X	X	1	1	2	4	OFF	2
Dolby Pro Logic Surround	L	X	X	3	3	1	1	OFF	2
	H					2			
Space surround / Echo	X	L (Surround)	L	2	2	1	2	ON	2
		H (Echo)	H				3		
	X	H (Echo)	X	1	1	2	4	OFF	1
				Delay mixing ON					
				Delay mixing OFF					
Mute	X	X	X	4	4	2	4	OFF	2

X:L or H

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Sch Volume Setting (D0="L",D1="L")

Cch Volume Setting (D0="L",D1="H")

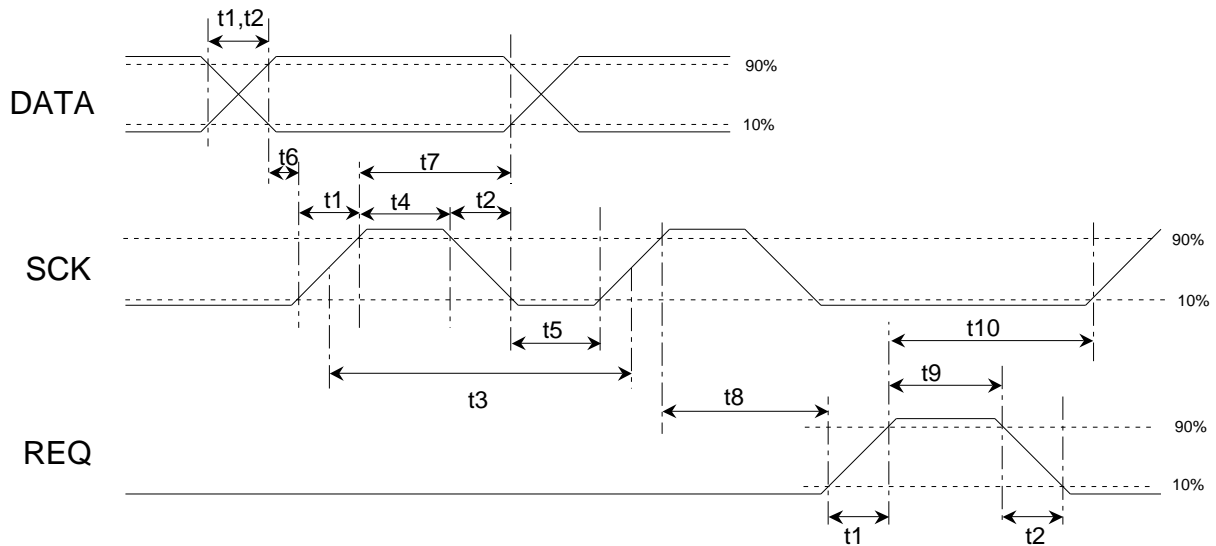
Volume Level	D7	D8	D9	D10	D11
0 dB	L	L	L	L	L
-2 dB	L	L	L	L	H
-4 dB	L	L	L	H	L
-6 dB	L	L	L	H	H
-8 dB	L	L	H	L	L
-10 dB	L	L	H	L	H
-12 dB	L	L	H	H	L
-14 dB	L	L	H	H	H
-16 dB	L	H	L	L	L
-18 dB	L	H	L	L	H
-20 dB	L	H	L	H	L
-22 dB	L	H	L	H	H
-24 dB	L	H	H	L	L
-26 dB	L	H	H	L	H
-28 dB	L	H	H	H	L
-30 dB	L	H	H	H	H
-32 dB	H	L	L	L	L
-34 dB	H	L	L	L	H
-36 dB	H	L	L	H	L
-40 dB	H	L	L	H	H
-44 dB	H	L	H	L	L
-48 dB	H	L	H	L	H
-52 dB	H	L	H	H	L
-56 dB	H	L	H	H	H
-60 dB	H	H	L	L	L
-64 dB	H	H	L	L	H
-68 dB	H	H	L	H	L
-72 dB	H	H	L	H	H
-76 dB	H	H	H	L	L
-80 dB	H	H	H	L	H
-84 dB	H	H	H	H	L
-∞	H	H	H	H	H

Volume Level	D12	D13
0 dB	L	L
-1 dB	L	H
-2 dB	H	L
-3 dB	H	H

Chip Address

D14	D15	Data Read
L	H	Enable
Others		Unable

(4)Data timing



Symbol	Name	Min	Typ	Max	Units
t1	Signal rise time	—	—	0.5	μs
t2	Signal fall time	—	—	0.5	μs
t3	SCK clock width	2	—	—	μs
t4	SCK "H" pulse width	0.8	—	—	μs
t5	SCK "L" pulse width	0.8	—	—	μs
t6	DATA setup time	0.8	—	—	μs
t7	DATA hold time	0.8	—	—	μs
t8	REQ rise hold time	1.6	—	—	μs
t9	REQ "H" pulse width	0.8	—	—	μs
t10	SCK setup time	1.6	—	—	μs

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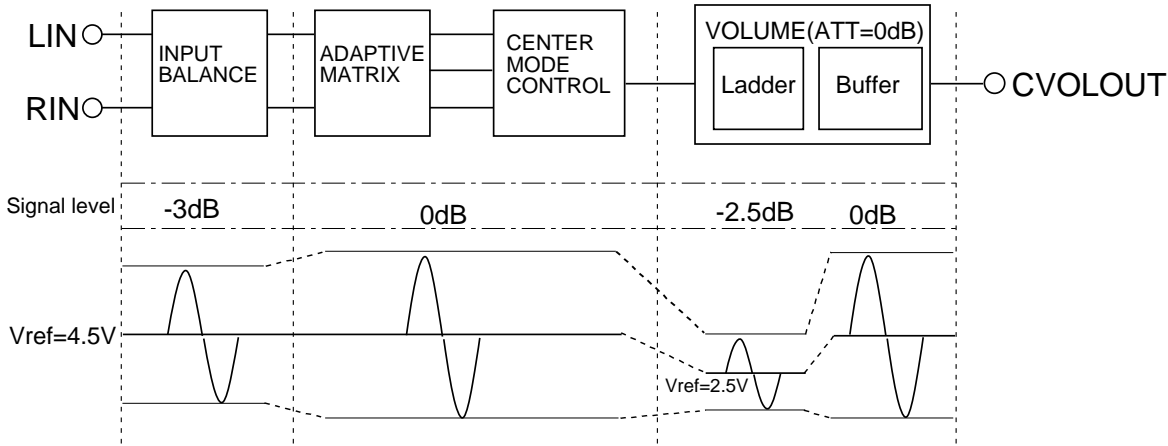
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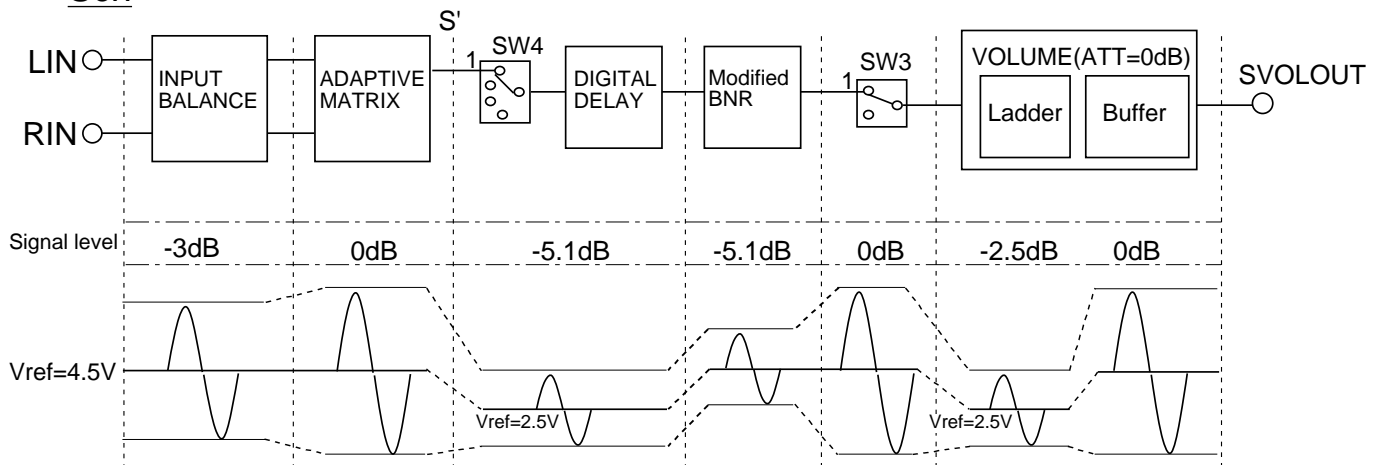
## Level Diagram

### (1)Dolby Pro Logic Surround Mode

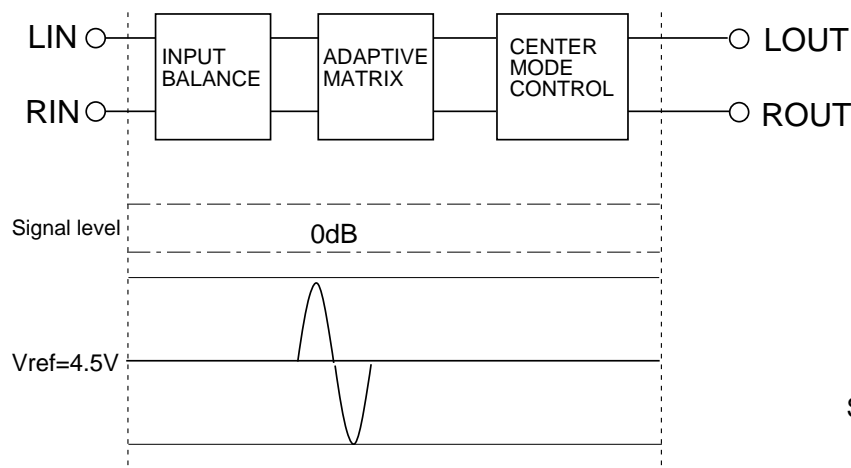
#### Cch



#### Sch



#### Lch,Rch



Signal level : 0dB=300mVrms(Typ.)

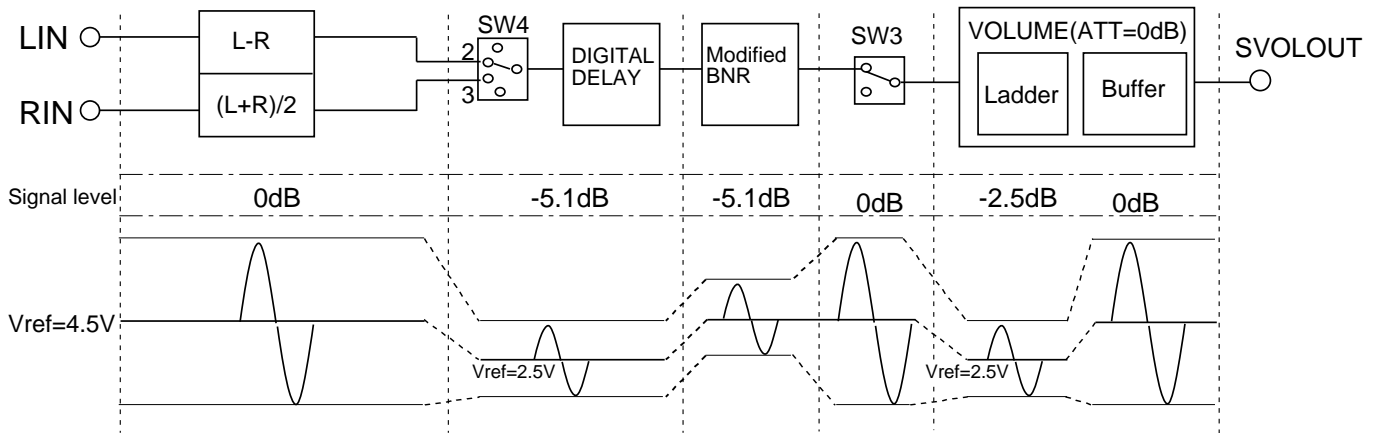
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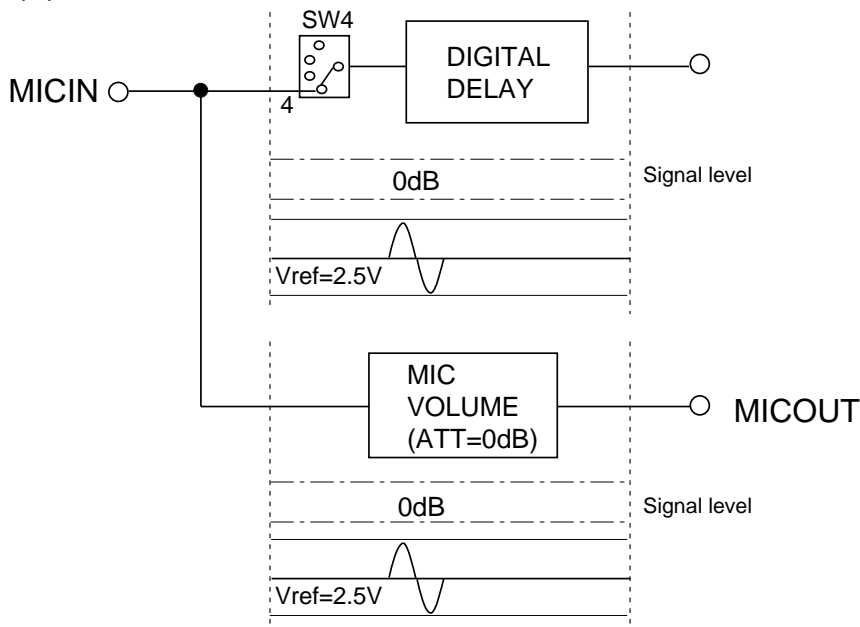
## Dolby Pro Logic Surround Decoder

### (2)Space Surround Mode

Sch



### (3)Echo Mode

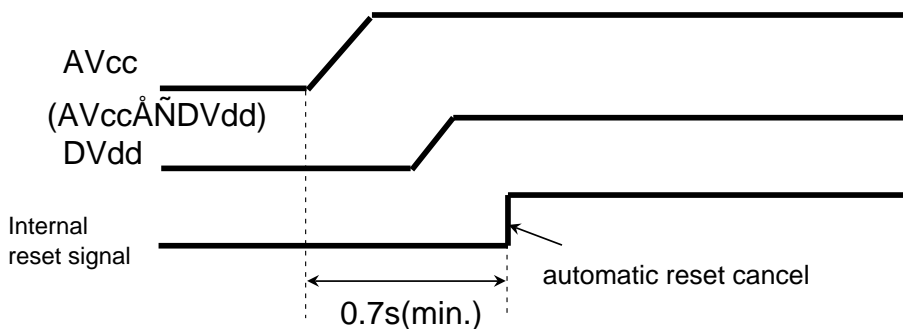


Signal level : 0dB=300mVrms(Typ.)

### Notice

Relation AVcc and DVdd at power supply

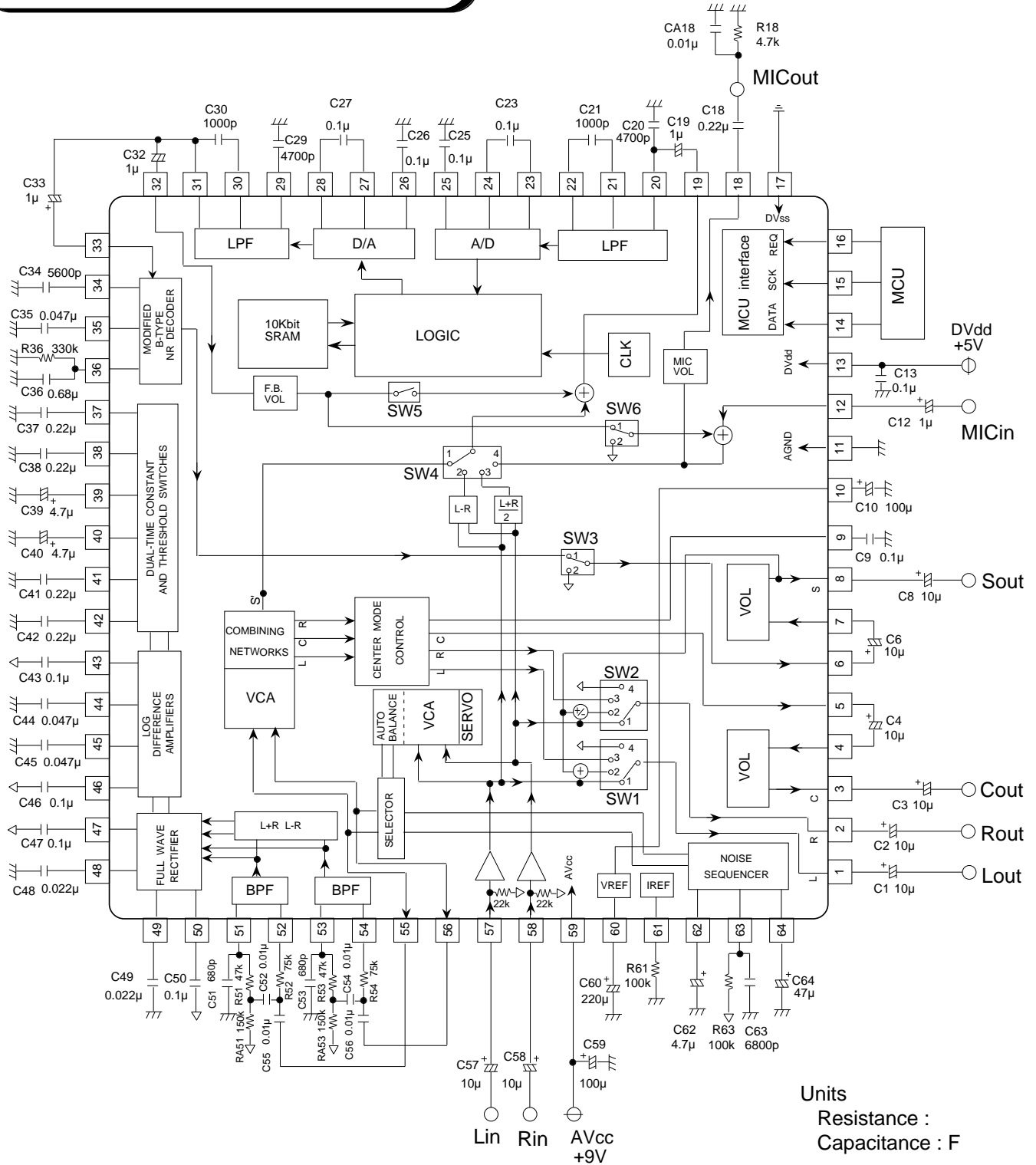
Digital Vdd must be supplied less than 0.7 seconds from analog Vcc supply.



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**APPLICATION EXAMPLE**





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## EXTERNAL PARTS LIST

Parts No.	Values	Unit	Tol.	Parts No.	Values	Unit	Tol.
C1	10	μF		C47	0.1	μF	20%
C2	10	μF		C48	0.022	μF	5%
C3	10	μF		C49	0.022	μF	5%
C4	10	μF		C50	0.1	μF	20%
C6	10	μF		C51	680	pF	5%
C8	10	μF		C52	0.01	μF	5%
C9	0.1	μF	10%	C53	680	pF	5%
C10	100	μF		C54	0.01	μF	5%
C12	10	μF		C55	0.01	μF	5%
C13	0.1	μF		C56	0.01	μF	5%
C18	0.22	μF		C57	10	μF	
CA18	0.01	μF		C58	10	μF	
C19	1.0	μF	non-polar	C59	100	μF	
C20	4700	pF	5%	C60	220	μF	
C21	1000	pF	5%	C62	4.7	μF	10%
C23	0.1	μF	5%	C63	6800	pF	5%
C25	0.1	μF	5%	C64	47	μF	
C26	0.1	μF	5%				
C27	0.1	μF	5%				
C29	4700	μF	5%	R18	4.7	k	10%
C30	1000	pF	5%	R36	330	k	10%
C32	1.0	μF		R51	47	k	5%
C33	1.0	μF		RA51	150	k	5%
C34	5600	pF	5%	R52	75	k	5%
C35	0.047	μF	5%	R53	47	k	5%
C36	0.68	μF	10%	RA53	150	k	5%
C37	0.22	pF	10%	R54	75	k	5%
C38	0.22	pF	10%	R61	100	k	1%
C39	4.7	μF	20%	R63	100	k	5%
C40	4.7	μF	20%				
C41	0.22	μF	10%				
C42	0.22	μF	10%				
C43	0.1	μF	20%				
C44	0.047	μF	5%				
C45	0.047	μF	5%				
C46	0.1	μF	20%				