Features

■ Core: ARM 32-bit Cortex™-M4 CPU with FPU,
Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 168 MHz (168 000 000Hz),
memory protection unit, 210 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
■ **Memories**
– Up to 1 Mbyte of Flash memory
– Up to 192+4 Kbytes of SRAM including 64-Kbyte of CCM (core coupled memory) data RAM
– Flexible static memory controller supporting Compact Flash, SRAM, PSRAM, NOR and NAND memories
■ **LCD parallel interface, 8080/6800 modes**
■ Clock, reset and supply management – 1.8 V to 3.6 V application supply and I/Os
– POR, PDR, PVD and BOR
– 4-to-26 MHz crystal oscillator
– Internal 16 MHz factory-trimmed RC (1% accuracy)
– 32 kHz oscillator for RTC with calibration
– Internal 32 kHz RC with calibration
● Low power
– Sleep, Stop and Standby modes
– V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
■ 3×12-bit, 2.4 MSPS A/D converters: up to 24 channels and 7.2 MSPS in triple interleaved mode
■ 2×12-bit D/A converters
■ General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
■ Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 168 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
■ Debug mode
– Serial wire debug (SWD) & JTAG interfaces
– Cortex-M4 Embedded Trace Macrocell™ 1. The WLCSP90 package will soon be available.
■ Up to 140 I/O ports with interrupt capability
– Up to 136 fast I/Os up to 84 MHz
– Up to 138 5 V-tolerant I/Os
■ Up to 15 communication interfaces
– Up to 3 × I^2C interfaces (SMBus/PMBus)
– Up to 4 USARTs/2 UARTs (10.5 Mbit/s, ISO 7816 interface, LIN, IrDA, modem control)
– Up to 3 SPIs (37.5 Mbits/s), 2 with muxed full-duplex I^2S to achieve audio class accuracy via internal audio PLL or external clock
– 2 × CAN interfaces (2.0B Active)
– SDIO interface
■ Advanced connectivity
– USB 2.0 full-speed device/host/OTG controller with on-chip PHY
– USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI – 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
■ 8- to 14-bit parallel camera interface up to 54 Mbytes/s
■ True random number generator
■ CRC calculation unit
■ 96-bit unique ID
■ RTC: subsecond accuracy, hardware calendar

Table 6. STM32F40x pin and ball definitions

Figure 11. STM32F40x LQFP100 pinout

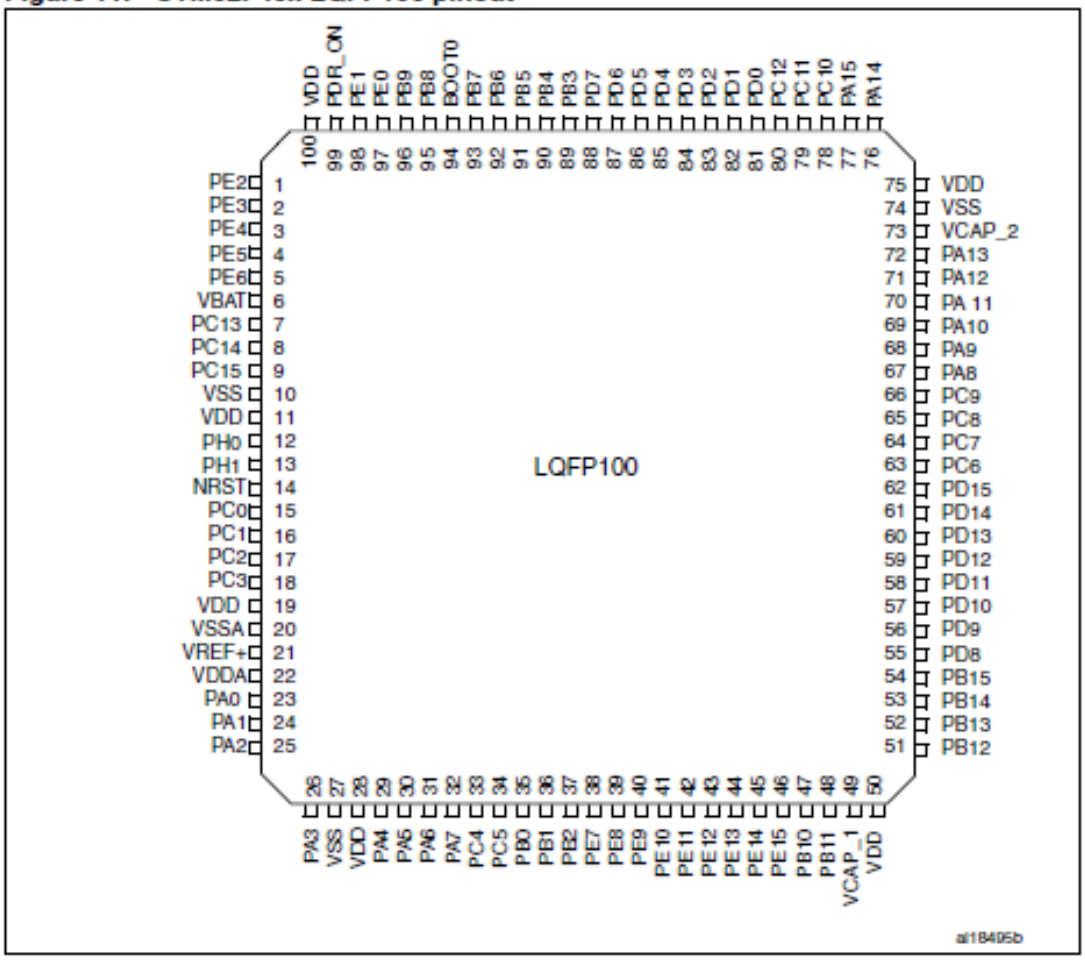

Figure 12. STM32F40x LQFP144 pinout

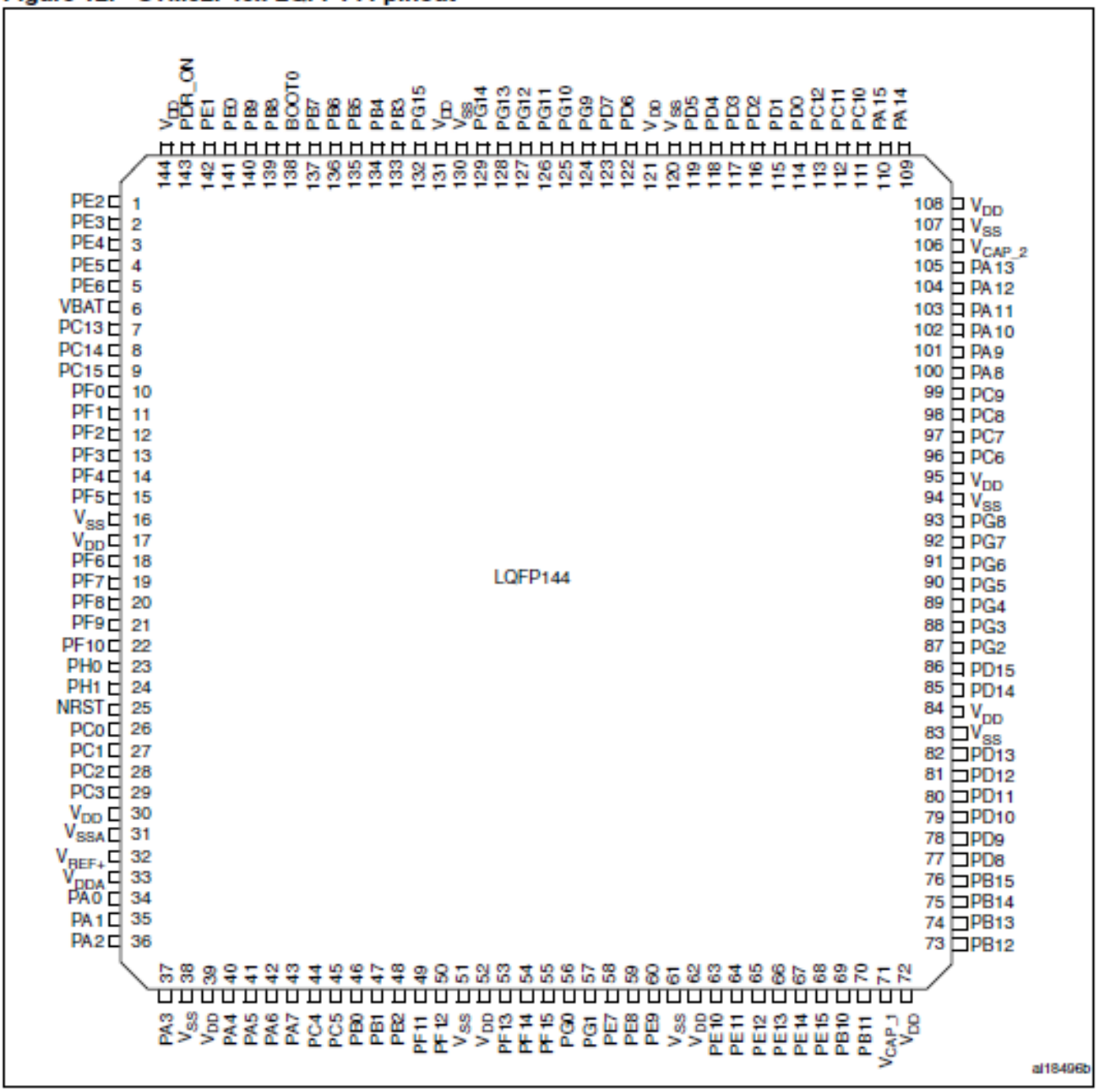

Table 5. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, FM+ capable
	TTa	3.3 V tolerant I/O directly connected to ADC
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	

Pin num		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
1	1	PE2	I/O	FT		TRACECLK/ FSMC_A23 / ETH_MII_TXD3 / EVENTOUT	
2	2	PE3	I/O	FT		TRACED0/FSMC_A19 / EVENTOUT	
3	3	PE4	I/O	FT		TRACED1/FSMC_A20 / DCMI_D4/ EVENTOUT	
4	4	PE5	I/O	FT		TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6 / EVENTOUT	
5	5	PE6	I/O	FT		TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7 / EVENTOUT	
6	6	V_{BAT}	S				
-	-	PI8	I/O	FT	(2)(3)	EVENTOUT	RTC_AF2
7	7	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1
8	8	PC14-OSC32_IN (PC14)	I/O	FT	(2)(3)	EVENTOUT	OSC32_IN[4]
9	9	PC15-OSC32_OUT (PC15)	I/O	FT	(2)(3)	EVENTOUT	OSC32_OUT[4]
-	10	PF0	I/O	FT		FSMC_A0 / I2C2_SDA / EVENTOUT	
-	11	PF1	I/O	FT		FSMC_A1 / I2C2_SCL / EVENTOUT	
-	12	PF2	I/O	FT		FSMC_A2 / I2C2_SMBA / EVENTOUT	
-	13	PF3	I/O	FT	(4)	FSMC_A3/EVENTOUT	ADC3_IN9
-	14	PF4	I/O	FT	(4)	FSMC_A4/EVENTOUT	ADC3_IN14
-	15	PF5	I/O	FT	(4)	FSMC_A5/EVENTOUT	ADC3_IN15

Pin nun		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
10	16	V_{SS}	S				
11	17	V_{DD}	S				
-	18	PF6	I/O	FT	(4)	TIM10_CH1 / FSMC_NIORD/ EVENTOUT	ADC3_IN4
-	19	PF7	I/O	FT	(4)	TIM11_CH1/FSMC_NREG/ EVENTOUT	ADC3_IN5
-	20	PF8	I/O	FT	(4)	TIM13_CH1 / FSMC_NIOWR/ EVENTOUT	ADC3_IN6
-	21	PF9	I/O	FT	(4)	TIM14_CH1 / FSMC_CD/ EVENTOUT	ADC3_IN7
-	22	PF10	I/O	FT	(4)	FSMC_INTR/ EVENTOUT	ADC3_IN8
12	23	PH0-OSC_IN (PH0)	I/O	FT		EVENTOUT	OSC_IN(4)
13	24	PH1-OSC_OUT (PH1)	I/O	FT		EVENTOUT	OSC_OUT(4)
14	25	NRST	I/O	RST			
15	26	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP/ EVENTOUT	ADC123_IN10
16	27	PC1	I/O	FT	(4)	ETH_MDC/ EVENTOUT	ADC123_IN11
17	28	PC2	I/O	FT	(4)	SPI2_MISO / OTG_HS_ULPI_DIR / TH_MII_TXD2 /I2S2ext_SD/ EVENTOUT	ADC123_IN12
18	29	PC3	I/O	FT	(4)	SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK/ EVENTOUT	ADC123_IN13
19	30	V_{DD}	S				
20	31	V_{SSA}	S				
-	-	V_{REF-}	S				
21	32	V_{REF+}	S				
22	33	V_{DDA}	S				

Pin nun		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
23	34	PA0-WKUP (PA0)	I/O	FT	(5)	USART2_CTS/ UART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/ EVENTOUT	ADC123_IN0/WKUP[4]
24	35	PA1	I/O	FT	(4)	USART2_RTS / UART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIMM2_CH2/ EVENTOUT	ADC123_IN1
25	36	PA2	I/O	FT	(4)	USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/ EVENTOUT	ADC123_IN2
26	37	PA3	I/O	FT	(4)	USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/ EVENTOUT	ADC123_IN3
27	38	V_{SS}	S				
		BYPASS_REG	I	FT			
28	39	V_{DD}	S				
29	40	PA4	I/O	TTa	(4)	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	ADC12_IN4 /DAC1_OUT
30	41	PA5	I/O	TTa	(4)	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CHIN/ EVENTOUT	ADC12_IN5/DAC2_OUT
31	42	PA6	I/O	FT	(4)	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6

Pin num		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
32	43	PA7	I/O	FT	(4)	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1/TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / RMII_CRS_DV/ EVENTOUT	ADC12_IN7
33	44	PC4	I/O	FT	(4)	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT	ADC12_IN14
34	45	PC5	I/O	FT	(4)	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ EVENTOUT	ADC12_IN15
35	46	PB0	I/O	FT	(4)	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT	ADC12_IN8
36	47	PB1	I/O	FT	(4)	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / OTG_HS_INTN / TIM1_CH3N/ EVENTOUT	ADC12_IN9
37	48	PB2-BOOT1 (PB2)	I/O	FT		EVENTOUT	
-	49	PF11	I/O	FT		DCMI_12/ EVENTOUT	
-	50	PF12	I/O	FT		FSMC_A6/ EVENTOUT	
-	51	V_{SS}	S				
-	52	V_{DD}	S				
-	53	PF13	I/O	FT		FSMC_A7/ EVENTOUT	
-	54	PF14	I/O	FT		FSMC_A8/ EVENTOUT	
-	55	PF15	I/O	FT		FSMC_A9/ EVENTOUT	
-	56	PG0	I/O	FT		FSMC_A10/ EVENTOUT	
-	57	PG1	I/O	FT		FSMC_A11/ EVENTOUT	
38	58	PE7	I/O	FT		FSMC_D4/TIM1_ETR/ EVENTOUT	
39	59	PE8	I/O	FT		FSMC_D5/ TIM1_CH1N/ EVENTOUT	
40	60	PE9	I/O	FT		FSMC_D6/TIM1_CH1/ EVENTOUT	
-	61	V_{SS}	S				

Pin nun		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
-	62	V_{DD}	S				
41	63	PE10	I/O	FT		FSMC_D7/TIM1_CH2N/ EVENTOUT	
42	64	PE11	I/O	FT		FSMC_D8/TIM1_CH2/ EVENTOUT	
43	65	PE12	I/O	FT		FSMC_D9/TIM1_CH3N/ EVENTOUT	
44	66	PE13	I/O	FT		FSMC_D10/TIM1_CH3/ EVENTOUT	
45	67	PE14	I/O	FT		FSMC_D11/TIM1_CH4/ EVENTOUT	
46	68	PE15	I/O	FT		FSMC_D12/TIM1_BKIN/ EVENTOUT	
47	69	PB10	I/O	FT		SPI2_SCK / I2S2_CK / I2C2_SCL/ USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / TIM2_CH3/ EVENTOUT	
48	70	PB11	I/O	FT		I2C2_SDA/USART3_RX/ OTG_HS_ULPI_D4 / ETH_RMII_TX_EN/ ETH_MII_TX_EN / TIM2_CH4/ EVENTOUT	
49	71	V_{CAP_1}	S				
50	72	V_{DD}	S				

Pin nur		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
51	73	PB12	I/O	FT		SPI2_NSS / I2S2_WS / I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID/ EVENTOUT	
52	74	PB13	I/O	FT		SPI2_SCK / I2S2_CK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1/ EVENTOUT	OTG_HS_VBUS
53	75	PB14	I/O	FT		SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM/ USART3_RTS / TIM8_CH2N/I2S2ext_SD/ EVENTOUT	
54	76	PB15	I/O	FT		SPI2_MOSI / I2S2_SD/ TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP/ EVENTOUT	
55	77	PD8	I/O	FT		FSMC_D13 / USART3_TX/ EVENTOUT	
56	78	PD9	I/O	FT		FSMC_D14 / USART3_RX/ EVENTOUT	
57	79	PD10	I/O	FT		FSMC_D15 / USART3_CK/ EVENTOUT	
58	80	PD11	I/O	FT		FSMC_CLE / FSMC_A16/USART3_CTS/ EVENTOUT	
59	81	PD12	I/O	FT		FSMC_ALE/ FSMC_A17/TIM4_CH1 / USART3_RTS/ EVENTOUT	

Pin nun		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
60	82	PD13	I/O	FT		FSMC_A18/TIM4_CH2/ EVENTOUT	
-	83	V_{SS}	S				
-	84	V_{DD}	S				
61	85	PD14	I/O	FT		FSMC_D0/TIM4_CH3/ EVENTOUT/ EVENTOUT	
62	86	PD15	I/O	FT		FSMC_D1/TIM4_CH4/ EVENTOUT	
-	87	PG2	I/O	FT		FSMC_A12/ EVENTOUT	
-	88	PG3	I/O	FT		FSMC_A13/ EVENTOUT	
-	89	PG4	I/O	FT		FSMC_A14/ EVENTOUT	
-	90	PG5	I/O	FT		FSMC_A15/ EVENTOUT	
-	91	PG6	I/O	FT		FSMC_INT2/ EVENTOUT	
-	92	PG7	I/O	FT		FSMC_INT3 /USART6_CK/ EVENTOUT	
-	93	PG8	I/O	FT		USART6_RTS / ETH_PPS_OUT/ EVENTOUT	
-	94	V_{SS}	S				
-	95	V_{DD}	S				
63	96	PC6	I/O	FT		I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT	
64	97	PC7	I/O	FT		I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2/ EVENTOUT	
65	98	PC8	I/O	FT		TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2/ EVENTOUT	
66	99	PC9	I/O	FT		I2S_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / /I2C3_SDA / DCMI_D3 / TIM3_CH4/ EVENTOUT	

Pin nun		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
67	100	PA8	I/O	FT		MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF/ EVENTOUT	
68	101	PA9	I/O	FT		USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/ EVENTOUT	OTG_FS_VBUS
69	102	PA10	I/O	FT		USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1/ EVENTOUT	
70	103	PA11	I/O	FT		USART1_CTS / CAN1_RX / TIM1_CH4 / OTG_FS_DM/ EVENTOUT	
71	104	PA12	I/O	FT		USART1_RTS / CAN1_TX/ TIM1_ETR/ OTG_FS_DP/ EVENTOUT	
72	105	PA1 (JTMS-SWDIO)	I/O	FT		JTMS-SWDIO/ EVENTOUT	
73	106	V_{CAP_2}	S				
74	107	V_{SS}	S				
75	108	V_{DD}	S				

Pin num		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
76	109	PA14 (JTCK-SWCLK)	I/O	FT		JTCK-SWCLK/ EVENTOUT	
77	110	PA15 (JTDI)	I/O	FT		JTDI/ SPI3_NSS/ I2S3_WS/TIM2_CH1_ETR / SPI1_NSS / EVENTOUT	
78	111	PC10	I/O	FT		SPI3_SCK / I2S3_CK/ UART4_TX/SDIO_D2 / DCMI_D8 / USART3_TX/ EVENTOUT	
79	112	PC11	I/O	FT		UART4_RX/ SPI3_MISO / SDIO_D3 / DCMI_D4/USART3_RX / I2S3ext_SD/ EVENTOUT	
80	113	PC12	I/O	FT		UART5_TX/SDIO_CK / DCMI_D9 / SPI3_MOSI /I2S3_SD / USART3_CK/ EVENTOUT	
81	114	PD0	I/O	FT		FSMC_D2/CAN1_RX/ EVENTOUT	
82	115	PD1	I/O	FT		FSMC_D3 / CAN1_TX/ EVENTOUT	
83	116	PD2	I/O	FT		TIM3_ETR/UART5_RX/ SDIO_CMD / DCMI_D11/ EVENTOUT	
84	117	PD3	I/O	FT		FSMC_CLK/USART2_CTS / EVENTOUT	
85	118	PD4	I/O	FT		FSMC_NOE/USART2_RTS / EVENTOUT	
86	119	PD5	I/O	FT		FSMC_NWE/USART2_TX/ EVENTOUT	
-	120	V_{SS}	S				
-	121	V_{DD}	S				
87	122	PD6	I/O	FT		FSMC_NWAIT/ USART2_RX/ EVENTOUT	
88	123	PD7	I/O	FT		USART2_CK/FSMC_NE1/ FSMC_NCE2/ EVENTOUT	
-	124	PG9	I/O	FT		USART6_RX / FSMC_NE2/FSMC_NCE3/ EVENTOUT	

Pin num		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
-	125	PG10	I/O	FT		FSMC_NCE4_1/ FSMC_NE3/ EVENTOUT	
-	126	PG11	I/O	FT		FSMC_NCE4_2 / ETH_MII_TX_EN/ ETH _RMII_TX_EN/ EVENTOUT	
-	127	PG12	I/O	FT		FSMC_NE4 / USART6_RTS/ EVENTOUT	
-	128	PG13	I/O	FT		FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ ETH_RMII_TXD0/ EVENTOUT	
-	129	PG14	I/O	FT		FSMC_A25 / USART6_TX /ETH_MII_TXD1/ ETH_RMII_TXD1/ EVENTOUT	
-	130	V_{SS}	S				
-	131	V_{DD}	S				
-	132	PG15	I/O	FT		USART6_CTS / DCMI_D13/ EVENTOUT	
89	133	PB3 (JTDO/ TRACESWO)	I/O	FT		JTDO/ TRACESWO/ SPI3_SCK / I2S3_CK / TIM2_CH2 / SPI1_SCK/ EVENTOUT	
90	134	PB4 (NJTRST)	I/O	FT		NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO / I2S3ext_SD/ EVENTOUT	
91	135	PB5	I/O	FT		I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH 2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD/ EVENTOUT	
92	136	PB6	I/O	FT		I2C1_SCL/ TIM4_CH1 / CAN2_TX / DCMI_D5/USART1_TX/ EVENTOUT	

Pin nun		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
93	137	PB7	I/O	FT		I2C1_SDA / FSMC_NL / DCMI_VSYNC / USART1_RX/ TIM4_CH2/ EVENTOUT	
94	138	BOOT0	I	B			V_{PP}
95	139	PB8	I/O	FT		TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX/ EVENTOUT	
96	140	PB9	I/O	FT		SPI2_NSS/ I2S2_WS / TIM4_CH4/ TIM11_CH1/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX/ EVENTOUT	
97	141	PE0	I/O	FT		TIM4_ETR / FSMC_NBL0 / DCMI_D2/ EVENTOUT	
98	142	PE1	I/O	FT		FSMC_NBL1 / DCMI_D3/ EVENTOUT	
99	-	V_{SS}	S				
-	143	PDR_ON	I	FT			
100	144	V_{DD}	S				

1. Funkció rendelkezésre állása függ a választott eszközön.
2. PC13, PC14, PC15 és PI8 kerülnek forgalomba át a hálózati kapcsolót. Mivel a kapcsoló csak süllyed korlátozott mennyiségű áram
(3 mA), a használata GPIOs PC13 a PC15 és PI8 kimeneti módban korlátozott:
- A sebesség nem haladhatja meg a 2 MHz maximális terhelhetősége 30 pF.
- Ezek az I / O nem lehet használni, mint egy áramforrást (például vezetni egy LED).
3. Fő funkciója az első biztonsági tartomány power-up. Később, ez függ a tartalma a RTC nyilvántartások után is reset (mert ezek a nyilvántartások nem lehet visszaállítani a fő visszaállítás). A részletekért, hogyan kell kezelni ezeket az I / O, lásd az RTC
Regiszter leírás szakaszok a STM32F4xx referencia kézikönyv, amely elérhető az STMicroelectronics honlapján: www.st.com
4. FT = 5 V toleráns, kivéve, ha az analóg módban vagy oszcillátor típusát (PC14, PC15, PH0 és PH1).

STM32F407ZET6 Board Pins! **BAL oldali 2 * 30 Csatlakozó sor.**

	Pin number		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
	LQFP100	LQFP144						
60	-	-	V_{DD}	S				
59	-	-	V_{SS} 5V	S				
58	-	-	V_{DD}	S				
57	-	-	V_{SS} 3.3V	S				
56	51	73	PB12	I/O	FT		SPI2_NSS / I2S2_WS / I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID/ EVENTOUT	
55	52	74	PB13	I/O	FT		SPI2_SCK / I2S2_CK / USART3_CTS/ TIM1_CH1N /CAN2_TX / OTG_HS_ULPI_D6 / ETH_RMII_TXD1 / ETH_MII_TXD1/ EVENTOUT	OTG_HS_VBUS
54	53	75	PB14	I/O	FT		SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM/ USART3_RTS / TIM8_CH2N/I2S2ext_SD/ EVENTOUT	
53	54	76	PB15	I/O	FT		SPI2_MOSI / I2S2_SD/ TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP/ EVENTOUT	
52	55	77	PD8	I/O	FT		FSMC_D13 / USART3_TX/ EVENTOUT	
51	56	78	PD9	I/O	FT		FSMC_D14 / USART3_RX/ EVENTOUT	
50	57	79	PD10	I/O	FT		FSMC_D15 / USART3_CK/ EVENTOUT	

49	58	80	PD11	I/O	FT		FSMC_CLE / FSMC_A16/USART3_CTS/ EVENTOUT	
48	59	81	PD12	I/O	FT		FSMC_ALE/ FSMC_A17/TIM4_CH1 / USART3_RTS/ EVENTOUT	
	Pin nur		Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions
	LQFP100	LQFP144						
47	60	82	PD13	I/O	FT		FSMC_A18/TIM4_CH2/ EVENTOUT	
46	61	85	PD14	I/O	FT		FSMC_D0/TIM4_CH3/ EVENTOUT/ EVENTOUT	
45	62	86	PD15	I/O	FT		FSMC_D1/TIM4_CH4/ EVENTOUT	
44	-	87	PG2	I/O	FT		FSMC_A12/ EVENTOUT	
43	-	88	PG3	I/O	FT		FSMC_A13/ EVENTOUT	
42	-	89	PG4	I/O	FT		FSMC_A14/ EVENTOUT	
41	-	90	PG5	I/O	FT		FSMC_A15/ EVENTOUT	
40	-	91	PG6	I/O	FT		FSMC_INT2/ EVENTOUT	
39	-	92	PG7	I/O	FT		FSMC_INT3/USART6_CK/ EVENTOUT	
38	-	93	PG8	I/O	FT		USART6_RTS / ETH_PPS_OUT/ EVENTOUT	
37	63	96	PC6	I/O	FT		I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT	
36	64	97	PC7	I/O	FT		I2S3_MCK / TIM8_CH2/SDIO_D7 / USART6_RX / DCMI_D1/TIM3_CH2/ EVENTOUT	

35	65	98	PC8	I/O	FT		TIM8_CH3/SDIO_D0 /TIM3_CH3/ USART6_CK / DCMI_D2/ EVENTOUT	

Pin numb		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP144						
34	66	99	PC9	I/O	FT		I2S_CKIN/ MCO2 / TIM8_CH4/SDIO_D1 / /I2C3_SDA / DCMI_D3 / TIM3_CH4/ EVENTOUT	
33	67	100	PA8	I/O	FT		MCO1 / USART1_CK/ TIM1_CH1/ I2C3_SCL/ OTG_FS_SOF/ EVENTOUT	
32	68	101	PA9	I/O	FT		USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/ EVENTOUT	OTG_FS_VBUS
31	69	102	PA10	I/O	FT		USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1/ EVENTOUT	
30	70	103	PA11	I/O	FT		USART1_CTS / CAN1_RX / TIM1_CH4 / OTG_FS_DM/ EVENTOUT	
29	71	104	PA12	I/O	FT		USART1_RTS / CAN1_TX/ TIM1_ETR/ OTG_FS_DP/ EVENTOUT	
28	72	105	PA13 (JTMS-SWDIO)	I/O	FT		JTMS-SWDIO/ EVENTOUT	

	Pin numbe		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
	LQFP100	LQFP144						
27	76	109	PA14 (JTCK/SWCLK)	I/O	FT		JTCK-SWCLK/ EVENTOUT	
26	77	110	PA15 (JTDI)	I/O	FT		JTDI/ SPI3_NSS/ I2S3_WS/TIM2_CH1_ETR / SPI1_NSS / EVENTOUT	
25	78	111	PC10	I/O	FT		SPI3_SCK / I2S3_CK/ UART4_TX/SDIO_D2 / DCMI_D8 / USART3_TX/ EVENTOUT	
24	79	112	PC11	I/O	FT		UART4_RX/ SPI3_MISO / SDIO_D3 / DCMI_D4/USART3_RX / I2S3ext_SD/ EVENTOUT	
23	80	113	PC12	I/O	FT		UART5_TX/SDIO_CK / DCMI_D9 / SPI3_MOSI /I2S3_SD / USART3_CK/ EVENTOUT	
22	81	114	PD0	I/O	FT		FSMC_D2/CAN1_RX/ EVENTOUT	
21	82	115	PD1	I/O	FT		FSMC_D3 / CAN1_TX/ EVENTOUT	
20	83	116	PD2	I/O	FT		TIM3_ETR/UART5_RX/ SDIO_CMD / DCMI_D11/ EVENTOUT	

	Pin numb		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
	LQFP100	LQFP144						
19	84	117	PD3	I/O	FT		FSMC_CLK/ USART2_CTS/ EVENTOUT	
18	85	118	PD4	I/O	FT		FSMC_NOE/ USART2_RTS/ EVENTOUT	
17	86	119	PD5	I/O	FT		FSMC_NWE/USART2_TX / EVENTOUT	
16	87	122	PD6	I/O	FT		FSMC_NWAIT/ USART2_RX/ EVENTOUT	
15	88	123	PD7	I/O	FT		USART2_CK/FSMC_NE1/ FSMC_NCE2/ EVENTOUT	
14	-	124	PG9	I/O	FT		USART6_RX / FSMC_NE2/FSMC_NCE3 / EVENTOUT	
13	-	125	PG10	I/O	FT		FSMC_NCE4_1/ FSMC_NE3/ EVENTOUT	
12	-	126	PG11	I/O	FT		FSMC_NCE4_2 / ETH_MII_TX_EN/ ETH _RMII_TX_EN/ EVENTOUT	
11	-	127	PG12	I/O	FT		FSMC_NE4 / USART6_RTS/ EVENTOUT	
10	-	128	PG13	I/O	FT		FSMC_A24 / USART6_CTS /ETH_MII_TXD0/ ETH_RMII_TXD0/ EVENTOUT	
9	-	129	PG14	I/O	FT		FSMC_A25 / USART6_TX /ETH_MII_TXD1/ ETH_RMII_TXD1/ EVENTOUT	

	Pin numb		Pin name (function after reset)[1]	Pin type	I / O structure	Notes	Alternate functions	Additional functions
	LQFP100	LQFP144						
8	-	132	PG15	I/O	FT		USART6_CTS / DCMI_D13/ EVENTOUT	
7	89	133	PB3 (JTDO/ TRACESWO)	I/O	FT		JTDO/ TRACESWO/ SPI3_SCK / I2S3_CK / TIM2_CH2 / SPI1_SCK/ EVENTOUT	
6	90	134	PB4 (NJTRST)	I/O	FT		NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO / I2S3ext_SD/ EVENTOUT	
5	91	135	PB5	I/O	FT		I2C1_SMBA/ CAN2_RX / OTG_HS_ULPI_D7 / ETH_PPS_OUT/TIM3_CH 2 / SPI1_MOSI/ SPI3_MOSI / DCMI_D10 / I2S3_SD/ EVENTOUT	
4	92	136	PB6	I/O	FT		I2C1_SCL/ TIM4_CH1 / CAN2_TX / DCMI_D5/USART1_TX/ EVENTOUT	
3	93	137	PB7	I/O	FT		I2C1_SDA / FSMC_NL / DCMI_VSYNC / USART1_RX/ TIM4_CH2/ EVENTOUT	
2	95	139	PB8	I/O	FT		TIM4_CH3/SDIO_D4/ TIM10_CH1 / DCMI_D6 / ETH_MII_TXD3 / I2C1_SCL/ CAN1_RX/ EVENTOUT	
1	96	140	PB9	I/O	FT		SPI2_NSS/ I2S2_WS / TIM4_CH4/ TIM11_CH1/ SDIO_D5 / DCMI_D7 / I2C1_SDA / CAN1_TX/ EVENTOUT	

STM32F407ZET6 Board Pins! **JOBB oldali 2 * 30 Csatlakozó sor.**

-	130	V_{SS}	S					60
-	130	V_{SS}	S					59
94	138	BOOT0	I	B			V_{PP}	58
37	48	PB2/BOOT1 (PB2)	I/O	FT		EVENTOUT		57
-	-	V_{DD}	S					56

Pin nun		Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions	
LQFP100	LQFP144							
49	71	V_{CAP_1}	S					55
48	70	PB11	I/O	FT		I2C2_SDA/USART3_RX/ OTG_HS_ULPI_D4 / ETH_RMII_TX_EN/ ETH_MII_TX_EN / TIM2_CH4/ EVENTOUT		54
47	69	PB10	I/O	FT		SPI2_SCK / I2S2_CK / I2C2_SCL/ USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / TIM2_CH3/ EVENTOUT		53
46	68	PE15	I/O	FT		FSMC_D12/TIM1_BKIN/ EVENTOUT		52
45	67	PE14	I/O	FT		FSMC_D11/TIM1_CH4/ EVENTOUT		51
44	66	PE13	I/O	FT		FSMC_D10/TIM1_CH3/ EVENTOUT		50
43	65	PE12	I/O	FT		FSMC_D9/TIM1_CH3N/ EVENTOUT		49

42	64	PE11	I/O	FT		FSMC_D8/TIM1_CH2/ EVENTOUT		48
41	63	PE10	I/O	FT		FSMC_D7/TIM1_CH2N/ EVENTOUT		47
40	60	PE9	I/O	FT		FSMC_D6/TIM1_CH1/ EVENTOUT		46
39	59	PE8	I/O	FT		FSMC_D5/ TIM1_CH1N/ EVENTOUT		45
38	58	PE7	I/O	FT		FSMC_D4/TIM1_ETR/ EVENTOUT		44
-	57	PG1	I/O	FT		FSMC_A11/ EVENTOUT		43
-	56	PG0	I/O	FT		FSMC_A10/ EVENTOUT		42
-	55	PF15	I/O	FT		FSMC_A9/ EVENTOUT		41
-	54	PF14	I/O	FT		FSMC_A8/ EVENTOUT		40
-	53	PF13	I/O	FT		FSMC_A7/ EVENTOUT		39
-	50	PF12	I/O	FT		FSMC_A6/ EVENTOUT		38
-	49	PF11	I/O	FT		DCMI_12/ EVENTOUT		37
37	48	PB2-BOOT1 (PB2)	I/O	FT		EVENTOUT		36
36	47	PB1	I/O	FT	(4)	TIM3_CH4 / TIM8_CH3N/ OTG_HS_ULPI_D2/ ETH_MII_RXD3 / OTG_HS_INTN / TIM1_CH3N/ EVENTOUT	ADC12_IN9	35
35	46	PB0	I/O	FT	(4)	TIM3_CH3 / TIM8_CH2N/ OTG_HS_ULPI_D1/ ETH_MII_RXD2 / TIM1_CH2N/ EVENTOUT	ADC12_IN8	34

34	45	PC5	I/O	FT	(4)	ETH_RMII_RX_D1 / ETH_MII_RX_D1/ EVENTOUT	ADC12_IN15	33
33	44	PC4	I/O	FT	(4)	ETH_RMII_RX_D0 / ETH_MII_RX_D0/ EVENTOUT	ADC12_IN14	32

Pin nun		Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions	
LQFP100	LQFP144							
32	43	PA7	I/O	FT	(4)	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1/TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / RMII_CRS_DV/ EVENTOUT	ADC12_IN7	31
31	42	PA6	I/O	FT	(4)	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6	30
30	41	PA5	I/O	TTa	(4)	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CHIN/ EVENTOUT	ADC12_IN5/DAC2_OUT	29
29	40	PA4	I/O	TTa	(4)	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	ADC12_IN4 /DAC1_OUT	28
26	37	PA3	I/O	FT	(4)	USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/ EVENTOUT	ADC123_IN3	27
25	36	PA2	I/O	FT	(4)	USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/ EVENTOUT	ADC123_IN2	26

24	35	PA1	I/O	FT	(4)	USART2_RTS / UART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIMM2_CH2/ EVENTOUT	ADC123_IN1	25

Pin nun		Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions	
LQFP100	LQFP144							
23	34	PA0-WKUP (PA0)	I/O	FT	(5)	USART2_CTS/ UART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/ EVENTOUT	ADC123_IN0/WKUP(4)	24
18	29	PC3	I/O	FT	(4)	SPI2_MOSI / I2S2_SD / OTG_HS_ULPI_NXT / ETH_MII_TX_CLK/ EVENTOUT	ADC123_IN13	23
17	28	PC2	I/O	FT	(4)	SPI2_MISO / OTG_HS_ULPI_DIR / TH_MII_TXD2 /I2S2ext_SD/ EVENTOUT	ADC123_IN12	22
16	27	PC1	I/O	FT	(4)	ETH_MDC/ EVENTOUT	ADC123_IN11	21
15	26	PC0	I/O	FT	(4)	OTG_HS_ULPI_STP/ EVENTOUT	ADC123_IN10	20
-	22	PF10	I/O	FT	(4)	FSMC_INTR/ EVENTOUT	ADC3_IN8	19
-	21	PF9	I/O	FT	(4)	TIM14_CH1 / FSMC_CD/ EVENTOUT	ADC3_IN7	18
-	20	PF8	I/O	FT	(4)	TIM13_CH1 / FSMC_NIOWR/ EVENTOUT	ADC3_IN6	17
-	19	PF7	I/O	FT	(4)	TIM11_CH1/FSMC_NREG/ EVENTOUT	ADC3_IN5	16

-	18	PF6	I/O	FT	(4)	TIM10_CH1 / FSMC_NIORD/ EVENTOUT	ADC3_IN4	15
-	15	PF5	I/O	FT	(4)	FSMC_A5/EVENTOUT	ADC3_IN15	14
-	14	PF4	I/O	FT	(4)	FSMC_A4/EVENTOUT	ADC3_IN14	13
-	13	PF3	I/O	FT	(4)	FSMC_A3/EVENTOUT	ADC3_IN9	12
-	12	PF2	I/O	FT		FSMC_A2 / I2C2_SMBA / EVENTOUT		11
-	11	PF1	I/O	FT		FSMC_A1 / I2C2_SCL / EVENTOUT		10
-	10	PF0	I/O	FT		FSMC_A0 / I2C2_SDA / EVENTOUT		9
7	7	PC13	I/O	FT	(2)(3)	EVENTOUT	RTC_AF1	8
5	5	PE6	I/O	FT		TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7 / EVENTOUT		7
4	4	PE5	I/O	FT		TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6 / EVENTOUT		6
3	3	PE4	I/O	FT		TRACED1/FSMC_A20 / DCMI_D4/ EVENTOUT		5
2	2	PE3	I/O	FT		TRACED0/FSMC_A19 / EVENTOUT		4
Pin nun		Pin name (function after reset)(1)	Pin type	I / O structure	Notes	Alternate functions	Additional functions	
LQFP100	LQFP144							
1	1	PE2	I/O	FT		TRACECLK/ FSMC_A23 / ETH_MII_TXD3 / EVENTOUT		3

98	142	PE1	I/O	FT		FSMC_NBL1 / DCMI_D3/ EVENTOUT	
97	141	PE0	I/O	FT		TIM4_ETR / FSMC_NBL0 / DCMI_D2/ EVENTOUT	

2

1

STM32F407ZET6 Board TFT LCD Pins:

P.num	name	J.B	J.J	alternate func	P.num	name	J.B	J.J	alternate func
1.	GND				2.	NRST		RST	
3.	PD10	B.50.		FSMC_D15	4.	PD9		B.51.	FSMC_D14
5.	PD8	B.52.		FSMC_D13	6.	PE15		J.52.	FSMC_D12
7.	PE14	J.51		FSMC_D11	8.	PE13		J.50	FSMC_D10
9.	PE12	J.49		FSMC_D9	10.	PE11		J.48	FSMC_D8
11.	PE10	J.47		FSMC_D7	12.	PE9		J.46	FSMC_D6
13.	PE8	J.45		FSMC_D5	14.	PE7		J.44	FSMC_D4
15.	PD1		B.21	FSMC_D3	16.	PD0	B.22		FSMC_D2
17.	PD15		B.45	FSMC_D1	18.	PD14	B.46		FSMC_D0
19.	PD4	B.18		FSMC_NOE	20.	PD5		B.17	FSMC_NWE
21.	PF12		J.38	FSMC_A6	22.	PG12		B.11	FSMC_NE4
23.	PB0		J.34		24.	PC13		J.8	
25.	PF11	J.37			26.	PB2		J.36	
27.	PB1	J.35			28.	PB15		B.53	LCD LED FET GATE
29.	NC.				30.	GND			
31.	+3.3V				32.	GND			

Magyarázat:

B.n = baloldali csatlakozó sorszám (J1)

J.n = jobb oldali csatlakozó sorszám (J2)

J.B = Jumper.Bal oldala

J.J = Jumper.Jobb oldala