# Zen → Cen → Sen - Evolution of a Minimalistic IV Conversion Circuit

*EUVL*

## How it started

I have to admit that the AD844 based RIAA preamp circuit from LC Audio [1] fascinates me. I was looking, once again, at their "optical supply" MC head amp [2] the other night, only to find out that it was adopted from Leach's common-base MC head amp [3] published a while ago.

There are already detailed descriptions of how the circuit works at both the LC Audio and the Leach websites, so I am not repeating that here. What interests me about the Leach head amp is that it is not a voltage amplifier. Rather it is a current conveyor, at the output of which the current is converted to voltage by means of the output resistor (Riv). There are a quite few threads on DIY Audio about the Leach Head Amp, and various people have commented about its noise level and distortion level, not always positively.

It still appealed to me somehow, because of its simplicity, and I thought something similar could be very useful for IV conversion for current-output DACs. I spent some time figuring out how to do it with JFETs instead. And the solution in the end was obvious.

Using JFETs in this circuit has some key advantages, at least for DAC IV conversion. It eliminates all the biasing resistors and capacitor around the base of the bipolar transistors, and you only need to tie both JFET gates to the DAC ground, thus simplifying the circuit even further. All is left now are a pair of complementary JFETs with matched Idss, a (battery) floating power supply, 2 decoupling caps, and one IV-conversion resistor. It all seems obvious, but the elimination, or at least drastic reduction, of the base current through the BJT's back to the DAC Gnd is a key performance advantage of this JFET based circuit compared to the original, as will be explained later.

I then noted the similarity of this circuit to Nelson Pass's Zen IV [4] (**Figure 1**) in terms of components, though there are also some key differences in circuitry. In the Zen IV, the IV conversion is done by the two 1k resistors at the positive and negative rails, connected to the output via two high-pass filters in parallel. Thus, the 10uF coupling caps are working in voltage mode, and their non-linearities will

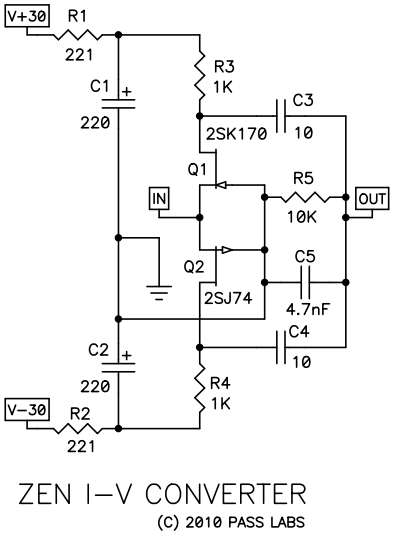


*Fig 1: Nelson Pass' Zen IV.*

appear as output distortion. On top of that, any noise on either power supply rail will be fed directly through to the output, i.e. there is no PSRR. This adds to the requirement for the power supply.

As I pointed out at the beginning of the Zen IV thread [5], there are a few more limitations of the Zen circuit. Let's take a DAC like PCM1704 with 1.2mA output. To get 2Vrms out, one needs to use 4.7k resistors at both rails for IV conversion. And in order to keep the current swing small compared to bias (for low distortion), the bias current, in this case also Idss, of the JFETs wants to be, say, 6mA minimum. This means, however, 28V across the 4.7k resistors, requiring +/- 37V rails or higher. The resistors see continuous dissipation of 170mW, increasing thermal noise in the resistors.

The equivalent input resistance of the Zen IV equals to the reciprocal of the sum of transconductances of the JFET pair, and is about 17 ohm. If one wishes to keep this lower, to say <10R, one needs to use 2 pairs of complementary JFETs in parallel, each with 6mA+ Idss. This, however, means +/- 65V rails, and 0.7W continuous dissipation per resistor.

Most of these drawbacks are not applicable to the JFET "Leach" circuit, which I nicknamed Cen IV (to reflect its complementary nature; **Figure 2**). An 18V supply across the two JFETs is quite sufficient, though you can go further to 27V or 36V if you wish. The benefit of higher voltage is lower JFET capacitances, which in turn means higher bandwidth and lower distortion. The Riv only carries the signal current from the DAC, and no quiescent current. Changing the IV conversion gain (from say 500R to 2.7k), or increasing the number of JFETs in parallel, does not affect the rest of the circuit – no changes in rail voltages, or resistor wattage, etc. And the battery only sees a constant current load,

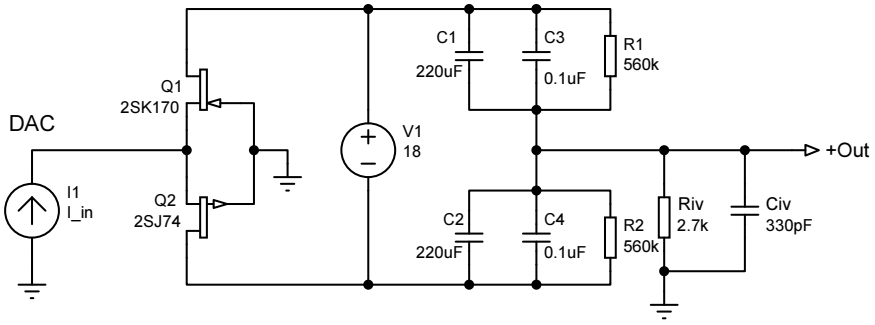


*Fig 2: The Cen IV ( 2SK170 / 2SJ74, matched Idss )*

as the DAC current runs in a separate loop and does not go through the batteries at all. The only drawback is the necessity of a floating power supply. But two 9V-block NiMH rechargables would easily provide 10 hours of operation. So this is not a real problem.

I made a direct comparison between the distortion performance of the Zen IV vs. the Cen IV in Spice, using the same JFET Spice models in both circuits. The Zen IV is the original circuit as published, and the Cen IV has a Riv of 500R for the same transimpedance gain as the Zen. The results are somewhat surprising. For a current input signal of +/- 1mA, 1kHz sine, THD is 0.000257% for Zen, and 0.000066% for Cen. The JFET models being identical, this is pure circuitry difference; a factor of four improvement. My interpretation is that the Zen IV is a push pull transimpedance amplifier, whereas the Leach circuit is a pure current conveyor, as the power supply is not connected to the DAC ground and therefore runs in a current loop totally separate from the signal current loop. Except for the JFET gate connections to DAC Gnd, the entire input signal current has to return to DAC Gnd via Riv. Thus, whatever non-linearities there are in the devices, Kirchhoff's law ensures near-zero distortion (the resistor Riv is also not 100.000000% distortion free [6]). However, because of the presence of Cgd and Cgs of the JFETs, there is a very tiny leakage current through the gates to DAC Gnd in the presence of an AC signal, and this tiny current is not flowing though Riv. If this current is not perfectly linearly proportional to the input current signal (and it is not), it is precisely this non-linearity that contributes to distortion in the CEN circuit. We shall expect that distortion decreases with JFET capacitances, and increases with frequency. What about a higher transimpedance than 500R? Using Riv of 2.7k in the Cen circuit, THD is 0.0019% at 1kHz. The floating PSU essentially swings together with the output signal relative to DAC Gnd. And the higher the output swing, the higher the leakage current through the JFET gates, and thus the higher the distortion. But still, the performance is very respectable by any standard.

I could have stopped here. But 2SJ74s are becoming increasingly difficult to get. And the 2J103 / 2SK246 pair is of little use here due to its low transconductance. So I wanted to come up with a design with only N-JFETs, and at the same time make use of their lower capacitance to reduce distor-

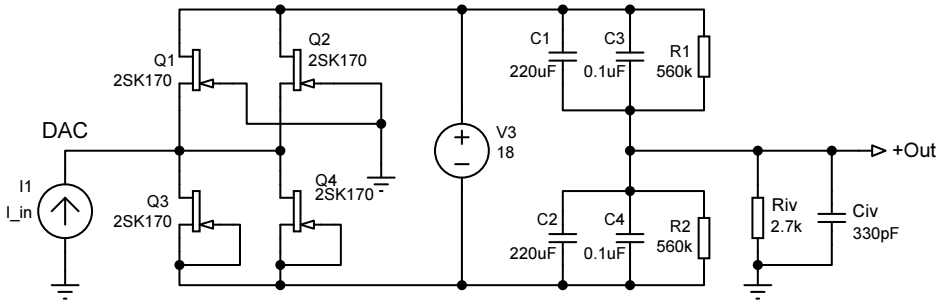


*Fig. 3: The Sen IV (4x 2SK170, matched Idss).*

tion further. The new circuit, which I named Sen IV (S for Single Ended; **Figure 3**), is much akin to the current-source-loaded JFET follower, published by Curl, Borbely, Feucht, and Pass on various occasions. To get close to the same input impedance as the 2SK170 / 2SJ74 pair, a total of 4x 2SK170's are used, as the two lower ones merely acts as current source and play no part in determining the input impedance. One penalty is increased current consumption. But even at about 20mA total bias, this is still not unacceptably high. Distortion now is 0.0012% (-98.4dB) with 2.7k Riv, a touch lower than Cen. As already mentioned, only the top two 2SK170's are contributing to gate leakage related distortion. Since the 2SK170 has lower capacitance as the 2SJ74, it is not too surprising that the distortion in the Sen IV is further reduced.

These THD figures do not necessarily represent reality, as they are only as accurate as the Spice models themselves, and all passive components, current sources, power supplies are assumed ideal. It does, however, indicate that the development of the circuitry itself is going in the right direction.

## Bread-boarding & First Measurements

Once I was happy with the circuit, it was time to build and test. Idss-matched devices (8.5mA) were dug out from my JFET stock and breadboard circuits were quickly assembled. Two important issues became obvious at this point – a true floating supply with no coupling to Ground (I used 2x 9V batteries which gave no problems at all), and the need of a potential divider to set the floating power supply symmetrically about Input Ground during start up. The latter was easily achieved by adding a pair of resistors of identical values in parallel to the output coupling caps. I tried anything from 68k to 560k, and they all worked fine, so the value is not critical. Eventually I settled on 560k.

For measurement purposes, the two decoupling capacitors are not so critical. I just used a pair of ordinary electrolytic capacitors, such as Panasonic FC 100uF 16V. There is room for experiment in the eventual application, where I plan to start off using German-made Frolyt Bipolar (220uF 25V), followed by ELNA RBP 220uF 16V bipolar, and Nichicon Muse ES 100uF 16V bipolar, in parallel with WIMA MKP2 0.1uF 250V. One could also use large-value film caps, such as WIMA MKS2-XL 15uF. The minimum value of the capacitance should not be less than 4.7uF, assuming a Riv of 2.7k at the out-

put. If you use a lower Riv value because of higher DAC current output, you should consider increasing the minimum value of the capacitors accordingly. The choice of capacitor is endless but at the same time controversial, so I shall leave you to experiment with whatever unobtainium caps you have in your stock.

To simulate a current-output DAC for testing purposes, I had to build a high bandwidth, ultra low distortion VCCS (voltage controlled current source). The circuit in Fig. 9 of National Semiconductor's AN1515 was chosen, and implemented using an OPA1642 dual opamp, 4 Caddock MKV132 10k resistors matched to 0.01%, and a 1k 0.1% Vishay Dale CMF55 as gain resistor (R13). It is essential to use very low distortion components, and I consider a JFET input opamp to be advantageous here. Measurements verified that the VCCS was low enough in distortion (<-90dB) and high enough in bandwidth (> 1MHz) to be not limiting the first measurements. Here are a few initial measurements.

**Figure 4 and 5** show the measurements for the Cen IV circuit. The -3dB bandwidth is around 220kHz

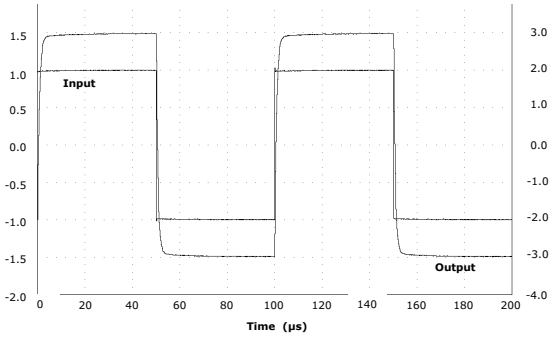


*Fig 4: Cen IV 10kHz +/-1mA Square Wave (Riv = 3k; smaller curve = Vin for VCCS, larger curve = Vout Cen IV, unfiltered)*

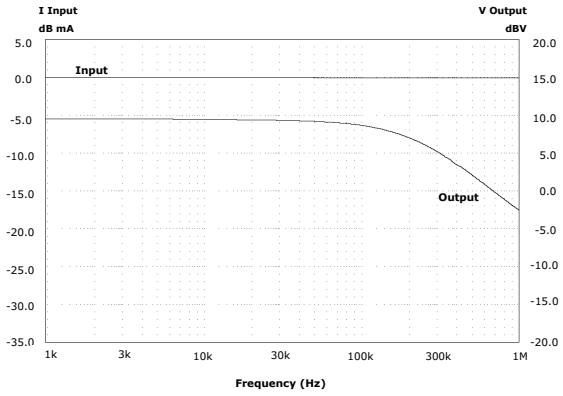


*Fig 5: Cen IV Frequency Response at +/-1mA sine wave input (Riv = 3k; top = Vin for VCCS, bottom = Vout Cen IV, unfiltered)*

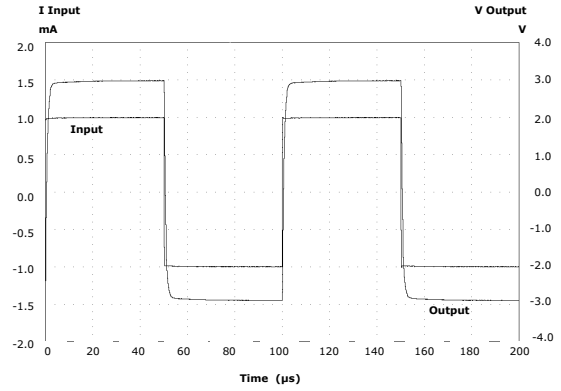


*Fig 6: Sen IV 10kHz +/-1mA Square Wave (Riv = 3k; smaller curve = Vin for VCCS, larger curve = Vout Sen IV, unfiltered)*

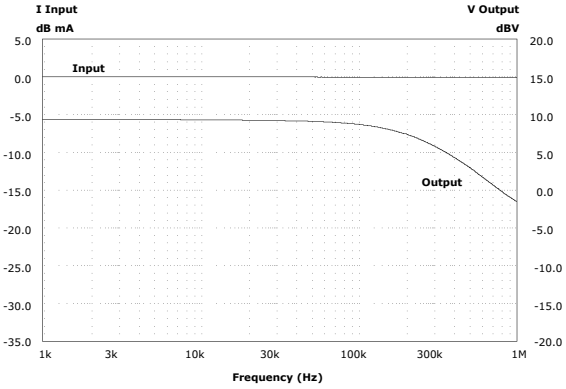


*Fig 7: Sen IV Frequency Response at +/-1mA sine wave input (Riv = 3k; top = Vin for VCCS, bottom = Vout Sen IV, unfiltered)*

This is followed in by the results for the Sen IV in **figures 6 and 7**. The -3dB bandwidth is now around 300kHz due to the lower capacitances of the N-JFETs.

## Circuit Variants

Now that the basic circuits have been proven, we can look at a couple of variants, apart from playing with passive components.

As already mentioned, both Cen (with one 2SK170 / 2SJ74 matched pair) and Sen (with 4x 2SK170 matched) have an input resistance of about 15R. If this is too high for your DAC, you can half that in value by using 2 pairs of 2SK170 / 2SJ74 for Cen, and 4 matched 2SK369 for Sen. The input capacitances will double in both cases, and so would distortion. So low input impedance comes at a cost, and has to be balanced against distortion reduction in the DAC itself with various input impedance values of the IV circuit.

The use of only N-JFETs in the Sen makes it really versatile. You can basically use any TO92 N-JFET at

Idss. If you can live with a slightly higher input resistance, say 25R, you may use 4 matched 2SK117BL; this device has 1/3 of the capacitance of the 2SK170. The bandwidth can then be increased to near 1MHz, and the distortion reduced by another 10dB. A truly excellent performer !!

## Application Limitations

As is the case for the Zen IV, these circuits work with DACs with symmetrical current outputs and at 0V DC nominal. With slight modifications and added complexity, however, it is possible to adapt the circuit for single rail DACs with DC biased voltage and/or current at their outputs. E.g. you can hang the gates of the JFETs at an elevated voltage from DAC to cater for voltage bias, or you can pick JFETs with different Idss on purpose to cope with current bias. I shall leave this as an exercise to those skilled in the art.

Also, using 4 FETs at 10mA Idss as in the Sen IV, the total quiescent current is 20mA. I would not swing more than 25% of this, so the i_out of your DAC should not be >5mA. If your DAC has a higher current output, you just have to put more JFETs in parallel, or use devices with an even higher Idss. With 9V across each JFET, 20mA bias is still not excessive in terms of dissipation, especially if you use a small heat sink on the devices.


## PCB Layout

A couple of PCBs were quickly put together (**Fig 8**). The most critical passive component for the entire circuit is probably Riv. The PCBs were designed to accept Caddock MKV132 or Texas TX2575. You may use other resistor types, and I recommend you to solder the resistor directly at the output connector anyhow. If you are using non-oversampling DACs and want to limit the bandwidth further, you can solder a film cap at the position marked Civ, such as WIMA FKP2 or MKP2. A 330pF film cap in combination with a Riv of 2.7k will form a first order LP filter at 180kHz, for example. For optimal thermal tracking, I made use of our famous JFET heat sinks produced by wire cut EDM.

*Fig 8: The Prototypes*

## Final Measurements

I took the prototypes together with the VCCS to Jan Didden's one evening. Before measuring the IV circuits, we first checked the signal source. To measure the VCCS, we connected a 20R resistor to its output, so as to simulate the input impedance of the IV circuit.

The FFT of the analogue generator of the AP at 1Vrms output shows a HD of -100dB for 2nd and 3rd, and -105dB at 4th. Adding the VCCS to that, and with a 20R load resistor at its output the distortions all rose to about -90dB (**Fig 9**). This might well be due to the fact that the signal level is low (20mVrms) and thus the relative noise level as well as the preamp distortion of the AP might add to the distortion of the VCCS itself.

After some discussions and experiments, Jan and I decided to use a 20k resistor directly in series with the AP analogue generator output set at 20Vrms output to simulate a 1mA rms current source. This might still not be totally distortion free, but it appears that we can get better results than the VCCS. It just proves once again that measuring very low distortion levels is not a simple matter.

At 20Vrms output, the HD of the signal source is -115dB for 2nd, and about -105dB for 3rd and 4th. Almost identical or a very slight improvement relative to 1Vrms

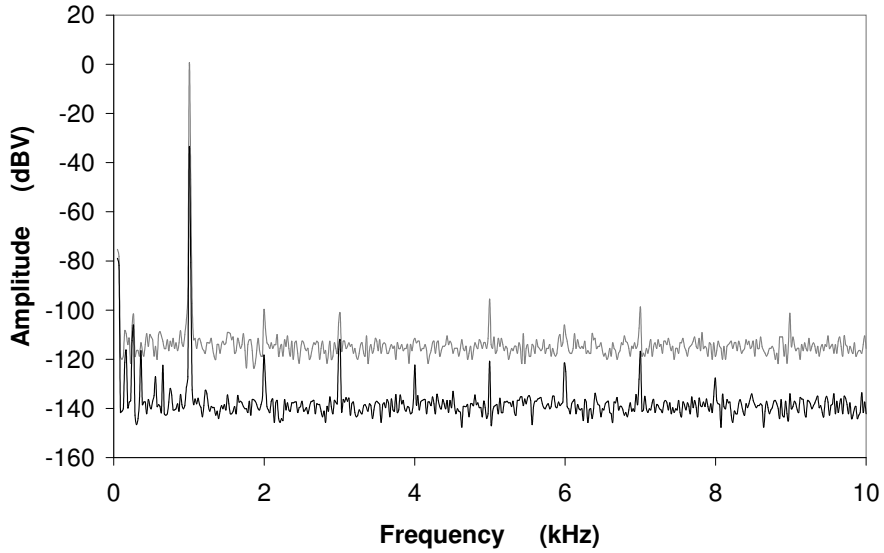


*Fig 9: FFT of VCCS with 20R resistor at output (top : Signal Source 1Vrms, bottom : VCCS Voltage Output at 20mV RMS)*

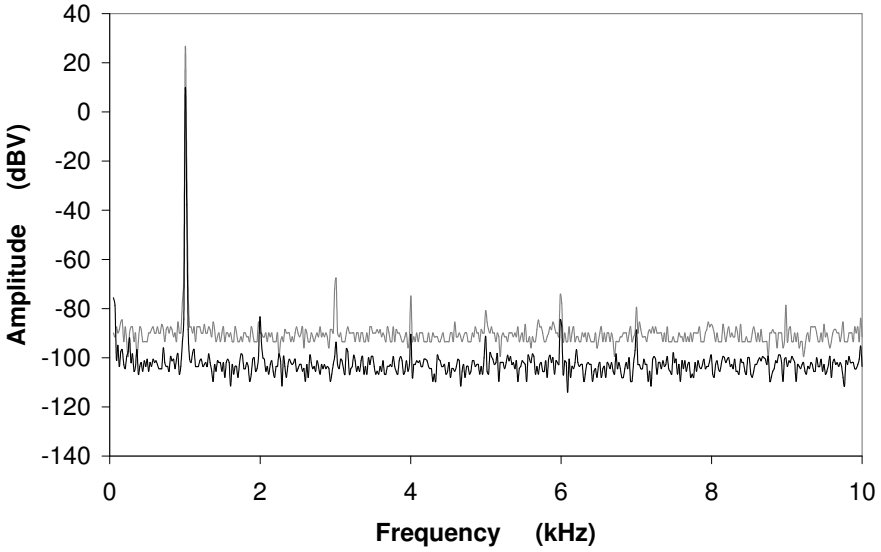


*Fig 10: FFT of Sen IV using 20k series resistor at input (top : Signal Source, bottom : IV Voltage Output)*

Then we proceeded to measure both the Cen & Sen IV's, each using 2.7k in parallel with 330p at the output. As the measurement was done at 1kHz, we would not see too much of a LP filter at 180kHz, but noise floor will improve at HF.

Apply 20Vrms input to the 20k series resistor, the input current is 1mA rms. The measured distortion of the Sen (**Fig 10**) circuit (after correcting for the distortion of the signal source) is -93dB 2nd, -100dB 3rd, and -110dB 4th. For any of the values to be totally reliable below -100dB, we need a much better signal source, and ideally a current signal source first.

Similarly, for the Cen circuit (**Fig 11**), the corrected distortions are -92dB for 2nd, -101dB 3rd, and -110dB 4th, essentially identical to the SEN and indicating that the distortion in the current signal source is masking the accuracy of the measurement of the IV circuit. Reducing the input amplitude by half reduces THD by some 4dB, but again the signal source is likely to be masking the performance of the IV circuit itself.

The orders of magnitude of these values are similar to those of the simulation. Rather than chasing academically perfect figures and 100% correlation between theory & measurement, I consider these decent enough. In practice, one can easily reduce all even harmonics further by running two of them in balanced mode.

We also did a quick frequency sweep to verify the hypothesis that THD increases with frequency (**Fig 12**).

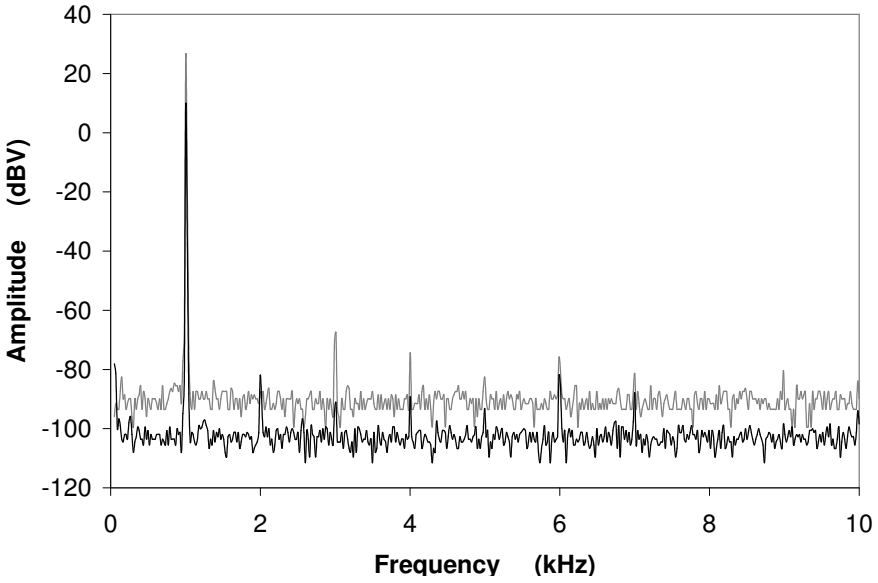


*Fig 11: FFT of Cen IV using 20k series resistor at input (top : Signal Source, bottom : IV Voltage Output)*

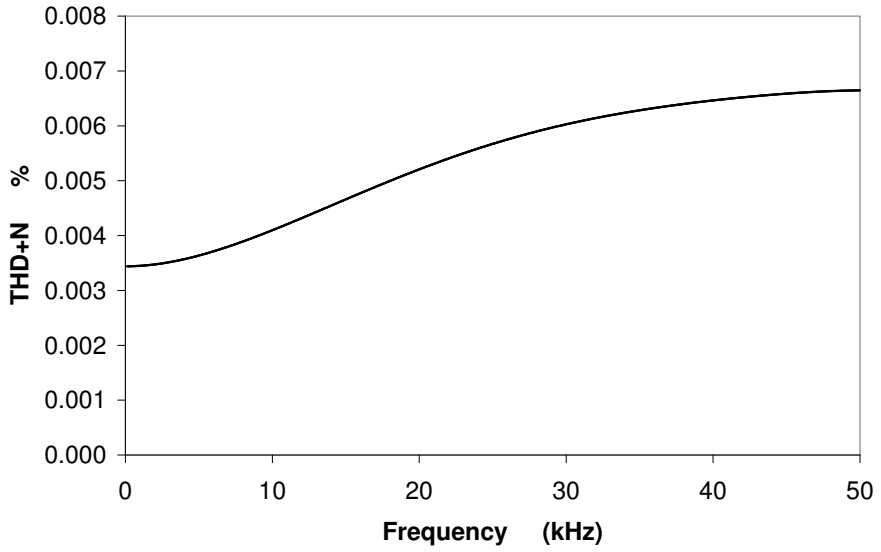


*Fig 12: THD vs. Frequency of Cen IV using 20k series resistor at input*

The inevitable question now is – how does it sound? We cannot possibly give you a neutral opinion, and shall therefore only urge you to try these simple yet high performance circuits for yourselves.

## Support

To enable the reader to experiment with these two simple yet elegant circuits themselves, an evaluation pack will be made available as a Group Buy on DIY Audio after the publication of the article. Each pack will include :

2x Cen IV PCBs (4 single ended or 2 balanced IV in total), single sided 35um copper, 1.6mm FR4
2x Sen IV PCBs (4 single ended or 2 balanced IV in total) , single sided 35um copper, 1.6mm FR4
4x Quad JFET heat sink Type 10 (for Sen IV)
4x Dual JFET heat sink Type 0 (for Cen IV)

Optionally
2x Idss matched 2SJ74BL

I included the 2SJ74 (limited to 40 pairs) as they are now hard to get, but 2SK170 and others are still easily available, so I shall leave you to source those separately.

## Acknowledge

Most sincere thanks to Jan Didden and WK Lai, for the many interesting discussions during the circuit development, and for helping with the simulation work, the measurements, and arranging the prototype PCBs. Nelson Pass kindly allowed the inclusion of the schematic for his Zen IV circuit for which I thank him.

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