The total equivalent junction capacitor C_{HB} of VS node is shown in **Figure 18**.

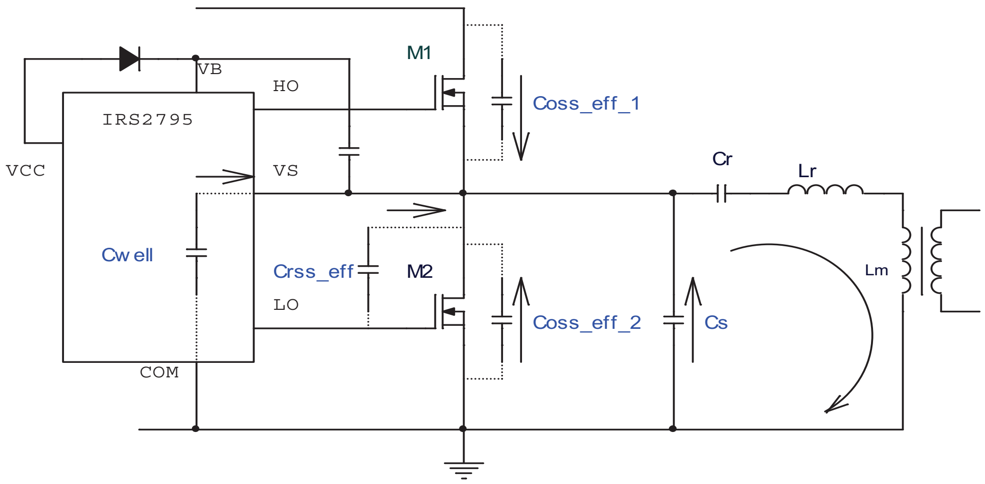

Figure 18: VS Equivalent junction capacitor

$$C_{HB} = 2 \cdot Coss\_eff + Crss\_eff + C_{Well} + Cs$$

It includes:

The *effective Coss* of the two MOSFETs (both high-side and low-side);

The *Coss_eff* as defined in the MOSFET datasheet is the effective capacitance of MOSFET that gives the same charging time as a fixed capacitor while V_{DS} is rising from 0 to 80% of V_{DS}. So the *Coss_eff* of a 500V MOSFET is defined under 0 to 400V V_{DS} which fits to this application.

The *effective Crss* of the low-side MOSFET;

The *Crss* of MOSFET is typically defined at VDS=25V. The *Crss* capacitance value reduces as VDS voltage increasing. So the *effective Crss* can be chose as ½ or 1/3 of *Crss*.

The stray capacitance *Cwell* of IRS2795(1,2);

The stray capacitance of IRS2795(1,2) is the high-side well capacitance of the 600V driver. The value of the stray capacitor is around 5pF.

The snubber capacitor Cs (if any) that is connected to the VS node.

For example, the *Coss_eff* of MOSFET STF13NM50N is 110pF, Crss is 5pF, and there is no snubber capacitor to the VS node, the (dis-)charging time of VS node can be calculated as:

$$Coss\_eff = 110\,pF,\ \ Crss\_eff = 2.5\,pF,\ \ C_{Well} = 5\,pF,\ \ Cs = 0\,pF$$

$$Tch = \frac{C_{HB} \cdot Vin\max}{I'\,pri(pk)}$$

$$Tch = 185ns$$

The dead-time calculation should also include the gate driver falling time. The MOSFET turn-off timing diagram is shown in **Figure 19**, which using LO and M2 as an example. In the first time interval t1, gate voltage discharges to a plateau voltage V'm, and both VDS voltage and I_D current