Pi3560/3660 Block Diagram

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU CORE ISL6266A P40

CPU Penryn
478P (uPGA)/35W
P3

CPU THERMAL SENSOR

14.318MHz
CLOCK GEN
CK505
SLG8SP568 P2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

VCCP +1.5V AND GMCH 1.05V(RT8204) P37, 38

DDRIII SMDDR_VTERM +1.8VSUS(TPS51116RGER) P36

DDRII-SODIMM1 — DDRII 800MHz — P10
DDRII-SODIMM2 — DDRII 800MHz

NORTH BRIDGE
Cantiga
PM45
P5

PCI-E GFx X 16

27MHz
VGA
nVidia N10P-GS
P12

A-CH
B-CH
VRAM DDR3
VRAM DDR3
P17

CRT P23
HDMI P23
LCD CONN P24

DMI LINK

32.768KHz
NBSRCCLK, NBSRCCLK#

SATA - HDD — SATA0 3GBPS — P29
SATA - CD - ROM — SATA13GBPS

SOUTH BRIDGE
ICH-9M
PCIE X 6
USB X 12
P19

USB2.0

USB2.0 Ports X 2 P29
USB2.0/ e SATA Ports X 1 P29
Webcam P33
Mini PCI-E x1 P30
Express Card P30

PCI-E

Azalia

Mini PCI-E Card X 1 P30
LAN Realtek 10/100/1000M RTL8111DL P25
Express Card power switch RICOH R5538D (NewCard) P30
Realtek RTS5158E P28
24.576MHz
Memory CardReader

25MHz
RJ45

Codec Realtek ALC272 P26
Audio Amplifier TPA6017A2 P27
Speaker P27

Headphone LINE Out SPDIF P27
LINE IN P27
MIC P27

SYSTEM POWER MAX17101

32.768KHz
LPC

KBC
ITE 8502E
P31

P32 Keyboard
P32 Touch Pad
P35 SYSTEM CHARGER MAX17005

FAN P33
SPI ROM 16Mbits P31

PROJECT : EF7/9A
Quanta Computer Inc.

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02

<4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
<3,4,5,6,8,9,12,13,14,19,22,23,34,38,40> +1.05V

+3V
L18 HCB1608KF-181T15_1.5A
C325 10U/6.3V/X5_8
C335 .1U/10V/X5_4
C326 .1U/10V/X5_4
C359 .1U/10V/X5_4
C324 .1U/10V/X5_4
C332 .1U/10V/X5_4
+CK_VDD_MAIN
L21 HCB1608KF-181T15_1.5A
VDDCPU
C350 10U/6.3V/X5_8
C343 .1U/10V/X5_4
L22 HCB1608KF-181T15_1.5A
+CK_VDD_MAIN2
C371 10U/6.3V/X5_8
C352 .1U/10V/X5_4
C358 .1U/10V/X5_4
C360 .1U/10V/X5_4
C338 .1U/10V/X5_4
C341 .1U/10V/X5_4
C323 .1U/10V/X5_4

Y6 XTAL_14.318MH
CG_XIN 1 2 CG_XOUT
C337 27P/50V/NPO_4
C339 27P/50V/NPO_4

U16
CK505
+CK_VDD_MAIN → 23 VDDPLL3, 16 VDD48, 9 VDDPCI, 4 VDDREF, 46 VDDSRC, 62 VDDCPU
VDDCPU
+CK_VDD_MAIN2 → 19 VDD96I/O, 27 VDDPLL3I/O, 33 VDDSRCI/O, 43 VDDSRCI/O, 52 VDDSRCI/O, 56 VDDCPU_IO
55 NC
CG_XIN → 3 X1
CG_XOUT → 2 X2
<21> CK_PWG → CPU_BSEL1 R441 2.2K_4 → FSB
63 CK_PWRGD/PD#
64 FSLB/TEST_MODE

0812 Del 0ohm in Ver.C.

<10,11,30> CGCLK_SMB → CGCLK_SMB → 7 SCLK
<10,11,30> CGDAT_SMB → CGDAT_SMB → 6 SDATA

C313 *27P/50V_4 for EMI

22 GND, 26 GND, 18 GND48, 59 GNDCPU, 15 GNDPCI, 1 GNDREF, 30 GNDSRC, 36 GNDSRC, 49 GNDSRC

65 EPAD

ICS9LPRS365BKLFT

CPUCLKT0 61 → CLK_CPU_BCLK <3>
CPUCLKC0 60 → CLK_CPU_BCLK# <3>
CPUCLKT1 58 → CLK_MCH_BCLK <5>
CPUCLKC1 57 → CLK_MCH_BCLK# <5>
CPUT2_ITP/SRCT8 54 → CPU_ITP → T50
CPUC2_ITP/SRCC8 53 → CPU_ITP# → T52
DOTT_96/SRCT0 20 → T41
DOTC_96/SRCC0 21 → T40
27MHz_Nonss/SRCCLK1/SE1 24 → CLK_27M_NONSS_C R525 33_4 → CLK_27M_NONSS <14>
27Mhz_ss/SRCCLC1/SE2 25 → CLK_27M_SS_C R526 33_4 → CLK_27M_SS <14>
SRCCLKT2/SATACL 28 → CLK_PCIE_SATA <19>
SRCCLKC2/SATACL 29 → CLK_PCIE_SATA# <19>
SRCCLKT3/CR#_C 31 → CLK_PCIE_VGA <12>
SRCCLKC3/CR#_D 32 → CLK_PCIE_VGA# <12>
SRCCLKT4 34 → CLK_PCIE_3GPLL <6>
SRCCLKC4 35 → CLK_PCIE_3GPLL# <6>
PCI_STOP# 45 → PM_STPPCI# <21>
CPU_STOP# 44 → PM_STPCPU# <21>
SRCCLKT6 48 → CLK_PCIE_MINI <30>
SRCCLKC6 47 → CLK_PCIE_MINI# <30>
SRCCLKT7/CR#_F 51 → CLK_PCIE_ICH <20>
SRCCLKC7/CR#_E 50 → CLK_PCIE_ICH# <20>
SRCCLKT9 37 → CLK_PCIE_LAN <25>
SRCCLKC9 38 → CLK_PCIE_LAN# <25>
SRCCLKT10 41 → R_CLK_PCIE_NEW_C → 2 4 *0X2 1 3 RP28 → CLK_PCIE_NEW_C <30>
SRCCLKC10 42 → R_CLK_PCIE_NEW_C# → CLK_PCIE_NEW_C# <30>
SRCCLKT11/CR#_H 40 → NEW-CARD_CLK_REQ#_R R232 475/F_4 → NEW-CARD_CLK_REQ# → NEW-CARD_CLK_REQ# <30>
SRCCLKC11/CR#_G 39 → CLK_3GPLLREQ#_R R218 475/F_4 → CLK_MCH_OE# → CLK_MCH_OE# <6>
PCICLK0/CR#_A 8 → PCI_ICH
PCICLK1/CR#_B 10 → PCIE_LANREQ#_R T42 R184 475/F_4 → PCIE_LANREQ# → PCIE_LANREQ# <25>
PCICLK2/TME 11 → PCLK_2
PCICLK3 12 → PCLK_MINI_LPC T37 R192 33_4 → PCLK_LPC_DEBUG → PCLK_LPC_DEBUG <30>
PCICLK4/27_SELECT 13 → FCTSEL1 R182 33_4 → PCLK_LPC_8512 → PCLK_LPC_8512 <31>
ITP_EN R181 33_4 → PCLK_ICH → PCLK_ICH <20>
PCI_F5/ITP_EN 14 → R178 22_4 → CLK_48M_USB_CR → CLK_48M_USB_CR <28>
R180 22_4 → CLK_48M_USB → CLK_48M_USB <21>
USB_48MHZ/FSLA 17 → FSA R179 *2.2K_4 → CPU_BSEL0
FSLC/TST_SL/REF 5 → R173 33_4 → CLK_14M_ICH → CLK_14M_ICH <21>
FSC R174 4.7K_4 → CPU_BSEL2

0513 SWAP
CLK_PCIE_3GPLL vs CLK_PCIE_LAN
CLK_PCIE_MINI vs CLK_PCIE_ICH

0907 Short RP29 in FAI.

0815 R177 change from 22 to 33 ohm
R178 change from 10K to 4.7K
for RTC timer issue in Ver. C.

+3V
CLK_MCH_OE# R223 10K_4
NEW-CARD_CLK_REQ# R231 10K_4
PCIE_LANREQ# R185 10K_4
PM_STPPCI# R523 *10K_4
PM_STPCPU# R524 *10K_4

+3V
R187 10K_4
R186 10K_4
<21> PDAT_SMB → Q9 2N7002 → CGDAT_SMB
+3V
<21> PCLK_SMB → Q8 2N7002 → CGCLK_SMB

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

+3V
R176 10K_4
PCLK_2
R183 *4.7K_4
0=overclocking of CPU and SRC Allowed
1 = overclocking of CPU and SRC not Allowed

0428 correct Net name PCLK_2

+3V
R172 10K_4
FCTSEL1
R191 *10K_4
PCI4/27_Select:
1=27MHz,0=SRC_100MHz
of Pin17 & Pin18.

0512 Change Strap

ITP_EN
R190 10K_4
Disable ITP

CPU Clock select

<3> CPU_BSEL0 → CPU_BSEL0 R170 *0_4S → MCH_BSEL0 <6>
R175 *1K_4
<3> CPU_BSEL1 → CPU_BSEL1 R432 *0_4S → MCH_BSEL1 <6>
+1.05V R433 *1K_4
<3> CPU_BSEL2 → CPU_BSEL2 R169 *0_4S → MCH_BSEL2 <6>
+1.05V R171 *1K_4

2	1	0			
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

0519 Update BSEL default follwed CPU.
0912 Short R117,R186,R189 in FAI.

0428 delete SIO connection

C315 27P/50V/NPO_4 CLK_48M_USB_CR
C316 27P/50V/NPO_4 CLK_48M_USB
C314 27P/50V/NPO_4 CLK_14M_ICH
C452 27P/50V/NPO_4 PCLK_LPC_DEBUG
C318 27P/50V/NPO_4 PCLK_LPC_8512
C317 27P/50V/NPO_4 PCLK_ICH
for EMI

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Quanta Computer Inc.

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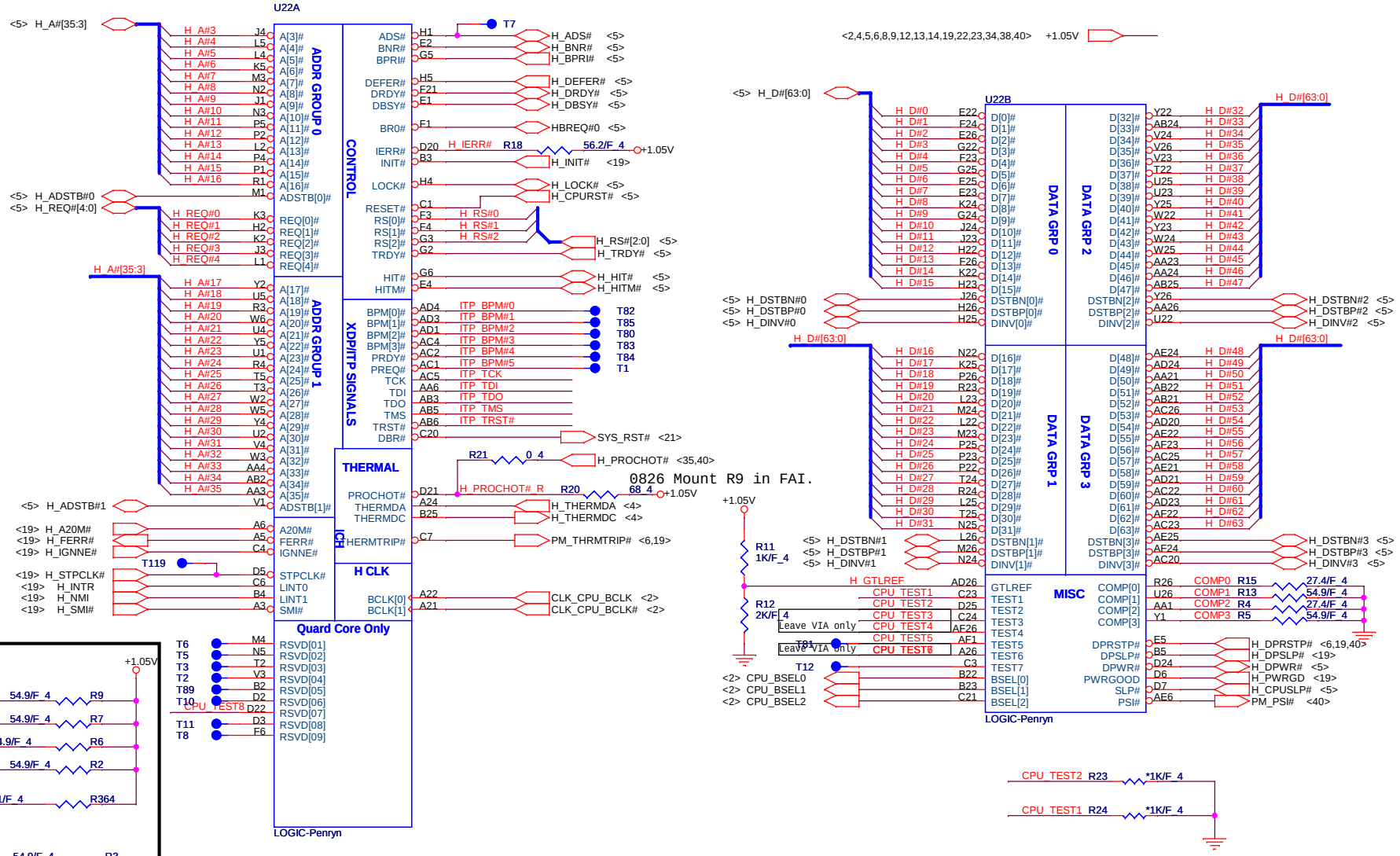

PROJECT : EF7/9A			
Quanta Computer Inc.			
Size: B	Document Number: Penryn 1/2 Host		Rev: 1A
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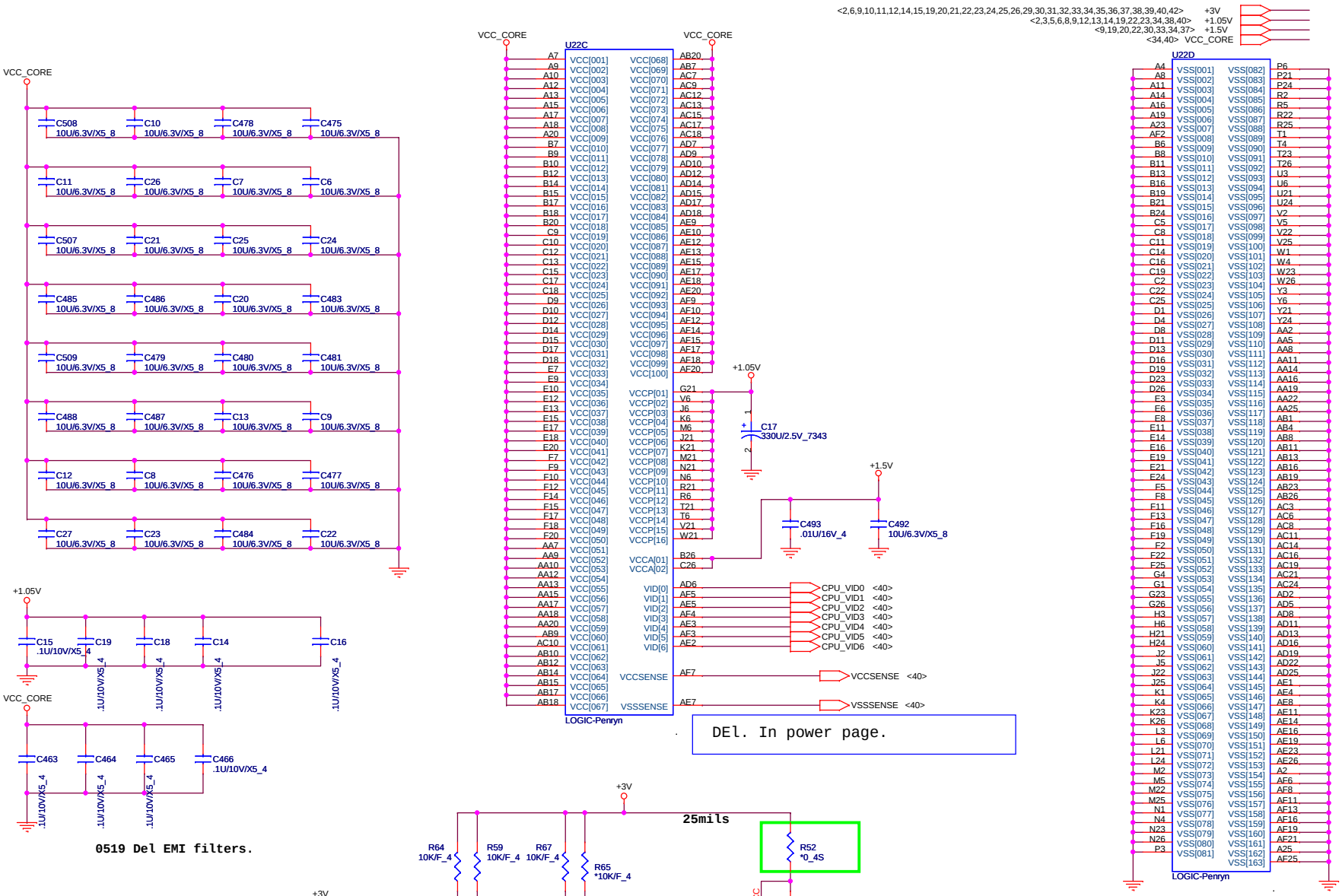
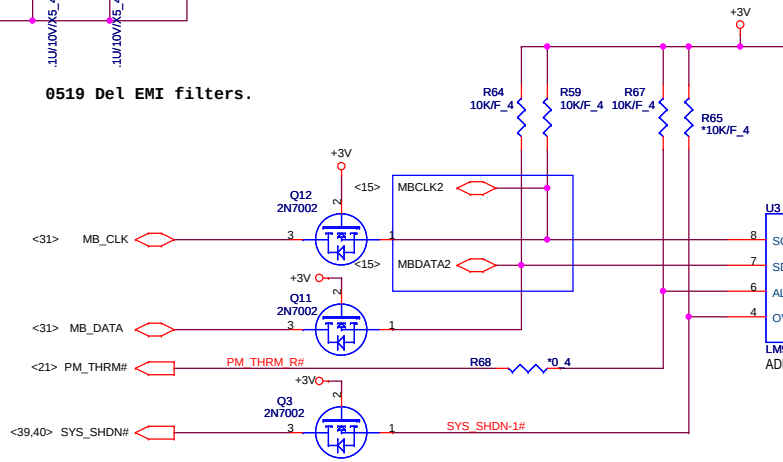


0519 Del EMI filters.

DEl. In power page.



0912 Replace R303 to Short in FAI.

PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn 2/2 Power&Thermal	1A
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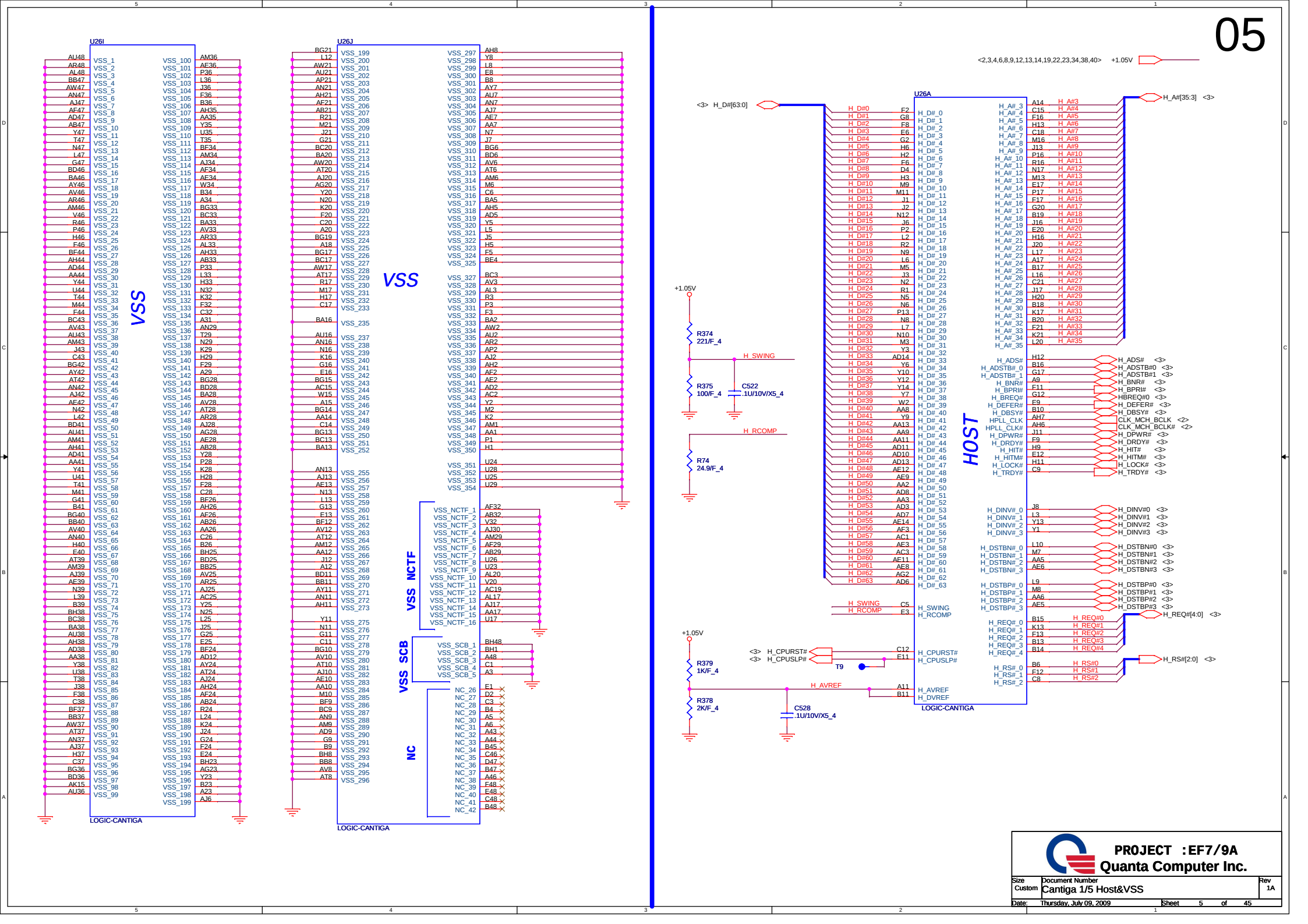
05
U26I
VSS
LOGIC-CANTIGA
U26J
VSS
VSS_NCTF
VSS_SCB
NC
LOGIC-CANTIGA
U26A
HOST
LOGIC-CANTIGA
<3> H_D#[63:0]
H_A#[35:3] <3>
<2,3,4,6,8,9,12,13,14,19,22,23,34,38,40> +1.05V
+1.05V
R374 221/F_4
H_SWING
R375 100/F_4
C522 .1U/10V/X5_4
H_RCOMP
R74 24.9/F_4
R379 1K/F_4
R378 2K/F_4
H_AVREF
C528 .1U/10V/X5_4
T9
H_CPURST#
H_CPUSLP#
H_REQ#[4:0] <3>
H_RS#[2:0] <3>
PROJECT : EF7/9A
Quanta Computer Inc.
Size Custom
Document Number Cantiga 1/5 Host&VSS
Rev 1A
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MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reversed

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

<2,4,9,10,11,12,14,15,19,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
<8,9,10,33,34,36> 1.8VSUS
<2,3,4,5,8,9,12,13,14,19,22,23,34,38,40> +1.05V
<9> +1.05V_PEG

PEG_TX#[15:0] PEG_TX#[15:0] <12>
PEG_TX[15:0] PEG_TX[15:0] <12>
PEG_RX#[15:0] PEG_RX#[15:0] <12>
PEG_RX[15:0] PEG_RX[15:0] <12>

U26B

RSVD: RSVD1 M36, RSVD2 N36, RSVD3 R33, RSVD4 T33, RSVD5 AH9, RSVD6 AH10, RSVD7 AH12, RSVD8 AH13, RSVD9 K12, RSVD14 T24, RSVD15 B31, RSVD16 B2, RSVD17 M1, RSVD20 AY21, RSVD22 BG23, RSVD23 BF23, RSVD24 BH18, RSVD25 BF18

DDR CLK/ CONTROL/COMPENSATION:
SA_CK_0 AP24 M_A_CLK0 <10>
SA_CK_1 AT21 M_A_CLK1 <10>
SB_CK_0 AV24 M_B_CLK0 <10>
SB_CK_1 AU20 M_B_CLK1 <10>
SA_CK#_0 AR24 M_A_CLK0# <10>
SA_CK#_1 AR21 M_A_CLK1# <10>
SB_CK#_0 AU24 M_B_CLK0# <10>
SB_CK#_1 AV20 M_B_CLK1# <10>
SA_CKE_0 BC28 M_A_CKE0 <10,11>
SA_CKE_1 AY28 M_A_CKE1 <10,11>
SB_CKE_0 AY36 M_B_CKE0 <10,11>
SB_CKE_1 BB36 M_B_CKE1 <10,11>
SA_CS#_0 BA17 M_A_CS#0 <10,11>
SA_CS#_1 AY16 M_A_CS#1 <10,11>
SB_CS#_0 AV16 M_B_CS#0 <10,11>
SB_CS#_1 AR13 M_B_CS#1 <10,11>
SA_ODT_0 BD17 M_A_ODT0 <10,11>
SA_ODT_1 AY17 M_A_ODT1 <10,11>
SB_ODT_0 BF15 M_B_ODT0 <10,11>
SB_ODT_1 AY13 M_B_ODT1 <10,11>
1.8VSUS
SM_RCOMP BG22 SM_RCOMP R109 80.6/F_4
SM_RCOMP# BH21 SM_RCOMP# R103 80.6/F_4
SM_RCOMP_VOH BF28 SM_RCOMP_VOH
SM_RCOMP_VOL BH28 SM_RCOMP_VOL
SM_VREF AV42 +0.9VSMVREF_MCH
SM_PWROK AR36 SW_PWROK_NB R142 10K_4
SM_RXT BF17 SM_REXT R93 499/F_4
SM_DRAMRST# BC36 DDR3_DRAMRST# TP10

CLK: DPLL_REF_CLK B38, DPLL_REF_CLK# A38, DPLL_REF_SSCLK E41, DPLL_REF_SSCLK# F41
96MHz (G)MCH (Display PLL Differential Clock)
PEG_CLK F43 CLK_PCIE_3GPLL <2>
PEG_CLK# E43 CLK_PCIE_3GPLL# <2>

ME JTAG: ME_JTAG_TCK T23 AL34, ME_JTAG_TDI T30 AK34, ME_JTAG_TDO T27 AN35, ME_JTAG_TMS T26 AM35

DMI:
DMI_RXN_0 AE41 DMI_TXN0
DMI_RXN_1 AE37 DMI_TXN1
DMI_RXN_2 AE47 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3
DMI_TXN[3:0] <20>
DMI_RXP_0 AE40 DMI_TXP0
DMI_RXP_1 AE38 DMI_TXP1
DMI_RXP_2 AE48 DMI_TXP2
DMI_RXP_3 AH40 DMI_TXP3
DMI_TXP[3:0] <20>
DMI_TXN_0 AE35 DMI_RXN0
DMI_TXN_1 AE43 DMI_RXN1
DMI_TXN_2 AE46 DMI_RXN2
DMI_TXN_3 AH42 DMI_RXN3
DMI_RXN[3:0] <20>
DMI_TXP_0 AD35 DMI_RXP0
DMI_TXP_1 AE44 DMI_RXP1
DMI_TXP_2 AE46 DMI_RXP2
DMI_TXP_3 AH43 DMI_RXP3
DMI_RXP[3:0] <20>

CFG: <2> MCH_BSEL0 T25, <2> MCH_BSEL1 R25, <2> MCH_BSEL2 P25
T15 MCH_CFG_3 P20, T21 MCH_CFG_4 P24, MCH_CFG_5 C25, MCH_CFG_6 N24, MCH_CFG_7 M24, T16 MCH_CFG_8 E21, MCH_CFG_9 C23, MCH_CFG_10 C24, MCH_CFG_11 N21, T20 MCH_CFG_12 P21, MCH_CFG_13 T21, T18 MCH_CFG_14 R20, T17 MCH_CFG_15 M20, MCH_CFG_16 L21, T19 MCH_CFG_17 H21, T24 MCH_CFG_18 P29, MCH_CFG_19 R28, MCH_CFG_20 T28
R386 *2.2K_4, R114 *2.2K_4, R115 *2.2K_4, R384 *2.2K_4, R385 *2.2K_4, R107 *2.2K_4, R106 *2.2K_4, R116 *2.2K_4, R118 *2.2K_4, R123 *2.2K_4, +3V
CFG_0 … CFG_20

PM: <21> PM_SYNC# R29 PM_SYNC#, <3,19,40> H_DPRSTP# B7 PM_DPRSTP#, <10,11> PM_EXTTS#0 N33 PM_EXT_TS#_0, <11> PM_EXTTS#1 P32 PM_EXT_TS#_1, <21,40> DELAY_VR_PWRGOOD AT40 PWROK, <20> PLT_RST-R# R89 100_4 RST_IN#_MCH AT11 RSTIN#, <3,19> PM_THRMTRIP# PM_THRMTRIP#_R T20 THERMTRIP#, <21,40> DPRSLPVR R96 *0_4 R32 DPRSLPVR

GRAPHICS VID:
GFX_VID_0 B33 GFXVR_VID_0 T103
GFX_VID_1 B32 GFXVR_VID_1 T101
GFX_VID_2 G33 GFXVR_VID_2 T29
GFX_VID_3 F33 GFXVR_VID_3 T28
GFX_VID_4 E33 GFXVR_VID_4 T25
GFX_VR_EN C34 GFXVR_EN T102

ME:
CL_CLK AH37 CL_CLK0 <21>
CL_DATA AH36 CL_DATA0 <21>
CL_PWROK AN36 ECPWROK <21,31>
CL_RST# AJ35 CL_RST#0 <21>
CL_VREF AH34 MCH_CLVREF
0.35 V
+1.05V
R126 1K/F_4
R133 499/F_4
C273 .1U/10V/X5_4

MISC:
DDPC_CTRLCLK N28 DDPC_CTRLCLK T22
DDPC_CTRLDATA N28 R124 *4.7K_4 +3V
SDVO_CTRLCLK G36 R130 *4.7K_4
SDVO_CTRLDATA E36 R131 *4.7K_4
CLKREQ# K36
ICH_SYNC# H36 CLK_MCH_OE# <2> MCH_ICH_SYNC# <21>
+1.05V
TSATN# B12 MCH_TSATN R380 56.2/F_4

HDA: HDA_BCLK B28 T97, HDA_RST# B30 T98, HDA_SDI B29 T99, HDA_SDO C29 T100, HDA_SYNC A28 T96
C-TEST

+3V
R134 10K_4 PM_EXTTS#0
R135 10K_4 PM_EXTTS#1

NC: NC_1 BG48 … NC_26 A47
LOGIC-CANTIGA

U26C

LVDS:
L_BKLT_CTRL L32, L_BKLT_EN G32, L_CTRL_CLK M32
L_CTRL_DATA M33, L_DDC_CLK K33, L_DDC_DATA J33
L_VDD_EN M29, LVDS_IBG C44, LVDS_VBG B43, LVDS_VREFH E37, LVDS_VREFL E38, LVDSA_CLK# C41, LVDSA_CLK C40, LVDSB_CLK# B37, LVDSB_CLK A37
LVDSA_DATA#_0 H47, LVDSA_DATA#_1 E46, LVDSA_DATA#_2 G40, LVDSA_DATA#_3 A40
LVDSA_DATA_0 H48, LVDSA_DATA_1 D45, LVDSA_DATA_2 F40, LVDSA_DATA_3 B40
LVDSB_DATA#_0 A41, LVDSB_DATA#_1 H38, LVDSB_DATA#_2 G37, LVDSB_DATA#_3 J37
LVDSB_DATA_0 B42, LVDSB_DATA_1 G38, LVDSB_DATA_2 F37, LVDSB_DATA_3 K37

TV:
TV_COMP1 F25, TV_Y/G1 H25, TV_C/R1 K25
TVA_DAC, TVB_DAC, TVC_DAC
TV_RTN H24
TV_DCONSEL0 C31, TV_DCONSEL1 E32
TP6, TP7
TV_DCONSEL_0, TV_DCONSEL_1

VGA:
INT_CRT_BLU E28, INT_CRT_GRN G28, INT_CRT_RED J28, G29
CRT_BLUE, CRT_GREEN, CRT_RED, CRT_IRTN
CRT_DDC_CLK H32, CRT_DDC_DATA J32, HSYNC_INT J29, CRTIREF E29, VSYNC_INT L29
TP9, TP4, TP5, TP8
CRT_HSYNC, CRT_TVO_IREF, CRT_VSYNC

LOGIC-CANTIGA

PCI-EXPRESS GRAPHICS:
PEG_COMPI T37, PEG_COMPO T36, PEG_COMP, R136 49.9/F_4, +1.05V_PEG
PEG_RX#_0 H44 PEG_RX#0, PEG_RX#_1 J46 PEG_RX#1, PEG_RX#_2 L44 PEG_RX#2, PEG_RX#_3 L40 PEG_RX#3, PEG_RX#_4 N41 PEG_RX#4, PEG_RX#_5 P48 PEG_RX#5, PEG_RX#_6 N44 PEG_RX#6, PEG_RX#_7 T43 PEG_RX#7, PEG_RX#_8 U43 PEG_RX#8, PEG_RX#_9 Y43 PEG_RX#9, PEG_RX#_10 Y48 PEG_RX#10, PEG_RX#_11 Y36 PEG_RX#11, PEG_RX#_12 AA43 PEG_RX#12, PEG_RX#_13 AD37 PEG_RX#13, PEG_RX#_14 AC47 PEG_RX#14, PEG_RX#_15 AD39 PEG_RX#15
PEG_RX_0 H43 PEG_RX0, PEG_RX_1 J44 PEG_RX1, PEG_RX_2 L43 PEG_RX2, PEG_RX_3 L41 PEG_RX3, PEG_RX_4 N40 PEG_RX4, PEG_RX_5 P47 PEG_RX5, PEG_RX_6 N43 PEG_RX6, PEG_RX_7 T42 PEG_RX7, PEG_RX_8 U42 PEG_RX8, PEG_RX_9 Y42 PEG_RX9, PEG_RX_10 W47 PEG_RX10, PEG_RX_11 Y37 PEG_RX11, PEG_RX_12 AA42 PEG_RX12, PEG_RX_13 AD36 PEG_RX13, PEG_RX_14 AC48 PEG_RX14, PEG_RX_15 AD40 PEG_RX15
PEG_TX#_0 J41 C_PEG_TX#0 C555, PEG_TX#_1 M46 C_PEG_TX#1 C601, PEG_TX#_2 M47 C_PEG_TX#2 C605, PEG_TX#_3 M40 C_PEG_TX#3 C561, PEG_TX#_4 M42 C_PEG_TX#4 C567, PEG_TX#_5 R48 C_PEG_TX#5 C606, PEG_TX#_6 N38 C_PEG_TX#6 C565, PEG_TX#_7 T40 C_PEG_TX#7 C576, PEG_TX#_8 U37 C_PEG_TX#8 C577, PEG_TX#_9 U40 C_PEG_TX#9 C582, PEG_TX#_10 Y40 C_PEG_TX#10 C584, PEG_TX#_11 AA46 C_PEG_TX#11 C594, PEG_TX#_12 AA37 C_PEG_TX#12 C592, PEG_TX#_13 AA40 C_PEG_TX#13 C597, PEG_TX#_14 AD43 C_PEG_TX#14 C609, PEG_TX#_15 AC46 C_PEG_TX#15 C611
PEG_TX_0 J42 C_PEG_TX0 C554, PEG_TX_1 L46 C_PEG_TX1 C599, PEG_TX_2 M48 C_PEG_TX2 C604, PEG_TX_3 M39 C_PEG_TX3 C558, PEG_TX_4 M43 C_PEG_TX4 C563, PEG_TX_5 R47 C_PEG_TX5 C607, PEG_TX_6 N37 C_PEG_TX6 C569, PEG_TX_7 T39 C_PEG_TX7 C571, PEG_TX_8 U36 C_PEG_TX8 C573, PEG_TX_9 U39 C_PEG_TX9 C579, PEG_TX_10 Y39 C_PEG_TX10 C583, PEG_TX_11 Y46 C_PEG_TX11 C591, PEG_TX_12 AA36 C_PEG_TX12 C585, PEG_TX_13 AA39 C_PEG_TX13 C596, PEG_TX_14 AD42 C_PEG_TX14 C608, PEG_TX_15 AD46 C_PEG_TX15 C610
0.1U/10V/X5R_4 PEG_TX#0 … PEG_TX#15
0.1U/10V/X5R_4 PEG_TX0 … PEG_TX15

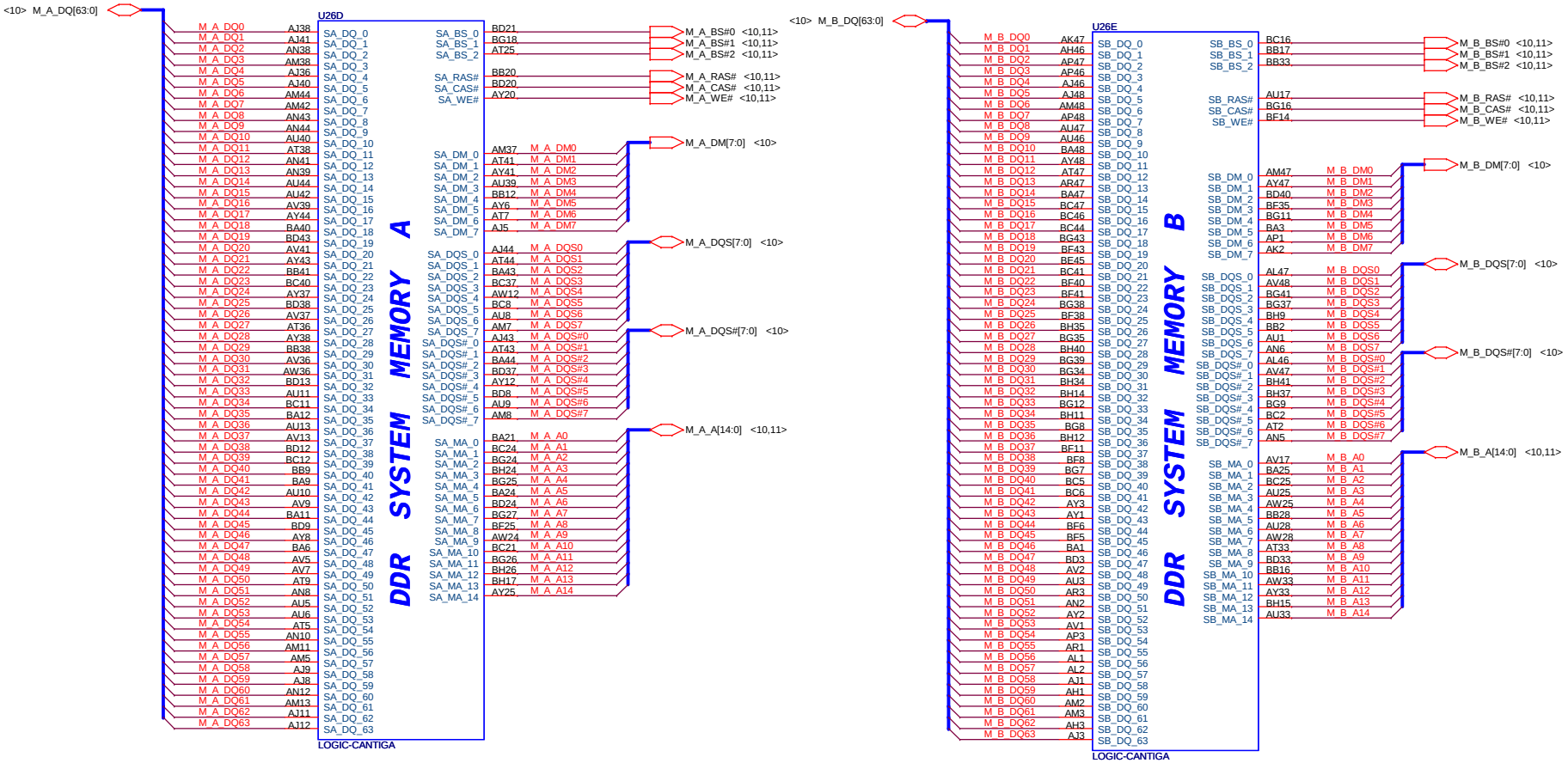
1.8VSUS
R155 *1K/F_4
R156 0_4 +0.9VSMVREF <10,36>
R152 *1K/F_4
+0.9VSMVREF_MCH
C292 .1U/10V/X5_4
C291 470P/50V_4

1.8VSUS
R132 1K/F_4
SM_RCOMP_VOH
C259 .01U/16V_4
C266 2.2U/6.3V/X5_6
R137 3.01K/F_4
SM_RCOMP_VOL
C260 .01U/16V_4
C268 2.2U/6.3V/X5_6
R138 1K/F_4

PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga 2/5 DMI/DISP	1A

Date: Thursday, July 09, 2009 Sheet 6 of 45



PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga 3/5 DDR2	1A
Date: Thursday, July 09, 2009	Sheet 7 of 45	

<6,9,10,33,34,36> 1.8VSUS
<2,3,4,5,6,9,12,13,14,19,22,23,34,38,40> +1.05V

1.8VSUS

U26G

VCC_SM 3000mA

VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desgins.

C743 *.1U/10V/X5_4
C746 *.1U/10V/X5_4
C748 *.1U/10V/X5_4
VCC_SM_VIA0
VCC_SM_VIA1
VCC_SM_VIA2
VCC_SM_VIA3
Keep VIA

VCC SM POWER

VCC GFX NCTF

VCC GFX

VCC SM LF

+1.05V

R92 10_4
R90 10_4
VCC_AXG_SENSE
VSS_AXG_SENSE

LOGIC-CANTIGA

Ivcc=1930.4+508.12=2438.52mA

C519 *330u_2.5V_7343
C92 10U/6.3V/X5_8
C621 10U/6.3V/X5_8
C180 .33U/10V_4
C211 .33U/10V_4
C186 .1U/10V/X5_4

C255 10U/6.3V/X5_8
C270 10U/6.3V/X5_8
C269 10U/6.3V/X5_8
C256 10U/6.3V/X5_8
C258 .1U/10V/X5_4
C194 .1U/10V/X5_4
C230 .1U/10V/X5_4

0505 EMI Added

U26F

VCC CORE POWER

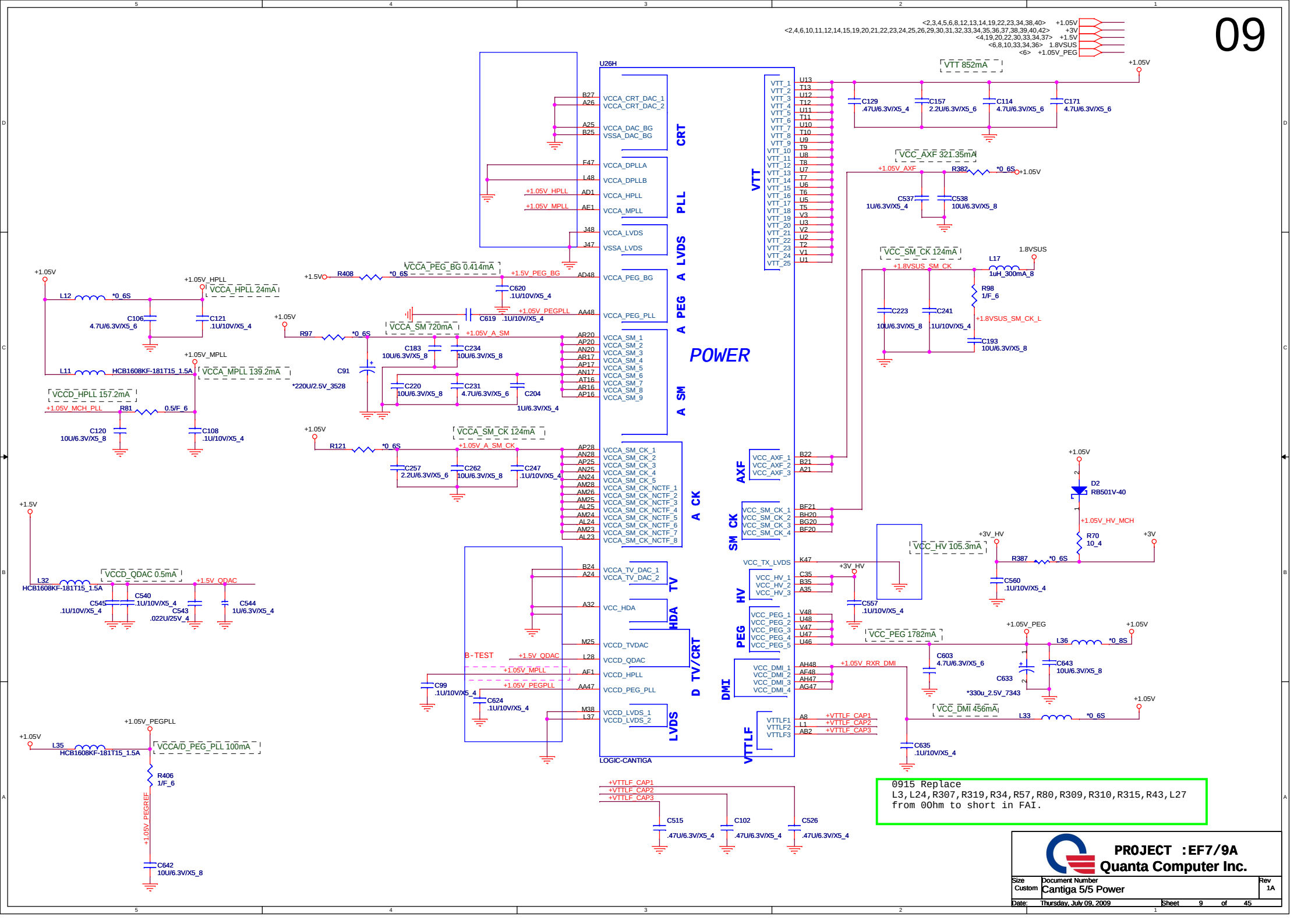
VCC NCTF

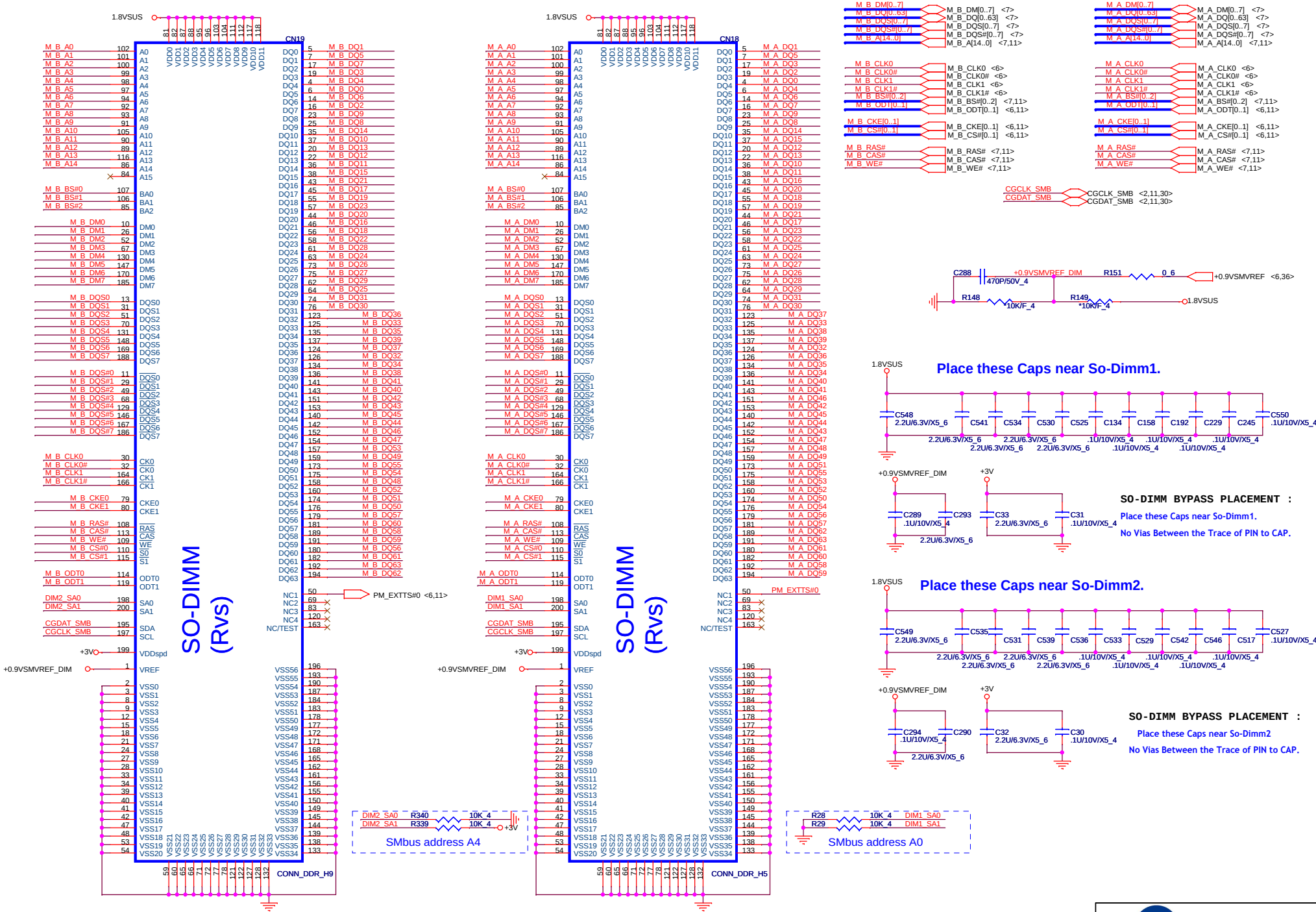
LOGIC-CANTIGA

C178 .1U/10V/X5_4
C141 .1U/10V/X5_4
C103 .33U/10V_4
C232 .33U/10V_4
C279 .47U/6.3V/X5_4
C281 1U/6.3V/X5_4
C280 1U/6.3V/X5_4

Size: Custom	Document Number: Cantiga 4/5 VCC	Rev: 1A
Date: Thursday, July 09, 2009	Sheet 8 of 45	

PROJECT :EF7/9A
Quanta Computer Inc.


POWER
U26H
LOGIC-CANTIGA
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT 852mA
VCC_AXF 321.35mA
VCC_SM_CK 124mA
VCC_HV 105.3mA
VCC_PEG 1782mA
VCC_DMI 456mA
VCCA_PEG_BG 0.414mA
VCCA_SM 720mA
VCCA_SM_CK 124mA
VCCA_HPLL 24mA
VCCA_MPLL 139.2mA
VCCD_HPLL 157.2mA
VCCD_QDAC 0.5mA
VCCA/D_PEG_PLL 100mA
B-TEST
0915 Replace
L3,L24,R307,R319,R34,R57,R80,R309,R310,R315,R43,L27
from 0Ohm to short in FAI.
PROJECT :EF7/9A
Quanta Computer Inc.
Cantiga 5/5 Power
Thursday, July 09, 2009
Sheet 9 of 45


1.8VSUS
CN19
SO-DIMM (Rvs)
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_A14
M_B_A15
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
M_B_DQS0#
M_B_DQS1#
M_B_DQS2#
M_B_DQS3#
M_B_DQS4#
M_B_DQS5#
M_B_DQS6#
M_B_DQS7#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_CKE0
M_B_CKE1
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CS#0
M_B_CS#1
M_B_ODT0
M_B_ODT1
DIM2_SA0
DIM2_SA1
CGDAT_SMB
CGCLK_SMB
+3V
+0.9VSMVREF_DIM
M_B_DQ0
M_B_DQ1
M_B_DQ2
M_B_DQ3
M_B_DQ4
M_B_DQ5
M_B_DQ6
M_B_DQ7
M_B_DQ8
M_B_DQ9
M_B_DQ10
M_B_DQ11
M_B_DQ12
M_B_DQ13
M_B_DQ14
M_B_DQ15
M_B_DQ16
M_B_DQ17
M_B_DQ18
M_B_DQ19
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M_B_DQ57
M_B_DQ58
M_B_DQ59
M_B_DQ60
M_B_DQ61
M_B_DQ62
M_B_DQ63
PM_EXTTS#0 <6,11>
NC/TEST
CONN_DDR_H9
H 9.2
DIM2_SA0 R340 10K_4
DIM2_SA1 R339 10K_4 +3V
SMbus address A4
CN18
SO-DIMM (Rvs)
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_A14
M_A_A15
M_A_BS#0
M_A_BS#1
M_A_BS#2
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7
M_A_DQS0#
M_A_DQS1#
M_A_DQS2#
M_A_DQS3#
M_A_DQS4#
M_A_DQS5#
M_A_DQS6#
M_A_DQS7#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_CKE0
M_A_CKE1
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CS#0
M_A_CS#1
M_A_ODT0
M_A_ODT1
DIM1_SA0
DIM1_SA1
CGDAT_SMB
CGCLK_SMB
+3V
+0.9VSMVREF_DIM
M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
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M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63
PM_EXTTS#0
NC/TEST
CONN_DDR_H5
H 5.2
R28 10K_4 DIM1_SA0
R29 10K_4 DIM1_SA1
SMbus address A0
M_B_DM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[14..0]
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_A_DM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_DQS#[0..7]
M_A_A[14..0]
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#
CGCLK_SMB
CGDAT_SMB
C288 470P/50V_4
+0.9VSMVREF_DIM
R151 0_6
+0.9VSMVREF <6,36>
R148 10K/F_4
R149 *10K/F_4
1.8VSUS
Place these Caps near So-Dimm1.
C548 2.2U/6.3V/X5_6
C541 2.2U/6.3V/X5_6
C534 2.2U/6.3V/X5_6
C530 2.2U/6.3V/X5_6
C525 .1U/10V/X5_4
C134 .1U/10V/X5_4
C158 .1U/10V/X5_4
C192 .1U/10V/X5_4
C229 .1U/10V/X5_4
C245 .1U/10V/X5_4
C550 .1U/10V/X5_4
C289 .1U/10V/X5_4
C293 2.2U/6.3V/X5_6
C33 2.2U/6.3V/X5_6
C31 .1U/10V/X5_4
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
C549 2.2U/6.3V/X5_6
C535 2.2U/6.3V/X5_6
C531 2.2U/6.3V/X5_6
C539 2.2U/6.3V/X5_6
C536 .1U/10V/X5_4
C533 .1U/10V/X5_4
C529 .1U/10V/X5_4
C542 .1U/10V/X5_4
C546 .1U/10V/X5_4
C517 .1U/10V/X5_4
C527 .1U/10V/X5_4
C294 .1U/10V/X5_4
C290 2.2U/6.3V/X5_6
C32 2.2U/6.3V/X5_6
C30 .1U/10V/X5_4
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.
<6,8,9,33,34,36> 1.8VSUS
<2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
PROJECT :EF7/9A
Quanta Computer Inc.
Size Custom
Document Number DDR2 1/2 DIMM
Rev 1A
Date: Thursday, July 09, 2009
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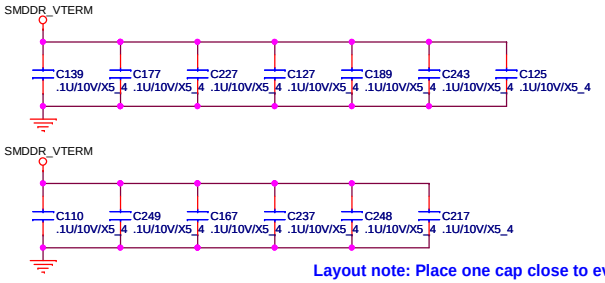
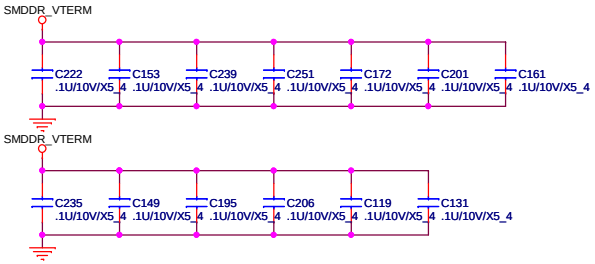
<33,34,36> SMDDR_VTERM
<2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V

DDRII DUAL CHANNEL A,B.

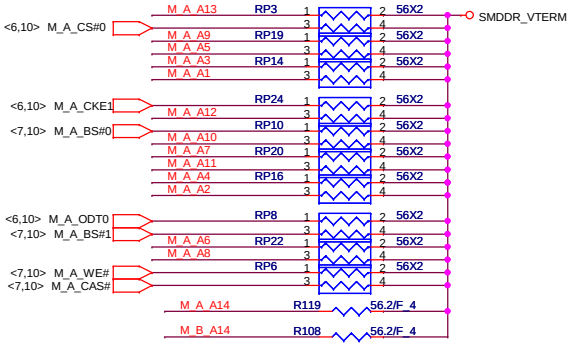
DDRII A CHANNEL

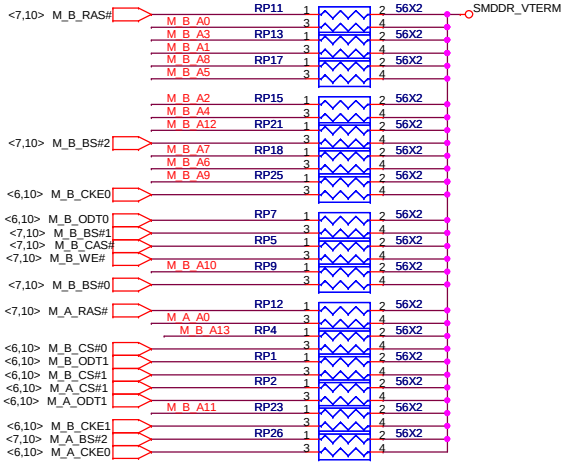


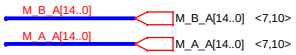
DDRII B CHANNEL

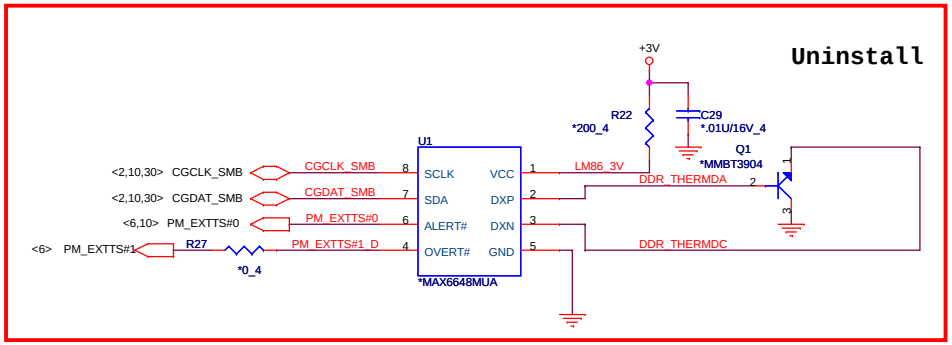


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM









PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 2/2 termination	1A

Date: Thursday, July 09, 2009 Sheet 11 of 45

<2,3,4,5,6,8,9,13,14,19,22,23,34,38,40> +1.05V
<2,4,6,9,10,11,14,15,19,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

+1.05V
~ 500mA (1.05 +/- 5%)
C169 22U_8 | C152 10U/6.3V_6S | C203 4.7U/6.3V_6 | C185 1U/6.3V_4 | C136 1U/6.3V_4 | C277 .1U/10V_4 | C202 .1U/10V_4

+1.05V
1600mA(1.05 +/- 5%)
C570 22U_8 | C275 10U/6.3V_6S | C111 4.7U/6.3V_6 | C274 1U/6.3V_4 | C187 1U/6.3V_4 | C150 .1U/10V_4 | C144 .1U/10V_4

Near BGA

03/31 nVidia review
+3V
C98 4.7U/6.3V_6 | C88 1U/6.3V_4 | C72 .1U/10V_4 | C89 .1U/10V_4

<42> GPU_VDD_SENSE — GPU_VDD_SENSE

+1.05V
L10 10nH_6 +PEX_PLLVDD
110mA(1.05 +/- 5%)
12~16 mils width
C506 1U/6.3V_4 | C514 1U/6.3V_4 | C132 4.7U/6.3V_6 | C116 1U/6.3V_4 | C117 1U/6.3V_4 | C118 .1U/10V_4

+3V L6 0_6 +PEX_SVDD_3V3
C81 4.7U/6.3V_6 | C170 .1U/10V_4 | C154 .01U/16V_4

U25A
BGA969-NVIDIA-N89P-GS
COMMON

PCI EXPRESS

AK16	PEX_IOVDD_1	PEX_RX0	AP17
AK17	PEX_IOVDD_2	PEX_RX0*	AN17
AK21	PEX_IOVDD_3	PEX_RX1	AN19
AK24	PEX_IOVDD_4	PEX_RX1*	AP19
AK27	PEX_IOVDD_5	PEX_RX2	AR19
		PEX_RX2*	AR20
AG11	PEX_IOVDDQ_1	PEX_RX3	AP20
AG12	PEX_IOVDDQ_2	PEX_RX3*	AN20
AG13	PEX_IOVDDQ_3	PEX_RX4	AN22
AG15	PEX_IOVDDQ_4	PEX_RX4*	AP22
AG16	PEX_IOVDDQ_5	PEX_RX5	AR22
AG17	PEX_IOVDDQ_6	PEX_RX5*	AR23
AG18	PEX_IOVDDQ_7	PEX_RX6	AP23
AG22	PEX_IOVDDQ_8	PEX_RX6*	AN23
AG23	PEX_IOVDDQ_9	PEX_RX7	AN25
AG24	PEX_IOVDDQ_10	PEX_RX7*	AP25
AG25	PEX_IOVDDQ_11	PEX_RX8	AR25
AG26	PEX_IOVDDQ_12	PEX_RX8*	AR26
AJ14	PEX_IOVDDQ_13	PEX_RX9	AP26
AJ15	PEX_IOVDDQ_14	PEX_RX9*	AN26
AJ19	PEX_IOVDDQ_15	PEX_RX10	AN28
AJ21	PEX_IOVDDQ_16	PEX_RX10*	AP28
AJ22	PEX_IOVDDQ_17	PEX_RX11	AR28
AJ24	PEX_IOVDDQ_18	PEX_RX11*	AR29
AJ25	PEX_IOVDDQ_19	PEX_RX12	AP29
AJ27	PEX_IOVDDQ_20	PEX_RX12*	AN29
AK18	PEX_IOVDDQ_21	PEX_RX13	AN31
AK20	PEX_IOVDDQ_22	PEX_RX13*	AP31
AK23	PEX_IOVDDQ_23	PEX_RX14	AR31
AK26	PEX_IOVDDQ_24	PEX_RX14*	AR32
AL16	PEX_IOVDDQ_25	PEX_RX15	AR34
		PEX_RX15*	AP34

PEG_TX0 <6> … PEG_TX#15 <6>

J10	VDD33_1	PEX_TX0	AL17	C_PEG_RX0 C133 .1U/10V_4
J11	VDD33_2	PEX_TX0*	AM17	C_PEG_RX#0 C123 .1U/10V_4
J12	VDD33_3	PEX_TX1	AM18	C_PEG_RX1 C135 .1U/10V_4
J13	VDD33_4	PEX_TX1*	AM19	C_PEG_RX#1 C143 .1U/10V_4
J9	VDD33_5	PEX_TX2	AL19	C_PEG_RX2 C145 .1U/10V_4
		PEX_TX2*	AK19	C_PEG_RX#2 C155 .1U/10V_4
AD20	VDD_SENSE	PEX_TX3	AL20	C_PEG_RX3 C151 .1U/10V_4
D35	NC_9/ VDD_SENSE	PEX_TX3*	AM20	C_PEG_RX#3 C162 .1U/10V_4
P7	NC_16/ VDD_SENSE	PEX_TX4	AM21	C_PEG_RX4 C168 .1U/10V_4
		PEX_TX4*	AM22	C_PEG_RX#4 C174 .1U/10V_4
AD19	GND_SENSE	PEX_TX5	AL22	C_PEG_RX5 C190 .1U/10V_4
E35	NC_10/ GND_SENSE	PEX_TX5*	AK22	C_PEG_RX#5 C198 .1U/10V_4
R7	NC_17/ GND_SENSE	PEX_TX6	AL23	C_PEG_RX6 C175 .1U/10V_4
		PEX_TX6*	AM23	C_PEG_RX#6 C191 .1U/10V_4
AG14	PEX_PLLVDD	PEX_TX7	AM24	C_PEG_RX7 C200 .1U/10V_4
		PEX_TX7*	AM25	C_PEG_RX#7 C212 .1U/10V_4
AG19	PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3	PEX_TX8	AL25	C_PEG_RX8 C205 .1U/10V_4
F7	NC_12/ PEX_SVDD_3V3	PEX_TX8*	AK25	C_PEG_RX#8 C218 .1U/10V_4
		PEX_TX9	AL26	C_PEG_RX9 C221 .1U/10V_4
AG20	PEX_CAL_PU_GND/ NC	PEX_TX9*	AM26	C_PEG_RX#9 C226 .1U/10V_4
A2	NC_1	PEX_TX10	AM27	C_PEG_RX10 C228 .1U/10V_4
AB7	NC_2	PEX_TX10*	AM28	C_PEG_RX#10 C236 .1U/10V_4
AD6	NC_3	PEX_TX11	AL28	C_PEG_RX11 C240 .1U/10V_4
AF6	NC_4	PEX_TX11*	AK28	C_PEG_RX#11 C244 .1U/10V_4
AG6	NC_5	PEX_TX12	AL29	C_PEG_RX12 C253 .1U/10V_4
AJ5	NC_6	PEX_TX12*	AL29	C_PEG_RX#12 C250 .1U/10V_4
AK15	NC_7	PEX_TX13	AM29	C_PEG_RX13 C242 .1U/10V_4
AL7	NC_8	PEX_TX13*	AM30	C_PEG_RX#13 C246 .1U/10V_4
E7	NC_11	PEX_TX14	AM31	C_PEG_RX14 C254 .1U/10V_4
H32	NC_13	PEX_TX14*	AM32	C_PEG_RX#14 C263 .1U/10V_4
M7	NC_14	PEX_TX15	AN32	C_PEG_RX15 C264 .1U/10V_4
P6	NC_15	PEX_TX15*	AP32	C_PEG_RX#15 C267 .1U/10V_4
U7	NC_18			
V6	NC_19			

PEG_RX0 <6> … PEG_RX#15 <6>

PEX_REFCLK	AR16	CLK_PCIE_VGA
PEX_REFCLK*	AR17	CLK_PCIE_VGA#

CLK_PCIE_VGA <2> / CLK_PCIE_VGA# <2>

PEX_TSTCLK_OUT / PEX_TSTCLK_OUT* — AJ17 PEX_TSTCLK, AJ18 PEX_TSTCLK# — R83 *200_4

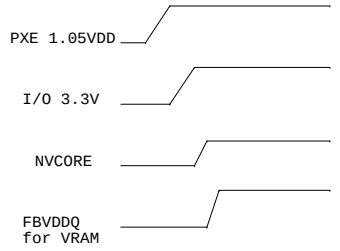
PEX_RST* — AM16 VGA_RST# — R368 0_4 — PLTRST# <20,25,30>

PEX_CLKREQ* — AR13 PEX_CLKREQ# — R369 10K/F_4 — +3V

PEX_TERMP — AG21 PEX_TERMP — R69 2.49K/F_4

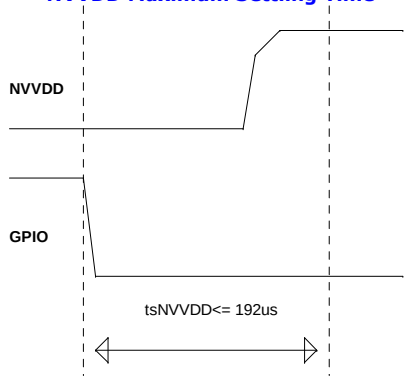
TESTMODE — AP35 TESTMODE — R120 10K/F_4

power up sequence

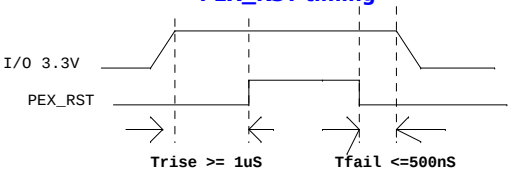


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



VGA Thermal Circuit

+3V
R43 *2.2K_4
I2C ADDRESS: 0x98H

U2 *MAX6649

<15,24> EDIDDATA — EDIDDATA — R31 *0_4 — GFX_SDA — SDAT
<15,24> EDIDCLK — EDIDCLK — R30 *0_4 — GFX_SCL — SCLK

+3V R37 *200_4 MAX6649_V — VCC
C34 *.1U/10V_4 — GND

OVT — MAX6649_O# — R39 *0_4 — VGA_OVT# — VGA_OVT# <15>
ALERT — MAX6649_A# — R40 *0_4 — ALERT — ALERT <15>
DXP — GFX_THMD+ — GFX_THMD+ <15>
DXN — C43 *2200P/50V_4 — GFX_THMD- — GFX_THMD- <15>

THERMAL TRACE CONSTRAINTS
Use 10MIL Guard(GND) Trace around THERMDC and THERMDA
10/10/10
11/19

+1.05V
C532 .1U/10V_4 | C551 .1U/10V_4 | C523 .1U/10V_4 | C122 .1U/10V_4 | C547 .1U/10V_4

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Quanta Computer Inc.

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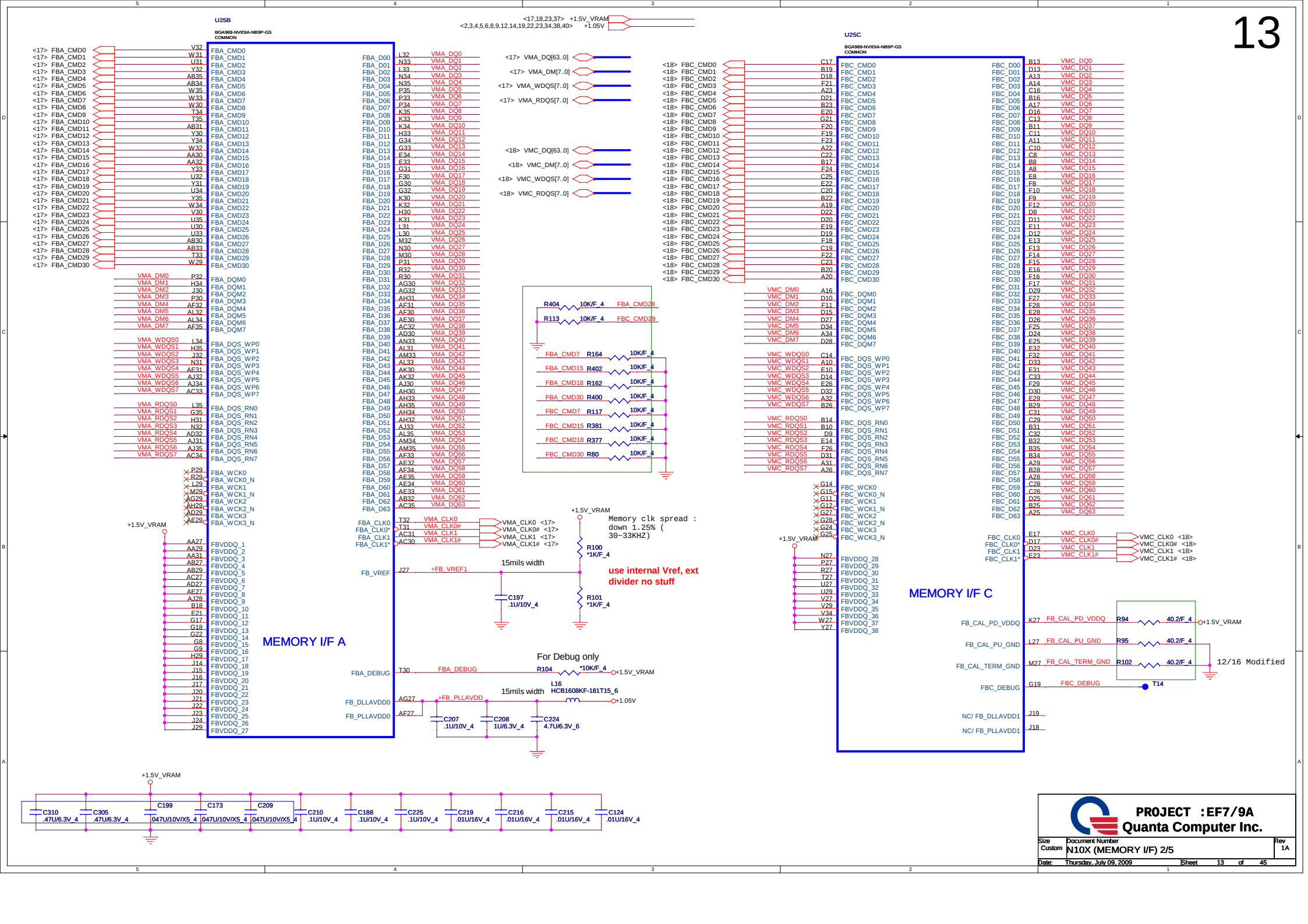

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U25D
BGA969-NVIDIA-NB9P-GS
COMMON

<2,4,6,9,10,11,12,15,19,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42>
<2,3,4,5,6,8,9,12,13,19,22,23,34,38,40>
+3V
+1.05V

LVDS clk spread : Center
+/-0.5% (30~33KHZ)

IFPAB(LVDS)

+1.05V — L30 FCM2012VF_8 — C634 near the GPU — +IFPAB_PLLVDD — 200 mA — AK9
C511 4.7U/6.3V_6, C513 4700P/25V_4, C518 1U/6.3V_4, C516 .1U/10V_4, C84 .1U/10V_4
R51 *1K/F_4 IFPAB_RSET — AJ11

+1.8V — L4 FBMA-10-160808-300T_6 — +IFPAB_IOVDD — 200 mA — AG9, AG10
C45 4.7U/6.3V_6, C47 1U/6.3V_4, C46 .1U/10V_4, C96 4700P/25V_4

IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD

IFPA_TXC	AM11	EXT_TXLCLKOUT+ <24>
IFPA_TXC*	AM12	EXT_TXLCLKOUT- <24>
IFPA_TXD0	AM8	EXT_TXLOUT0+ <24>
IFPA_TXD0*	AL8	EXT_TXLOUT0- <24>
IFPA_TXD1	AM10	EXT_TXLOUT1+ <24>
IFPA_TXD1*	AM9	EXT_TXLOUT1- <24>
IFPA_TXD2	AK10	EXT_TXLOUT2+ <24>
IFPA_TXD2*	AL10	EXT_TXLOUT2- <24>
IFPA_TXD3	AK11	
IFPA_TXD3*	AL11	
IFPB_TXC	AP13	EXT_TXUCLKOUT+ <24>
IFPB_TXC*	AN13	EXT_TXUCLKOUT- <24>
IFPB_TXD4	AN8	EXT_TXUOUT0+ <24>
IFPB_TXD4*	AP8	EXT_TXUOUT0- <24>
IFPB_TXD5	AP10	EXT_TXUOUT1+ <24>
IFPB_TXD5*	AN10	EXT_TXUOUT1- <24>
IFPB_TXD6	AR11	EXT_TXUOUT2+ <24>
IFPB_TXD6*	AR10	EXT_TXUOUT2- <24>
IFPB_TXD7	AN11	
IFPB_TXD7*	AP11	

IFPCD

+3V — L5 FBMA-10-160808-300T_6 — +IFPCD_PLLVDD — 120 mA — AJ9, AC6
C61 4.7U/6.3V_6, C66 2.2U/6.3V_6, C56 1U/6.3V_4, C60 1U/10V_4, C62 1U/10V_4, C74 1U/10V_4
R354 1K/F_4 IFPCD_RSET — AK7
R63 1K/F_4 — AB6

IFPCD_PLLVDD/ IFPC_PLLVDD
DACB_VDD/ IFPD_PLLVDD
IFPCD_RSET/ IFPC_RSET
DACB_RSET/ IFPD_RSET

IFPC

I2CW_SDA/ IFPC_AUX_N	AN3	HDMI_SDA <23>
I2CW_SCL/ IFPC_AUX	AP2	HDMI_SCL <23>
IFPC_L3_N	AR2	N_TXC_HDMI- — N_TXC_HDMI- <23>
IFPC_L3	AP1	N_TXC_HDMI+ — N_TXC_HDMI+ <23>
IFPC_L2_N	AM4	N_TX0_HDMI- — N_TX0_HDMI- <23>
IFPC_L2	AM3	N_TX0_HDMI+ — N_TX0_HDMI+ <23>
IFPC_L1_N	AM5	N_TX1_HDMI- — N_TX1_HDMI- <23>
IFPC_L1	AL5	N_TX1_HDMI+ — N_TX1_HDMI+ <23>
IFPC_L0_N	AM6	N_TX2_HDMI- — N_TX2_HDMI- <23>
IFPC_L0	AM7	N_TX2_HDMI+ — N_TX2_HDMI+ <23>

IFPD

I2CX_SDA/ IFPD_AUX_N	AN4	
I2CX_SCL/ IFPD_AUX	AP4	
IFPD_L3_N	AR4	
IFPD_L3	AR5	
IFPD_L2_N	AP5	
IFPD_L2	AN5	
IFPD_L1_N	AN7	
IFPD_L1	AP7	
IFPD_L0_N	AR7	
IFPD_L0	AR8	

TMDS channel two

+1.05V — L28 MLB-201209-0030P-N1-RU_8 — +IFPCD_IOVDD — 500 mA (1.05V +/- 3%) — AJ8, AK8
C495 4.7U/6.3V_6, C502 *2.2U/6.3V_6, C505 1U/6.3V_4, C500 .1U/10V_4, C65 .1U/10V_4

IFPC_IOVDD
IFPD_IOVDD

IFPEF

IFPEF_PLLVDD — AJ6
R62 10K/F_4 — AL1
IFPEF_RSET
IFPEF_IOVDD — AE7
R66 10K/F_4 — AD7
IFPE_IOVDD
IFPF_IOVDD

I2CY_SCL/ IFPE_AUX	AE4	
I2CY_SDA/ IFPE_AUX*	AD4	
IFPE_L0	AH6	
IFPE_L0*	AH5	
IFPE_L1	AH4	
IFPE_L1*	AG4	
IFPE_L2	AF4	
IFPE_L2*	AF5	
IFPE_L3	AE6	
IFPE_L3*	AE5	
I2CZ_SCL/ IFPF_AUX	AF3	
I2CZ_SDA/ IFPF_AUX*	AF2	
IFPF_L0	AL2	
IFPF_L0*	AL3	
IFPF_L1	AJ3	
IFPF_L1*	AJ2	
IFPF_L2	AJ1	
IFPF_L2*	AH1	
IFPF_L3	AH2	
IFPF_L3*	AH3	

Display port output

+3V — L3 HCB1608KF-181T15_6 — 120 mA — +DACA_VDD — AJ12
0827b
C57 4.7U/6.3V_6, C49 4700P/25V_4, C105 470P/50V_4, C95 .1U/10V_4, R367 124/F_4
DACA_VREF — AK12
DACA_RSET — AK13

DACA(CRT)

DACA_VDD
DACA_VREF
DACA_RSET

DACA_RED	AM15	L_CRT_R — R82 150/F_4 — CRT_R <23>
DACA_GREEN	AM14	L_CRT_G — R79 150/F_4 — CRT_G <23>
DACA_BLUE	AL14	L_CRT_B — R75 150/F_4 — CRT_B <23>
DACA_HSYNC	AM13	CRT_HSYNC — R73 33_4 — HSYNC_COM <23>
DACA_VSYNC	AL13	CRT_VSYNC — R76 33_4 — VSYNC_COM <23>
I2CA_SCL	G1	DDCCLK <23>
I2CA_SDA	G4	DDCDATA <23>

+DACB_VDD — AG7
R356 10K/F_4 — AK6
AH7

DACC(CRT2)

DACC_VDD/ DACB_VDD
DACC_VREF/ DACB_VREF
DACC_RSET/ DACB_RSET

/DACC_RED	AK4	
DACB_RED		
/DACC_GREEN	AL4	
DACB_GREEN		
/DACC_BLUE	AJ4	
DACB_BLUE		
DACB_HSYNC/ DACC_HSYNC	AM1	
DACB_VSYNC/ DACC_VSYNC	AM2	
I2CB_SCL	G3	I2CB_SCL R54 2.2K_4 — +3V
I2CB_SDA	G2	I2CB_SDA R49 2.2K_4 — +3V

DACB(TV)

DACB_VREF/ NC — AC5

NC/ DACB_RED	AA4	
NC/ DACB_GREEN	AB4	
NC/ DACB_BLUE	Y4	R48 10K/F_4 — +3V
CEC/ DACB_CSYNC	AB5	

+1.05V — L8 HCB1608KF-181T15_6 — +NV_PLLVDD — 65mA — AE9
C85 4.7U/6.3V_6, C86 .1U/10V_4, C71 .1U/10V_4, C70 4700P/25V_4

+1.05V — L2 HCB1608KF-181T15_6 — 50mA — AD9
C48 1U/6.3V_4, C78 .1U/10V_4

25mA — AF9

PLLVDD
VID_PLLVDD
SP_PLLVDD

XTAL_PLL

XTAL_SSIN	D2	XTAL_SSIN — R353 22_4 — CLK_27M_SS <2>
XTAL_OUTBUFF	D1	BXTALOUT
XTAL_IN	B1	XTALIN — R46 0_4 — CLK_27M_NONSS <2>
XTAL_OUT	B2	XTALOUT — Y1 *27MHZ (2, 1)

C44 *18P/50V_4
5*3 package
C53 *18P/50V_4

PLACE CLOSE TO GPU

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

XTAL_SSIN — R349 10K/F_4
BXTALOUT — R352 *10K/F_4

10 kΩ pull-down only if no spread chip used.

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GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

CS31002FB26 (RES CHIP 10K 1/16W +-1% (0402))
CS31502FB08 (RES CHIP 15K 1/16W +-1% (0402))
CS32002FB02 (RES CHIP 20K 1/16W +-1%(0402))

PCI_DEVID[4]/SUBVENDOR

Default: Qimonda VRAM

SEE Datasheet for details on N10P Straps!

1211 DEVICE ID CHANGE

nVidia request 35K

Delete C122,R145,R148,R127,R99

I2C addr???

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Strap1=GPU swing at PCIE interface

CHIP	PCI_DEVID:	STRAP2	
N10P-GE	0x0A28	1000	PU 5K
N10M-GE	0x0A68	1000	PU 5K
N10P-GS	0x0A34	0100	PD 25K

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

HDCP ROM

Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

VRAM Configuration Table

R358

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
0101		Reserved		
0110				
XXXX				
XXXX				

AKD5LZGTW00
AKD5LGGT502

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VRAM termination

<42> +VGACORE

+VGACORE +VGACORE

U25F

BGA969-NVIDIA-NB9P-GS
COMMON

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

U25G

BGA969-NVIDIA-NB9P-GS
COMMON

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

NVVDD Decoupling

+VGACORE

PLACE NEAR BALLS

C164 .033U/10V_4	C176 .033U/10V_4	C109 .1U/10V_4	C107 .22U/25V_6	C50 .22U/25V_6	C126 1U/6.3V_4
C179 .01U/16V_4	C196 .01U/16V_4	C163 .033U/10V_4	C128 .033U/10V_4	C113 .033U/10V_4	C51 .033U/10V_4
C148 .01U/16V_4	C104 .01U/16V_4	C140 .01U/16V_4	C147 .01U/16V_4	C146 .01U/16V_4	C130 .01U/16V_4

C166 4700P/25V_4 (2-1)

C165 6800P/25V_4 (2-1)

C55 1U/6.3V_4

PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10X (POWER & GND) 5/5	1A

Date: Thursday, July 09, 2009 Sheet 16 of 45

CHANNEL A: 256MB/512MB DDR3

<13> VMA_DQ[63..0]
<13> VMA_DM[7..0]
<13> VMA_WDQS[7..0]
<13> VMA_RDQS[7..0]

U9 / U28 / U10 / U29 — VRAM_DDR3 — 96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

11/17 Swap

R143 243/F_4
R401 243/F_4
R163 243/F_4
R389 243/F_4
R165 243/F_4
R160 243/F_4

R145 1.33K/F_4
R144 1.33K/F_4
C282 .1U/10V_4
R397 1.33K/F_4
R398 1.33K/F_4
C626 .1U/10V_4
R399 1.33K/F_4
R403 1.33K/F_4
C629 .1U/10V_4
R388 1.33K/F_4
R390 1.33K/F_4
C572 .1U/10V_4

C298 .1U/10V_4, C304 .1U/10V_4, C303 .1U/10V_4, C300 .1U/10V_4, C82 .1U/10V_4, C627 .1U/10V_4, C628 .1U/10V_4, C632 .1U/10V_4
C302 .1U/10V_4, C575 .1U/10V_4, C630 .1U/10V_4, C283 .1U/10V_4, C306 .1U/10V_4, C308 .1U/10V_4, C631 .1U/10V_4, C309 .1U/10V_4
C618 .1U/10V_4, C296 .1U/10V_4, C295 .1U/10V_4, C616 .1U/10V_4
C261 1U/6.3V_4, C75 1U/6.3V_4, C307 1U/6.3V_4, C299 1U/6.3V_4
C625 10U/6.3V_6S, C574 .1U/10V_4, C252 .1U/10V_4, C142 .1U/10V_4, C137 .1U/10V_4, C284 .1U/10V_4

PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM channel A	1A

Date: Thursday, July 09, 2009 Sheet 17 of 45

CHANNEL B: 256MB/512MB DDR3

<13> VMC_DQ[63..0]
<13> VMC_DM[7..0]
<13> VMC_WDQS[7..0]
<13> VMC_RDQS[7..0]

U24 / U5 / U7 / U27 — 96-BALL SDRAM DDR3 VRAM _DDR3

Should be 240 Ohms +-1%

R372 243/F_4
R84 243/F_4
R122 243/F_4
R383 243/F_4

R77 243/F_4
R87 1.33K/F_4
R86 1.33K/F_4
R365 1.33K/F_4
R366 1.33K/F_4
R125 *243/F_4
R105 1.33K/F_4
R110 1.33K/F_4
R140 1.33K/F_4
R139 1.33K/F_4

C138 .1U/10V_4
C520 .1U/10V_4
C238 .1U/10V_4
C272 .1U/10V_4

C501 .1U/10V_4
C498 .1U/10V_4
C69 .1U/10V_4
C564 .1U/10V_4
C276 .1U/10V_4
C68 .1U/10V_4
C100 .1U/10V_4
C271 .1U/10V_4
C494 .1U/10V_4
C156 .1U/10V_4
C512 .1U/10V_4
C499 .1U/10V_4
C556 .1U/10V_4
C504 .1U/10V_4
C510 .1U/10V_4
C568 .1U/10V_4
C552 1U/6.3V_4
C553 1U/6.3V_4
C496 1U/6.3V_4
C521 1U/6.3V_4
C181 10U/6.3V_6S
C559 .1U/10V_4
C578 .1U/10V_4
C497 .1U/10V_4
C562 .1U/10V_4
C285 .1U/10V_4

PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VRAM channel B	1A

Date: Thursday, July 09, 2009 Sheet 18 of 45

3VPCU <24,25,30,31,32,33,34,35,39,41>
5VPCU <34,35,36,38,39,40>
+3VRTC <22,31>
+3V <2,4,6,9,10,11,12,14,15,20,21,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42>
+1.5V <4,9,20,22,30,33,34,37>
+1.05V <2,3,4,5,6,8,9,12,13,14,22,23,34,38,40>
3V_S5 <20,21,22,34>

0804 Change RTC connector to cable type in Ver.C

0505 EMI added

Notice: GPIO33 is also a strap pin(internal pull up 20k). Don't pull -down.

SATA HDD

SATA ODD

ESATA

CLOSE CODEC

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

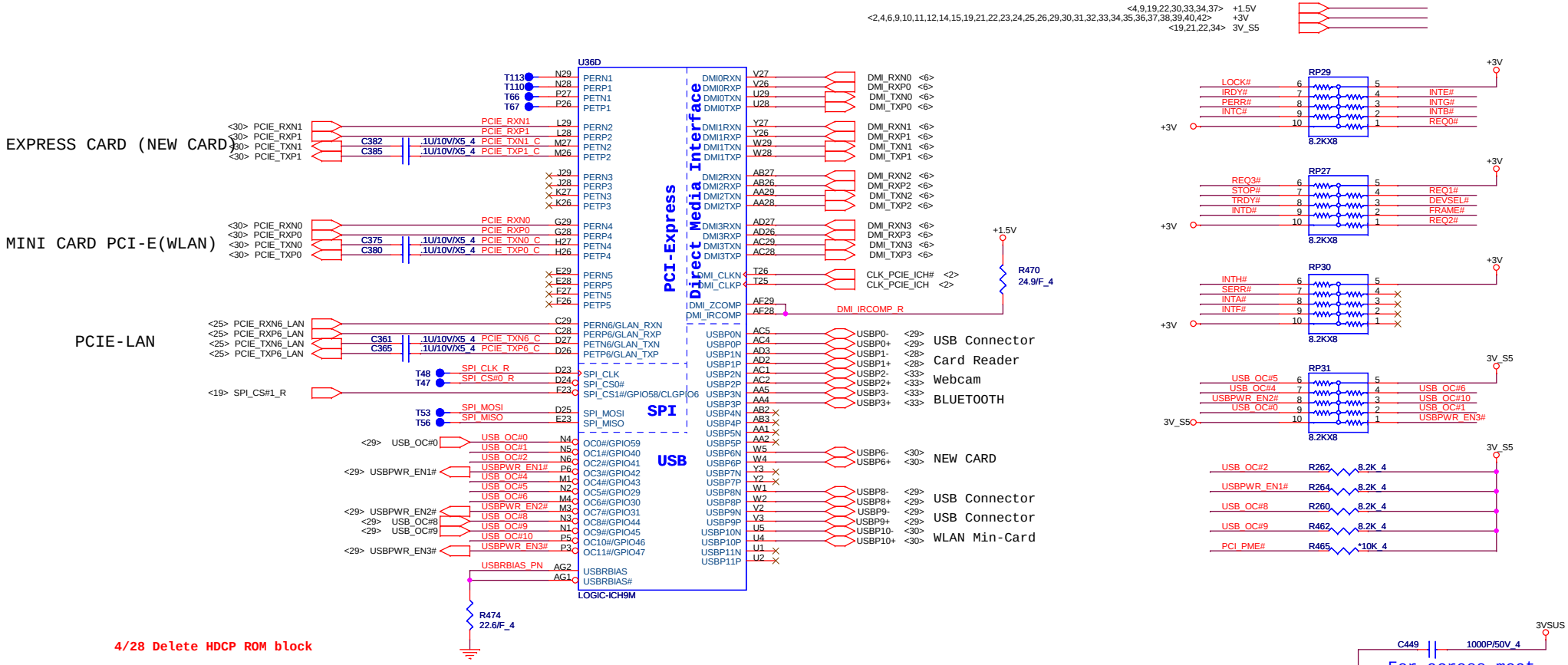
A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M 1/4 Host	1A

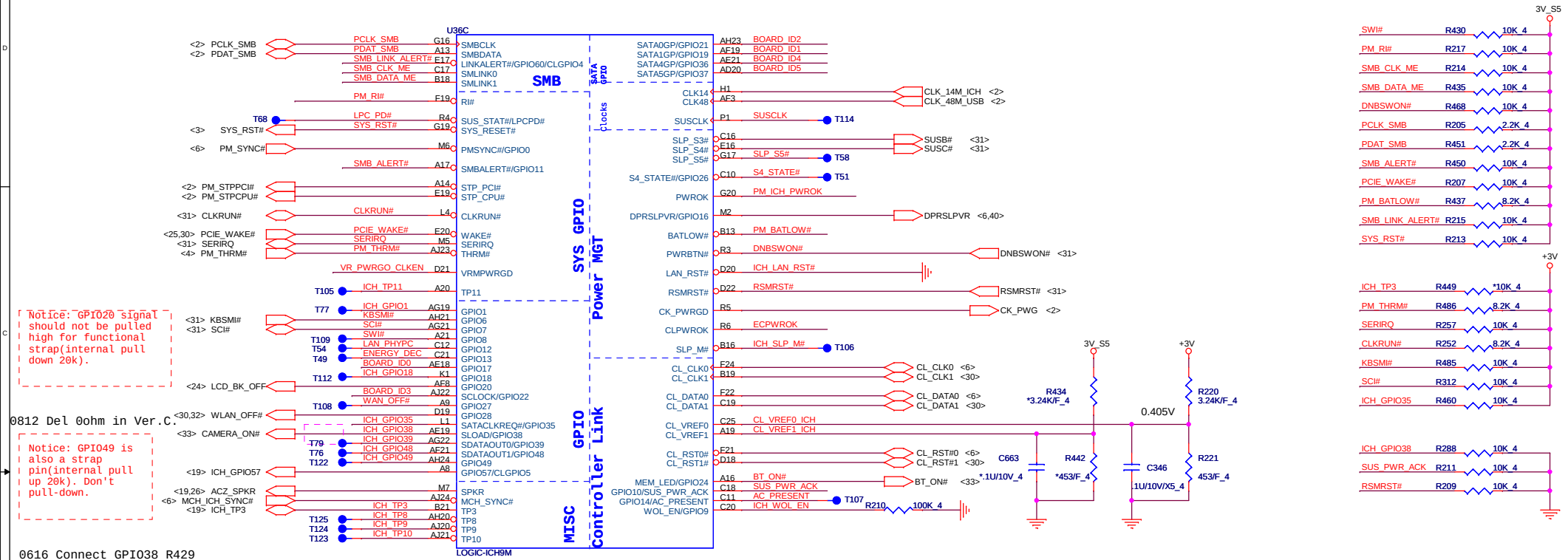
Date: Thursday, July 09, 2009 Sheet 19 of 45



PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus/1394 /Card Reader	AD21	0	E,F

<4,9,19,20,22,30,33,34,37> +1.5V
<2,4,6,9,10,11,12,14,15,19,20,22,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
<19,20,22,34> 3V_S5
<20,28,30,33,34,40,42> 3VSUS

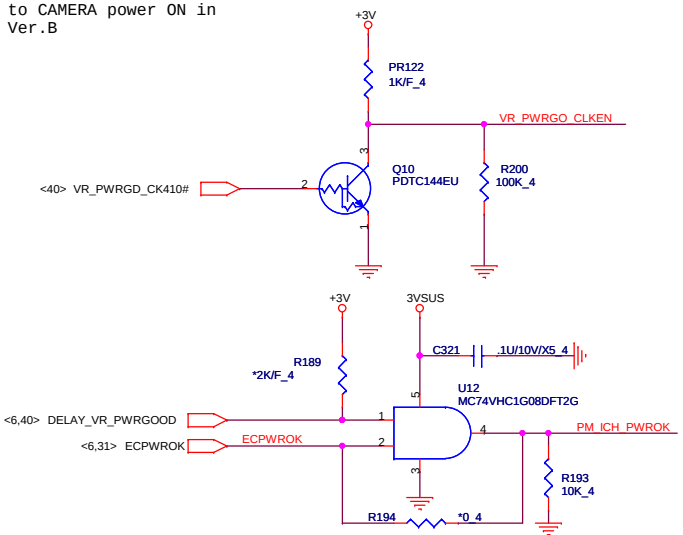


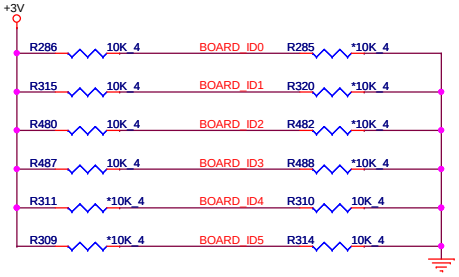
Notice: GPIO20 signal should not be pulled high for functional strap(internal pull down 20k).

0812 Del 0ohm in Ver.C.

Notice: GPIO49 is also a strap pin(internal pull up 20k). Don't pull-down.

0616 Connect GPIO38 R429 to CAMERA power ON in Ver.B





Board ID For Function	0	1
ID0, GPIO17	Camera attached	Camera NC<Default>
ID1, GPIO19	UXGA support	XGA support<Default>
ID2, GPIO21	EF7 Keyboard	EF9 Keyboard<Default>
ID3	Old EF79	EF79A
ID4	Default	
ID5	Default	

EC GPE2 Pin83 EF7 Keyboard EF9 Keyboard

Camera HW detection
XGA/UXGA selection
EF7/EF9 keyboard selection

0609 Define ID for Ver.B
0626 Modify ID2 for leakage concern in Ver.B

PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M 3/4 GPIO	1A
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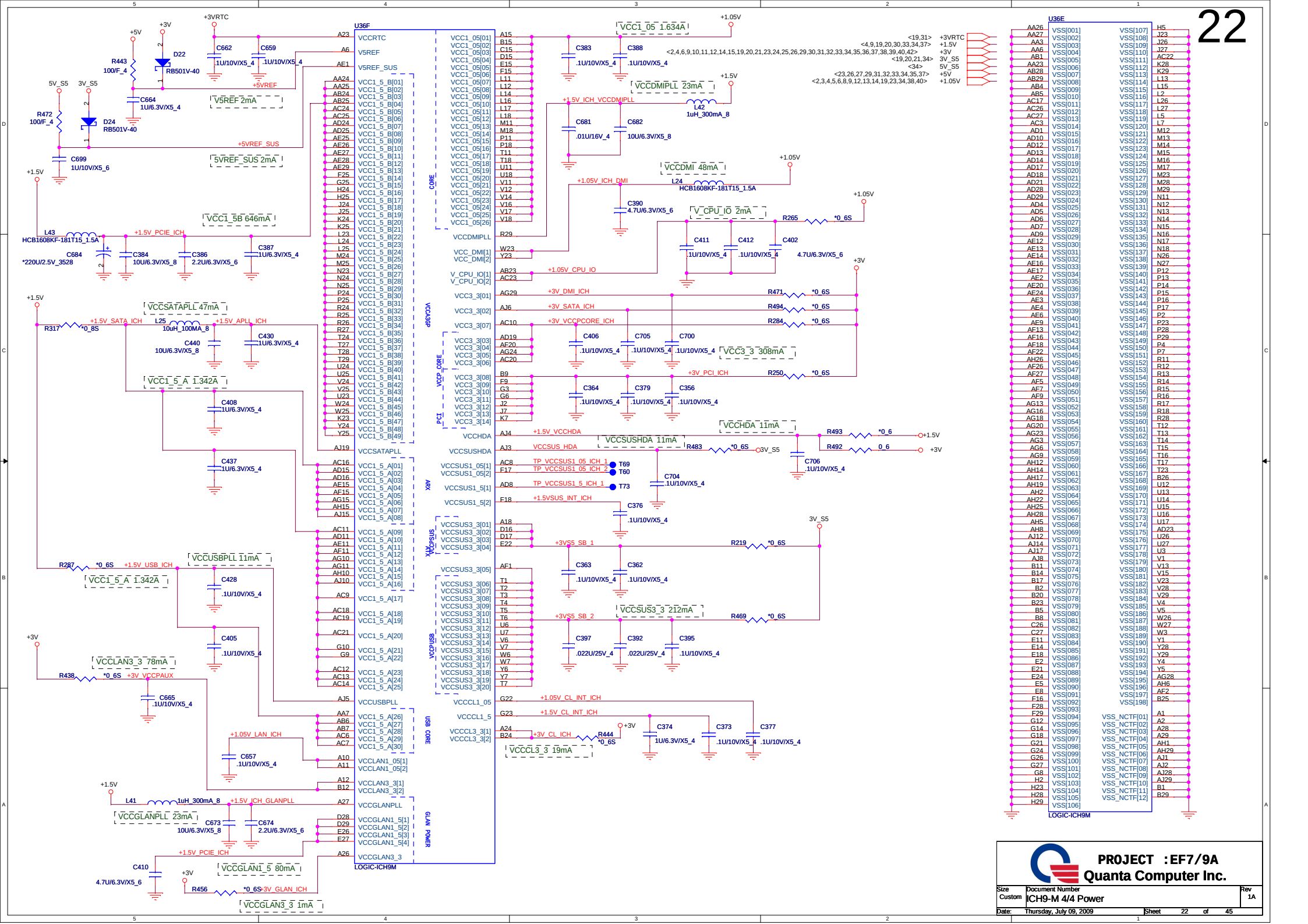
U36F
LOGIC-ICH9M
U36E
LOGIC-ICH9M
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
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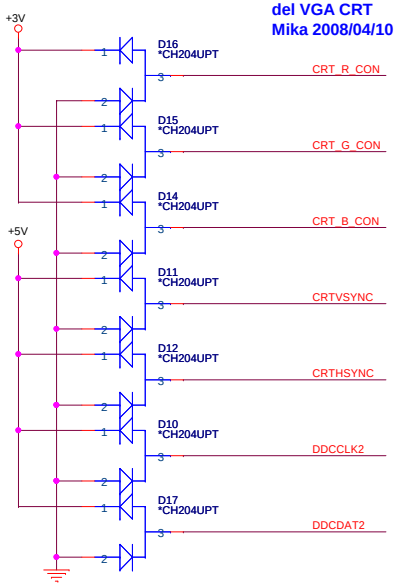
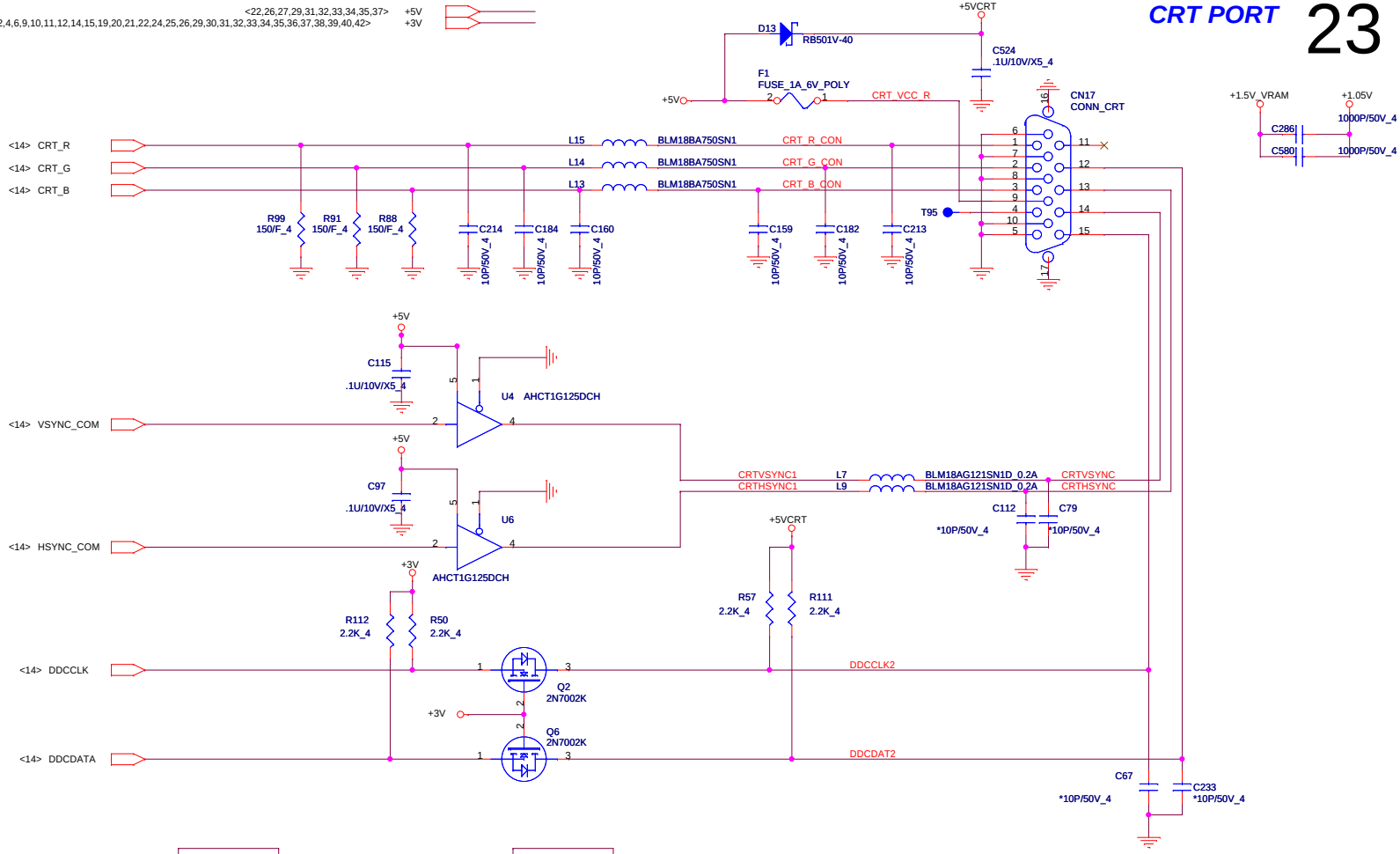
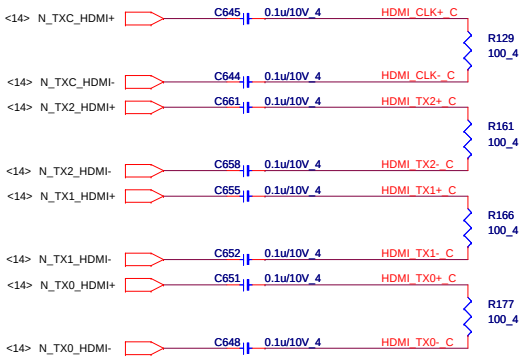
VSS[190]
VSS[191]
VSS[192]
VSS[193]
VSS[194]
VSS[195]
VSS[196]
VSS[197]
VSS[198]
VSS_NCTF[01]
VSS_NCTF[02]
VSS_NCTF[03]
VSS_NCTF[04]
VSS_NCTF[05]
VSS_NCTF[06]
VSS_NCTF[07]
VSS_NCTF[08]
VSS_NCTF[09]
VSS_NCTF[10]
VSS_NCTF[11]
VSS_NCTF[12]
+3VRTC
+5V
+3V
+1.5V
+1.05V
3V_S5
5V_S5
D22
RB501V-40
D24
RB501V-40
R443 100/F_4
R472 100/F_4
C662 1U/10V/X5_4
C659 .1U/10V/X5_4
C664 1U/6.3V/X5_4
C699 1U/10V/X5_6
V5REF 2mA
5VREF_SUS 2mA
VCC1_5B 646mA
L43 HCB1608KF-181T15_1.5A
C684 *220U/2.5V_3528
C384 10U/6.3V/X5_8
C386 2.2U/6.3V/X5_6
C387 1U/6.3V/X5_4
+1.5V_PCIE_ICH
VCCSATAPLL 47mA
R317 *0_8S
+1.5V_SATA_ICH
L25 10uH_100MA_8
+1.5V_APLL_ICH
C440 10U/6.3V/X5_8
C430 1U/6.3V/X5_4
VCC1_5_A 1.342A
C408 1U/6.3V/X5_4
C437 1U/6.3V/X5_4
R287 *0_6S
+1.5V_USB_ICH
VCCUSBPLL 11mA
VCC1_5_A 1.342A
C428 .1U/10V/X5_4
C405 .1U/10V/X5_4
VCCLAN3_3 78mA
R438 *0_6S
+3V_VCCPAUX
C665 .1U/10V/X5_4
+1.05V_LAN_ICH
C657 .1U/10V/X5_4
L41 1uH_300mA_8
+1.5V_ICH_GLANPLL
VCCGLANPLL 23mA
C673 10U/6.3V/X5_8
C674 2.2U/6.3V/X5_6
+1.5V_PCIE_ICH
C410 4.7U/6.3V/X5_6
R456 *0_6S
+3V_GLAN_ICH
VCCGLAN1_5 80mA
VCCGLAN3_3 1mA
VCC1_05 1.634A
C383 .1U/10V/X5_4
C388 .1U/10V/X5_4
VCCDMIPLL 23mA
L42 1uH_300mA_8
+1.5V_ICH_VCCDMIPLL
C681 .01U/16V_4
C682 10U/6.3V/X5_8
VCCDMI 48mA
L24 HCB1608KF-181T15_1.5A
+1.05V_DMI
C390 4.7U/6.3V/X5_6
V_CPU_IO 2mA
R265 *0_6S
C411 .1U/10V/X5_4
C412 .1U/10V/X5_4
C402 4.7U/6.3V/X5_6
+1.05V_CPU_IO
+3V_DMI_ICH
R471 *0_6S
+3V_SATA_ICH
R494 *0_6S
+3V_VCCPCORE_ICH
R284 *0_6S
C406 .1U/10V/X5_4
C705 .1U/10V/X5_4
C700 .1U/10V/X5_4
VCC3_3 308mA
+3V_PCI_ICH
R250 *0_6S
C364 .1U/10V/X5_4
C379 .1U/10V/X5_4
C356 .1U/10V/X5_4
VCCHDA 11mA
+1.5V_VCCHDA
R493 *0_6
R492 0_6
VCCSUSHDA 11mA
VCCSUS_HDA
R483 *0_6S
C706 .1U/10V/X5_4
TP_VCCSUS1_05_ICH_1
TP_VCCSUS1_05_ICH_2
TP_VCCSUS1_5_ICH_1
T69
T60
T73
C704 .1U/10V/X5_4
+1.5VSUS_INT_ICH
C376 .1U/10V/X5_4
+3VS5_SB_1
R219 *0_6S
C363 .1U/10V/X5_4
C362 .1U/10V/X5_4
VCCSUS3_3 212mA
+3VS5_SB_2
R469 *0_6S
C397 .022U/25V_4
C392 .022U/25V_4
C395 .1U/10V/X5_4
+1.05V_CL_INT_ICH
+1.5V_CL_INT_ICH
+3V_CL_ICH
R444 *0_6S
C374 1U/6.3V/X5_4
C373 .1U/10V/X5_4
C377 .1U/10V/X5_4
VCCCL3_3 19mA
<19,31> +3VRTC
<4,9,19,20,30,33,34,37> +1.5V
<2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
<19,20,21,34> 3V_S5
<34> 5V_S5
<23,26,27,29,31,32,33,34,35,37> +5V
<2,3,4,5,6,8,9,12,13,14,19,23,34,38,40> +1.05V
PROJECT : EF7/9A
Quanta Computer Inc.
Size Custom
Document Number ICH9-M 4/4 Power
Rev 1A
Date: Thursday, July 09, 2009
Sheet 22 of 45

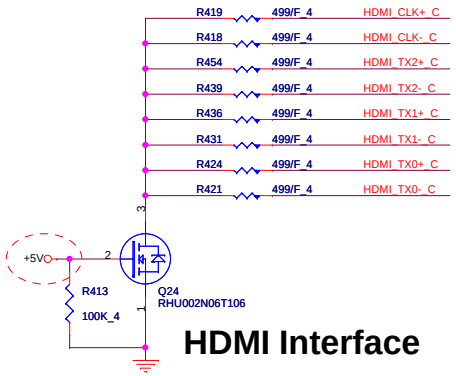
del VGA CRT
Mika 2008/04/10



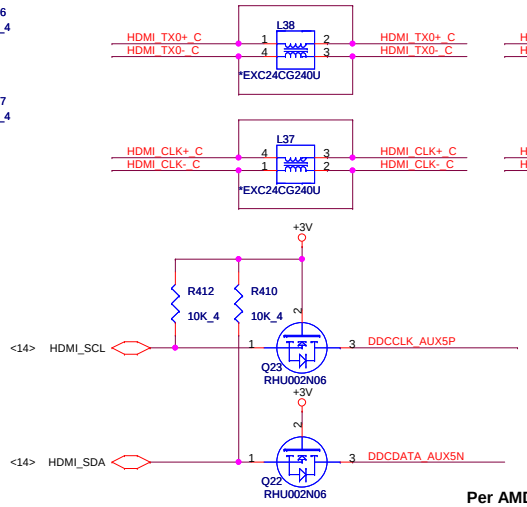


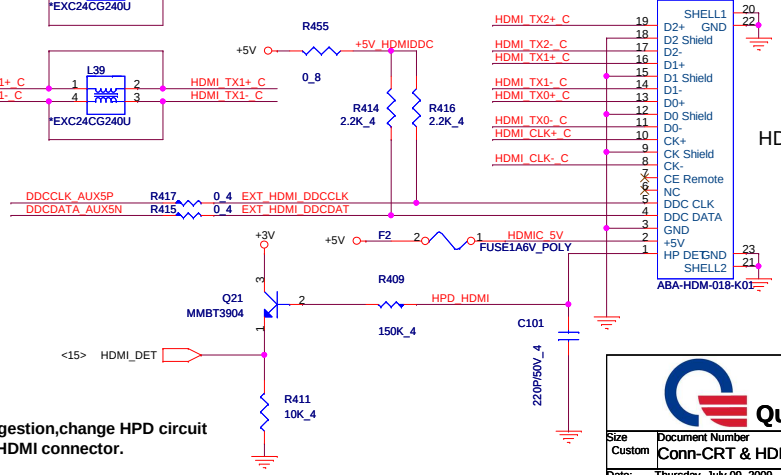
PLACE AC CAP
CLOSE TO CONNECTOR





HDMI Interface





HDMI PORT

Per AMD suggestion,change HPD circuit and close to HDMI connector.

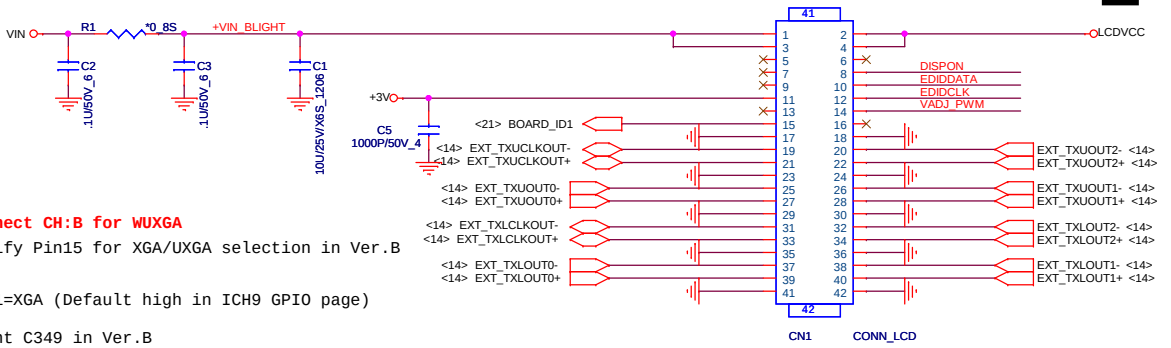
PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-CRT & HDMI	1A

Date: Thursday, July 09, 2009 Sheet 23 of 45

LVDS

<29,33,34,37,38,40,42> 5VSUS
<2,4,6,9,10,11,12,14,15,19,20,21,22,23,25,26,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
<27,33,34,36,37,39> +15V
<19,25,30,31,32,33,34,35,39,41> 3VPCU
<35,36,37,38,39,40,42> VIN
<22,23,26,27,29,31,32,33,34,35,37> +5V



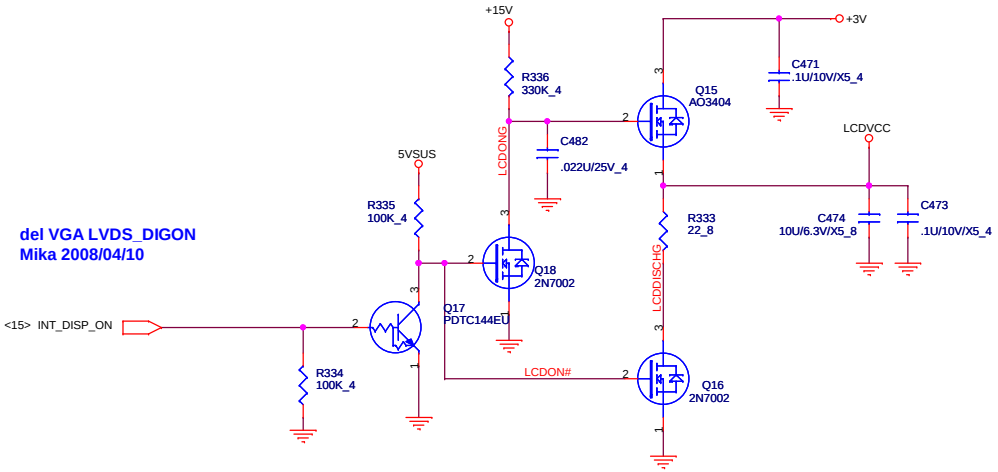
0430 Connect CH:B for WUXGA

0616 Modify Pin15 for XGA/UXGA selection in Ver.B
Pin15
0=UXGA, 1=XGA (Default high in ICH9 GPIO page)

0626 Mount C349 in Ver.B

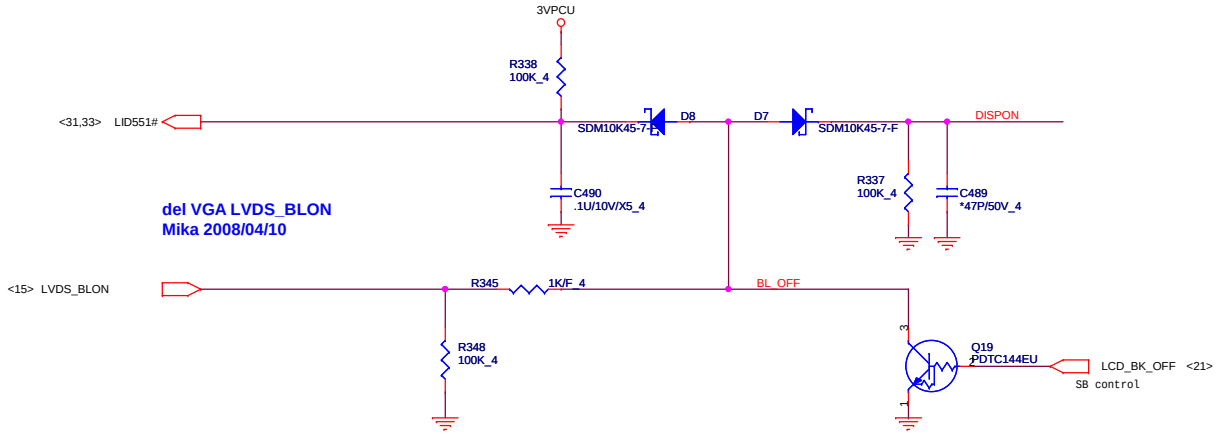
del VGA LVDS
Mika 2008/04/10

PANEL VCC CONTROL



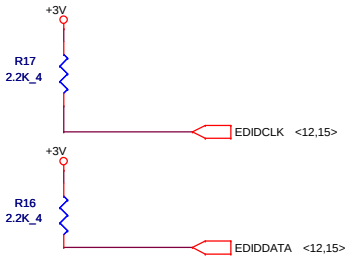
del VGA LVDS_DIGON
Mika 2008/04/10

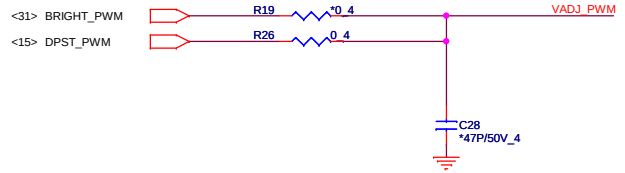
Backlight Control



del VGA LVDS_BLON
Mika 2008/04/10

del VGA EDID I2C
Mika 2008/04/10

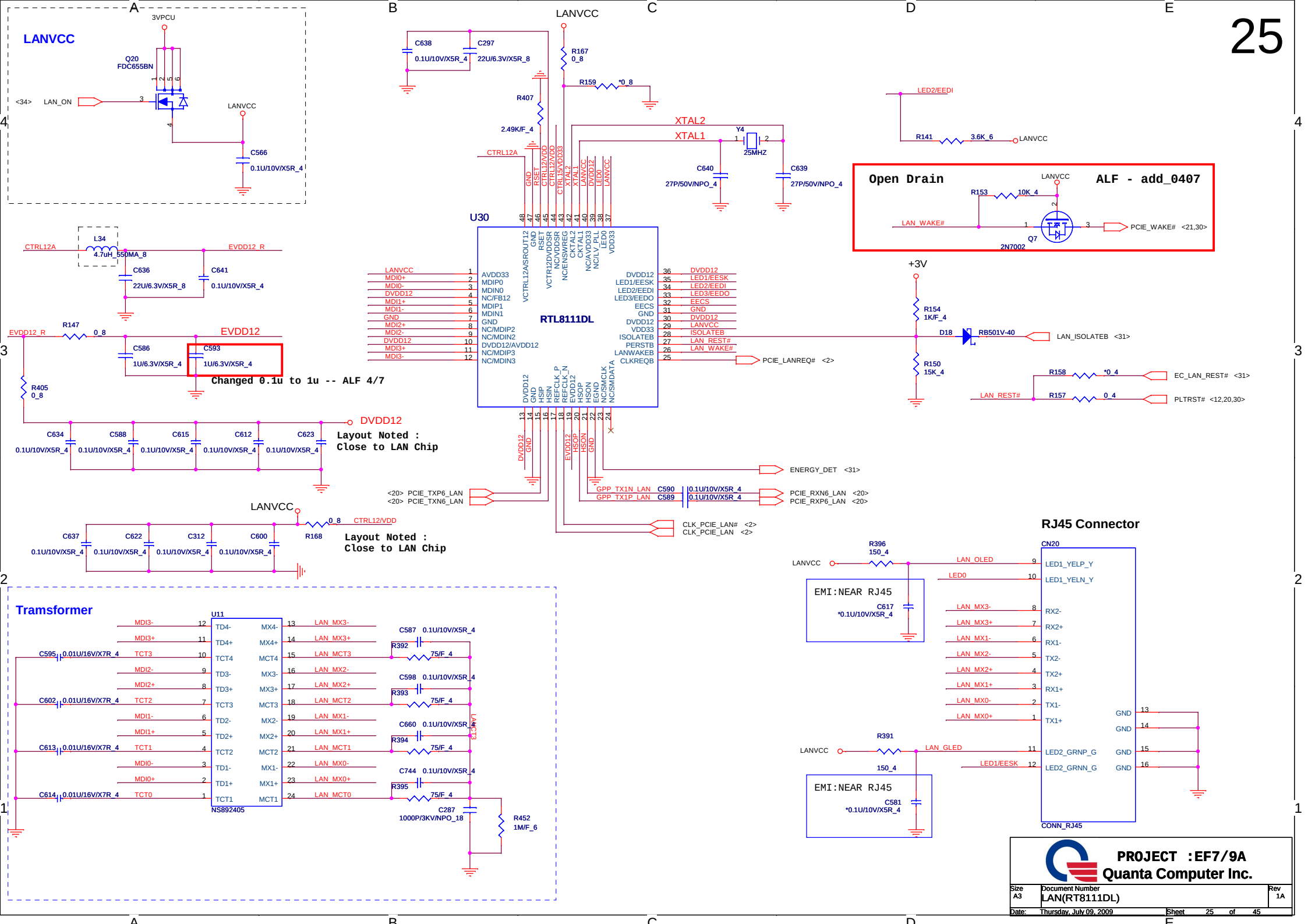




PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-LCD & LID	1A

Date: Thursday, July 09, 2009 Sheet 24 of 45



PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN(RT8111DL)	1A

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REALTEK

Headphone

HPOUT_L <27>
HPOUT_R <27>
MIC1_VREFO <27>

New

ALC272
(LQFP-48)

Analog
Digital

EAPD : codec defaul Low and
Pull high by Windows Vista
when enter Vista OS.

<27> HP_JD#
R490 5.1K/F_4
<27> AMPL
<27> AMPR
662_VREF
C719 *10U/10V/X5_8
C718 .1U/10V/X5_4
C723 10U/10V/X5_8
C722 .1U/10V/X5_4
U38
C714 2.2U/6.3V/X5_6
C715 2.2U/6.3V/X5_6
SENSE_B
FRONT-R
FRONT-L
Sense B
HPOUT-L
HPOUT-R
CPVEE
CBN
CBP
MIC1-VREFO
VREF
AVSS1
AVDD1
MONO-OUT
AVDD2
LOUT2-L
JDREF
LOUT2-R
AVSS2
NC
DMIC-CLK3/4
SPDIFO2
DMIC-CLK1/2
EAPD
SPDIFO1
LINE1-R
LINE1-L
MIC1-R
MIC1-L
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A
LINE_R <27>
LINE_L <27>
EXT_MIC_R <27>
EXT_MIC_L <27>
MIC2_VREFO_L
MIC2_VREFO_R
INT_MIC_R
INT_MIC_L
EXT_MIC_JD# <27>
LINE_JD# <27>
SENSE_A
R504 10K/F_4
R491 20K/F_4
C702 10U/10V/X5_8
C703 .1U/10V/X5_4
R478 20K/F_4
JDREF
<33> DMIC_CLK12
R479 *10K_4
D23 RB501V-40
<27> AMP_SHDN#
<27> SPDIF_OUT
DVDD2
DMIC-1/2/GPIO0
DMIC-3/4/GPIO1
DVSS
SDATA-OUT
BIT-CLK
DVSS1
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP
PC_BEEP1
C694 10U/10V/X5_8
C716 .1U/10V/X5_4
C693 10U/10V/X5_8
C711 10U/10V/X5_4
pin1
pin9
ACZ_RST#_AUDIO <19>
ACZ_SYNC_AUDIO <19>
SDI
R496 33_4
ACZ_SDIN0 <19>
R489 22_4
BITCLK <19>
ACZ_SDOUT_AUDIO <19>
DMIC_DAT12 <33>
C712 10P/50V/COG_4

<22,23,27,29,31,32,33,34,35,37> +5V
<2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,29,30,31,32,33,34,35,36,37,38,39,40,42> +3V
<20,21,28,30,33,34,40,42> 3VSUS

L26 *BLM11A601S_0.2A
U20
TPS793475DBVR
Vout
Vin
BYP
GND
EN
C456 .1U/10V/X5_4
C458 10U/10V/X5_8
C454 1U/10V/X5_6
C453 .047U/10V/X5_4
C455 .1U/10V/X5_4
C457 1U/10V/X5_6
C459 10U/10V/X5_8
MAINON
MAINON <31,34,36,37,38,42>
Vset=1.242V

TBD

PIN NAME	Location	Re-tasking
FRONT(35/36)	INTERNAL SPEAKERS	
LINE1(23/24)	LINE-IN	SURR OUT
MIC2(16/17)	EXT MIC	CEN / LEF OUT
LINE2(14/15)	HP-OUT	FRONT OUT

FOR EMI SOLUTION

R328 *0_6S
R473 *0_6S
R327 *0_6S
C724 .1U/10V/X5_4
C698 .1U/10V/X5_4

0922 Short R422,R373, R227 in FAI.

PC BEEP

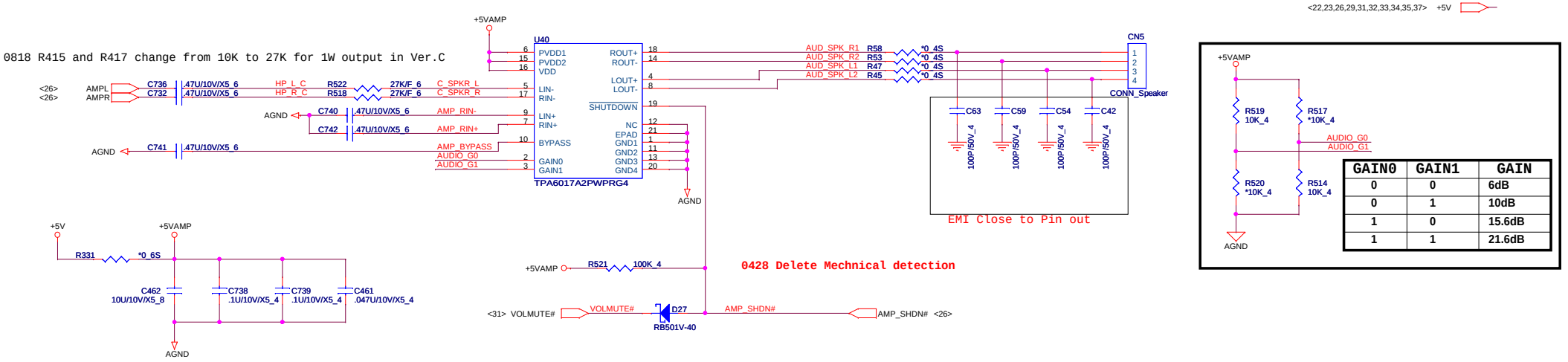
C717 .1U/10V/X5_4
<31> PCBEEP_AD
<19,21> ACZ_SPKR
U39
TC7SH86FU
PC_BEEP3
R500 47K_4
PC_BEEP2
C720 1U/6.3V/X5_4
PC_BEEP1
R501 4.7K_4
C721 100P/50V_4
R510 *0_4

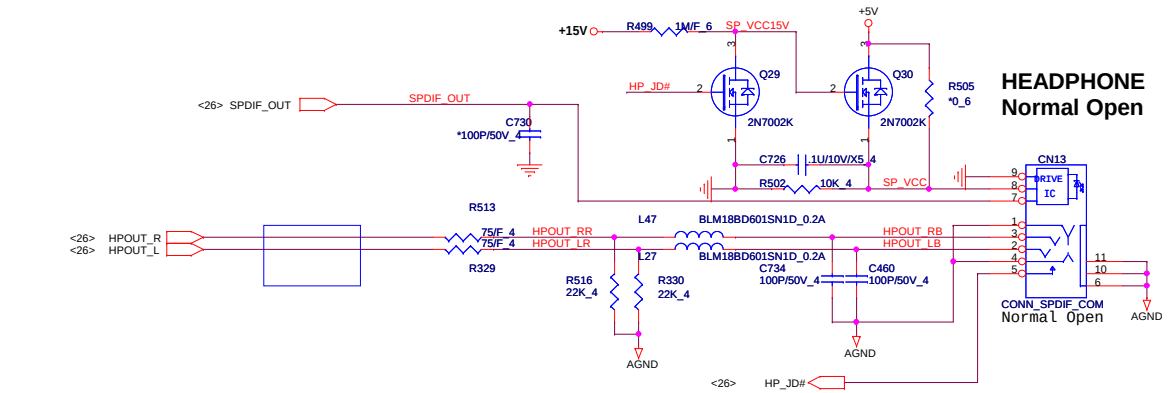
PROJECT : EF7/9A
Quanta Computer Inc.

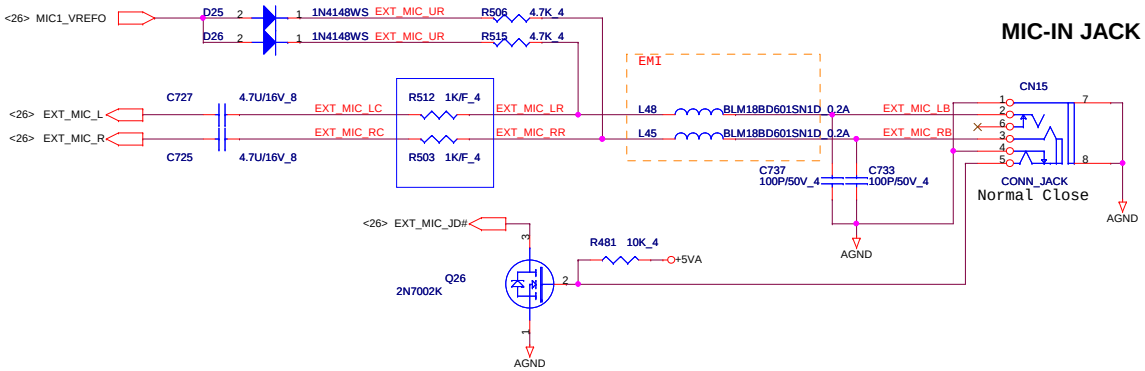
Size	Document Number	Rev
C	AUDIO-CODEC	1A

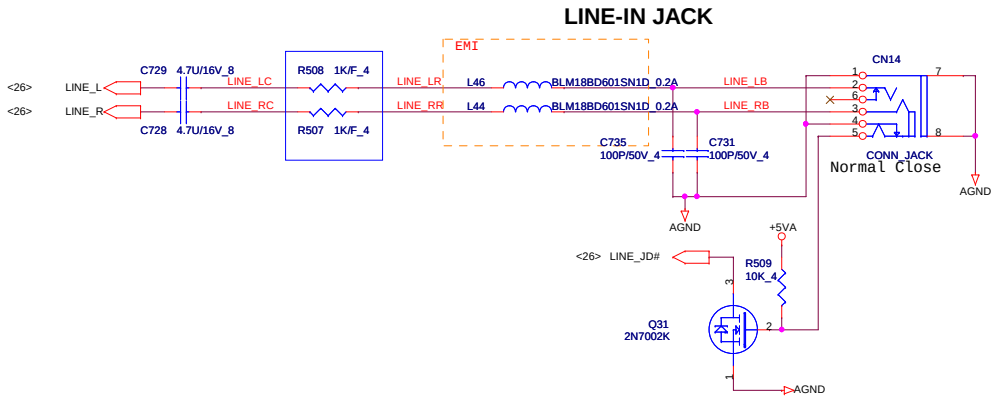
Date: Thursday, July 09, 2009 Sheet 26 of 45

INTERNAL SPEAKER AMPLIFIER





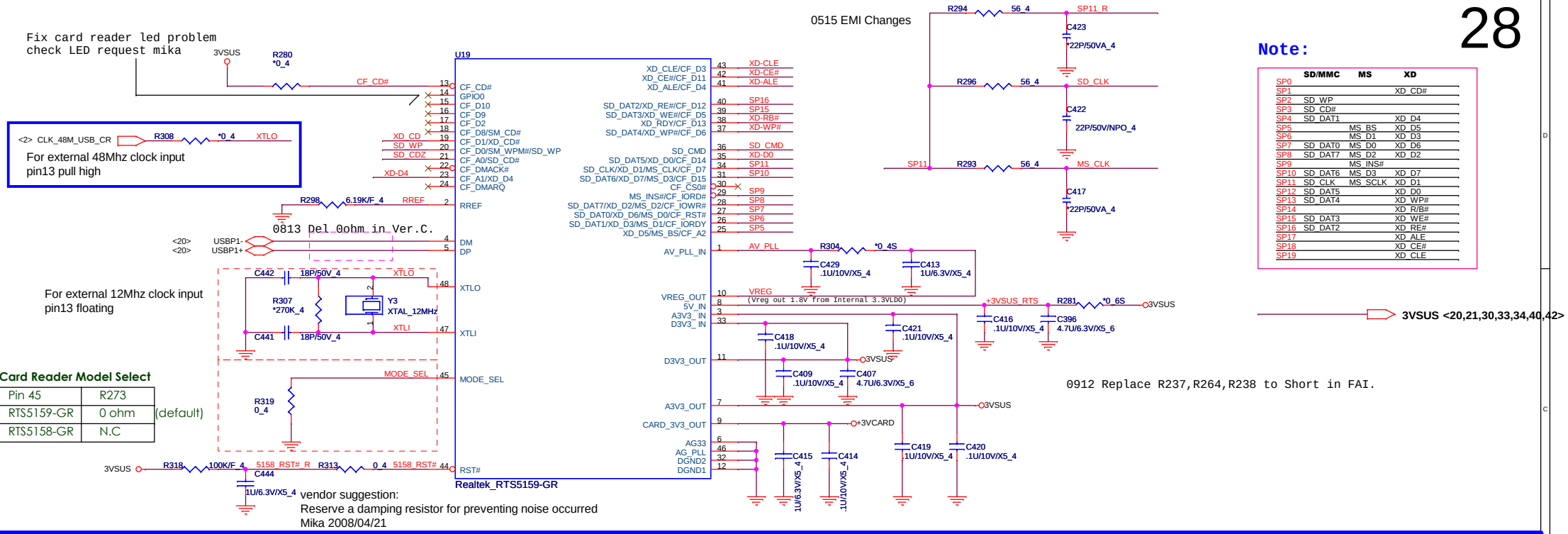




PROJECT : EF7/9A	
Quanta Computer Inc.	
Size: Custom	Document Number: AUDIO-AMP&JACKS
Rev: 1A	
Date: Thursday, July 09, 2009	Sheet 27 of 45

Fix card reader led problem
check LED request mika

0515 EMI Changes



Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

3VSUS <20,21,30,33,34,40,42>

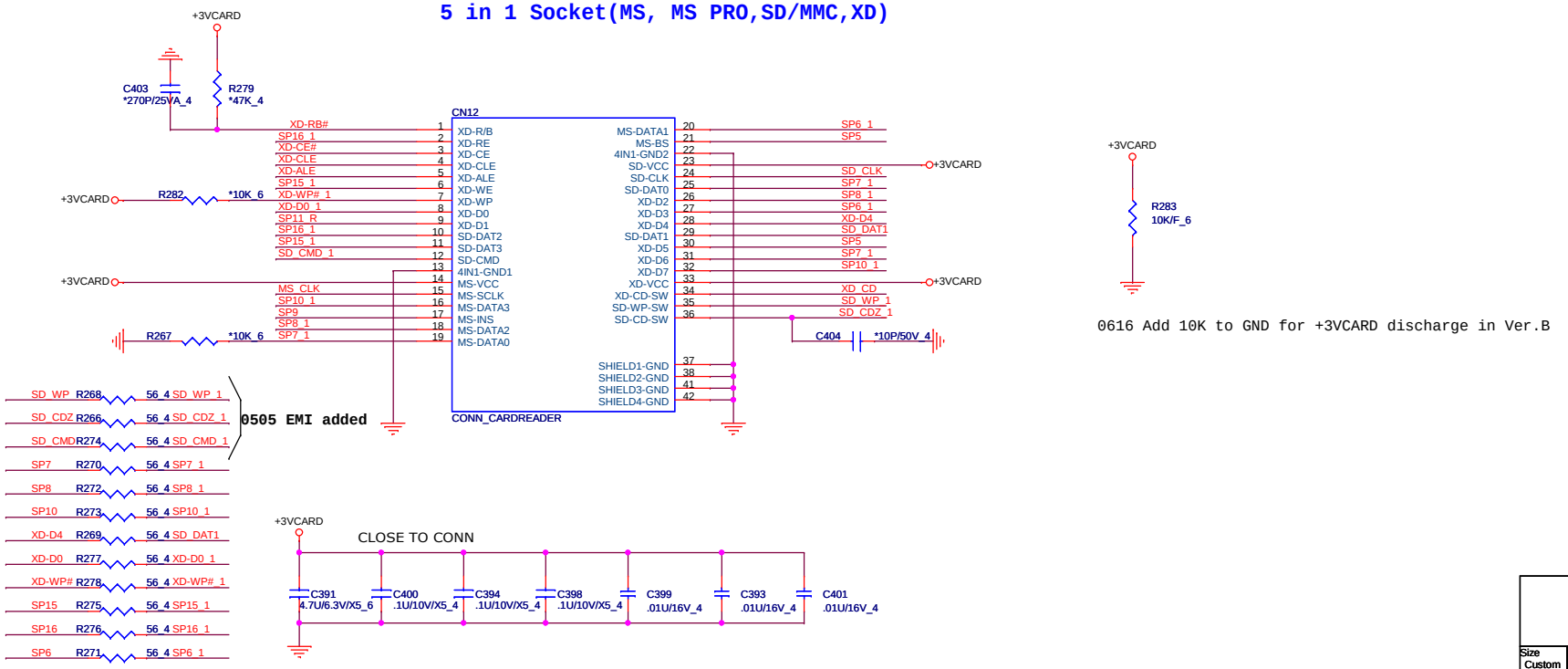
Card Reader Model Select

Pin 45	R273	
RTS5159-GR	0 ohm	(default)
RTS5158-GR	N.C	

vendor suggestion:
Reserve a damping resistor for preventing noise occurred
Mika 2008/04/21

0912 Replace R237,R264,R238 to Short in FAI.

5 in 1 Socket(MS, MS PRO,SD/MMC,XD)

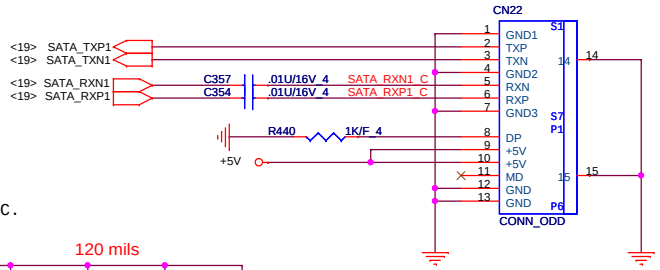


0616 Add 10K to GND for +3VCARD discharge in Ver.B

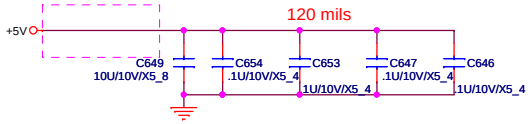
PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Card Reader-RTS5159	1A
Date: Thursday, July 09, 2009	Sheet 28 of 45	

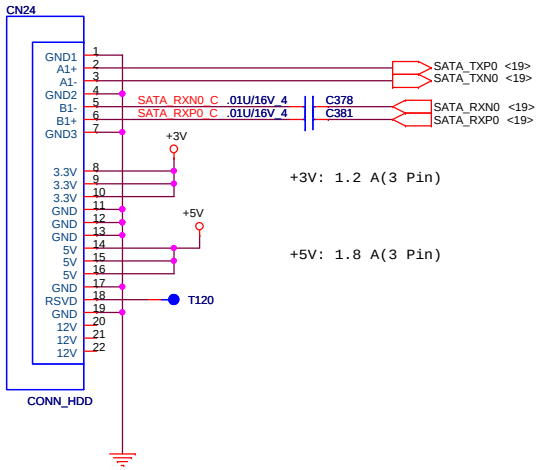
SATA CD-ROM



0812 Del 0ohm in Ver.C.

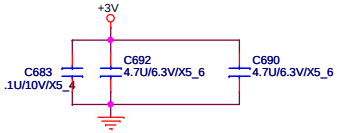


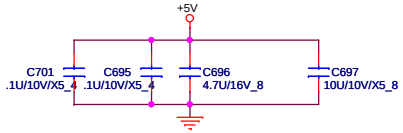
SATA-HDD CONNECTOR



+3V: 1.2 A(3 Pin)

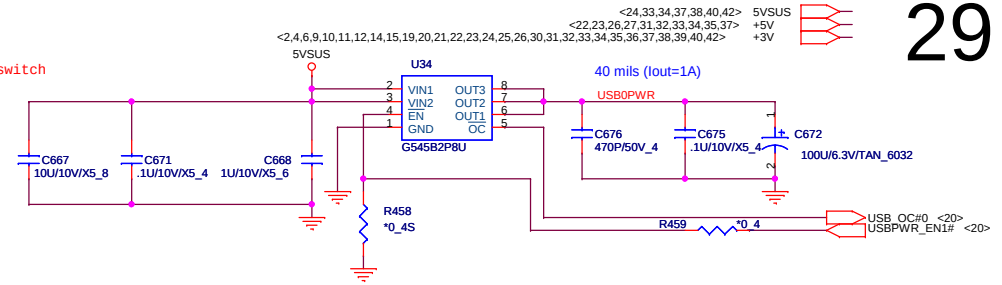
+5V: 1.8 A(3 Pin)



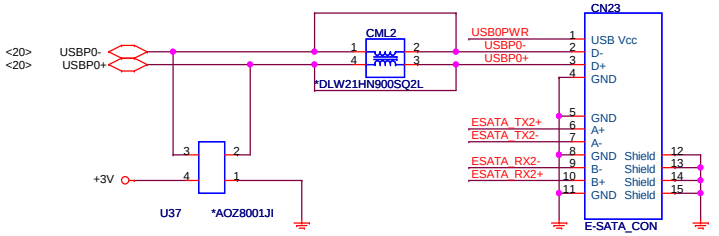


USBX3

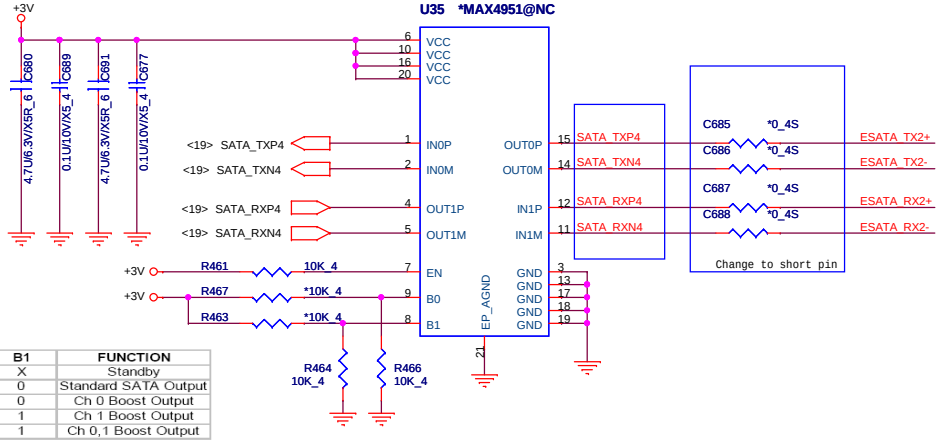
Close USB switch



USB/eSATA PORT at M/B

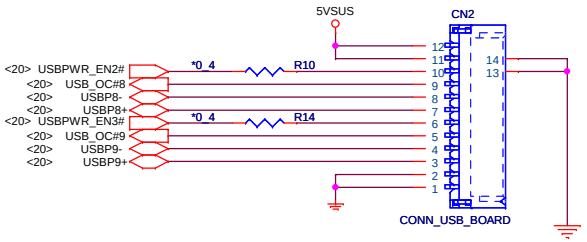


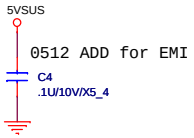
U35 *MAX4951@NC



EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

USB X2 at Daughter Board





PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-HDD/ODD/USB/eSATA	1A
Date: Thursday, July 09, 2009	Sheet 29 of 45	

Mini PCI-E Card 1
WLAN

0703 Change +3.3Vaux source to suspend power in Ver.B

<20,21,28,33,34,40,42> 3VSUS
<4,9,19,20,22,33,34,37> +1.5V
<2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,29,31,32,33,34,35,36,37,38,39,40,42> +3V

Del R268 &R269

?? -- ALF 4/7

0617 Correct RF LED connection to WLAN_OFF# in Ver.B

0812 Del 0ohm in Ver.C.

INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

EC - Reserve Power Control for WLAN -- 0205

?? -- ALF 4/7

EMI

Express Card

0812 Del 0ohm in Ver.C.

0627 Update Footprint (Foxconn type) in Ver.B
0702 Add R436 to Disconnect PCIE_WAKE# in Ver.B
0820 Update Footprint (Honda type) in Ver.C

PROJECT : EF7/9A Quanta Computer Inc.			
Size: Custom	Document Number: Conn-Xpress Card		Rev: 1A
Date: Thursday, July 09, 2009	Sheet 30 of 45		

IT8502E

0616 Modify Pin83 for EF7/EF9 keyboard selection in Ver.B
0616 Mount R139 for EC_ACTIVE debug in Ver.B
0626 Correct MB_ID2EC netname in Ver.B
0826 Remove R139 in FAI

(For PLL Power)

0516 Change ECACTIVE

0912 Replace R187,R192,R211 to Short in FAI.

0516 Change NBSWON control to Page33.

0812 Del 0ohm in Ver.C.

N10P power saving mode control
0505 Connect PCBEEP

0428 Delete RF ON/OFF function

0616 Reserve EC Pin81 in Ver.B

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R?	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

IT8502IX / IT8502JX
IT8512DX

C723	0	0.1uF
C724	NC	1uF

For 8502JX 0729 Remove C246 for ITE8502 power sequence issue in Ver.C

16MBit
FLASH_SST25VF016B

Battery

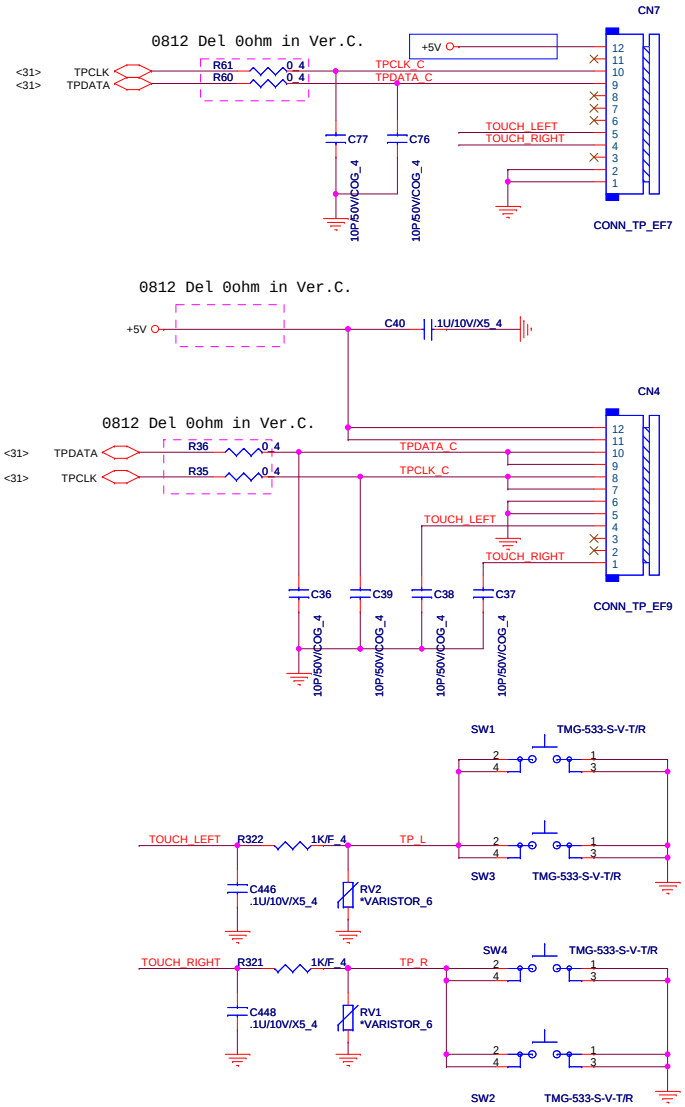
PROJECT : EF7/9A
Quanta Computer Inc.
Size: Custom | Document Number: EC-KBC IT8502E | Rev: 1A
Date: Thursday, July 09, 2009 | Sheet 31 of 45

DUAL Layout for both 15.6"/16" and 18"

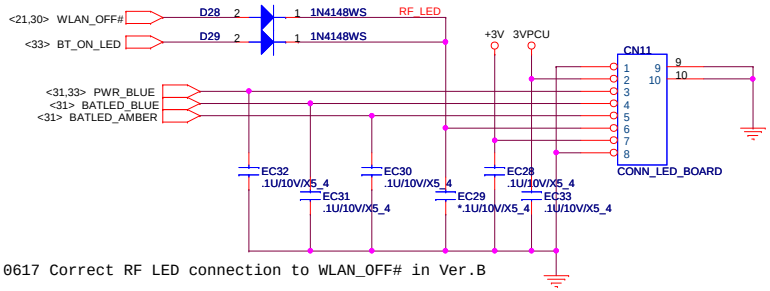
TOUCH PAD

<2,4,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,29,30,31,33,34,35,36,37,38,39,40,42> +3V
<22,23,26,27,29,31,33,34,35,37> +5V
<19,24,25,30,31,33,34,35,39,41> 3VPCU

0617 Add one more touch PAD connector for EF7 different pin definition.
0625 Del C548/C549, Change R432/R433 to 0603 in Ver.B



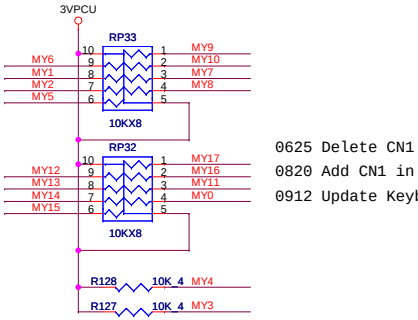
LED Board



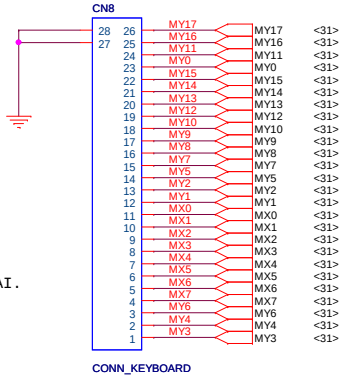
0617 Correct RF LED connection to WLAN_OFF# in Ver.B

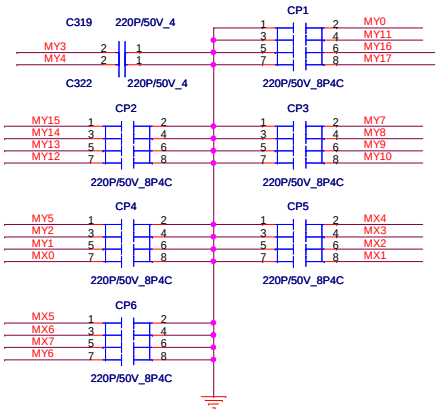
DUAL Layout for both 16" and 18.4"

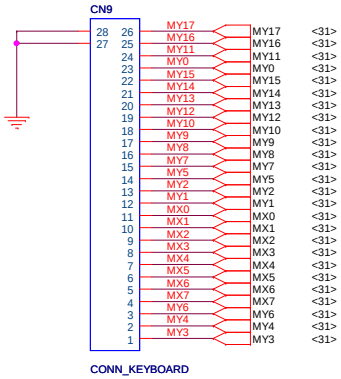
KEYBOARD



0625 Delete CN1 in Ver.B
0820 Add CN1 in Ver.C
0912 Update Keyboard conn. footprint in FAI.







0514 Change CP6 to 2 0402 Capacitor
0514 Swap nets.

PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Conn-KB/TB/LEDs	1A

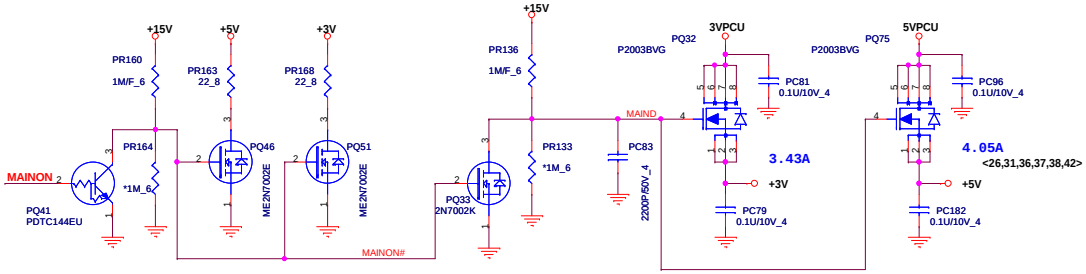
Date: Thursday, July 09, 2009 Sheet 32 of 45

PROJECT : EF7/9A
Quanta Computer Inc.
Size: Custom
Document Number: Conn-BtoB/Fan/Holes/BT
Rev: 1A
Date: Thursday, July 09, 2009
Sheet 33 of 45

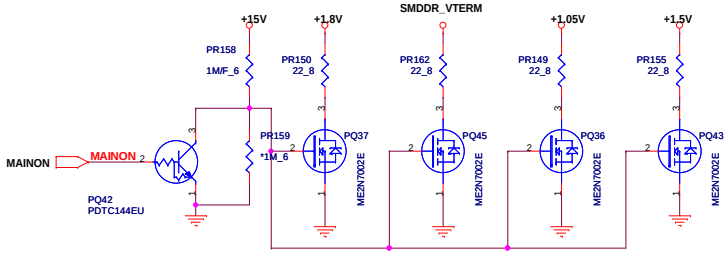
<20,21,28,30,33,40,42> 3VSUS
<24,29,33,37,38,40,42> 5VSUS

DISCHARGE

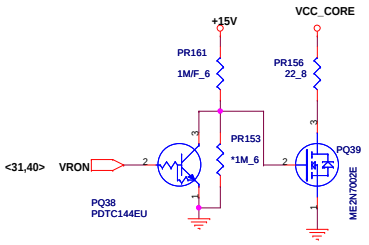
+3V, +5V



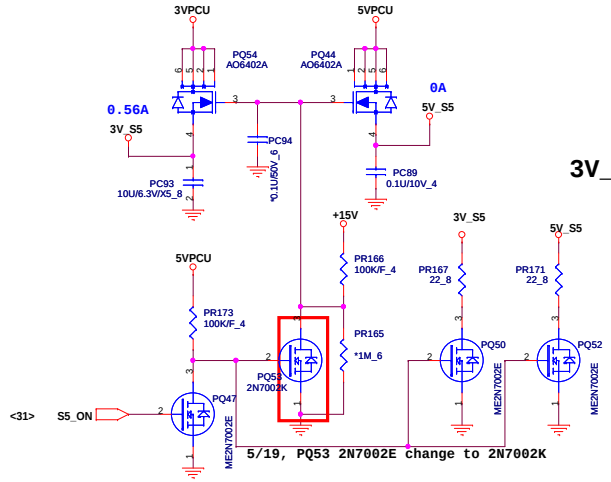
+1.8V, SMDDR_VTERM, +1.05V, +1.5V



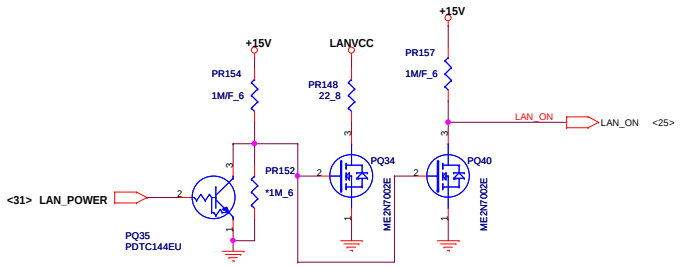
VCC_CORE



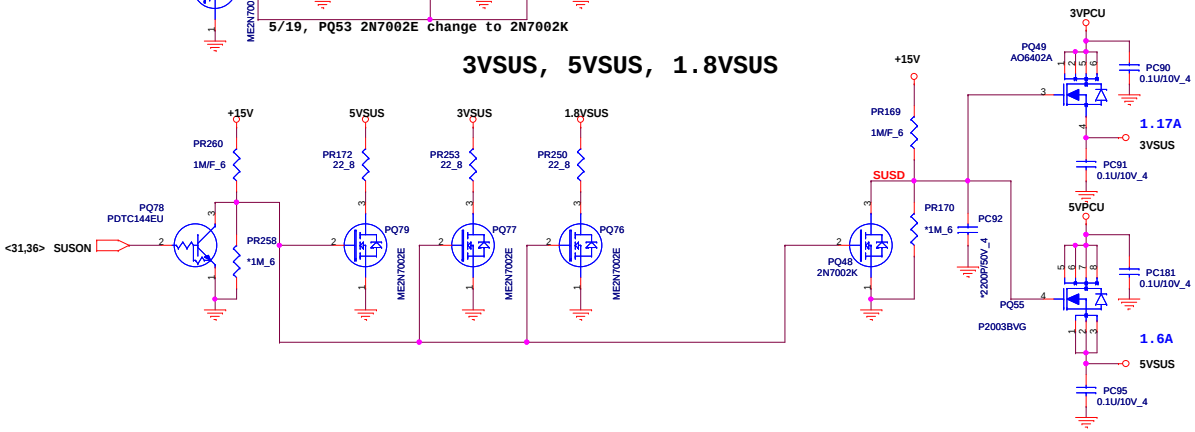
3V_S5, 5V_S5



LANVCC



3VSUS, 5VSUS, 1.8VSUS



PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power-Discharge	1A

Date: Thursday, July 09, 2009 Sheet 34 of 45

R138=12m ohm for 90W adapter-->current limit is 5A;

AD_ID	
3.5A	0.841V
3.75A	0.901V
4.4A	1.057V
4.5A	1.081V

CC_SET	Current
0.970V	2770mA
0.7V	2000mA
0.525V	1500mA
0.14V	400mA
0.0875V	250mA
0V	0mA

CELL_SET	
H	16.8V (4CELL)
L	12.6V (3CELL)

Add 0 Ohm

5/19, Del CO_LAY PC132 & PC134

7/3,modify PC131 and PC135 footprint

VOUT = (GAIN) (RSENSE)(ILOAD)

500mV/A for Batt I dicharge sensing

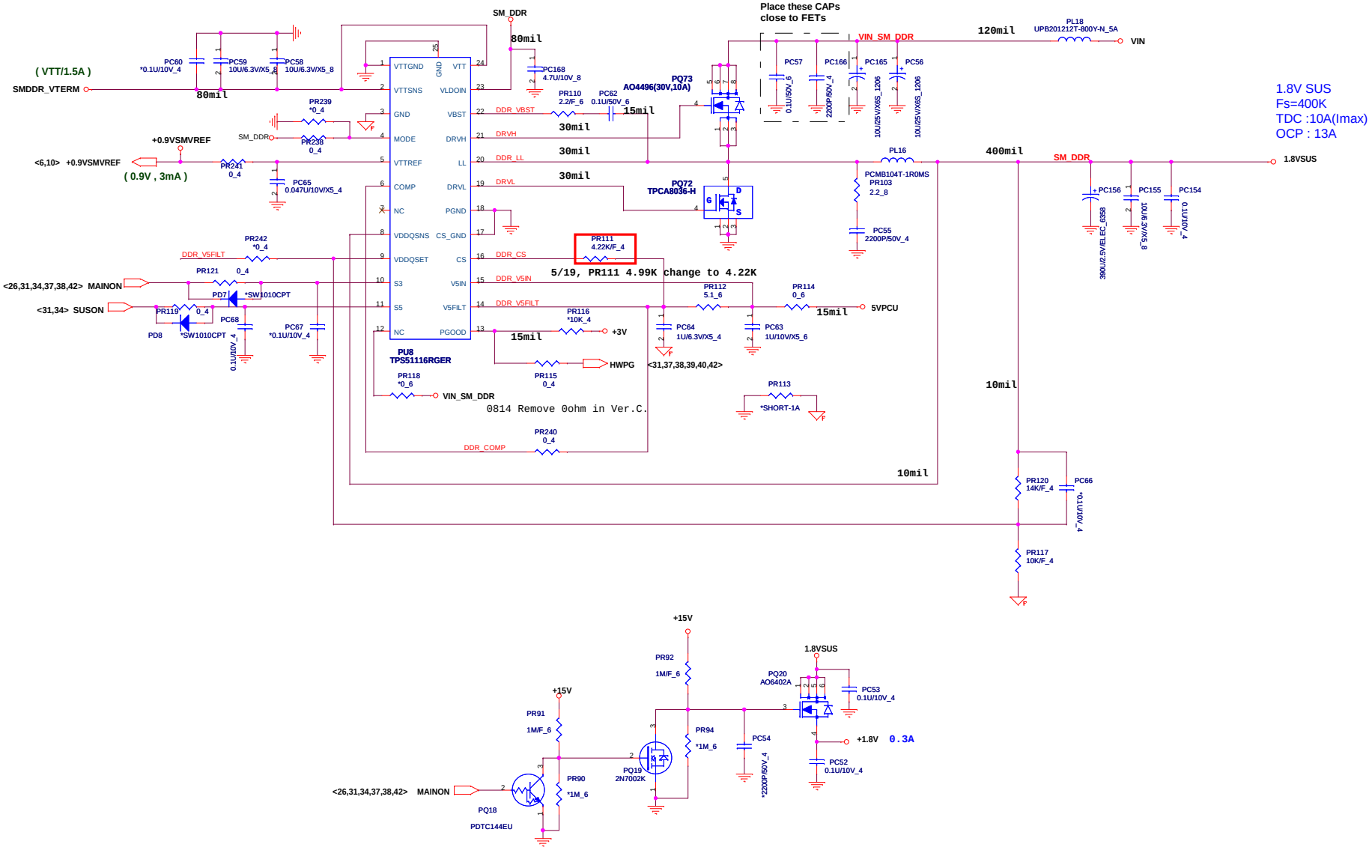
DAREF	
2A	1V
3A	1.5V
4A	2V
5A	2.5V
6A	3V

4 cell overload throtling

Close to EC

AO4413(30V,15A)

PROJECT : EF7/9A Quanta Computer Inc.			
Size: Custom	Document Number: Power-Charger (MAX17005)		Rev: 1A
Date: Thursday, July 09, 2009	Sheet 35 of 45		



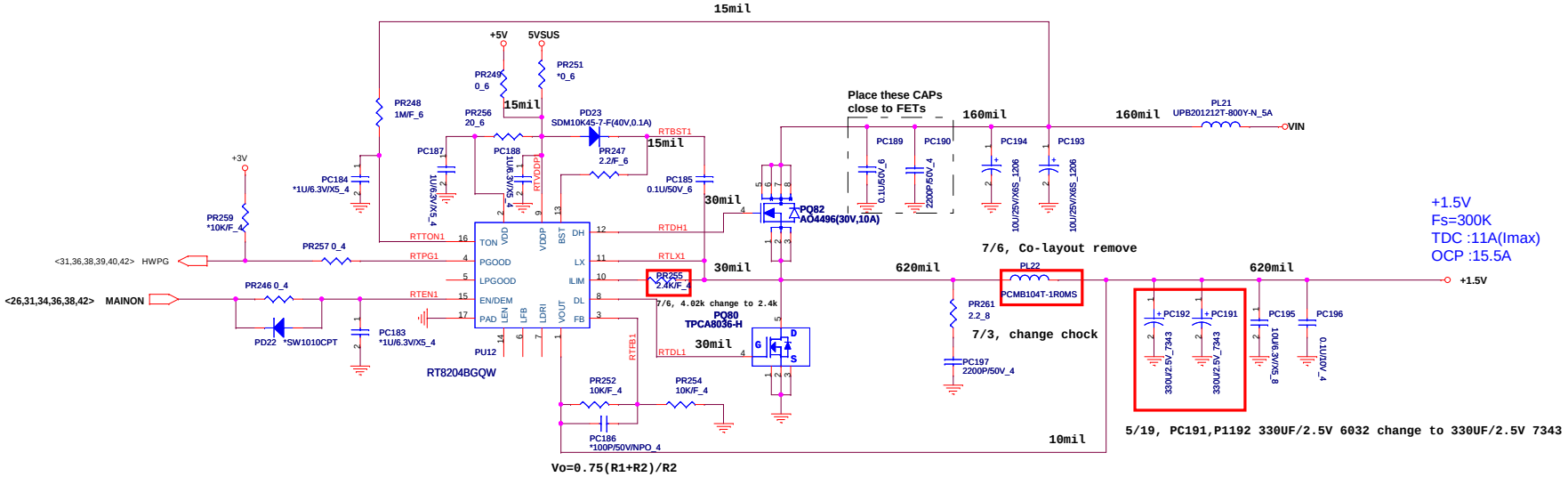
PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SM_DDR2_1.8V (TPS51116REGR)	1A

Date: Thursday, July 09, 2009 Sheet 36 of 45

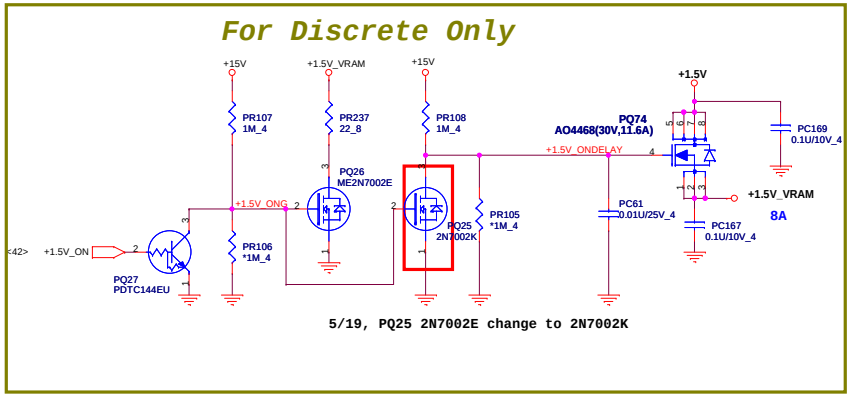
<4,9,19,20,22,30,33,34> +1.5V

<13,17,18,23> +1.5V_VRAM



+1.5V
Fs=300K
TDC :11A(Imax)
OCP :15.5A

For Discrete Only

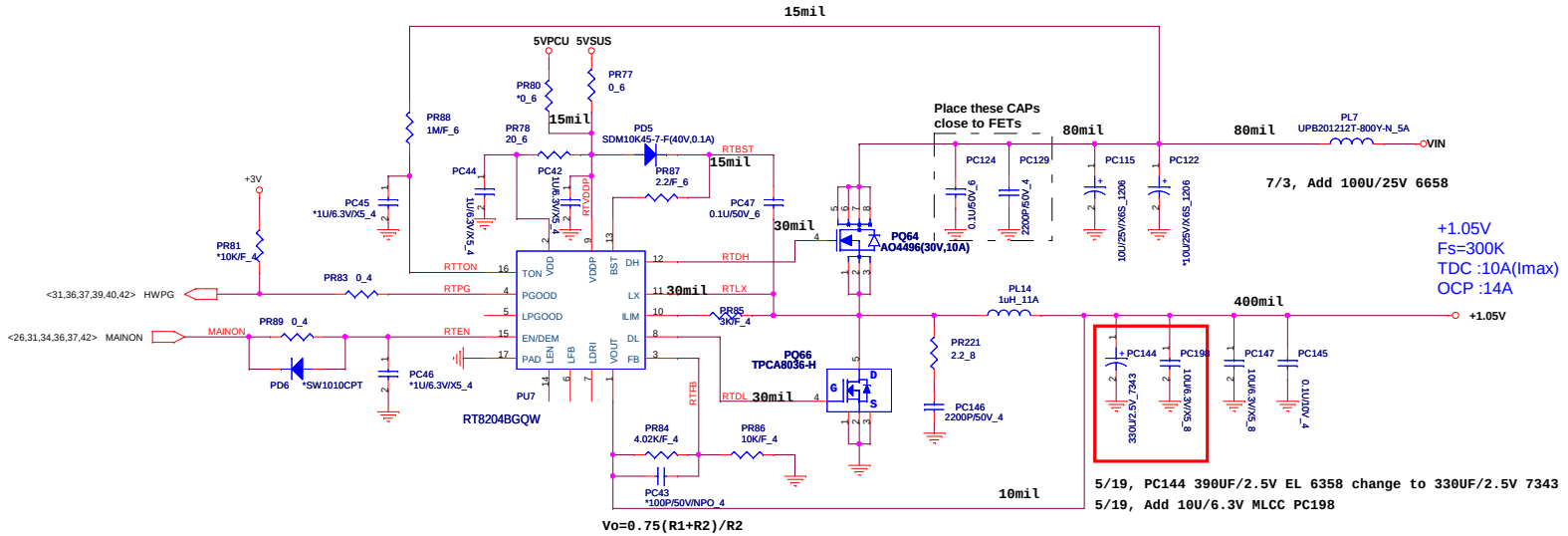


PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA_DDR3_1.5V (RT8204)	1A

Date: Thursday, July 09, 2009 Sheet 37 of 45

<2,3,4,5,6,8,9,12,13,14,19,22,23,34,40> +1.05V



+1.05V
Fs=300K
TDC :10A(Imax)
OCP :14A

5/19, PC144 390UF/2.5V EL 6358 change to 330UF/2.5V 7343
5/19, Add 10U/6.3V MLCC PC198

PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power-1.05V (RT8204)	1A

Date: Thursday, July 09, 2009 Sheet 38 of 45

<19,24,25,30,31,32,33,34,35,41> 3VPCU

5 Volt +/- 5%
Fs=400K
Countinue current:5.5A
OCP minimum 7A

3.3 Volt +/- 5%
Fs=500K
Countinue current:7A
OCP minimum 9A

Place these CAPs close to FETs

Place these CAPs close to FETs

PU9 MAX17020ETJ+

PQ30 AO4496(30V,10A)

PQ31 AO4468(30V,11.6A)

PQ29 AO4496(30V,10A)

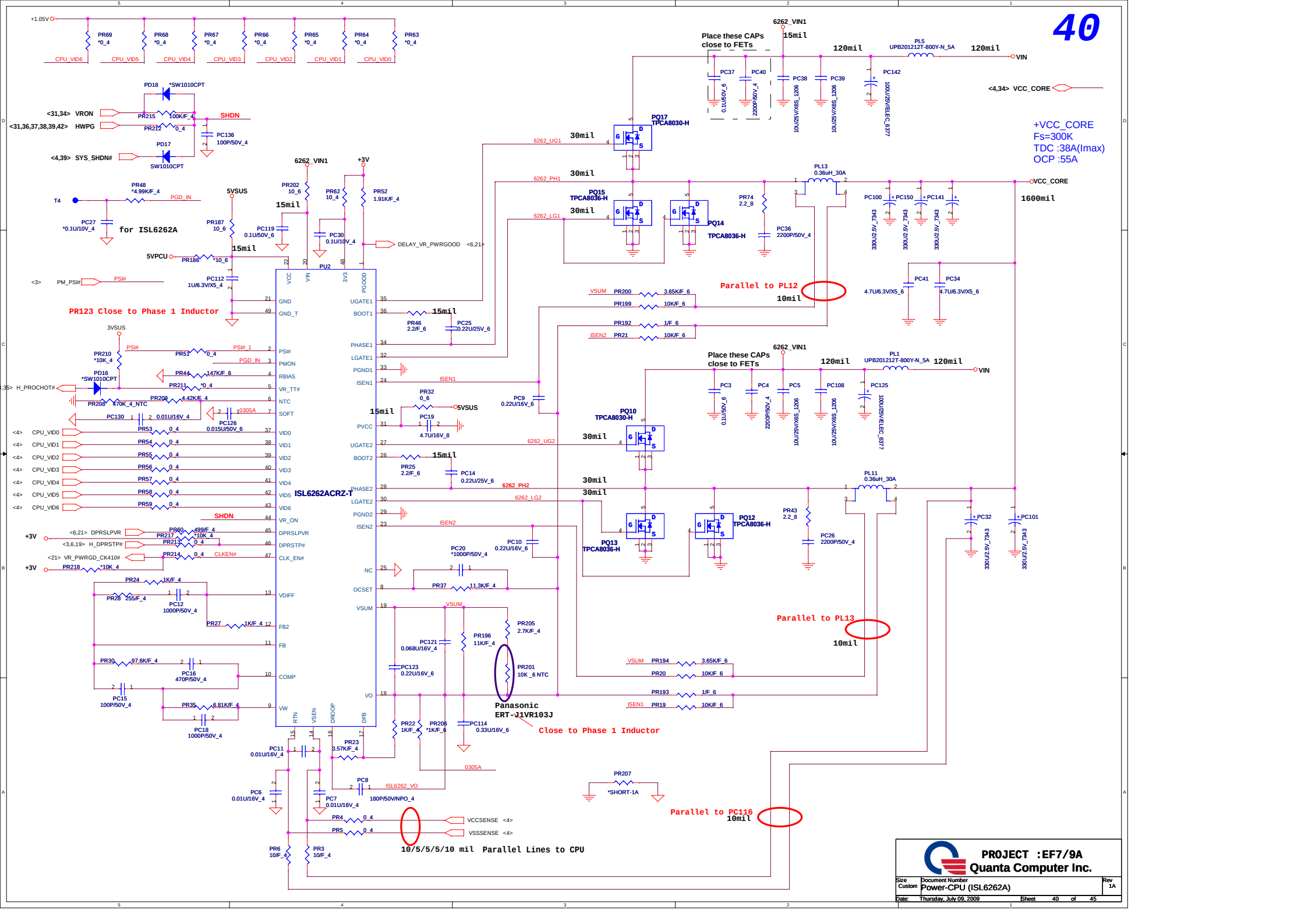
PQ28 AO4468(30V,11.6A)

PD9 BAT54SPT

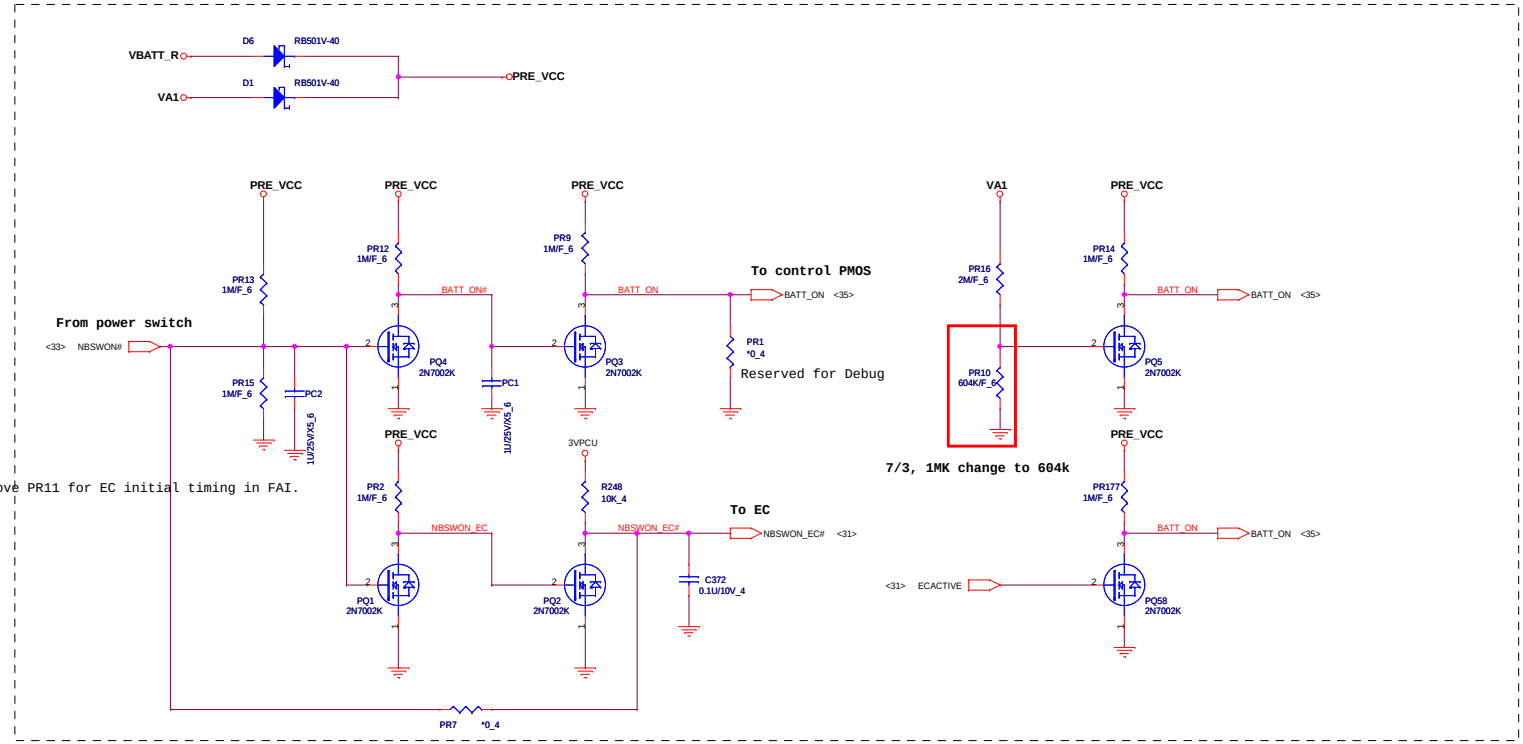
PD10 BAT54SPT

PD11 ZD5.6V

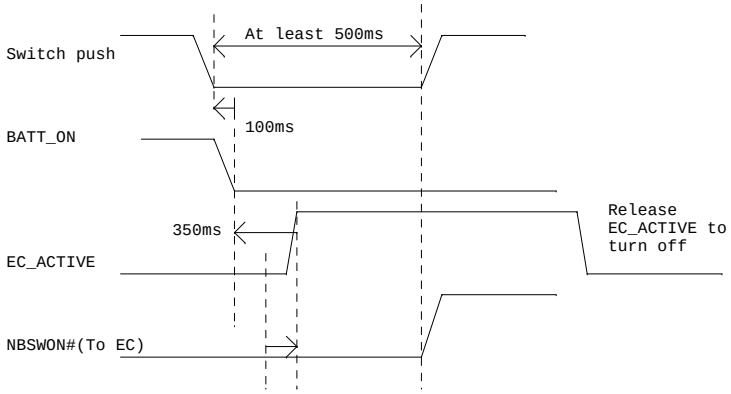
5/19, NETchange to SYS_VIN


+VCC_CORE
Fs=300K
TDC :38A(Imax)
OCP :55A
ISL6262ACRZ-T
PR123 Close to Phase 1 Inductor
for ISL6262A
Place these CAPs close to FETs
Parallel to PL12
Parallel to PL13
Parallel to PC116
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
10/5/5/5/10 mil Parallel Lines to CPU
PROJECT :EF7/9A
Quanta Computer Inc.
Power-CPU (ISL6262A)
Thursday, July 09, 2009

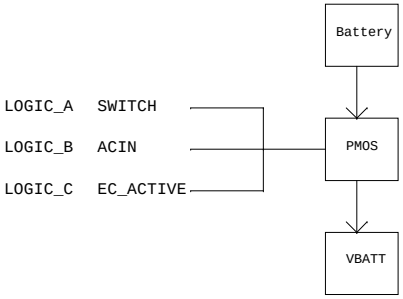
0616 Remove PC2, Mount PC1 for S5-off circuit fine tune in Ver.B
0625 Mount PR1 to disable S5_off function in Ver.B
0826 Remove EC non Active BOM, Add PR217 in FAI



0922 Remove PR11 for EC initial timing in FAI.

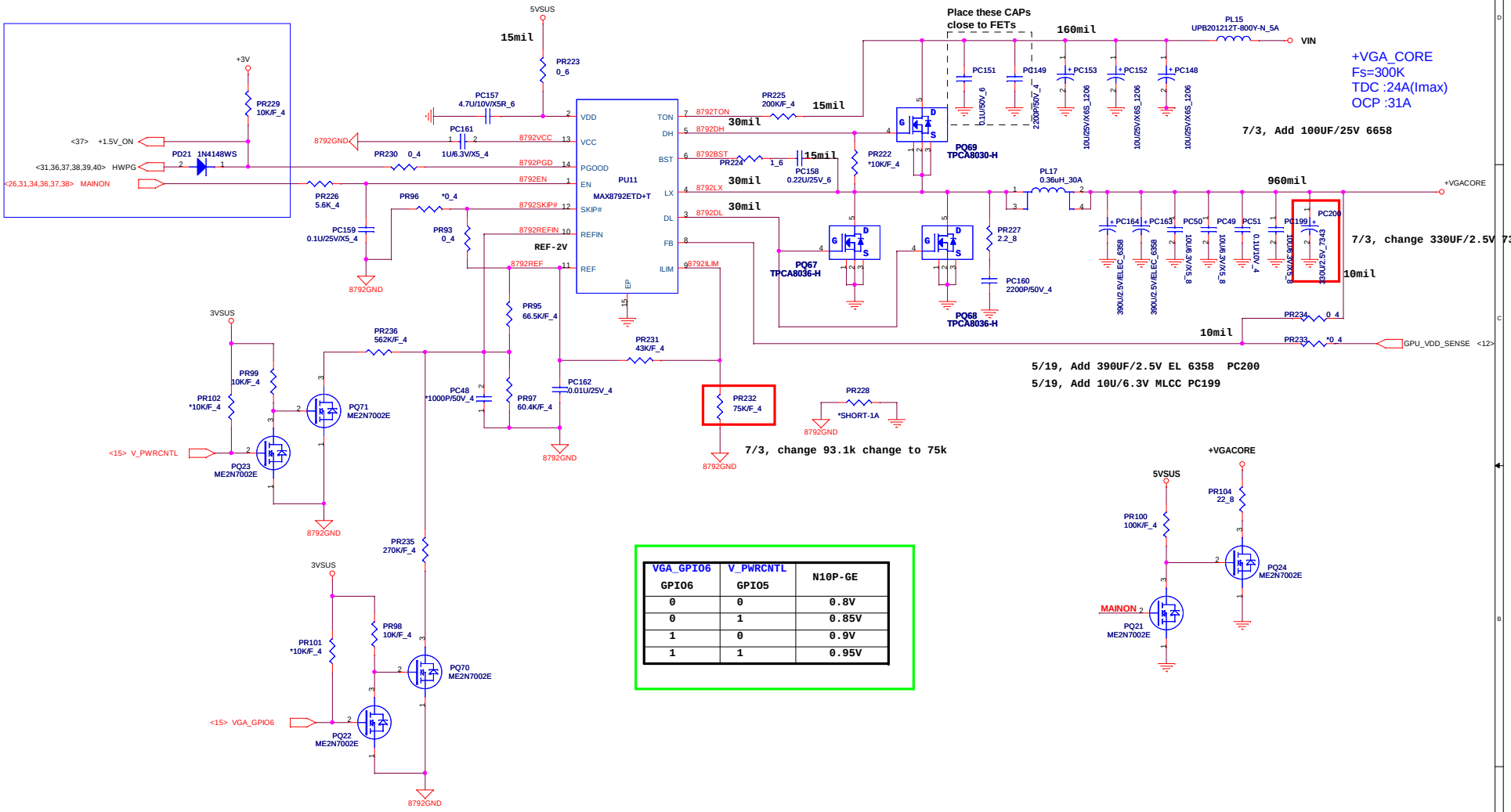


NBSWON# to trigger EC and apply EC_ACTIVE to high.



PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power-S5 Off circuit	1A
Date: Thursday, July 09, 2009	Sheet 41 of 45	



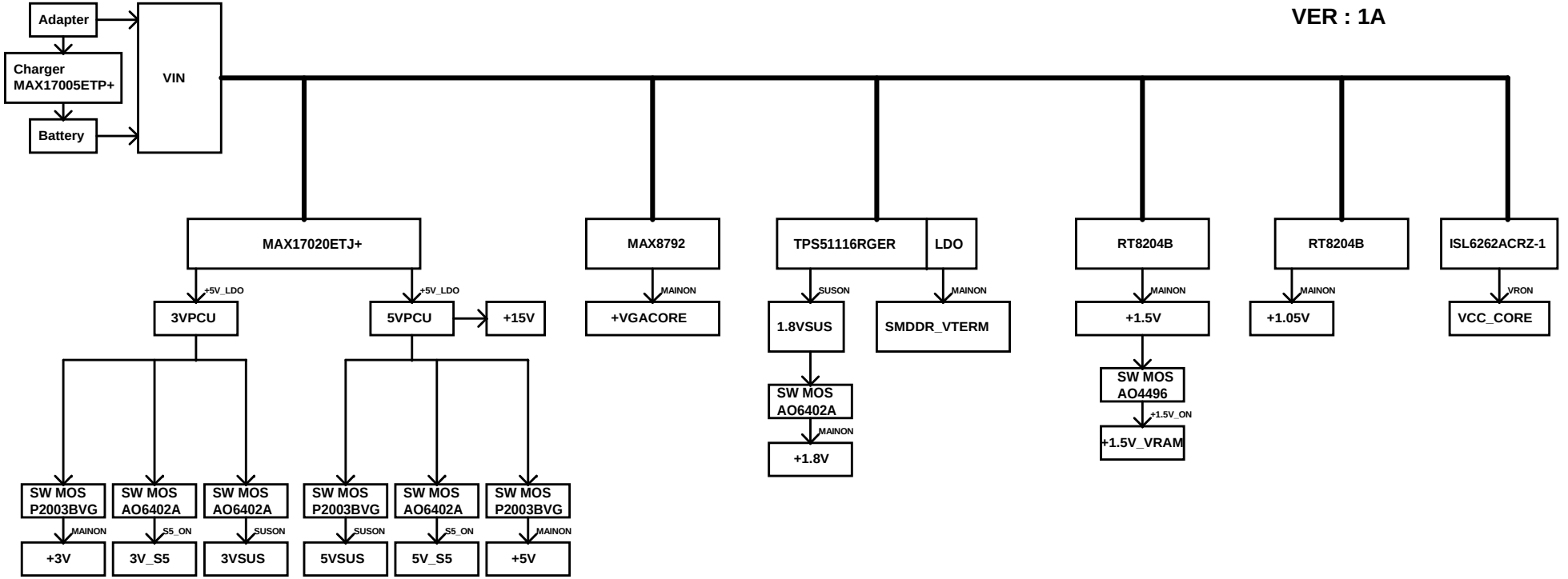
VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V

PROJECT :EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DIS_GFX_VCC (MAX8792)	1A

Date: Thursday, July 09, 2009 Sheet 42 of 45

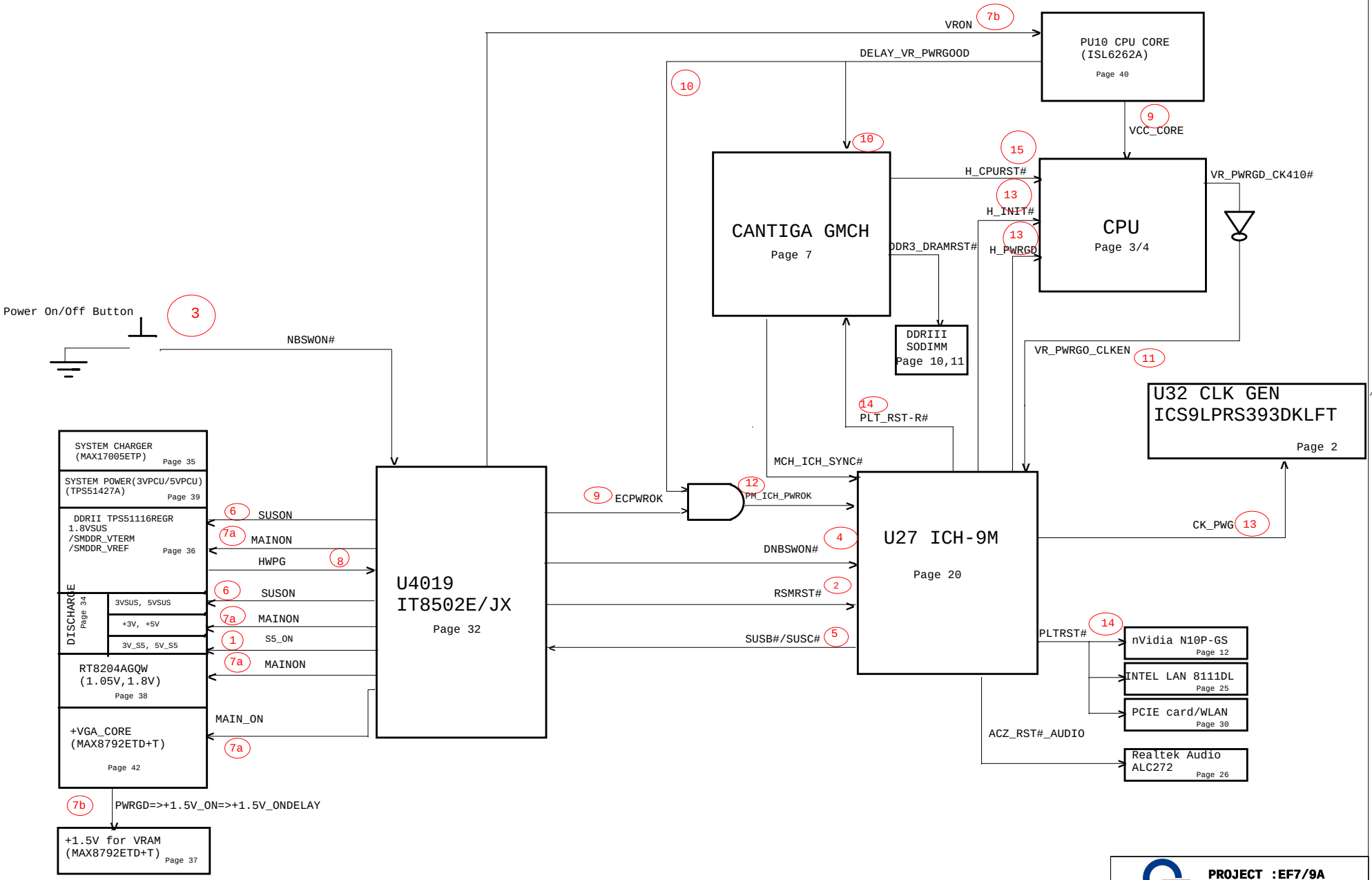
VER : 1A



PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
C	Power Block Diagram	1A

Date: Thursday, July 09, 2009 Sheet 43 of 45



PROJECT : EF7/9A
Quanta Computer Inc.

Size	Document Number	Rev
C	Power Sequence	1A
Date: Thursday, July 09, 2009	Sheet 44 of 45	

Schematics Change History

Version	Date / Author	
C	05/25 '09 Martin Chang	1. Page 13. Pop R113 R117, R381, R377, R80. For channel C implement. Change R94 to 40.2 ohm Add R95, R102 to 40.2 ohm. For nVidia fine tune result. 2. Page 17, 18. Change DDR3 clock termination Resistor to parallel 243 ohm. It's follow the nvidia fine tune result. 3. Page 21. Change Q10 from MOS 2n7002 to BJT. Prenent the +3V power rising too close to SUS-power The wrong power sequence signal may happen. 4. Page 23. Del U31, U32, U33. R452, R455. Add HDMI parallel resistor 100 ohm. Change HDMI connector from AGND to GND. For EMI solution. 5. Page 25. Add R452 1M ohm at tramsformer. For prevent ESD damage. 6. Page 29. Change C685, 686, 687,688 to short pin. If no re-driver. those 4 CAP need short to pass SATA signal. 7. Page 31. Del R177 and short it. For EC direct connect to S5 control circuit. Fix Battery mode only mode issue. 8. Page 33. Add Hole26, 27 for MCH nuts.Remove R204 for double fan contral conflict. 9. Page 36, 37, 38, 39,42. Remove all the power jumper(PJP*)