AN1606

Using the Configurable Logic Cell (CLC) to Interface a PIC16F1509 and WS2811 LED Driver

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INTRODUCTION

The Configurable Logic Cell (CLC) peripheral in the PIC16F1509 device is a powerful way to create custom interfaces that would otherwise be very difficult. One example is the single-wire PWM signal, used by the WS2811 LEDs, well known in LED video display systems. This application note will provide a simple demonstration of a WS2811 LED Strip driver.

The serial protocol used by the WS2811 has three states. State 1 is a logical '0', state 2 is a logical '1' and state 3 is a latch. The data is accepted and used to drive the LED intensity. State 1 is a high output for 500 ns ± 150 ns, followed by 2000 ns ± 150 ns. State 2 is a high output for 120 ns ± 150 ns, followed by a low output for 130 ns ± 150 ns. State 3 is a low output for more than 50 us. There is a fast mode that reduces all of these times (except for state 3) by a factor of two, so that more LEDs can be driven in the same period of time.

Driving an I/O pin in software could create this serial protocol, but this creates two problems:

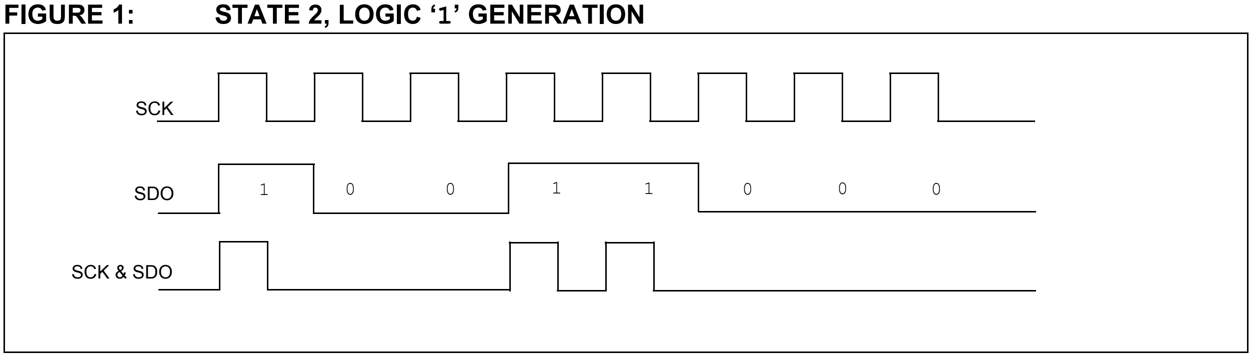
1. 100% of the CPU is used for the entire duration of the LED string update. (15.3 ms for 256 LEDs at the low rate).
2. Very little time is allowed to decide the color for the next LED.

The ideal condition is to create a custom serial communications peripheral to transmit entire bytes in the correct format. For more information see the CLC chapter in the PIC16F1509 data sheet, "*20-Pin Flash, 8-Bit Microcontrollers with nanoWatt XLP Technology*" (DS41609).

CUSTOM PERIPHERAL

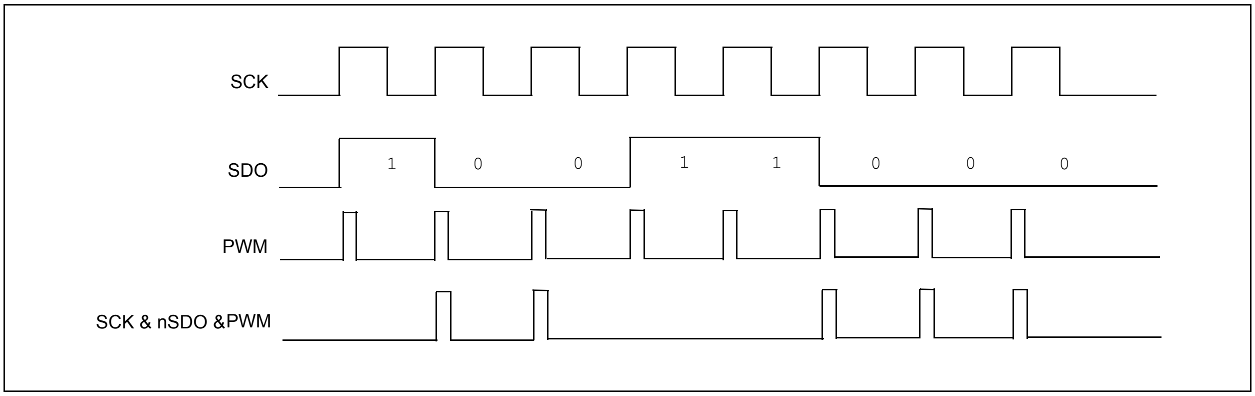
The CLC connects to a variety of peripherals in the PIC16F1509, including the MSSP. Because the MSSP can shift out eight bits at a time, this is the perfect starting point for this new peripheral. Looking at the MSSP output waveforms, Figure 1 illustrates the following:

FIGURE 1: STATE 2, LOGIC '1' GENERATION



If SCK and SDO are simply combined with AND, then the logic '1' (state 2) is covered. In order to create the shorter logic '0' (state 1) pulse, another signal is needed. If PWM is included as a short pulse generator, the following signals are obtained (see Figure 2).

FIGURE 2: STATE 1, LOGIC '0' GENERATION



When both logic '0' and logic '1' are obtained, they need to be 'ORed' together to produce the desired waveform (see Figure 3).

FIGURE 3: LOGIC '0' AND '1' GENERATION

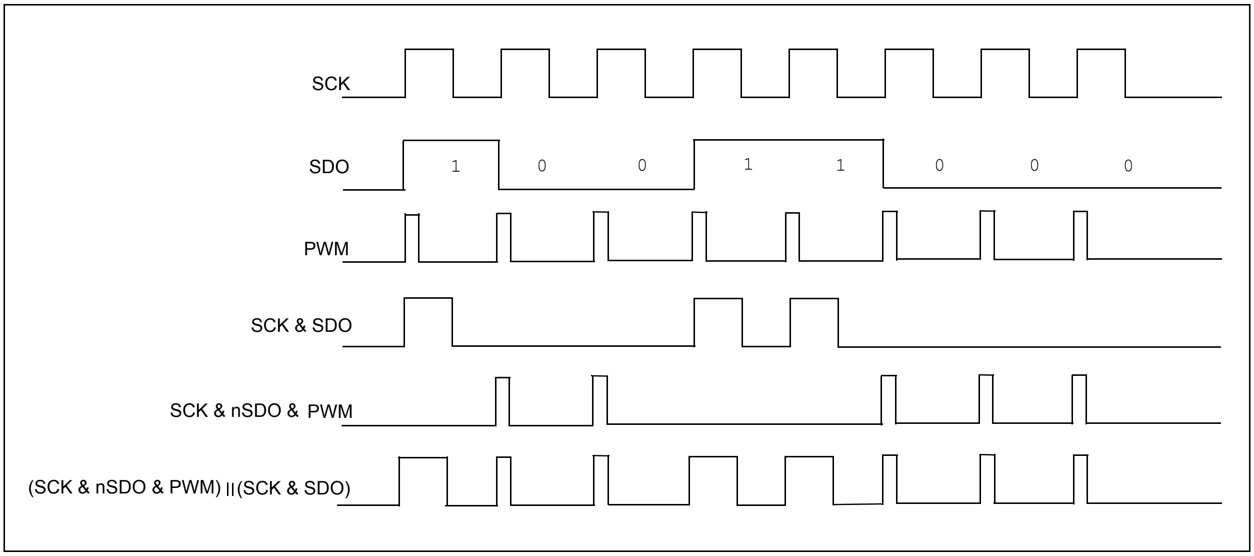
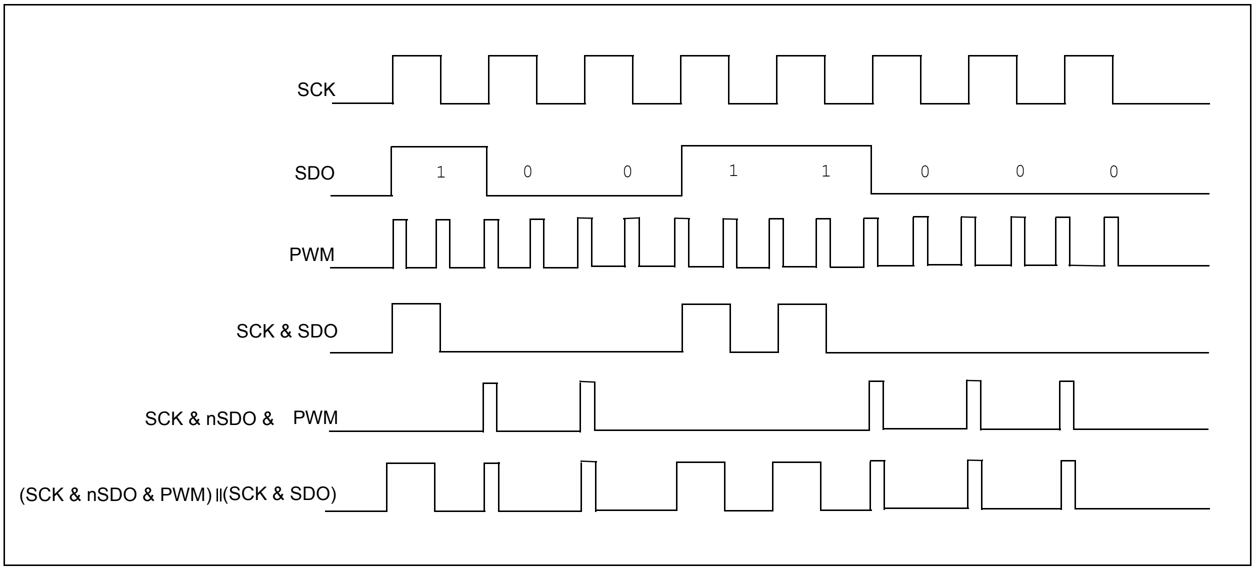


Figure 3 appears to be the correct waveform, but there is still one issue to be resolved. How can the PWM and the MSSP be synchronized so that the rising edge of the PWM pulse matches the start of a data bit? It turns out the MSSP can be set to a baud rate of ½ the TMR2 period, and the PWM period can be one TMR2 period.

Taking into consideration this new information, Figure 2 and Figure 3 above are incorrect. The new combined waveform can be seen in Figure 4:

FIGURE 4: FINAL WAVEFORMS



Note that the only difference is double the number of PWM pulses, but none of them has any effect because they occur while the SCK signal is low.

IMPLEMENTATION

To create the final configuration, the layout of the CLC peripherals in PIC16F1509 has to be studied.

TABLE 1: CLCx DATA INPUT SELECTION

Data Input	lcxd1 D1S	lcxd2 D1S	lcxd3 D1S	lcxd4 D1S	CLC 1	CLC 2	CLC 3	CLC 4
CLCxIN0	000	—	—	100	CLC1IN0	CLC2IN0	CLC3IN0	CLC4IN0
CLCxIN1	001	—	—	101	CLC1IN1	CLC2IN1	CLC3IN1	CLC4IN1
CLCxIN2	010	—	—	110	SYNCC1OUT	SYNCC1OUT	SYNCC1OUT	SYNCC1OUT
CLCxIN3	011	—	—	111	SYNCC2OUT	SYNCC2OUT	SYNCC2OUT	SYNCC2OUT
CLCxIN4	100	000	—	—	FOSC	FOSC	FOSC	FOSC
CLCxIN5	101	001	—	—	TMR0IF	TMR0IF	TMR0IF	TMR0IF
CLCxIN6	110	010	—	—	TMR1IF	TMR1IF	TMR1IF	TMR1IF
CLCxIN7	111	011	—	—	TMR2 = PR2	TMR2 = PR2	TMR2 = PR2	TMR2 = PR2
CLCxIN8	—	100	000	—	lc1_out	lc1_out	lc1_out	lc1_out
CLCxIN9	—	101	001	—	lc2_out	lc2_out	lc2_out	lc2_out
CLCxIN10	—	110	010	—	lc3_out	lc3_out	lc3_out	lc3_out
CLCxIN11	—	111	011	—	lc4_out	lc4_out	lc4_out	lc4_out
CLCxIN12	—	—	100	000	NCO1OUT	LFINTOSC	TX (EUSART)	SCK (MSSP)
CLCxIN13	—	—	101	001	HFINTOSC	ADFRC	LFINTOSC	SDO (MSSP)
CLCxIN14	—	—	110	010	PWM3OUT	PWM1OUT	PWM2OUT	PWM1OUT
CLCxIN15	—	—	111	011	PWM4OUT	PWM2OUT	PWM3OUT	PWM4OUT

The MSSP outputs are both available in CLC4. Note that PWM1 and PWM 4 are also on CLC4. However, they are all in the same logic group and only two of the four signals can be used in each group. The CLCs can be combined using LCx_OUT signals in a different logic group. The selection will be to combine PWM1OUT in CLC2 and send it to CLC4 via LC2_OUT. Therefore, the logic will be built in CLC4 as:

LC4_OUT = (SDO & SCK) || (!SDO & SCK & LC2_OUT)

and the logic in CLC2 will be:

LC2_OUT = PWM1OUT

The final configuration requires that the TMR2 be activated with the correct bit time:

T2CON = 0x04

PR2 = (bit time/2) * (FOSC/4)

If the slow bit time of 2.5 us and the 16 MHz internal oscillator are run, then:

PR2 = 5.

The PWM duty cycle must be configured for the '0' pulse width.

PWM1DCH = pr2/3.

The slow bit rate requires that the value be 2 for 16 MHz.

PWM1DCH = 2.

Configuring SSP1CON1 to use the TMR2 Period/2 as the clock results in:

SSP1CON1 = 0x23.

To allow the pin to output the signal, TRISC4 must be cleared to 0.

CONCLUSION

The CLC easily allows multiple peripherals in the PIC16F1509 to work together to produce a new composite peripheral that is suitable for the user's application. With a dozen lines of code, the MSSP is now a custom WS2811 driver. Please refer to the Example A for more information.

APPENDIX A:

EXAMPLE 1: SOURCE CODE

```
void WS2811_Init(void)
{
    // Initialize PIC16(L)F1509 CLC2, CLC4, Timer2, and MSSP
    // for WS2811 signal transmission protocol
    // Loading SSP1BUF register sends that data byte out the RC4/CLC4 pin

    // PWM1 routed straight through CLC2

         CLC2GLS0  = 0x20;
         CLC2GLS1  = 0x00;
         CLC2GLS2  = 0x00;
         CLC2GLS3  = 0x00;
         CLC2SEL0  = 0x00;
         CLC2SEL1  = 0x06;
         CLC2POL   = 0x0E;
         CLC2CON   = 0x82;

    //  (SPI SDO & SPI CLK) || (nSPI SDO & SPI CLK & PWM1)
    //  PWM1 comes through CLC2
         CLC4GLS0  = 0x44;
         CLC4GLS1  = 0x10;
         CLC4GLS2  = 0x80;
         CLC4GLS3  = 0x20;
         CLC4SEL0  = 0x50;
         CLC4SEL1  = 0x05;
         CLC4POL   = 0x01;
         CLC4CON   = 0xC0;

    // Adjust Timer2 period for desired baud rate
    // One bit period is two Timer2 periods

         T2CON     = 0x04;
         PR2       = 5;

    // Adjust PWM1 duty cycle for desired "0" data-bit duty cycle
    // '1' data-bit duty cycle is automatically 50%

         PWM1CON   = 0xE0;
         PWM1DCH   = 2;
         PWM1DCL   = 0;

    // MSSP configured for SPI master with Timer2_Period/2 clock

         SSP1CON1  = 0x23;

    // Output on RC4/CLC4

         TRISC    &= 0xEF;
}
```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