X552 SCHEMATIC R1.0
DGPU=Nvidia N15V GM

BLOCK DIAGRAM

YSTEM PAGE REF.

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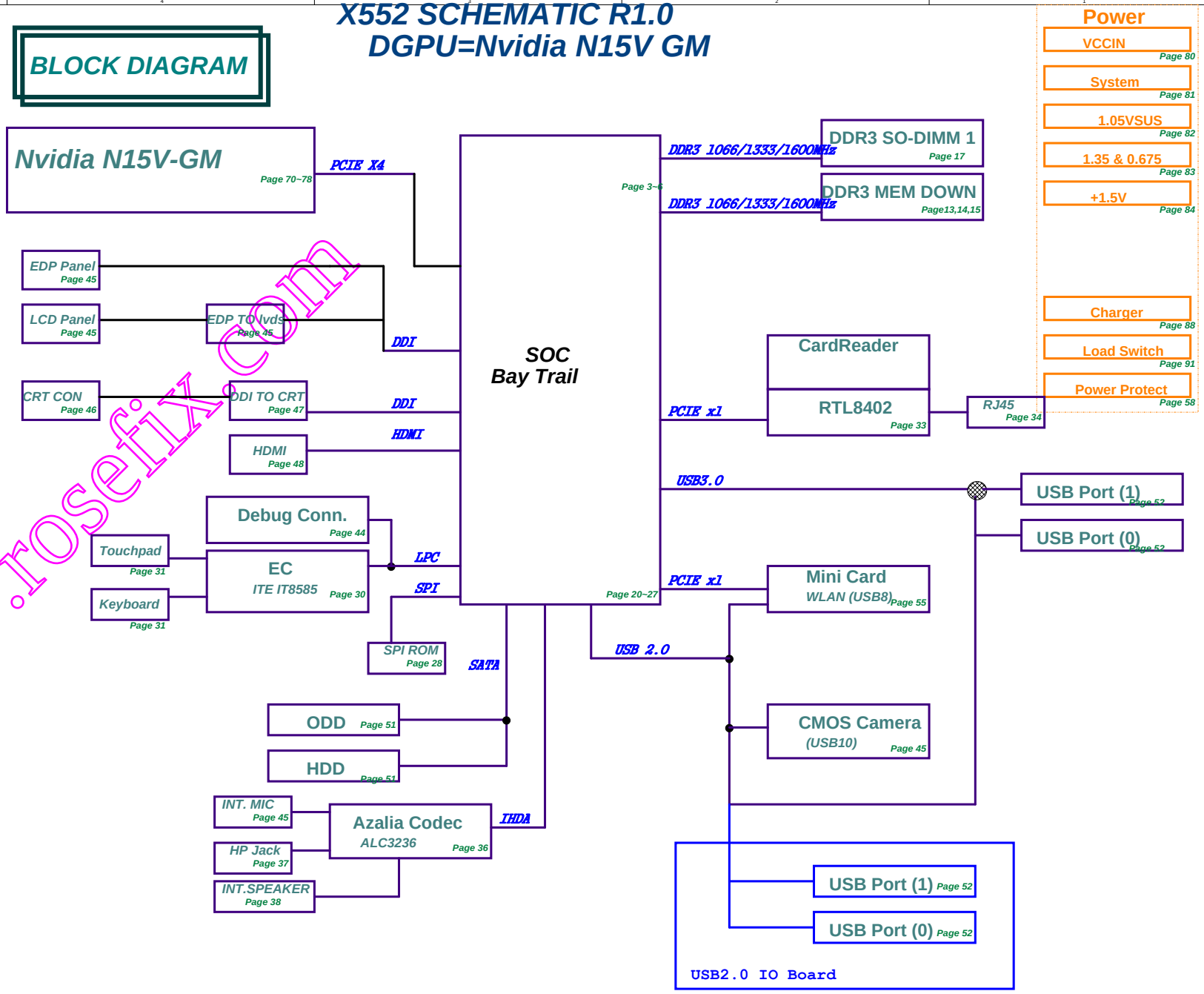


<Variant Name>

ASUSTeK COMPUTER INC. NB4

Title : Block Diagram

Engineer: RD1_EE3

Size	Project Name	Rev
C	X552MD	R1.3

Date: Friday, March 14, 2014 Sheet 1 of 98

EE PART

SKU Table

	CPU	DIMM	USB3/USB2	TV	3G	VRAM	BT	HDMI	2D/3D	TPM	PCH	DRAM	VRAM
Option	/CPU	/DIMM	/USB3; /USB2	/TV	/3G	/VRAM	/BT	/HDMI	/2D; /3D	/TPM	/PCH		
60NB06P0-MB1110	N3530	4G_KINGSTON	-	-	-	-	-	-	-	-		4G HYNIX	V2G-MICRON
60NB06P0-MB1500	N2830	4G_SAMSUNG	-	-	-	-	-	-	-	-		4G MICRON	V2G-HYNIX
60NB06P0-MB1600	N2830	4G_HYX	-	-	-	-	-	-	-	-		4G HYNIX	V1G-SAMSUNG
60NB06P0-MB1700	N2930	2G_HYN	-	-	-	-	-	-	-	-		0M	V1G-HYNIX

Title	<Title>		
Size: D	Document Number: <Doc>		Rev: <RevCode>
Date: Friday, March 14, 2014	Sheet 1 of 1		

SOC (Bay Trail) GPIO Setting

SOC_GPIO	Use As	Signal Name	Int & Ext Pull-up/down	Power
GPIO_S0_SC[00]	GPI	EXT_SCI#	INT PD	+1.8VS
GPIO_S0_SC[01]	Native	NC	INT PD	+1.8VS
GPIO_S0_SC[02]	Native	SATA_LED#	EXT PU	+1.8VS
GPIO_S0_SC[03]	Native	CLKREQ_WLAN#	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[04]	Native	CLKREQ1# (NC)	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[05]	Native	CLKREQ2# (NC)	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[06]	Native	CLKREQ_GLAN#	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[07]				
GPIO_S0_SC[08]	Native	ACZ_RST#	INT PD	+1.5VS
GPIO_S0_SC[09]	Native	ACZ_SYNC	INT PD	+1.5VS
GPIO_S0_SC[10]	Native	ACZ_BCLK	INT PD	+1.5VS
GPIO_S0_SC[11]	Native	ACZ_SDOUT	INT PD	+1.5VS
GPIO_S0_SC[12]	Native	ACZ_SDIN0_AUD	INT PD	+1.5VS
GPIO_S0_SC[13]	Native	NC	INT PD	+1.5VS
GPIO_S0_SC[14]	Native	NC	INT PD	+1.5VS
GPIO_S0_SC[15]	Native	NC	INT PD	+1.5VS
GPIO_S0_SC[16]	Native	NC	INT PD	+1.8VS
GPIO_S0_SC[24:17]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[25]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[26]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[27]	Native	NC	INT PD	+1.8VS
GPIO_S0_SC[31:28]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[32]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[33]	Native	SD3_CLK	INT PD & EXT PU	+1.8VS/+3VS
GPIO_S0_SC[37:34]	Native	SD3_D[3:0]	INT PU & EXT PU	+1.8VS/+3VS
GPIO_S0_SC[38]	Native	SD3_CD#	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[39]	Native	SD3_CMD	INT PU & EXT PU	+1.8VS/+3VS
GPIO_S0_SC[40]	Native	SD3_1P8_EN	INT PD	+1.8VS
GPIO_S0_SC[41]	Native	SD3_PWR_EN#	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[45:42]	Native	LPC_AD[3:0]	INT PU	+3VS
GPIO_S0_SC[46]	Native	LPC_FRAME#	INT PU	+3VS
GPIO_S0_SC[47]	Native	L_CLKOUT0	INT PD	+3VS
GPIO_S0_SC[48]	Native	L_CLKOUT1	INT PD	+3VS
GPIO_S0_SC[49]	Native	PM_CLKRUN#_R	INT PU & EXT PU	+3VS
GPIO_S0_SC[50]	Native	INT_SERIRQ_SOC_R	INT PU	+1.8VS
GPIO_S0_SC[51]	Native	SMB_DATA_SOC	INT PU & EXT PU(NC)	+1.8VS
GPIO_S0_SC[52]	Native	SMB_CLK_SOC	INT PU & EXT PU(NC)	+1.8VS
GPIO_S0_SC[53]	Native	SMB_ALERT#_SOC	INT PU & EXT PU	+1.8VS
GPIO_S0_SC[54]	GPI	EC_SMB_INT2#		
GPIO_S0_SC[55]	GPO	WWAN_ON#		+1.8VS
GPIO_S0_SC[56]	GPI	STRAP_A16_SWAP	EXT PU	+1.8VS
GPIO_S0_SC[57]	GPO	UART_TXD_DBG		+1.8VS
GPIO_S0_SC[58]	GPI	MEMID0		+1.8VS
GPIO_S0_SC[59]	GPI	MEMID1		+1.8VS
GPIO_S0_SC[60]	GPI	MEMID2		+1.8VS
GPIO_S0_SC[61]	GPI	UART_RXD_DBG		+1.8VS
GPIO_S0_SC[62]	Native	NC		+1.8VS
GPIO_S0_SC[63]	GPI	I2S_2_FRM	EXT PU	+1.8VS
GPIO_S0_SC[64]	Native	NC		+1.8VS
GPIO_S0_SC[65]	GPI	I2S_2_TXD	EXT PU	+1.8VS
GPIO_S0_SC[66]	GPI	PCB_ID0	EXT PD	+1.8VS
GPIO_S0_SC[67]	GPI	PCB_ID1	EXT PD	+1.8VS
GPIO_S0_SC[68]	Native	NC		+1.8VS
GPIO_S0_SC[69]	Native	NC		+1.8VS
GPIO_S0_SC[77:70]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[83:78]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[84]	Native	EC_SMB_DAT2		+1.8VS
GPIO_S0_SC[85]	Native	EC_SMB_CLK2		+1.8VS
GPIO_S0_SC[86]	Native	EC_SMB_DAT3		+1.8VS
GPIO_S0_SC[87]	Native	EC_SMB_CLK3		+1.8VS
GPIO_S0_SC[88]	GPO	WLAN_LED	INT PU	+1.8VS
GPIO_S0_SC[89]	GPO	BT_LED	INT PU	+1.8VS
GPIO_S0_SC[90]	Native	NC	INT PU	+1.8VS
GPIO_S0_SC[91]	GPIO	SD3_WP	INT PU & EXT PU(NC)	+1.8VS
GPIO_S0_SC[92]	GPO	WLAN_ON#		+1.8VS
GPIO_S0_SC[93]	GPO	BT_ON#		+1.8VS
GPIO_S0_SC[94]	Native	NC		+1.8VS
GPIO_S0_SC[95]	Native	NC		+1.8VS
GPIO_S0_SC[:10196]	Native	NC		+1.8VS

SOC (Bay Trail) GPIO Setting

SOC_GPIO	Use As	Signal Name	Int & Ext Pull-up/down	Power
GPIO_S5[0]	GPI	EC_WAKE_SCI_SOC		+1.8VSUS
GPIO_S5[3:1]	Native	NC	INT PU	+1.8VS
GPIO_S5[4]	Native	NC		+1.8VS
GPIO_S5[6:5]	Native	NC		+1.8VS
GPIO_S5[7]	GPI	EXT_SMI#_SOC		+1.8VSUS
GPIO_S5[8]	Native	NC		+1.8VS
GPIO_S5[9]	Native	NFC_RST#_R		+1.8VS
GPIO_S5[10]	Native	NFC_INT_R		+1.8VS
GPIO_S5[11]	Native	ME_SUSPWRDNACK		+1.8VS
GPIO_S5[12]	Native	NC		+1.8VS
GPIO_S5[13]	Native	SLP_S0IX#_18		+1.8VSUS
GPIO_S5[14]	Native	SLP_LAN#	EXT PU(NC)	+1.8VS
GPIO_S5[15]	Native	PCIE_WAKE#	INT PU & EXT PU	+1.8VSUS
GPIO_S5[16]	Native	PM_PWRBTN#_18	INT PU	+1.8VSUS
GPIO_S5[17]	Native	NC		+1.8VS
GPIO_S5[18]	Native	NC		+1.8VS
GPIO_S5[19]	Native	USB_OC_0#	INT PU & EXT PU	+1.8VSUS
GPIO_S5[20]	Native	USB_OC_0#	INT PU & EXT PU	+1.8VSUS
GPIO_S5[21]	GPI	SPI_SO_SPI	INT PU	+1.8VS
GPIO_S5[30:22]	GPIO	XDP_GPIO_DFX[8:0]		+1.8VS
GPIO_S5[31]	GPI	EC_SMB_INT3#		+1.8VSUS
GPIO_S5[43:32]	Native	NC		+1.8VS

EC IT8585E

EC GPIO	Use As	Signal Name
GPA0	O	PWR_LED#
GPA1	OD	CHG_LED#
GPA2	OD	CHG_FULL_LED#
GPA3	OD	AOAC_WLANLED# R1.1_0220-17
GPA4	OD	NC R1.1_0220-17
GPA5	ALT	FAN_PWM
GPA6	ALT	GPA6 (NC)
GPA7	O	OS_LED#
GPB0	ALT	AC_IN_OC#
GPB1	I	LID_SW#
GPB2	OD	THRO_CPU#
GPB3	ALT	PWR_SW#
GPB4	O	PS_ON
GPB5	OD	EC_SMB_INT2# R1.1_0220-17
GPB6	OD	EC_SMB_INT3# R1.1_0220-17
GPC0	I	AOAC_WLANON# R1.1_0220-17
GPC1	ALT	SMB1_CLK
GPC2	ALT	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	NC
GPC5	I	PM_SUSC#
GPC6	ALT	BAT1_IN_OC#
GPC7	I	NC
GPD0	I	NC
GPD1	OD	CAP_LED#
GPD2	ALT	BUF_PLT_RST#
GPD3	OD	EXT_SCI#
GPD4	OD	EXT_SMI#
GPD5	O	OP_SD#
GPD6	ALT	FAN0_TACH
GPD7	O	LCD_BACKOFF#
GPE0	O	SUSB_EC#
GPE1	O	SUSC_EC#
GPE2	O	1.35V_ON
GPE3	O	EC_WAKE_SCI
GPE4	O	NC
GPE5	I	PM_SUSB#
GPE6	O	ME_AC_PRESENT
GPE7	I	NC
GPF0	O	5VSUS_ON
GPF1	O	3VSUS_ON
GPF2	ALT	SMB0_CLK
GPF3	ALT	SMB0_DAT
GPF4	ALT	TP_CLK
GPF5	ALT	TP_DAT
GPF6	ALT	EC_SMB_CLK2
GPF7	ALT	EC_SMB_DAT2
GPG0	O	NC
GPG1	O	NC
GPG2	I	PWRLIMIT#_EC
GPG3	O	EC_SCE#_PCH
GPG4	I	EC_SI_PCH
GPG5	O	EC_SO_PCH
GPG6	O	USB30_5VBUS R1.1_0208-21
GPG7	O	EC_SCK_PCH
GPH0	ALT	PM_CLKRUN#
GPH1	OD	EC_SMB_CLK3
GPH2	O	EC_SMB_DAT3
GPH3	O	PM_RSMRST#
GPH4	O	NC
GPH5	O	PM_PWROK
GPH6	O	NC
GPI0	I	NC
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	CORE_PWRGD
GPI4	I	NC
GPI5	I	ME_SusPwrDnAck_EC
GPI6	I	A/D_Max_Power
GPI7	ALT	USB_CHARGE_ON# R1.1_0208-21
GPJ0	I	NC
GPJ1	O	NC
GPJ2	O	PL_REF_EC
GPJ3	O	NC
GPJ4	O	NC
GPJ5	O	DRAMRST_EC R1.3_0606-11
GPJ6	OD	NC
GPJ7	OD	NC
GPM0	IO	LPC_AD0
GPM1	IO	LPC_AD1
GPM2	IO	LPC_AD2
GPM3	IO	LPC_AD3
GPM4	I	CLK_KBCPCI_PCH
GPM5	I	LPC_FRAME#
GPM6	OD	INT_SERIRQ

PCI Express

PCIE 0	
PCIE 1	WLAN
PCIE 2	
PCIE 3	GLAN

R1.1_0208-14

USB Port

USB 0	USB 3.0 Port
USB 1	USB 2.0 Port
USB 2	USB 2.0 Port
USB 3	Camera
USB 4	
USB 5	
USB 6	
USB 7	
USB 8	
USB 9	
USB 10	
USB 11	
USB 12	
USB 13	

SATA Port

SATA 0	HDD
SATA 1	HDD (2nd)

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	**SM-Bus Address**	
DIGI POTEN(ISL90727WIE627Z-TK)	1011100x (5C)	
DIGI POTEN(ISL90728WIE627Z-TK)	1111100x (7C)	
EC Master (SMB1)		
SM-Bus Device	**SM-Bus Address**	
Thermal IC(G781)	1001100x (98)	R1.0
Thermal IC(NCT7717U)	1001000x (90)	R2.0

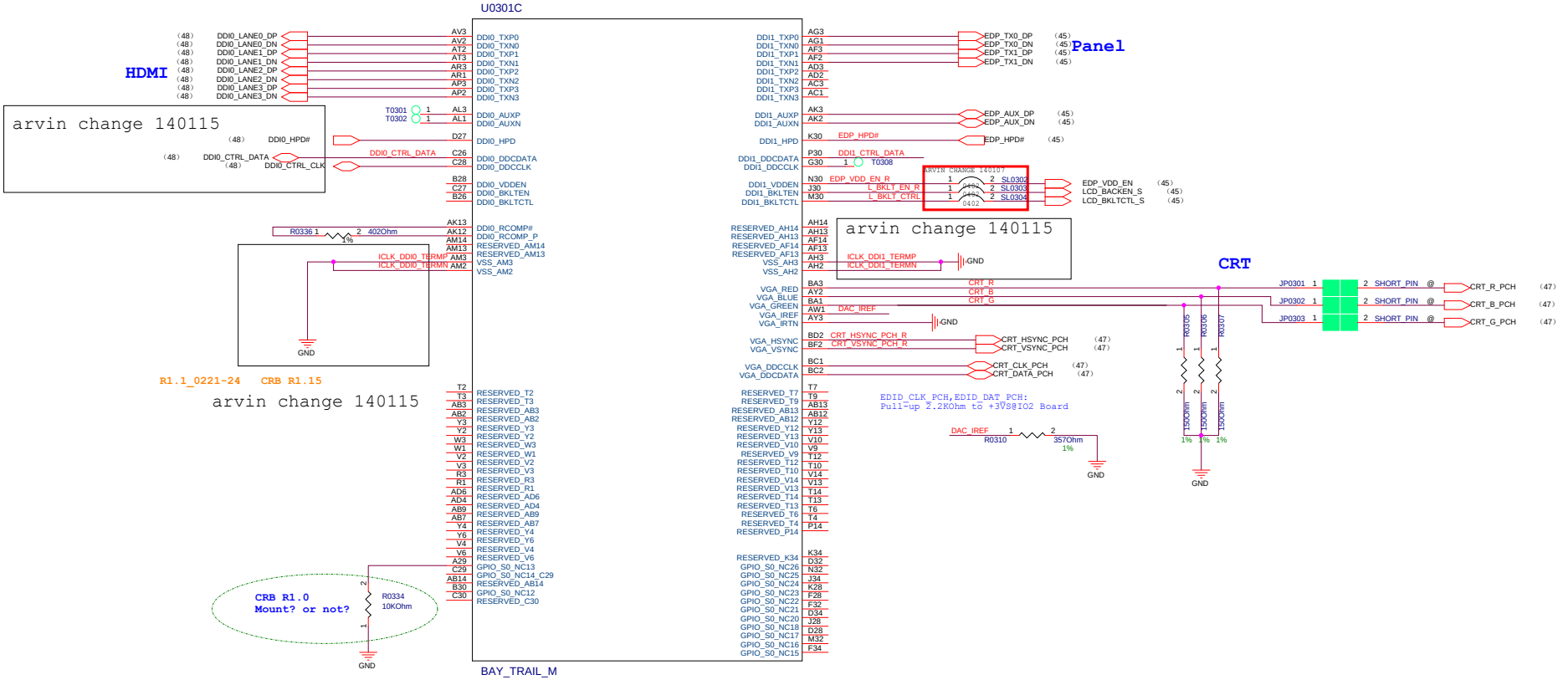
ASUSTeK COMPUTER INC.

Title : System Setting

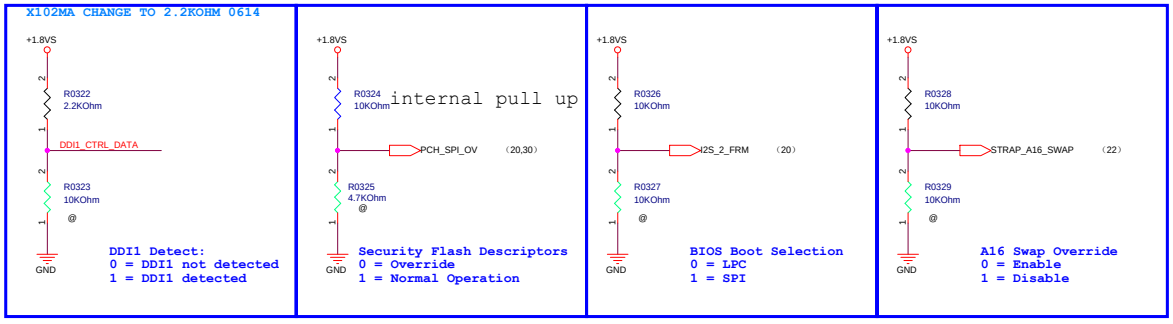
Engineer: RD1_EE2-1

Size: D | Project Name: X102MA_Bay Trail-M | Rev: 1.0

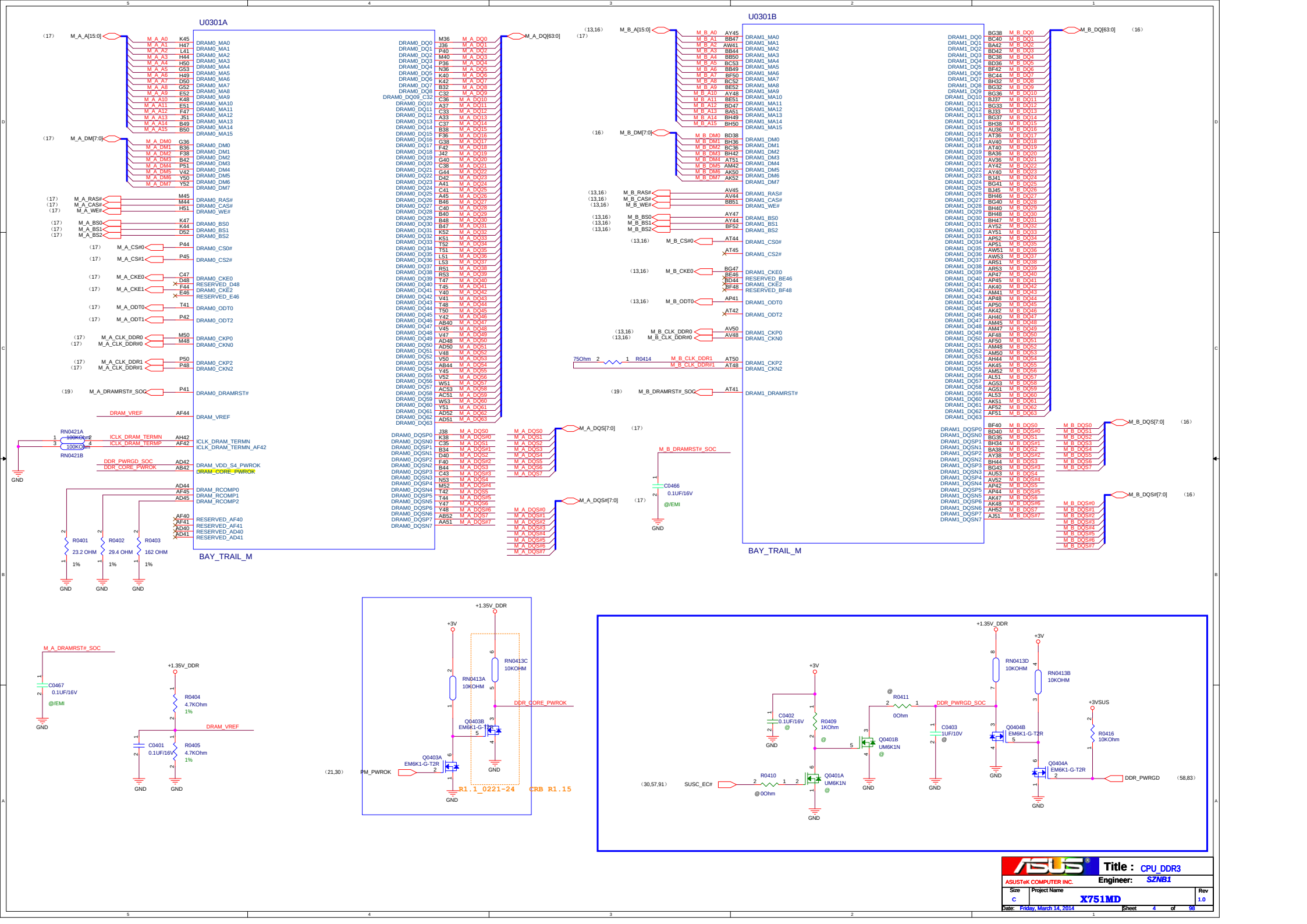
Date: Friday, March 14, 2014 | Sheet 2 of 58



Straps



ASUSTeK COMPUTER INC.	Title : CPU_DDI,VGA	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 3 of 98	


U0301A
BAY_TRAIL_M
U0301B
BAY_TRAIL_M
M_A_A[15:0]
M_A_DM[7:0]
M_A_DQ[63:0]
M_A_DQS[7:0]
M_A_DQS#[7:0]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_BS0
M_A_BS1
M_A_BS2
M_A_CS#0
M_A_CS#1
M_A_CKE0
M_A_CKE1
M_A_ODT0
M_A_ODT1
M_A_CLK_DDR0
M_A_CLK_DDR#0
M_A_CLK_DDR1
M_A_CLK_DDR#1
M_A_DRAMRST#_SOC
DRAM_VREF
ICLK_DRAM_TERMN
ICLK_DRAM_TERMP
DDR_PWRGD_SOC
DDR_CORE_PWROK
DRAM_RCOMP0
DRAM_RCOMP1
DRAM_RCOMP2
RESERVED_AF40
RESERVED_AF41
RESERVED_AD40
RESERVED_AD41
M_B_A[15:0]
M_B_DM[7:0]
M_B_DQ[63:0]
M_B_DQS[7:0]
M_B_DQS#[7:0]
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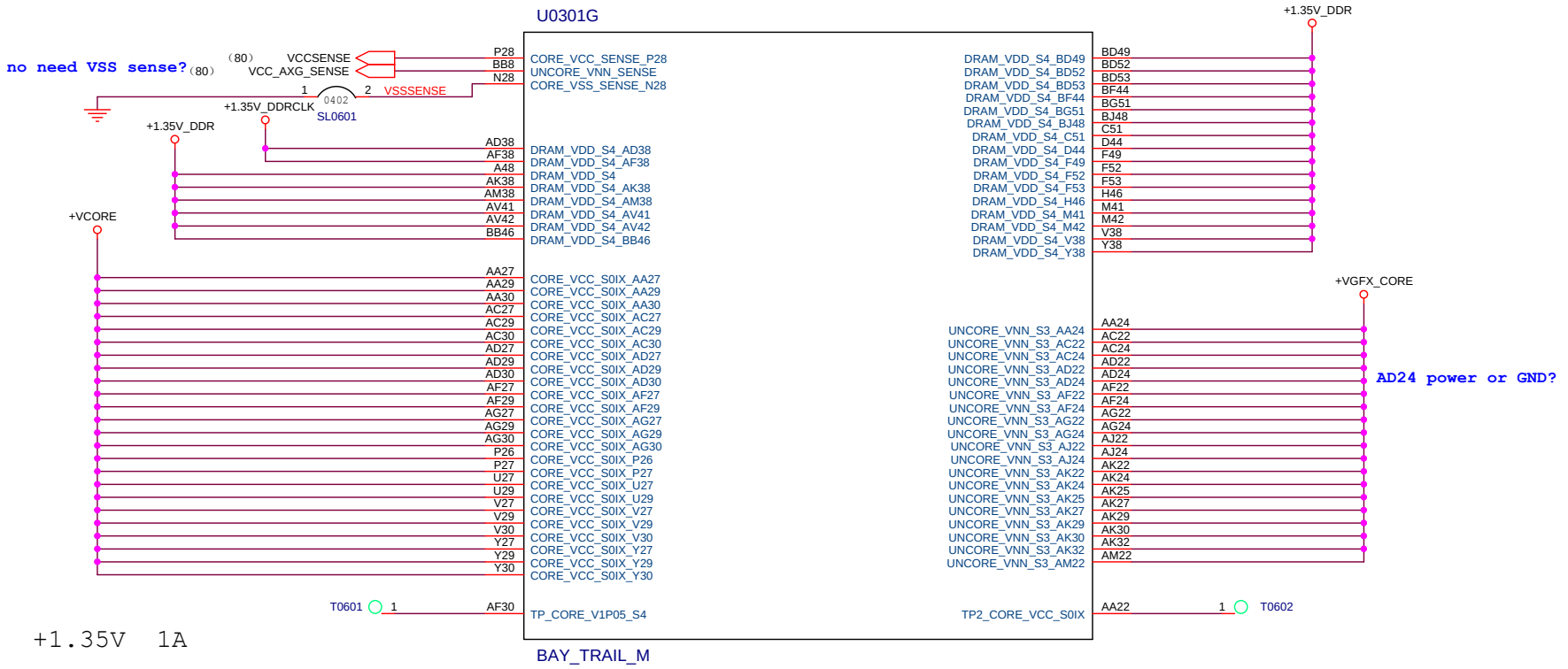
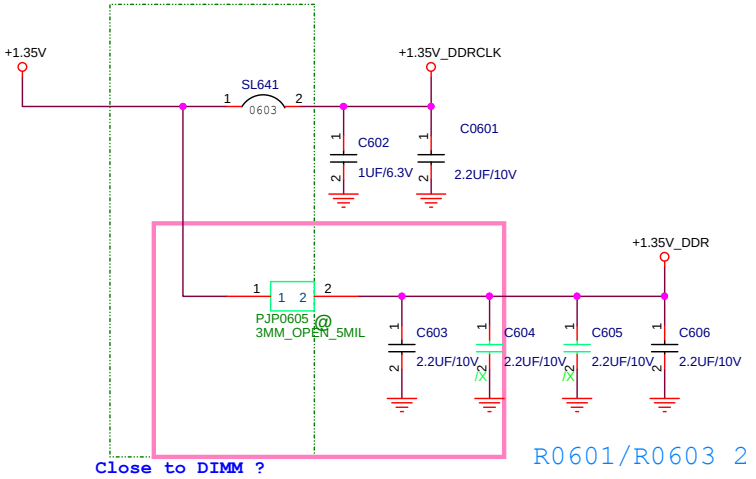
M_B_CAS#
M_B_WE#
M_B_BS0
M_B_BS1
M_B_BS2
M_B_CS#0
M_B_CKE0
M_B_ODT0
M_B_CLK_DDR0
M_B_CLK_DDR#0
M_B_CLK_DDR1
M_B_CLK_DDR#1
M_B_DRAMRST#_SOC
RESERVED_BE46
RESERVED_BF48
RN0421A
RN0421B
100KOhm
R0401
R0402
R0403
23.2 OHM
29.4 OHM
162 OHM
1%
R0414
750Ohm
C0466
0.1UF/16V
@/EMI
GND
C0467
C0401
C0402
C0403
1UF/10V
R0404
R0405
4.7KOhm
R0409
1KOhm
R0410
0Ohm
R0411
RN0413A
RN0413B
RN0413C
RN0413D
10KOHM
Q0403A
Q0403B
EM6K1-G-T2R
Q0401A
Q0401B
UM6K1N
Q0404A
Q0404B
R0416
10KOhm
+3V
+3VSUS
+1.35V_DDR
PM_PWROK
SUSC_EC#
DDR_PWRGD
R1.1_0221-24
CRB R1.15
ASUSTeK COMPUTER INC.
Title : CPU_DDR3
Engineer: SZNB1
Size C
Project Name X751MD
Rev 1.0
Date: Friday, March 14, 2014
Sheet 4 of 98

ASUSTeK COMPUTER INC.	Title : CPU_CFG,RSVD,GND	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 5 of 98	

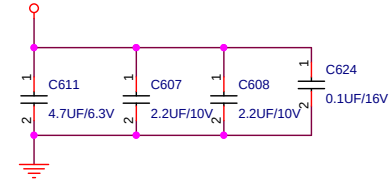


+1.35V 1A



R0601/R0603 2 OHM 1% 換为PJP0605 0610

+VCORE +VCORE 15A



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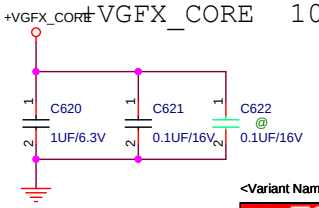


<Variant Name>

ASUSTeK COMPUTER INC.	Title : CPU_PWR	
	Engineer: RD1_EE2-1	
Size: B	Project Name: X102MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 6 of 98	

Title : XDP Debug Board

ASUSTeK COMPUTER INC. NB3

Engineer: RD1_EE2-1

Size	Project Name	Rev
B	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 7 of 98

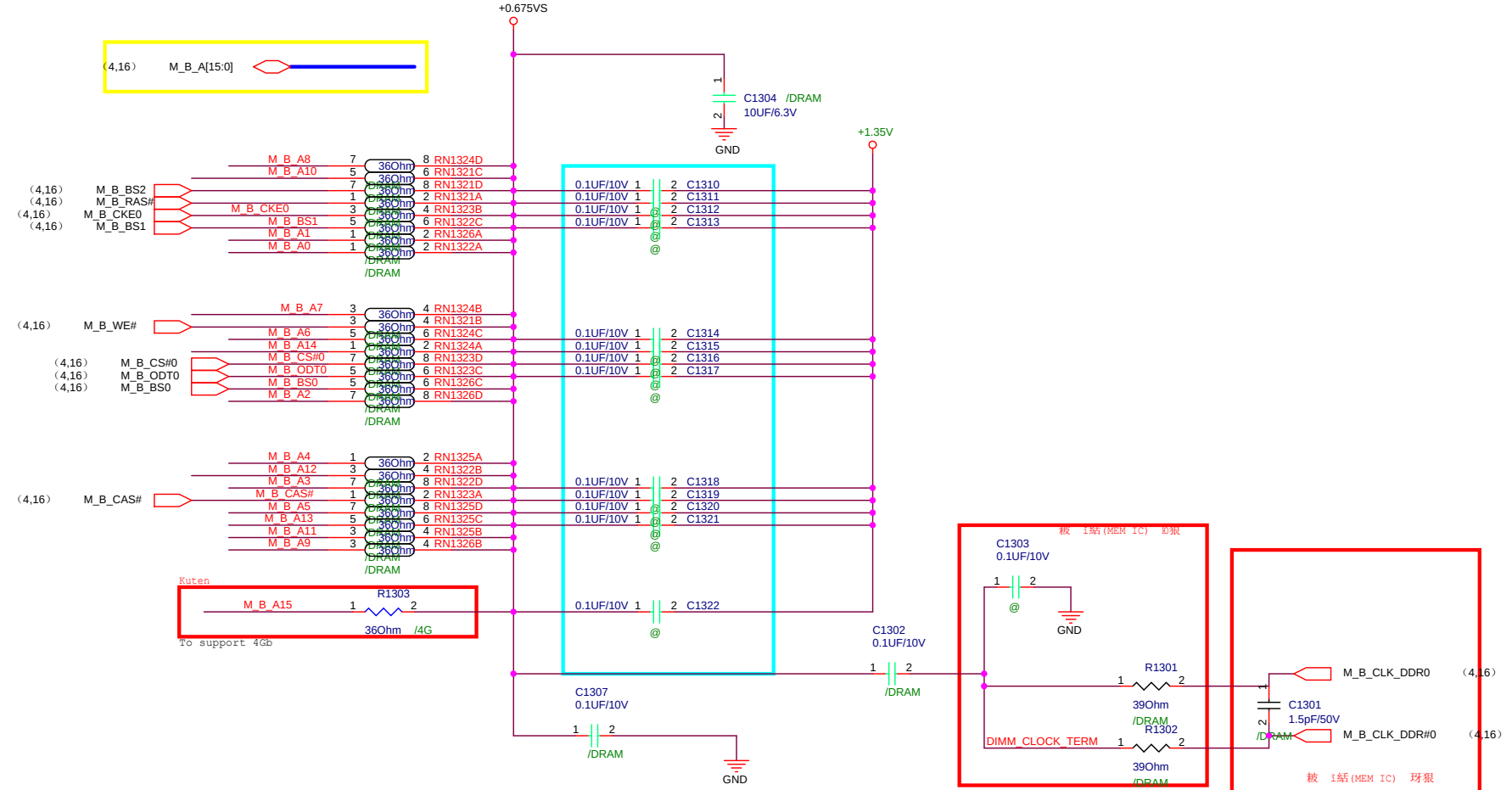
ASUSTeK COMPUTER INC.	Title : NB_****	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 8 of 98	

ASUSTeK COMPUTER INC.	Title : NB_****	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 9 of 98	

ASUSTeK COMPUTER INC.	Title : NB_****	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 10 of 98	

ASUSTeK COMPUTER INC.	Title : NB_****	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 11 of 98	

ASUSTeK COMPUTER INC.	Title : NB_****	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 12 of 98	



ASUSTeK COMPUTER INC.	Title : DDR3_TERMINATION_A		
	Engineer: RD1_EE2-1		
Size: B	Project Name: S200T_Bay Trail-M		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 13 of 98		

ASUSTeK COMPUTER INC. NB3	Title : SBU_DGPU_NB_****_R1.0		
	Engineer: SZ/EE		
Size: C	Project Name: X552MD		Rev: R2.0
Date: Friday, March 14, 2014	Sheet 14 of 98		

Title : DDR3_ON-BOARD_B(2)

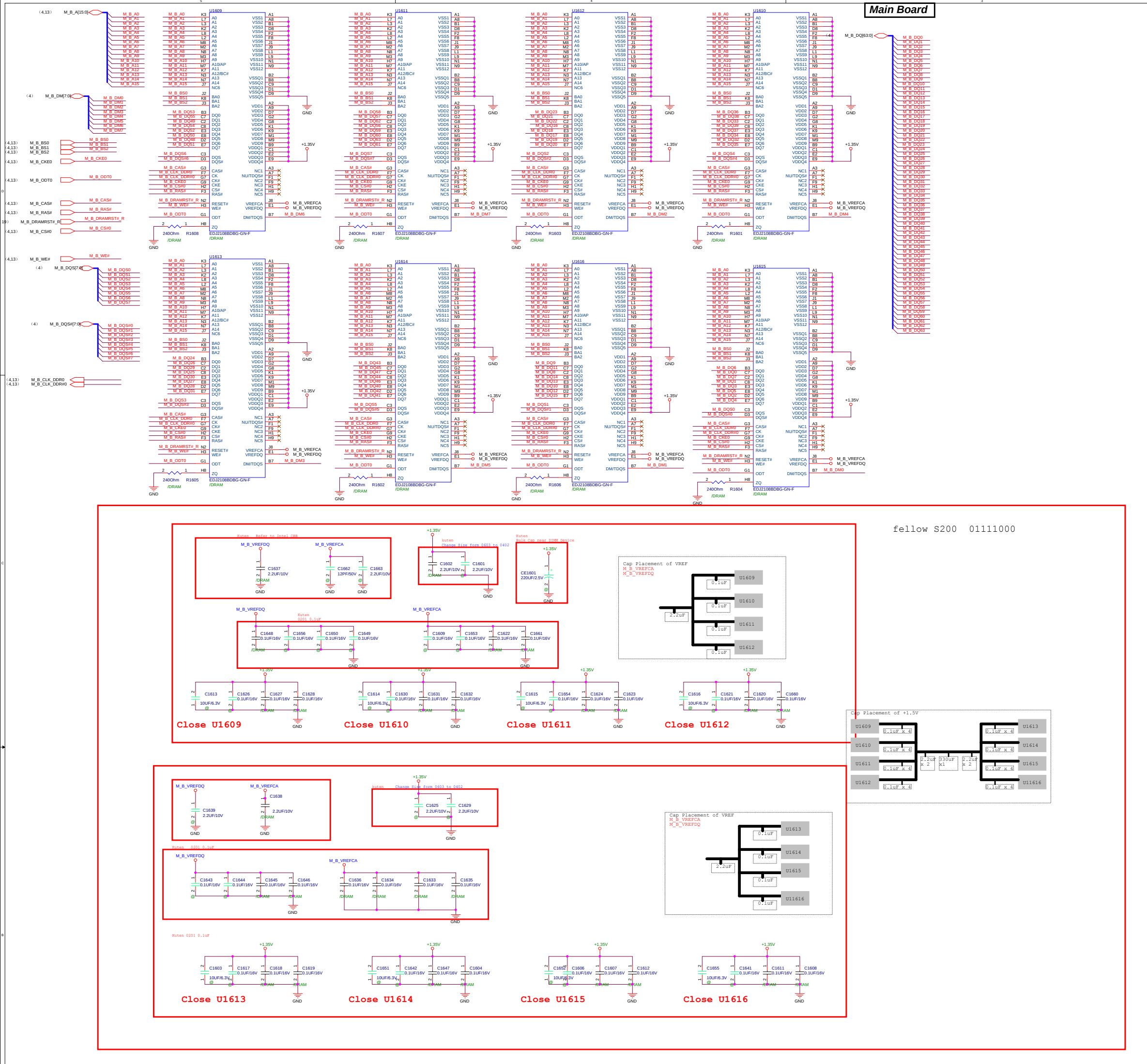
ASUSTeK COMPUTER INC.

Engineer: RD1_EE2-1

Size	Project Name	Rev
C	S200T_Bay Trail-M	1.0

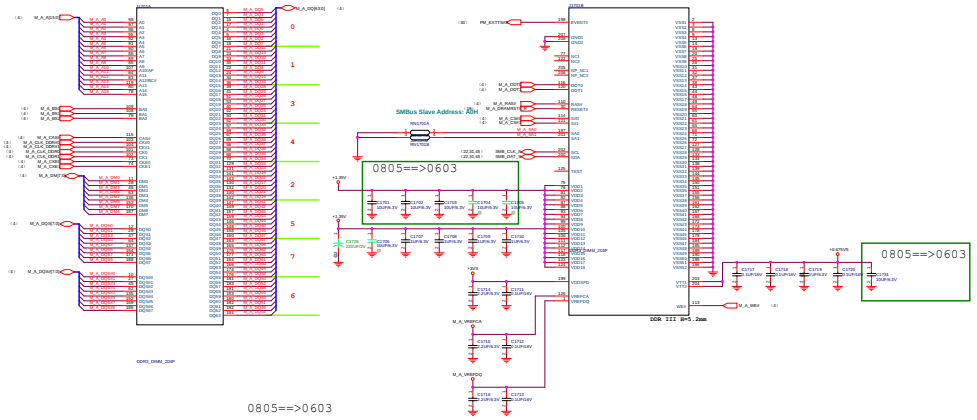
Date: Friday, March 14, 2014 Sheet 15 of 98

Main Board



ASUSTeK COMPUTER INC. NB1	Title : DDR3-On Board Memory	Engineer: SZ/EE
Size: E	Project Name: X751MD	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 16 of 98	

SODIMM CHA-DIMM0



Title :	SB_DIM_DDR3SO-DIMM0(B)_R1.4		
Engineer:	SIZE		
Size	Project Name		Rev
B	X751LD		1.4
Date: Friday, March 14, 2014		Sheet 37 of 38	

Title : DIM_CA/DQ Voltage

ASUSTeK COMPUTER INC.

Engineer: RD1_EE2-1

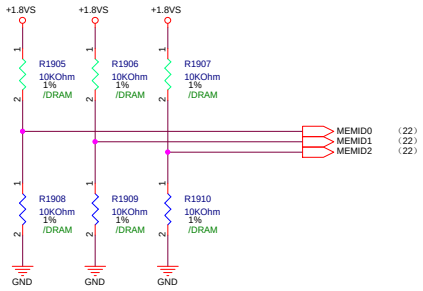
Size	Project Name	Rev
C	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 18 of 98

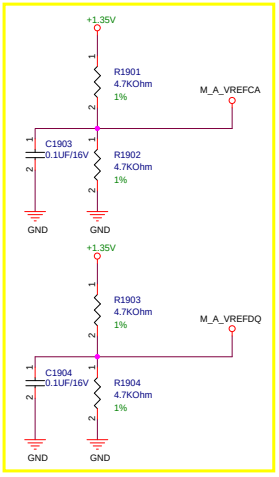
Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details

DDR3 Vref

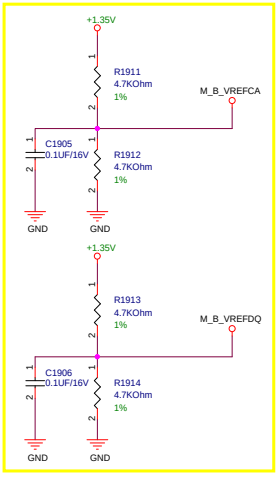
Intel Document Number: 400755

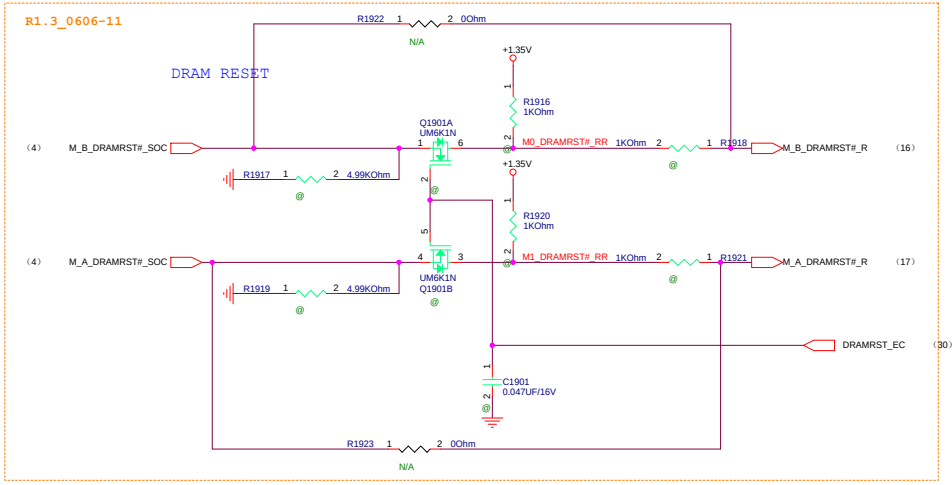


MEM ID			
MEMID2 (GPIO23)	MEMID1 (GPIO17)	MEMID0 (GPIO16)	NOTE
0	0	0	OG
0	0	1	03006-00011400 MICRON/MT41K512M8RH-125:E 4GB
0	1	0	03006-00011600 HYNIX/H5TC4G83AFR-PBA 4GB
0	1	1	
0	0	0	
0	0	1	
0	1	0	
0	1	1	

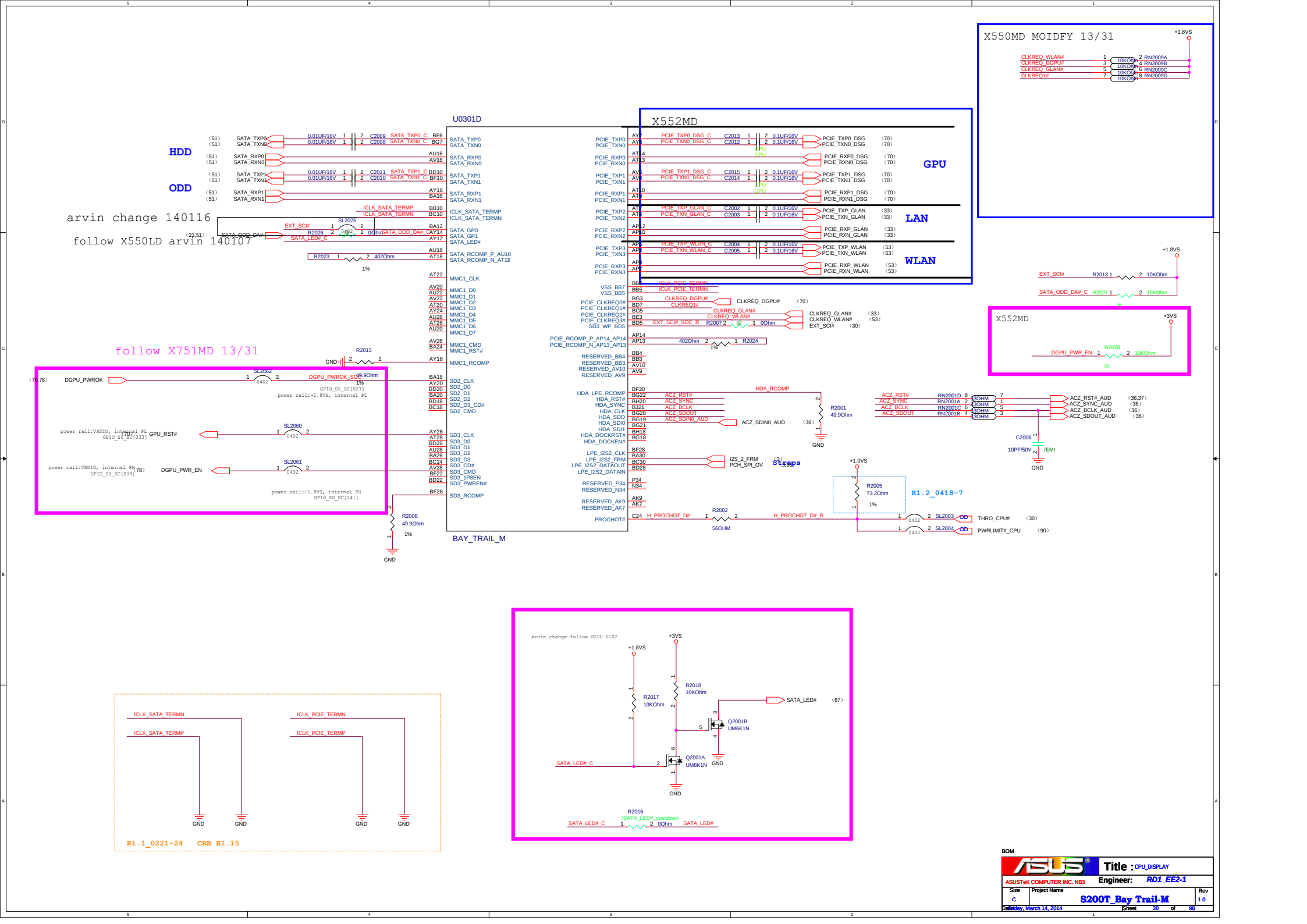


Near DIMM Device <5000 mil

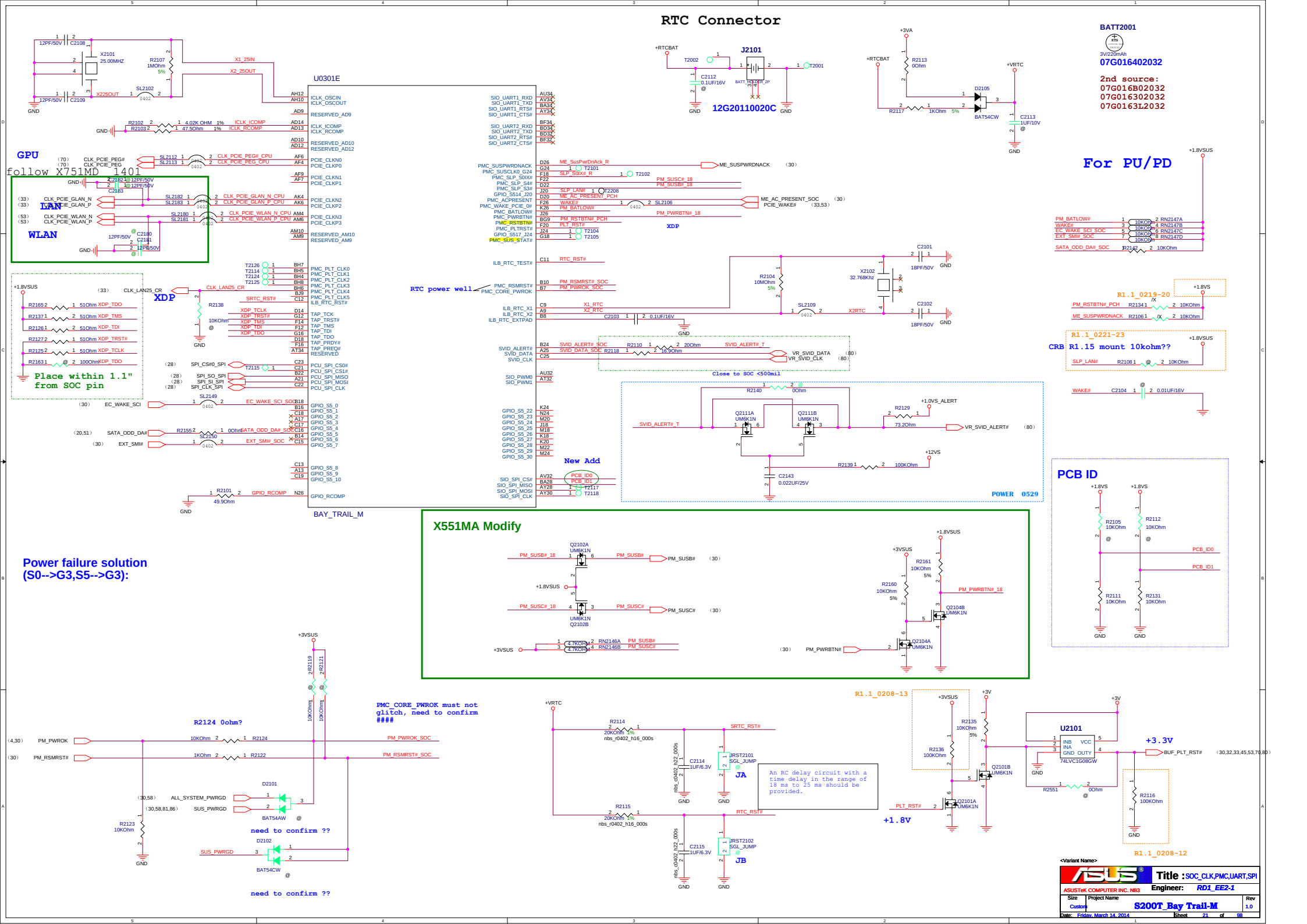


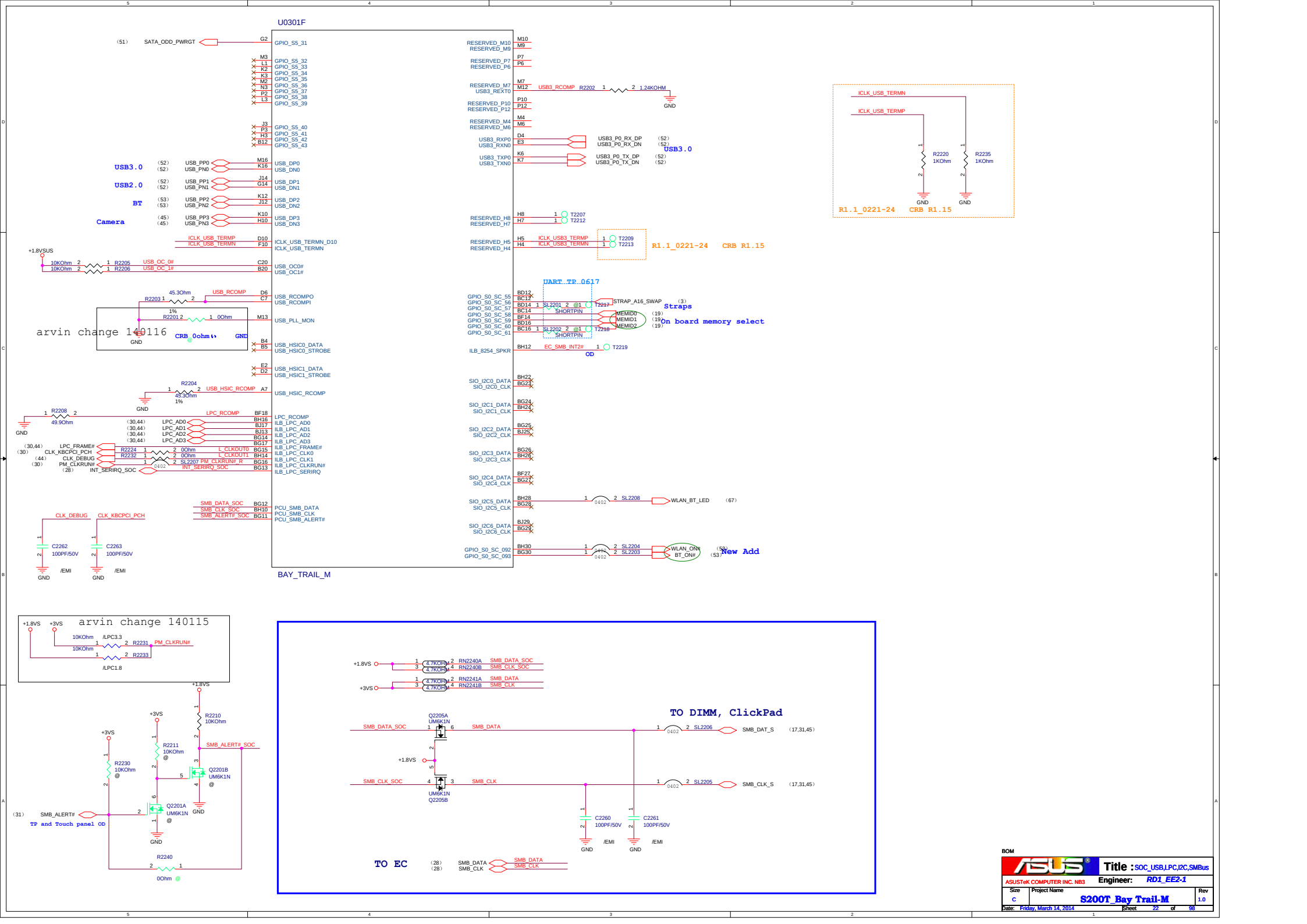


ASUSTeK COMPUTER INC.	Title : DDR3 CA_DQ VOLTAGE		
	Engineer: RD1_EE2-1		
Size: C	Project Name: S200T_Bay Trail-M		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 19 of 98		


X550MD MOIDFY 13/31
+1.8VS
CLKREQ_WLAN#
CLKREQ_DGPU#
CLKREQ_GLAN#
CLKREQ1#
10KOHM
RN2009A
RN2009B
RN2009C
RN2009D
U0301D
X552MD
HDD
ODD
GPU
LAN
WLAN
arvin change 140116
follow X550LD arvin 140107
follow X751MD 13/31
SATA_TXP0
SATA_TXN0
SATA_RXP0
SATA_RXN0
SATA_TXP1
SATA_TXN1
SATA_RXP1
SATA_RXN1
ICLK_SATA_TERMP
ICLK_SATA_TERMN
SATA_ODD_DA#
SATA_LED#_C
SATA_GP0
SATA_GP1
SATA_LED#
SATA_RCOMP_P_AU18
SATA_RCOMP_N_AT18
MMC1_CLK
MMC1_D0
MMC1_D1
MMC1_D2
MMC1_D3
MMC1_D4
MMC1_D5
MMC1_D6
MMC1_D7
MMC1_CMD
MMC1_RST#
MMC1_RCOMP
SD2_CLK
SD2_D0
SD2_D1
SD2_D2
SD2_D3_CD#
SD2_CMD
SD3_CLK
SD3_D0
SD3_D1
SD3_D2
SD3_D3
SD3_CD#
SD3_CMD
SD3_1P8EN
SD3_PWREN#
SD3_RCOMP
BAY_TRAIL_M
PCIE_TXP0_DSG_C
PCIE_TXN0_DSG_C
PCIE_TXP1_DSG_C
PCIE_TXN1_DSG_C
PCIE_TXP_GLAN_C
PCIE_TXN_GLAN_C
PCIE_TXP_WLAN_C
PCIE_TXN_WLAN_C
CLKREQ_DGPU#
CLKREQ1#
CLKREQ_GLAN#
CLKREQ_WLAN#
EXT_SCI#_SOC_R
SD3_WP_BD5
HDA_RCOMP
ACZ_RST#
ACZ_SYNC
ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0_AUD
I2S_2_FRM
PCH_SPI_OV
H_PROCHOT_D#
H_PROCHOT_D#_R
THRO_CPU#
PWRLIMIT#_CPU
R1.2_0418-7
DGPU_PWROK
DGPU_PWROK_SC
DGPU_RST#
DGPU_PWR_EN
R2015
R2006
R2001
R2005
R2002
SL2062
SL2060
SL2061
SL2003
SL2004
R2013
R2027
R2028
EXT_SCI#
SATA_ODD_DA#_C
DGPU_PWR_EN
+3VS
C2006
10PF/50V
/EMI
ICLK_SATA_TERMN
ICLK_SATA_TERMP
ICLK_PCIE_TERMN
ICLK_PCIE_TERMP
R1.1_0221-24
CRB R1.15
arvin change follow S200 0102
R2018
10KOhm
R2017
10KOhm
Q2001B
UM6K1N
Q2001A
UM6K1N
SATA_LED#
SATA_LED#_C
R2016
/SATA_LED#_costdown
GND
BOM
Title : CPU_DISPLAY
ASUSTeK COMPUTER INC. NB3
Engineer: RD1_EE2-1
Size C
Project Name S200T_Bay Trail-M
Rev 1.0
Date: Friday, March 14, 2014
Sheet 20 of 98

RTC Connector




U0301F
BAY_TRAIL_M
USB3.0
USB2.0
BT
Camera
arvin change 140116
arvin change 140115
CRB 0ohm
R1.1_0221-24 CRB R1.15
UART TP 0617
Straps
On board memory select
TO DIMM, ClickPad
TO EC
New Add
TP and Touch panel OD
BOM
Title : SOC_USB,LPC,I2C,SMBus
ASUSTeK COMPUTER INC. NB3
Engineer: RD1_EE2-1
Project Name S200T_Bay Trail-M
Size C
Rev 1.0
Date: Friday, March 14, 2014
Sheet 22 of 98

<Variant Name>

Title : CPU_PCIE,USB

ASUSTeK COMPUTER INC. NB3

Engineer: RD1_EE2-1

Size	Project Name	Rev
B	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 23 of 98

BOM

Title : CPU_PCHCLOCK SIGNALS

ASUSTeK COMPUTER INC. NB1

Engineer: RD1_EE2-1

Size	Project Name	Rev
B	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 24 of 98

BOM

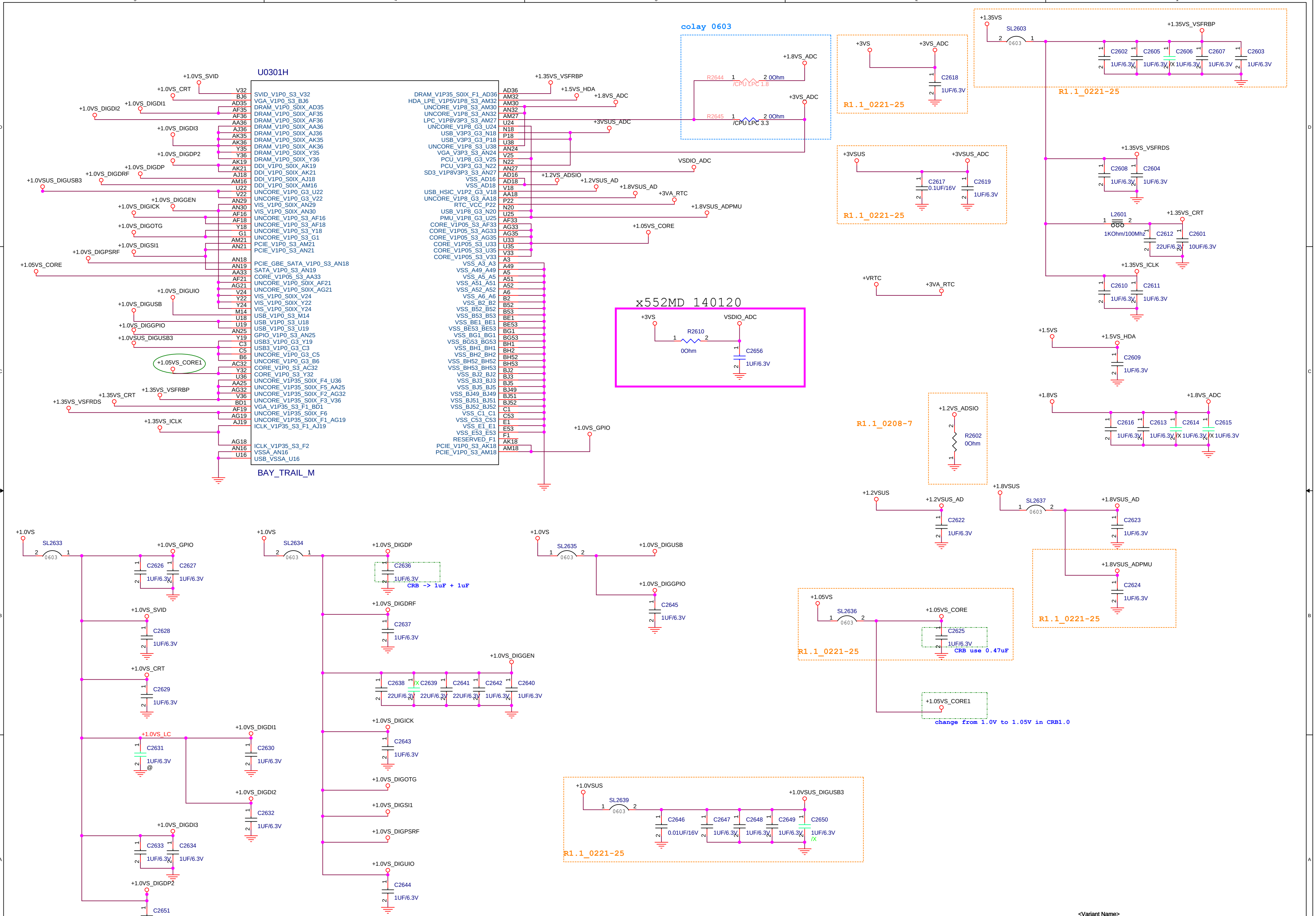
ASUSTeK COMPUTER INC. NB1

Title : CPU_PCH_SYS_POWER

Engineer: RD1_EE2-1

Size	Project Name	Rev
Custom	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 25 of 98



<Variant Name>

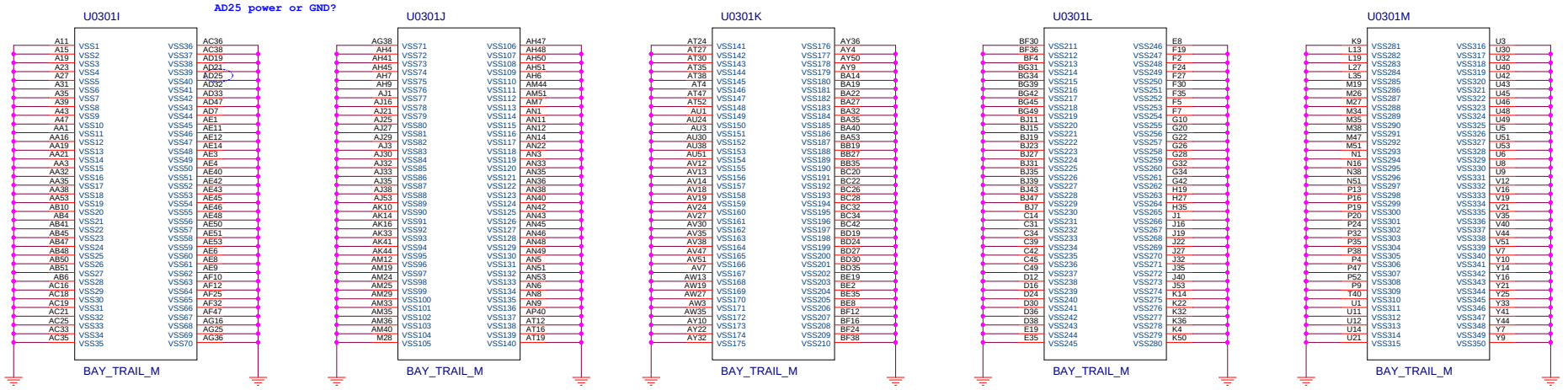
Title : SOC_POEWR,GND

ASUSTeK COMPUTER INC. NB3

Engineer: RD1_EE2-1

Size	Project Name	Rev
C	S200T_Bay Trail-M	1.0

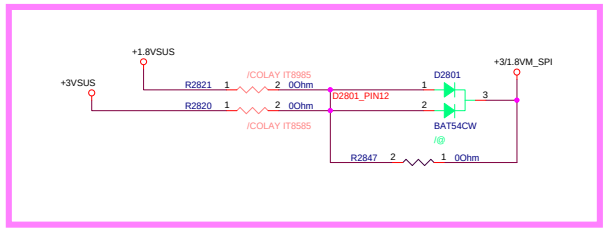
Date: Friday, March 14, 2014 Sheet 26 of 98

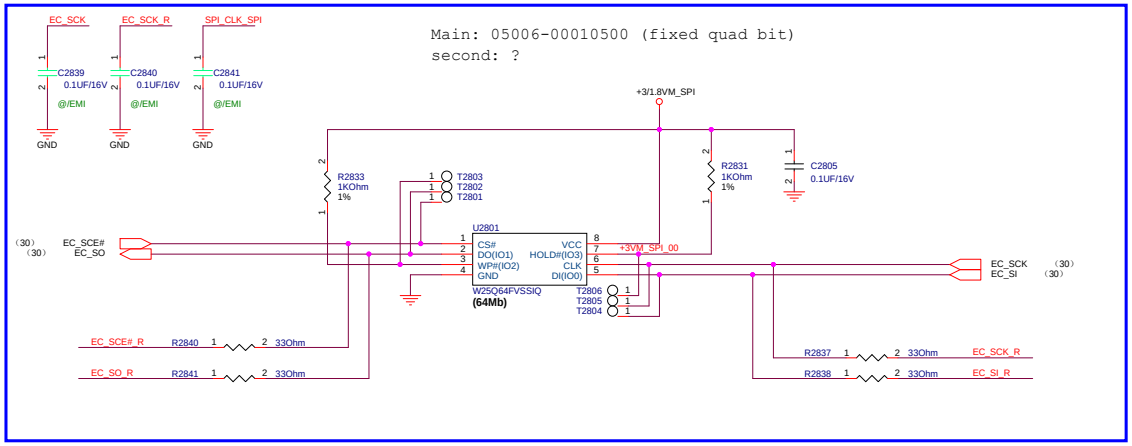


BOM

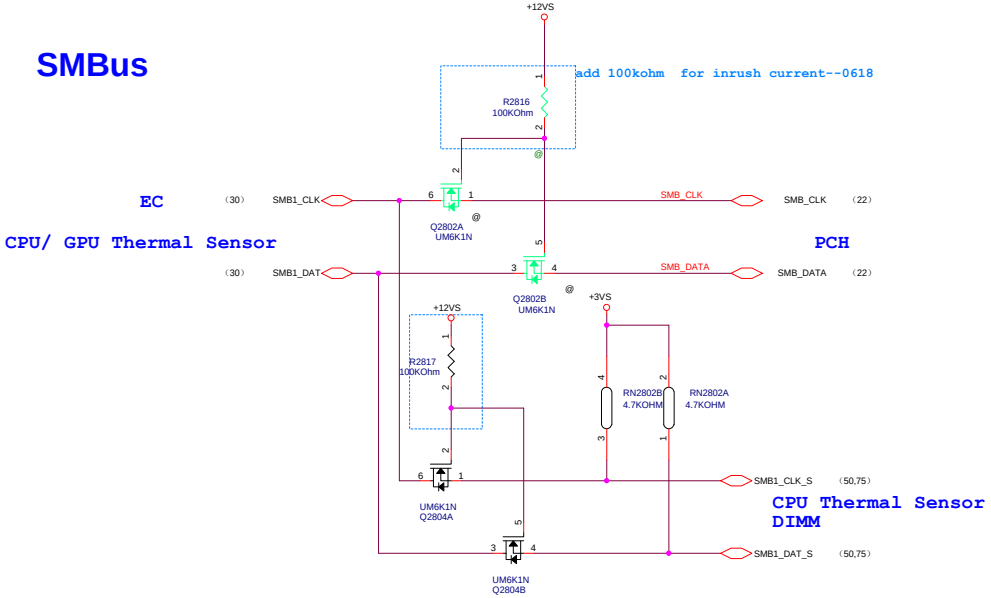
ASUSTeK COMPUTER INC. NB3	Title : SOC_POEWR,GND	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 27 of 98	

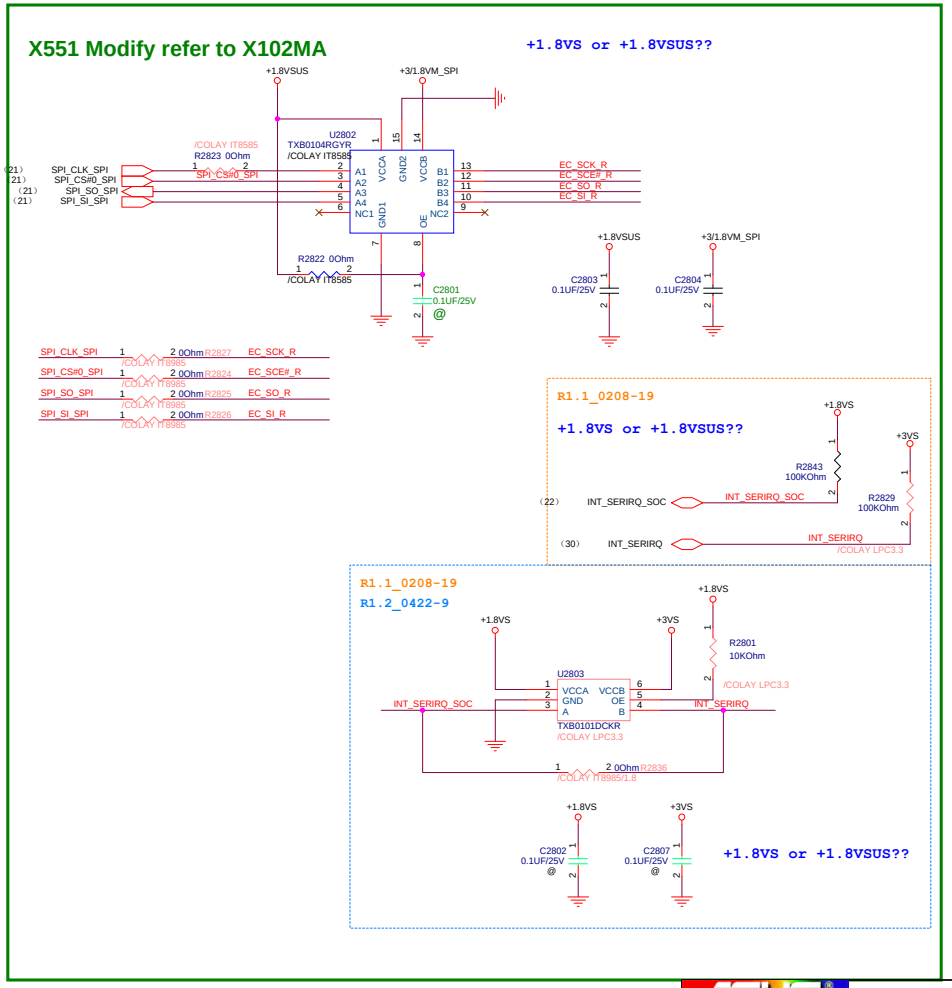
PCH SPI ROM





SMBus





ASUSTeK COMPUTER INC.	Title : PCH_SPI ROM,OTH	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 28 of 98	

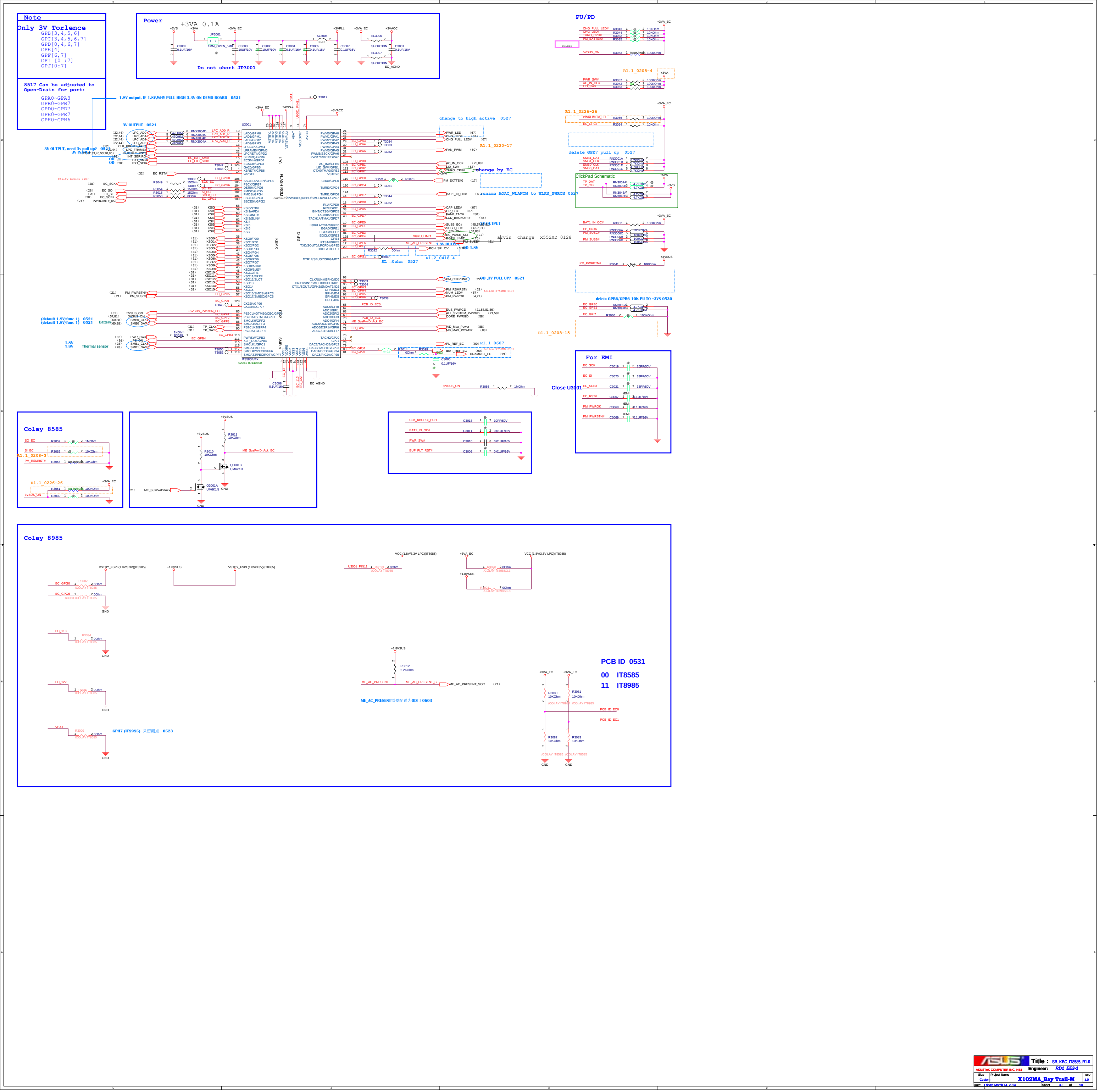
Title : CLK_****

ASUSTeK COMPUTER INC.

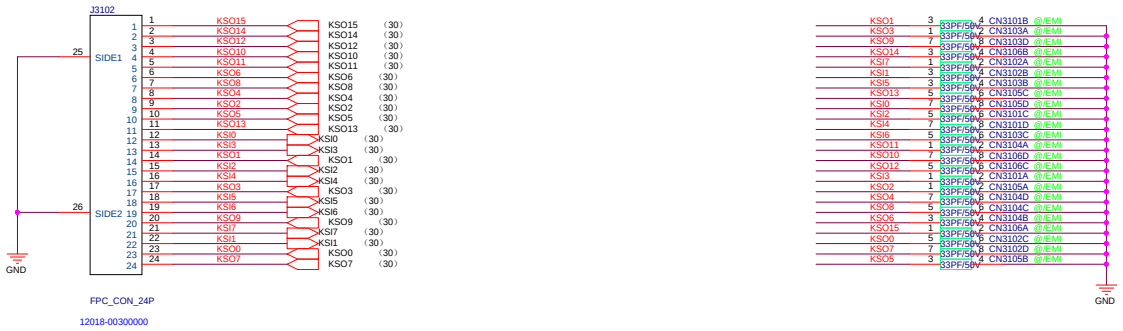
Engineer: RD1_EE2-1

Size	Project Name	Rev
C	S200T_Bay Trail-M	1.0

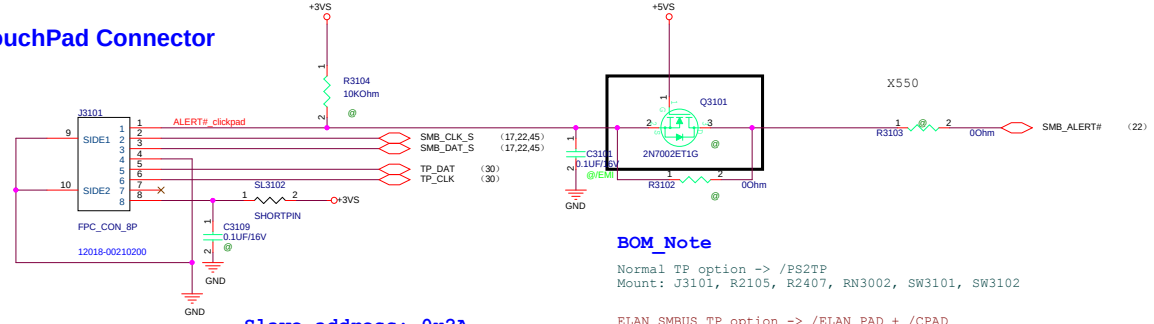
Date: Friday, March 14, 2014 Sheet 29 of 98


Note
Only 3V Torlence
GPB[3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPI [0 :7]
GPJ[0:7]
8517 Can be adjusted to Open-Drain for port:
GPA0-GPA3
GPB0-GPB7
GPD0-GPD7
GPE0-GPE7
GPH0-GPH6
Power
+3VA 0.1A
Do not short JP3001
PU/PD
change to high active 0527
delete GPE7 pull up 0527
ClickPad Schematic
delete GPB6/GPB6 10K PU TO +3VS 0530
For EMI
Close U3001
Colay 8585
Colay 8985
PCB ID 0531
00 IT8585
11 IT8985
Title : SB_KBC_IT8585_R1.0
ASUSTeK COMPUTER INC. NB1
Engineer: RD1_EE3-1
X102MA_Bay Trail-M

Keyboard Connector



TouchPad Connector



Slave address: 0x2A

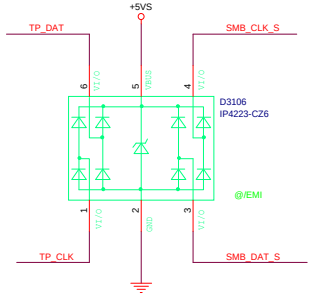
BOM_Note

Normal TP option -> /PS2TP
Mount: J3101, R2105, R2407, RN3002, SW3101, SW3102

ELAN SMBUS TP option -> /ELAN_PAD + /CPAD
Mount: R2106,R2408, RN3008,Q3102,J3104

Synaptics SMBUS TP option -> /CPAD
Mount: J3104, R2408, RN3008

Reserved for EMI



<Variant Name>

ASUSTeK COMPUTER INC. NB1

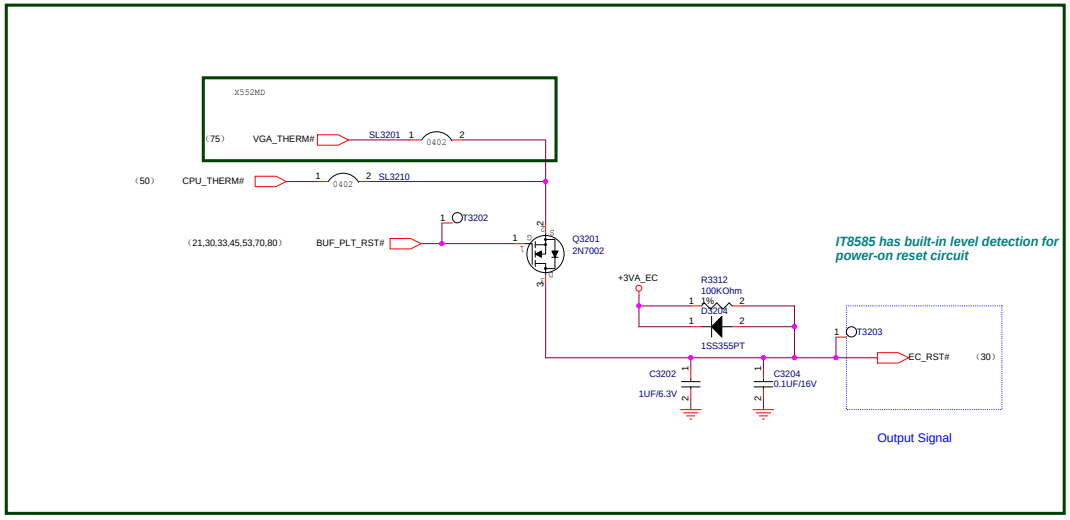
Title : CR_KBC_KB & TP_R0.5

Engineer: SZ2_Team3

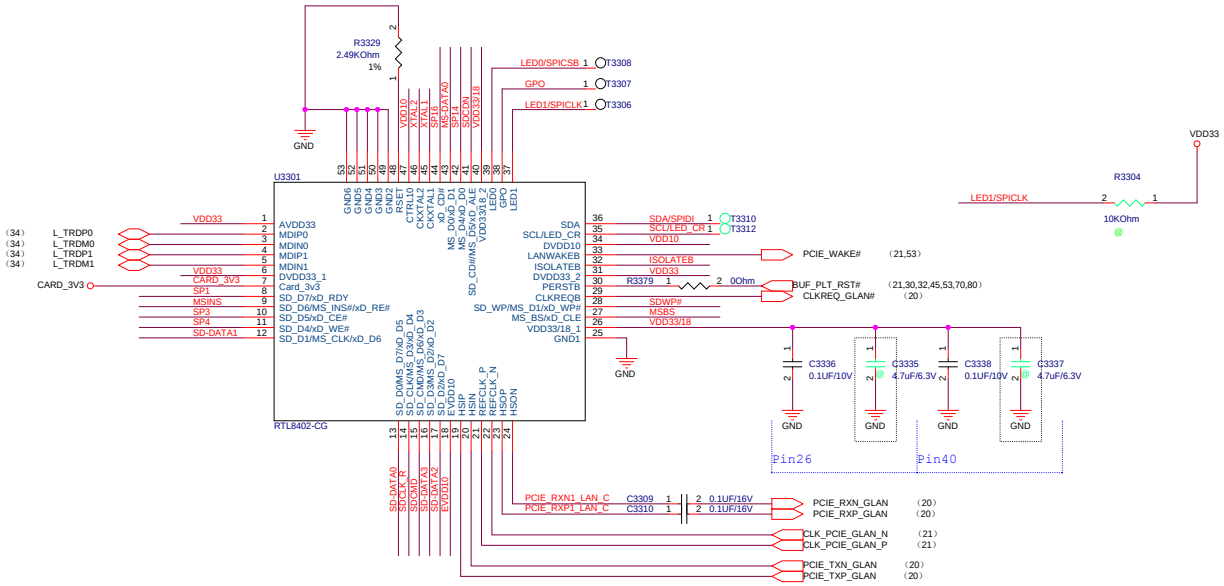
Size	Project Name	Rev
C	X550LC	1.0

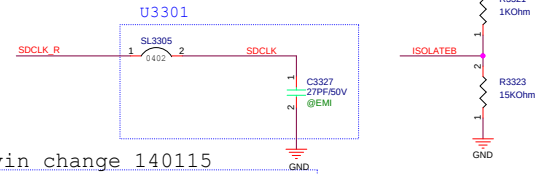
Date: Friday, March 14, 2014 Sheet 31 of 98

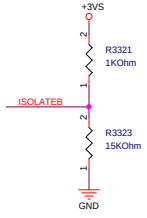
Thermal Policy



ASUSTeK COMPUTER INC.	Title : RST_Reset Circuit	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 32 of 98	







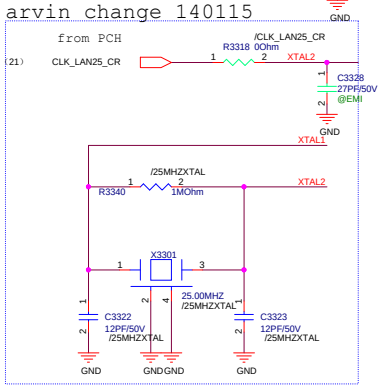
Card Reader Interface

SP1 — T3323
MSINS — T3321
SP3 — T3317
SP4 — T3324

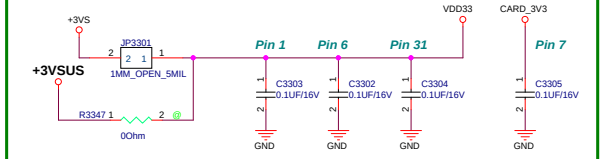
SD-DATA1 (41)
SD-DATA0 (41)
SDCLK (41)
SDCMD (41)
SD-DATA3 (41)
SD-DATA2 (41)
SDWP# (41)
SDCDN (41)

MSBS — T3318
SP14 — T3322
MS-DATA0 — T3319
SP16 — T3320

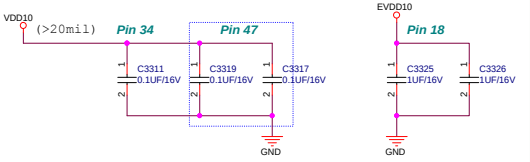
arvin change 140115



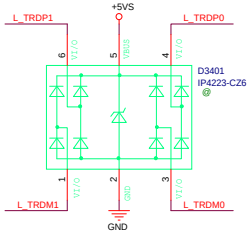
3.3V POWER



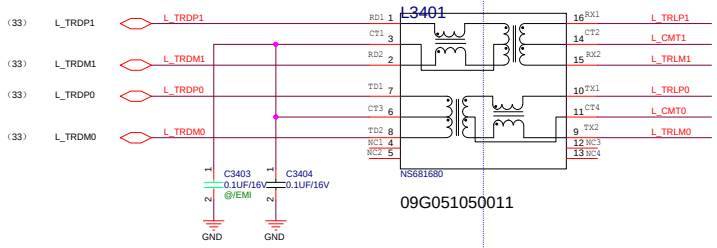
1V POWER



ASUSTeK COMPUTER INC.	Title : LAN-CLARKVILLE		
	Engineer: SZ_SYS2		
Size: C	Project Name: X551CA		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 33 of 98		

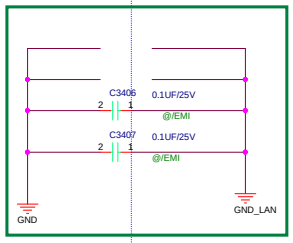


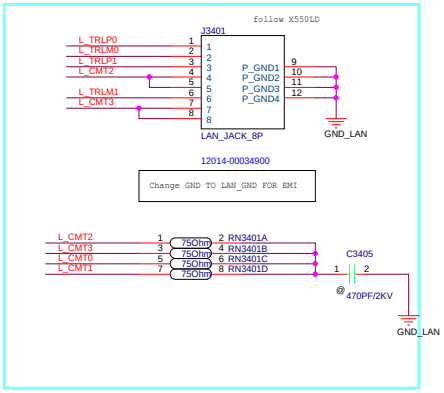
GND **GND_LAN**



09G051050011

C3403,C3404 close to L3401 pin3 and pin6 each





ASUSTeK COMPUTER INC.	Title : LAN-RJ45	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 34 of 98	

<Variant Name>

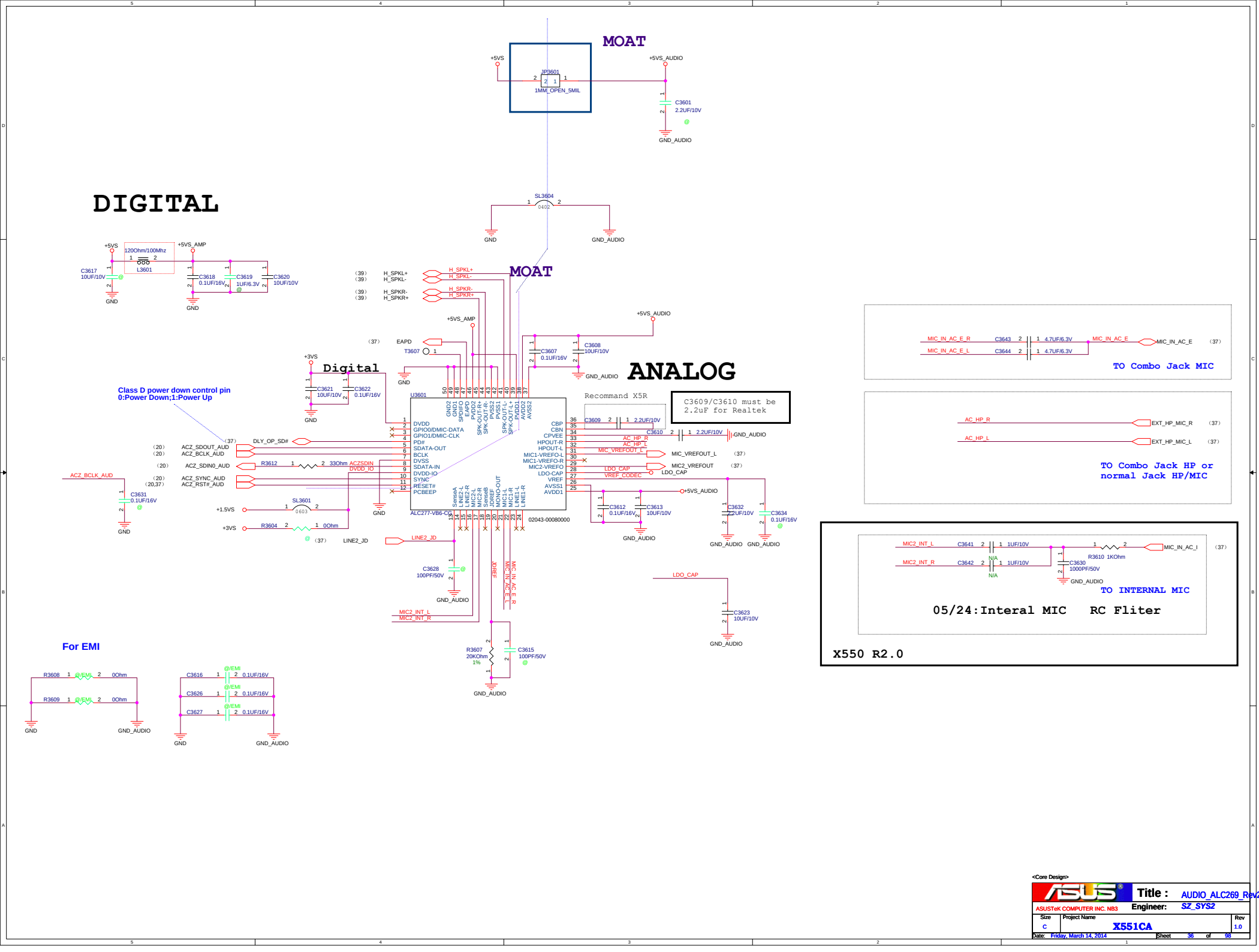
Title : SERIAL PORT

ASUSTeK COMPUTER INC. NB1

Engineer: RD1_EE2-1

Size	Project Name	Rev
Custom	X102MA_Bay Trail-M	1.0

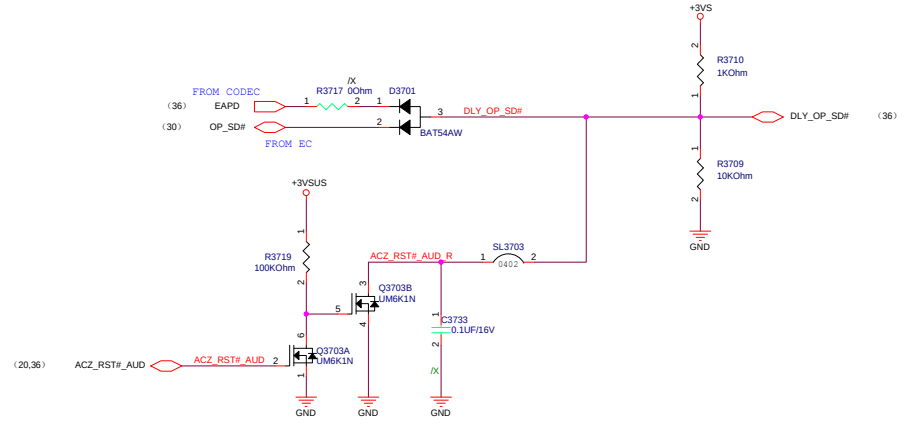
Date: Friday, March 14, 2014 Sheet 35 of 98

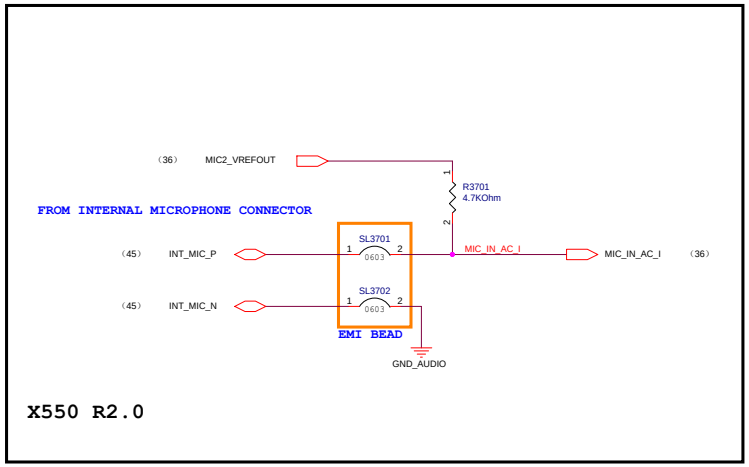


<Core Design>

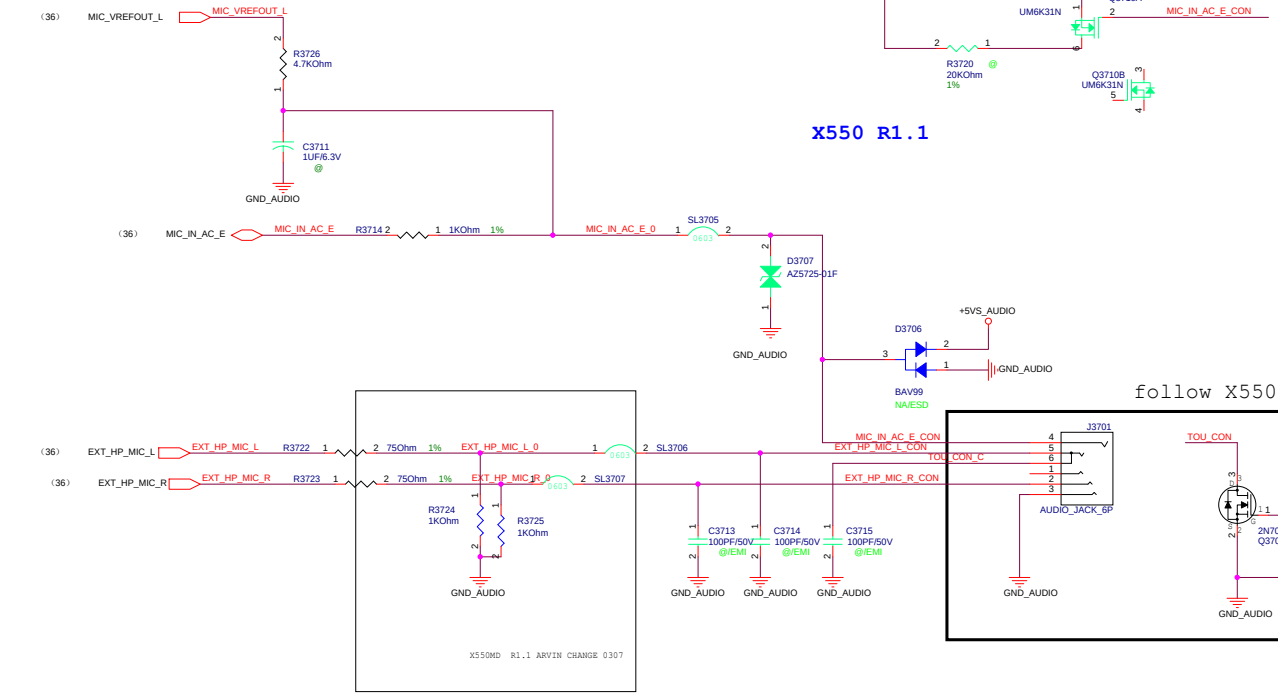
ASUSTeK COMPUTER INC. NB3	Title : AUDIO_ALC269_Rev2.5_1	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 36 of 98	

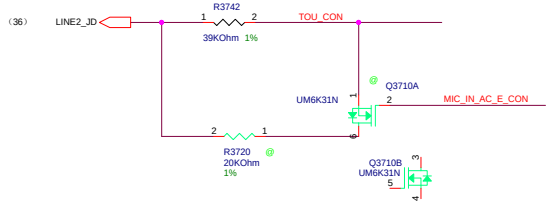
MUTE CONTROL





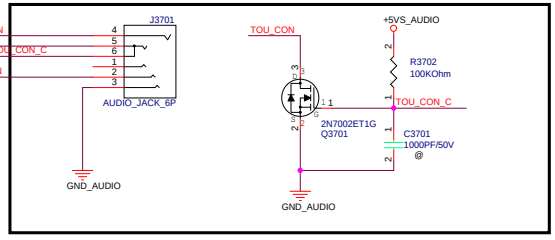
X550 R1.1





X550 R1.1

follow X550LD 140113

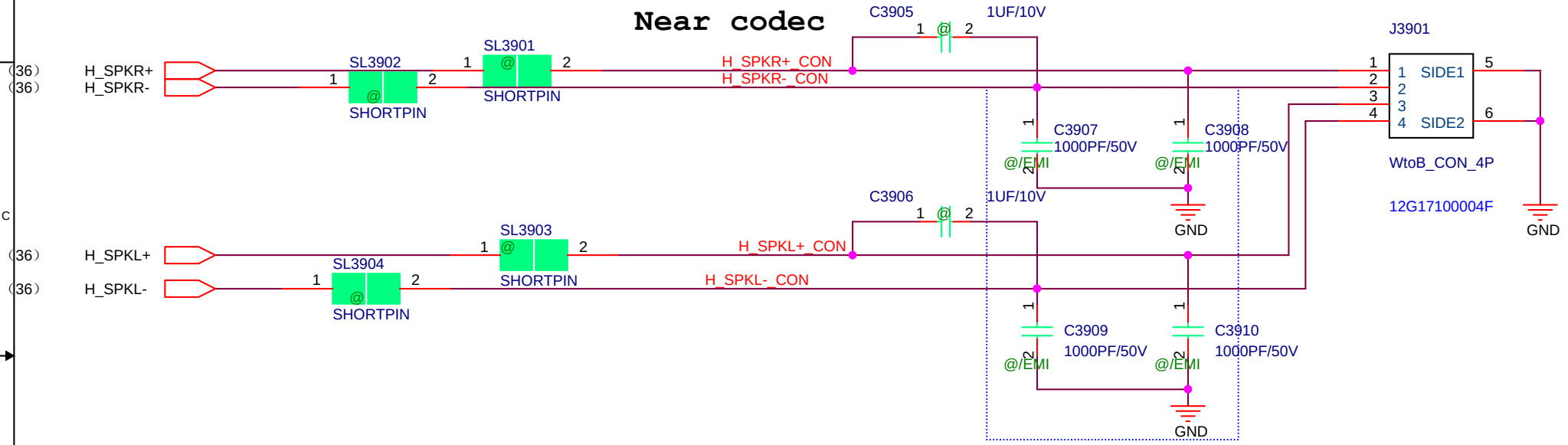


ASUSTeK COMPUTER INC. NB3	Title : Phone_Jack		
	Engineer: SZ_SYS2		
Size: C	Project Name: X551CA		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 37 of 98		

<Variant Name>

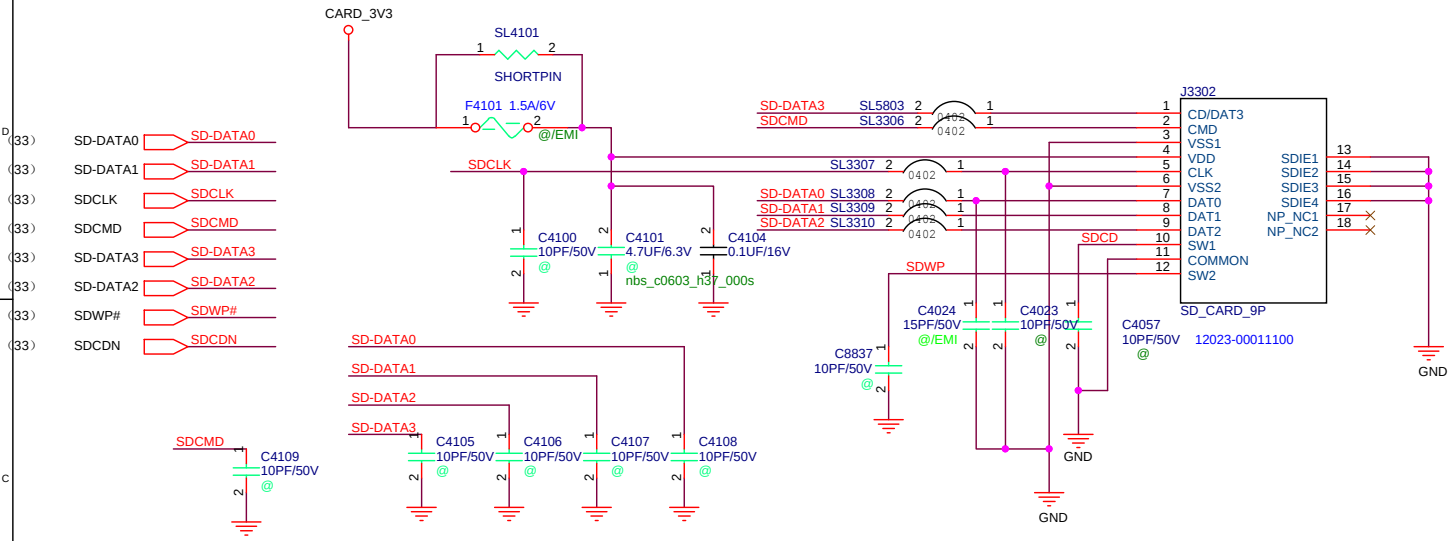
ASUSTeK COMPUTER INC.	Title : ****	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 38 of 98	

Audio Speaker



ASUSTeK COMPUTER INC.	Title : AUD-SPEAKER CONN.	
	Engineer: SZ_SYS2	
Size: A	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 39 of 98	

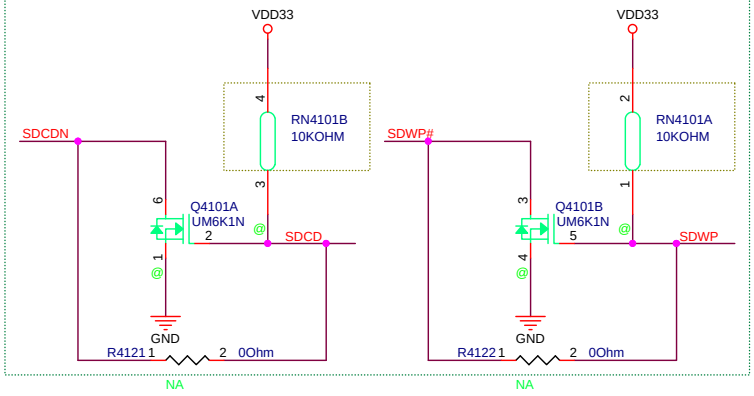
Title :	Card Reader-AU6437
ASUSTeK COMPUTER INC.	Engineer: SZ_SYS2
Size: C	Project Name: X551CA
Rev: 1.0	
Date: Friday, March 14, 2014	Sheet 40 of 98



SDWP: Internal Pull-up
SDCDN: Internal Pull-up

SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card inserted

Add Q4101 RN4101 for J4100 SDWP/SDCD signal reverse



(4)OPENING/CLOSE OF SD SWITCH :

	PROTECT CONTACT		DETECT CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	CLOSE	CLOSE	CLOSE
CARD HALF INSERTION	OPEN	OPEN	CLOSE
CARD INSERTION	CLOSE	OPEN	OPEN

ASUSTeK COMPUTER INC.

Title : CB_****

Engineer: SZ_SYS2

Size	Project Name	Rev
B	X551CA	1.0

Date: Friday, March 14, 2014 Sheet 41 of 98

Title : RTS5139

ASUSTeK COMPUTER INC. NB3

Engineer: SZ_SYS2

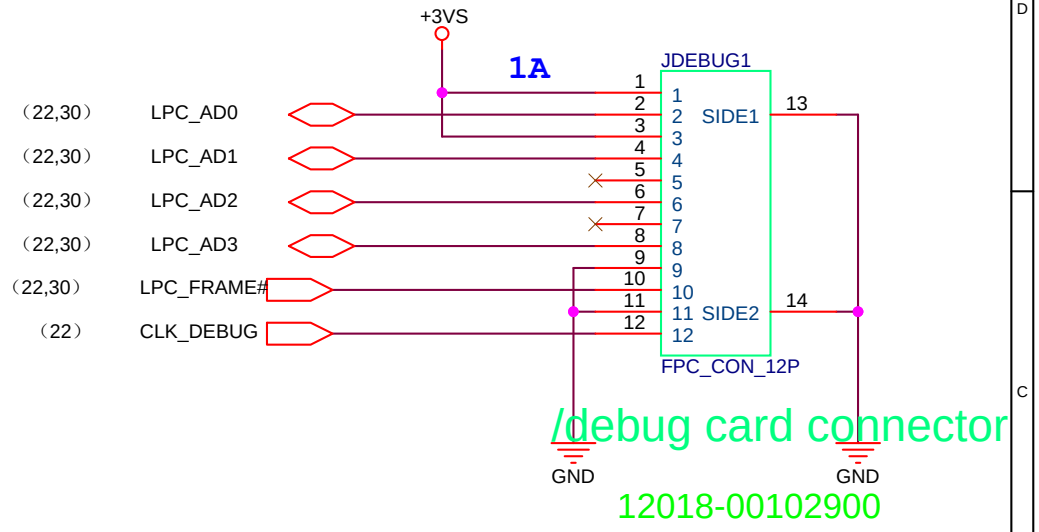
Size	Project Name	Rev
C	X551CA	1.0

Date: Friday, March 14, 2014 Sheet 42 of 98

<Variant Name>

ASUSTeK COMPUTER INC.	Title : ****	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 43 of 98	

LPC DEBUG PORT



LPC DEBUG PORT

TPM interface signals
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
+3V
LPCPD#
INT_SERIRQ
BUF_PLT_RST#
CLK_33M_TPM
TPM_CLKRUN#
+3VS

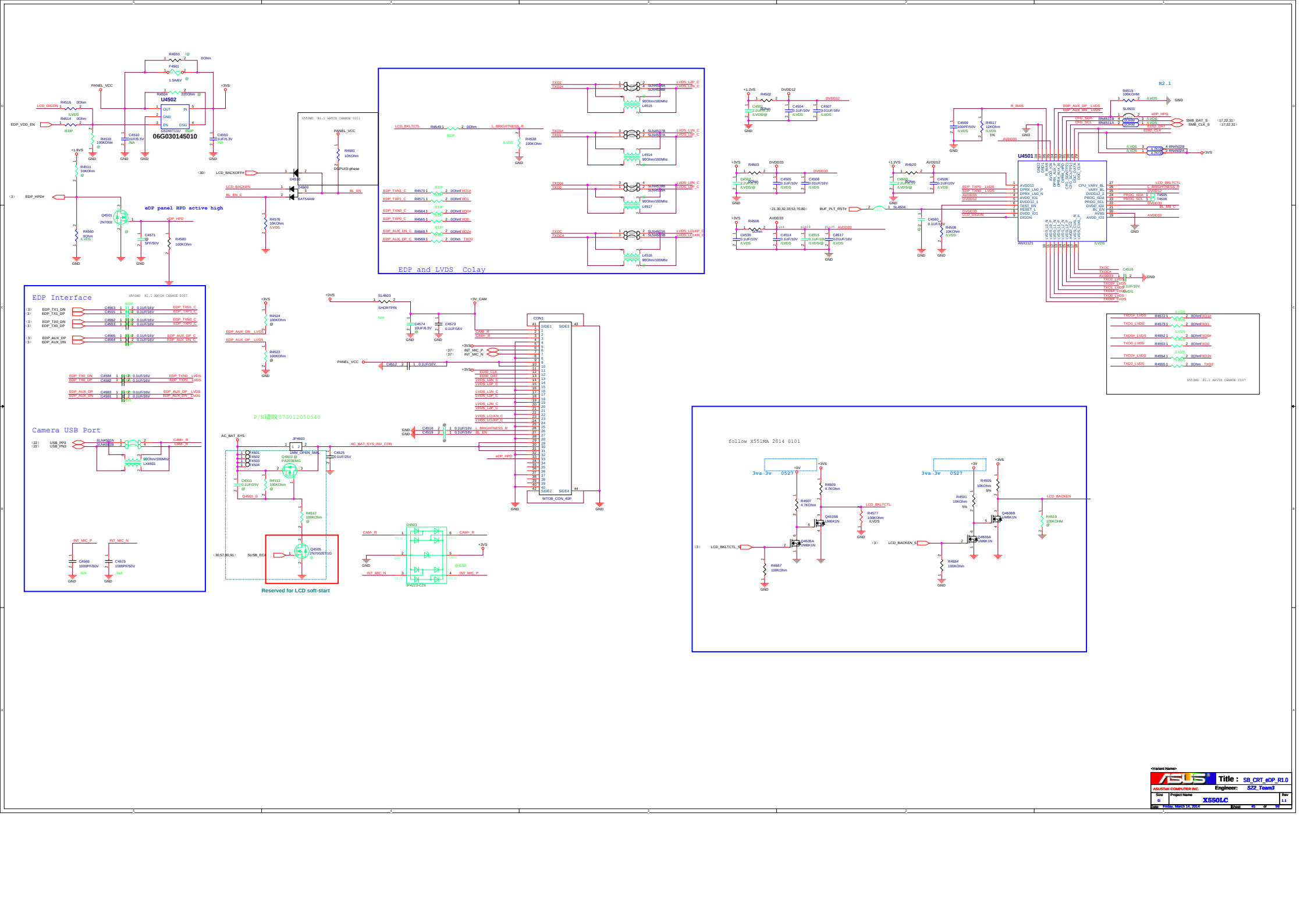
ASUSTeK COMPUTER INC.

Title : DEBUG PORT

Engineer: SZ_SYS2

Size	Project Name	Rev
A	X551CA	1.0

Date: Friday, March 14, 2014 Sheet 44 of 98



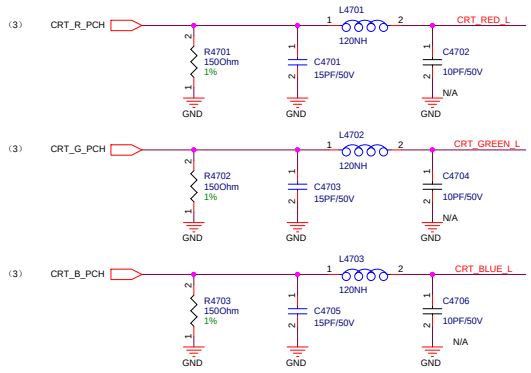
<Variant Name>				
ASUSTeK COMPUTER INC.	Title : SB_CRT_eDP_R1.0			
	Engineer: SZ2_Team3			
Size: D	Project Name: X550LC			Rev: 1.1
Date: Friday, March 14, 2014		Sheet 45 of 58		

Title :	****
ASUSTeK COMPUTER INC.	Engineer: RD1_EE2-1
Size: A	Project Name: X102MA_Bay Trail-M
Rev: 1.0	
Date: Friday, March 14, 2014	Sheet 46 of 98

2nd source:
09G023152003
09G023152202
09G023152500

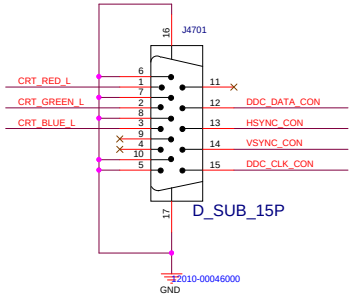
DAC Signal

BOM Mount: 09G023152401



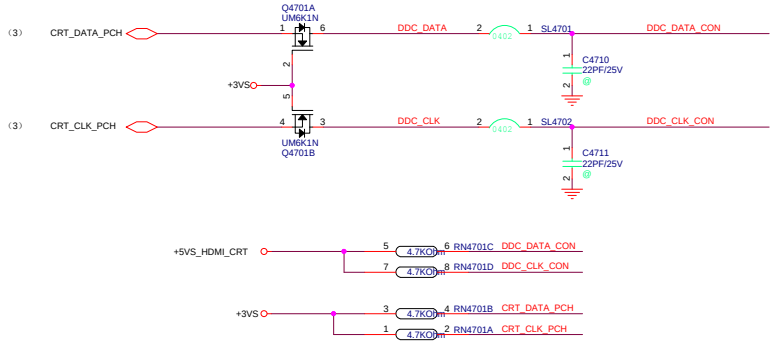
follow X550LD

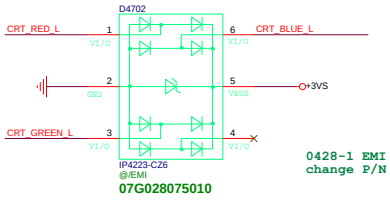
CRT Connector



SYNC Signal

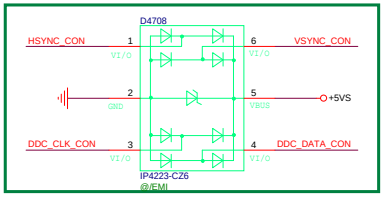
Control Signal





07G028075010

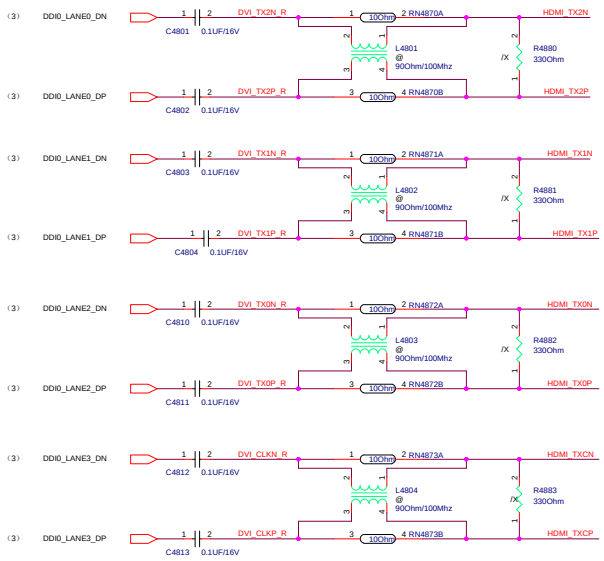
0428-1 EMI D3401, D3402, D4702, D5201, PD6001
change P/N to 07G028176010

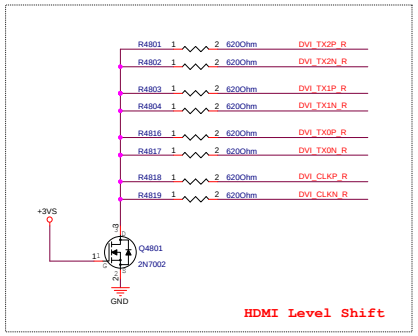


ASUSTeK COMPUTER INC.	Title : CRT D-SUB		
	Engineer: SZ_SYS2		
Size: C	Project Name: X551CA		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 47 of 98		

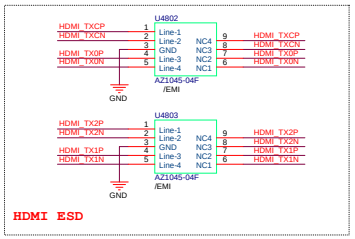
Close to CONNECTOR

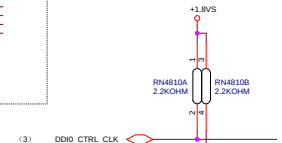
Near CON J4801

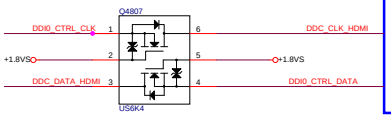


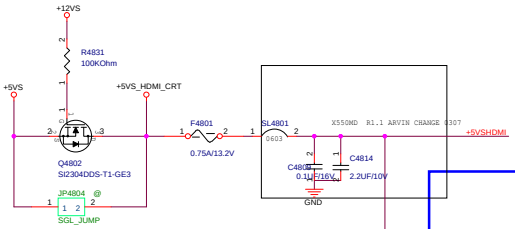


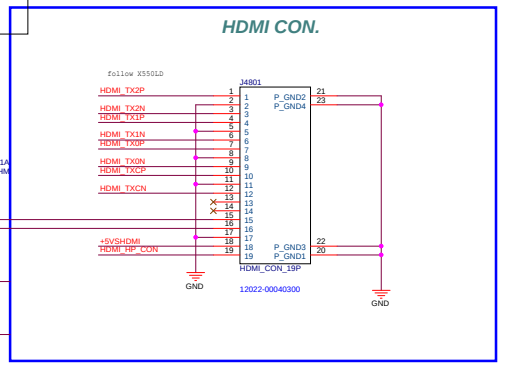
X552MD 01202100

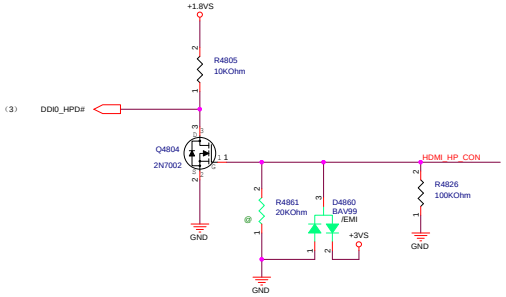


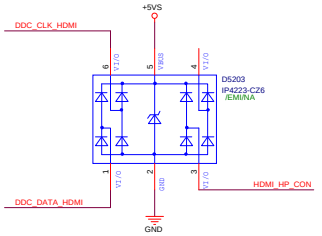












BOM

ASUSTeK COMPUTER INC

Title : HDMI-type D

Engineer: RD1_EE2-1

Size	Project Name	Rev
Custom	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 48 of 58

BOM

Title : ****

ASUSTeK COMPUTER INC

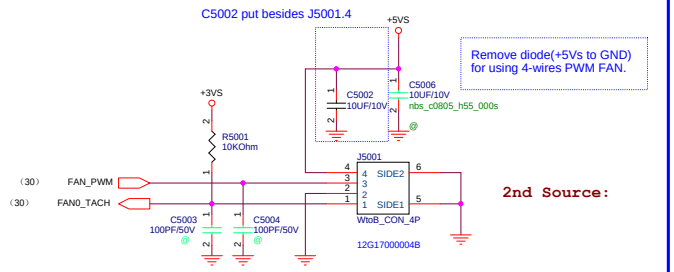
Engineer: RD1_EE2-1

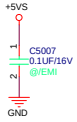
Size	Project Name	Rev
B	X102MA_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 49 of 98

GPU Thermal Sensor

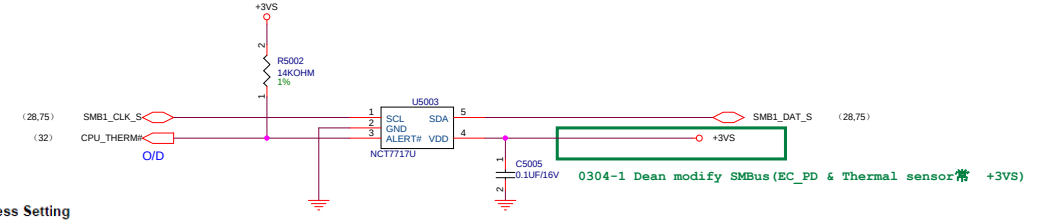
PWM Fan





CPU Thermal Sensor

R5002:14Kohm-->2Kohm
Baytrail Tj,max = 75degC (reason: Tj-sdp = 80degC)



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

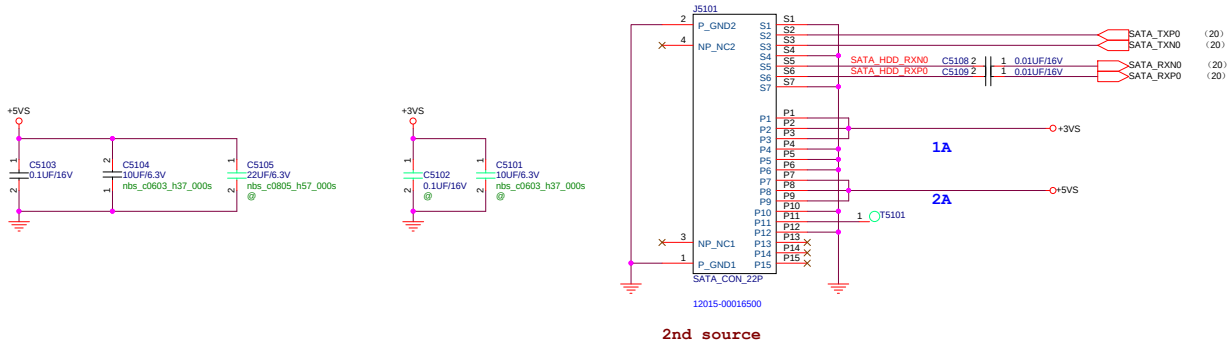
5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

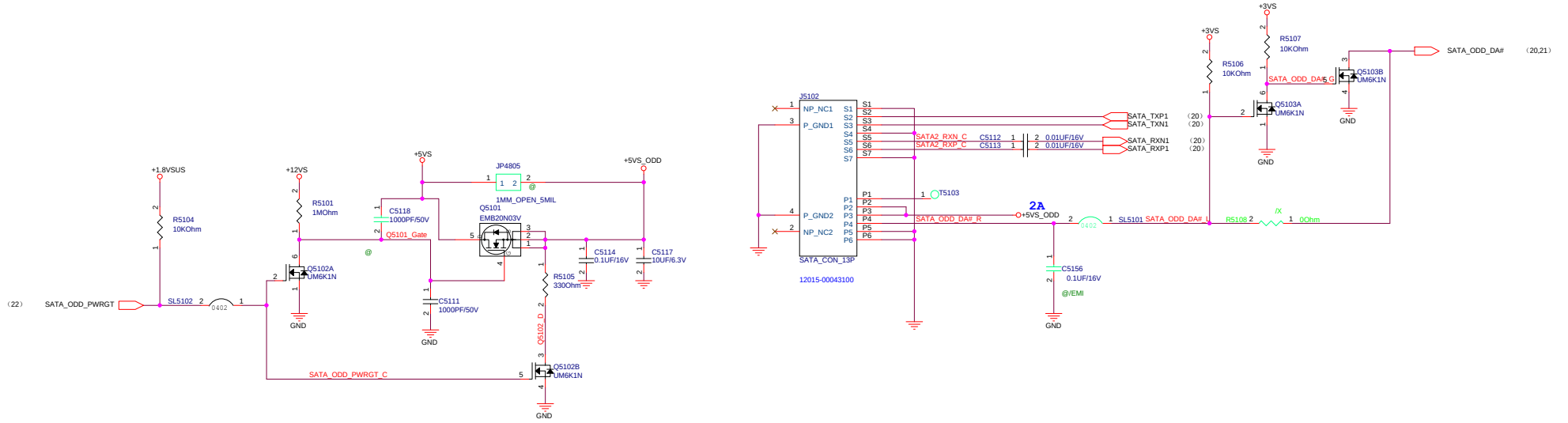
ASUSTeK COMPUTER INC.	Title : FAN_Fan & Sensor		
	Engineer: SZ_SYS2		
Size: C	Project Name: X551CA		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 50 of 98		

SATA HDD



2nd source

SATA ODD

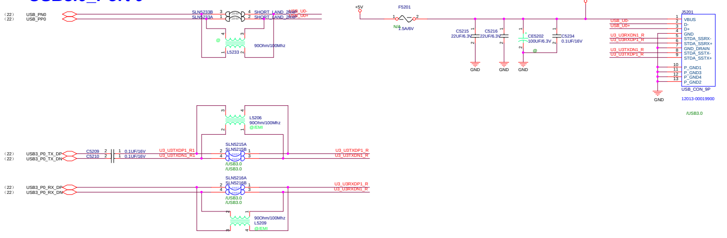


ASUSTeK COMPUTER INC.	Title : SATA HDD & ODD	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 51 of 98	

X552MD

USB3.0_Port 0

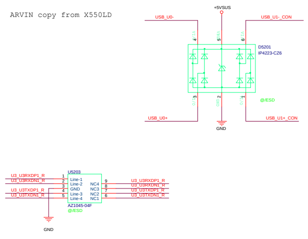
ARVIN copy from X550LD



X552MD

ESD-Protection

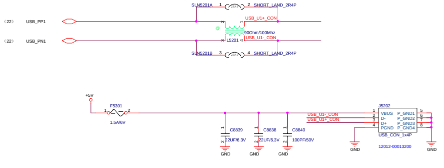
ARVIN copy from X550LD



X552MD

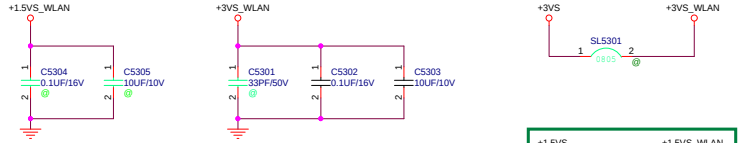
USB2.0_Port 1

ARVIN copy from X550LD

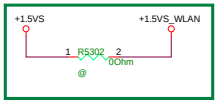


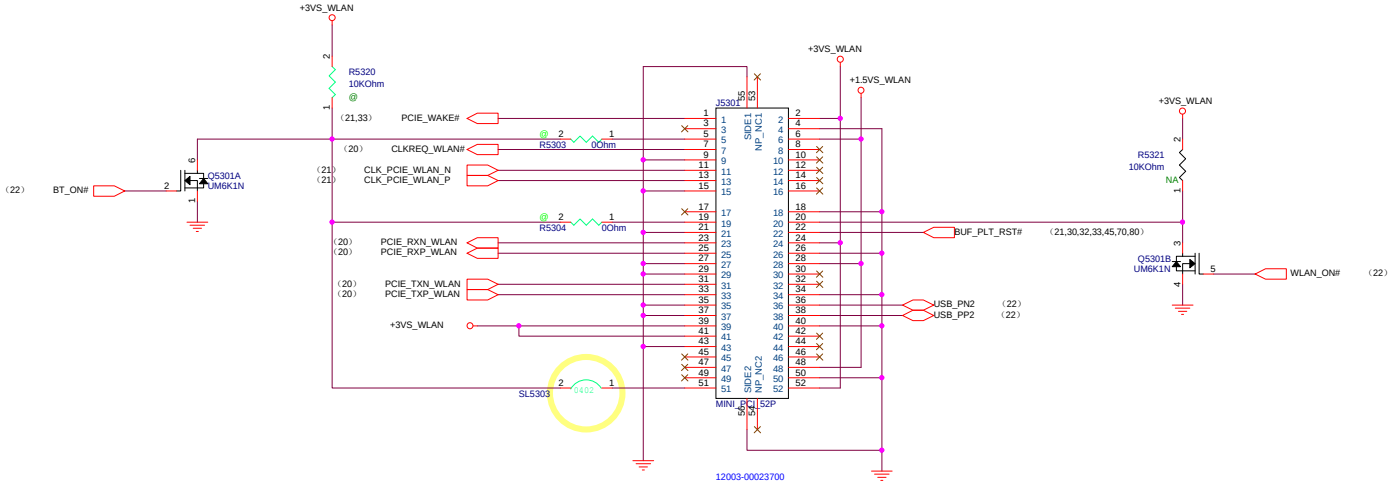
ASUSTeK COMPUTER INC.	Title : USB 3.0 + 2.0 CONN.		
	Engineer: SZ_SYS2		
Size: E	Project Name: X551CA		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 52	of 98	

0520-11 Dean Merge BOM L3000 L5301 L2603 L2604 L2707
=> 120OHM/2A 09G013120802



0309-11 Dean_cost check keypart list WLANA磧+1.5V 惠-
=> unstuff C5304, C5305





2nd source:
12003-00024000

ASUSTeK COMPUTER INC.	Title : MINICARD(WLAN)	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 53 of 98	

Title : USB HSIC Hub

ASUSTeK COMPUTER INC.

Engineer: RD1_EE2-1

Size	Project Name	Rev
C	X102MA_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 54 of 98

<Variant Name>

Title : NFC

ASUSTeK COMPUTER INC. NB8

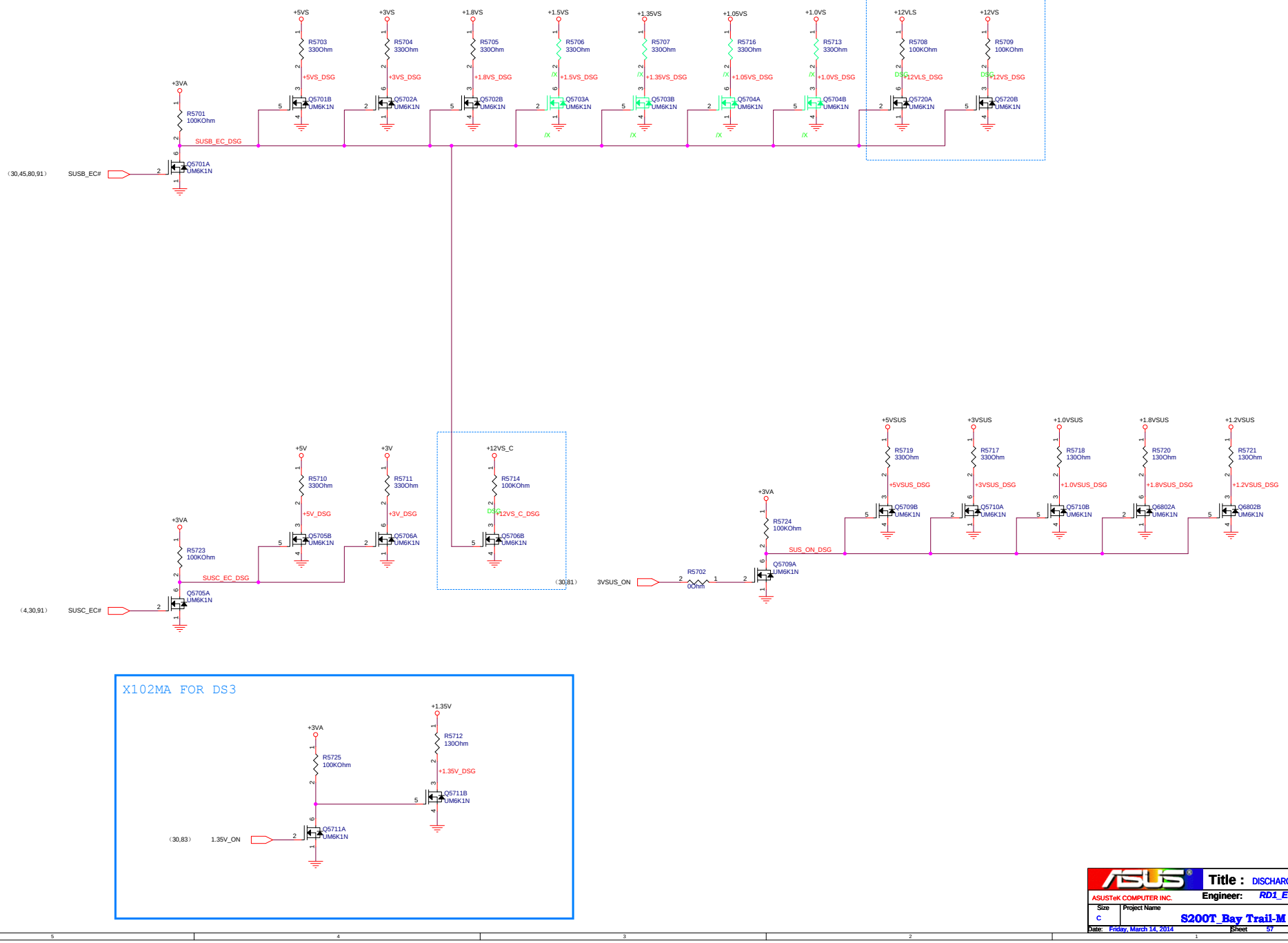
Engineer: RD1_EE2-1

Size	Project Name	Rev
A3	X102MA_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 55 of 98

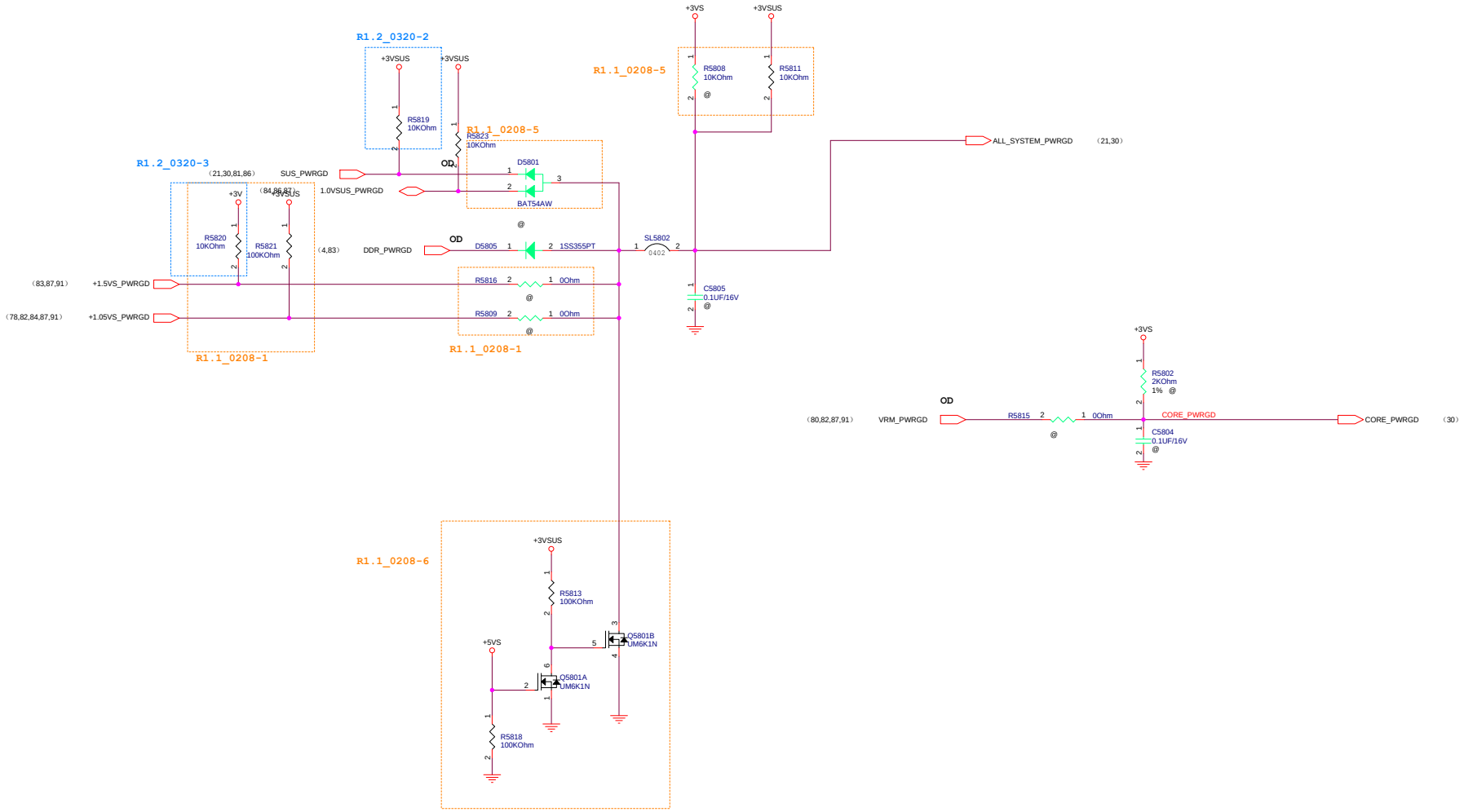
ASUSTeK COMPUTER INC.	Title : PWR_SW&HALL_SW	
	Engineer: SZ_SYS2	
Size: C	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 56 of 98	

X102MA R1.1 0606



X102MA FOR DS3

ASUSTeK COMPUTER INC.	Title : DISCHARGE CIRCUIT	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 57 of 98	



ASUSTeK COMPUTER INC.	Title : POWER_PROTECT	
	Engineer: RD1_EE2-1	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 58 of 98	

<Variant Name>

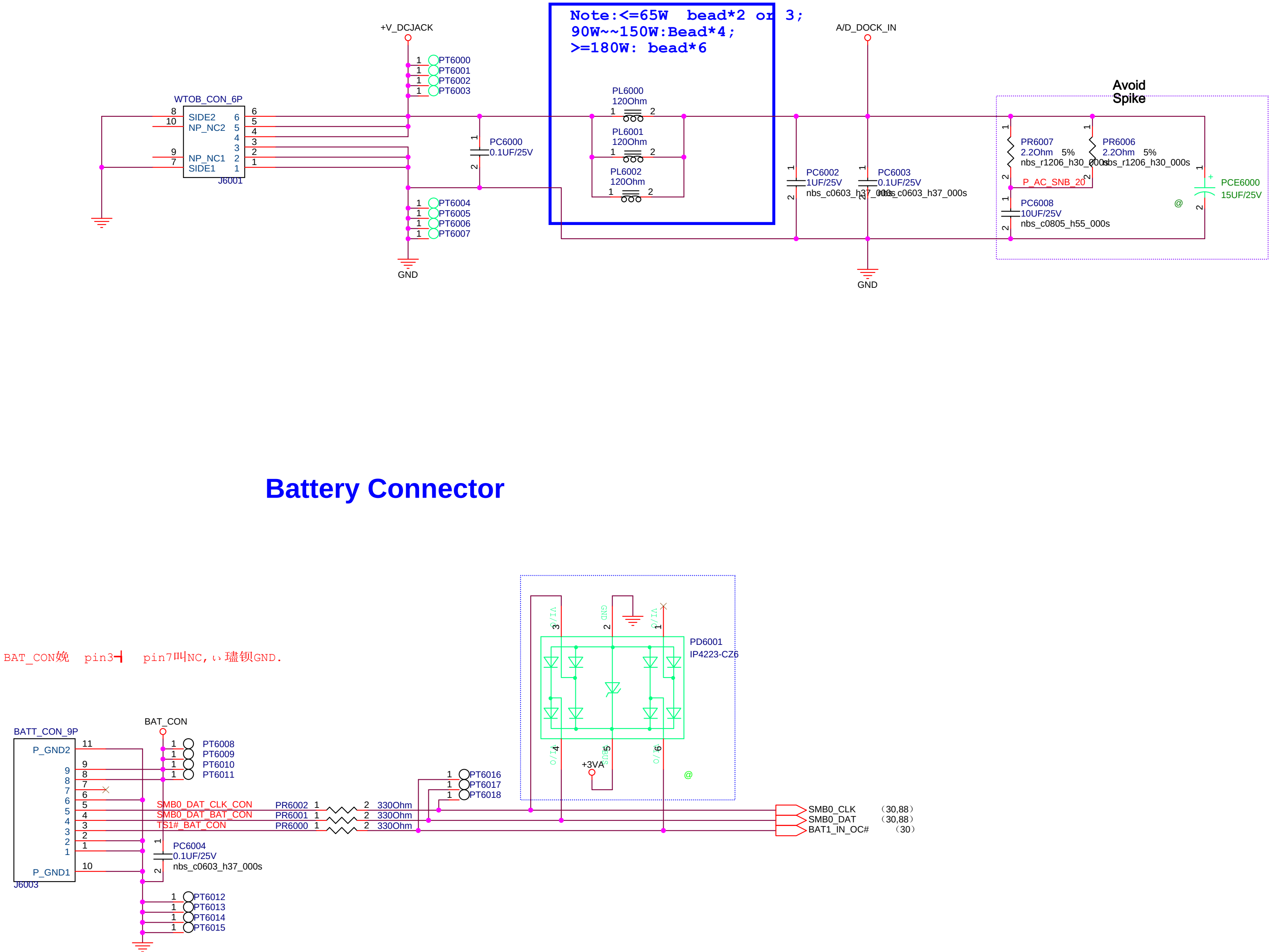
Title : ****

ASUSTeK COMPUTER INC.

Engineer: SZ_SYS2

Size	Project Name	Rev
C	X551CA	1.0

Date: Friday, March 14, 2014 Sheet 59 of 98



BAT_CON娩 pin3┤ pin7叫NC,い璩钡GND.

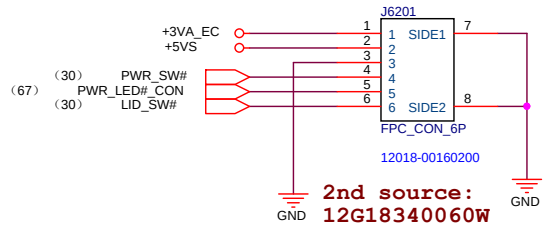
<Variant Name>

ASUSTeK COMPUTER INC.	Title : DC & BAT Connector	Engineer:
Size: Custom	Project Name: KX STD	Rev: R1.2
Date: Friday, March 14, 2014	Sheet 60 of 98	

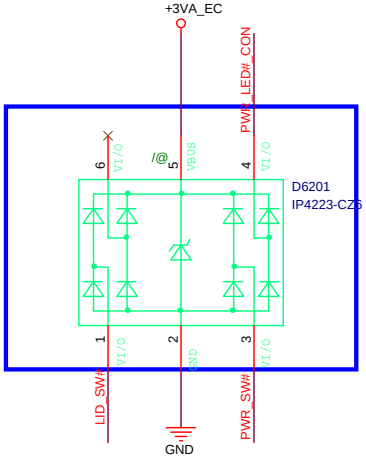
<Variant Name>

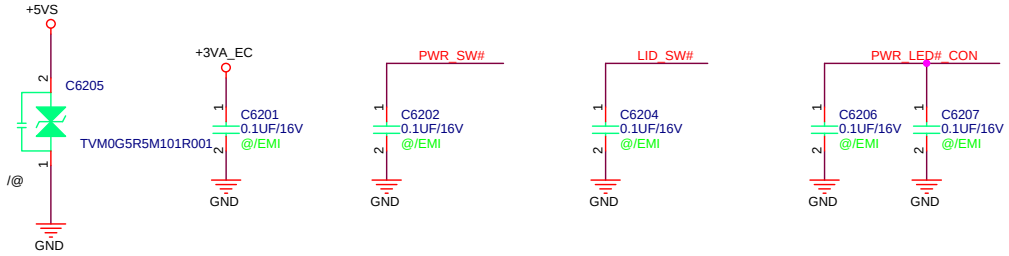
Title	<Title>	
Size C	Document Number X550	Rev 1.0
Date: Friday, March 14, 2014	Sheet 61 of 98	

PWR_SW
PWR_LED
LID_SW



2nd source:
12G18340060W





<Variant Name>

ASUSTeK COMPUTER INC.	Title : B TO B CONNECTOR	
	Engineer: SZ2_Team3	
Size: B	Project Name: X550LC	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 62 of 98	

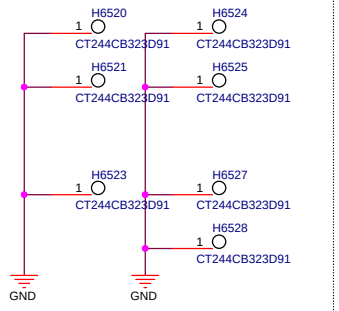
ASUSTeK COMPUTER INC.	Title : FP.****	
	Engineer: RD1_EE2-1	
Size: C	Project Name: X102MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 63 of 98	

UART Debug Board

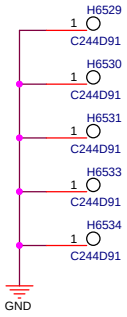
ASUSTeK COMPUTER INC.	Title : UART Debug Board		
	Engineer: RD1_EE2-1		
Size: B	Project Name: X102MA_Bay Trail-M		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 64 of 98		

Screw Hole & SMT Nut

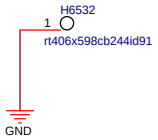
Hole A



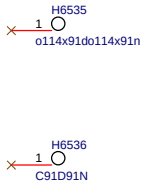
Hole B



Hole H

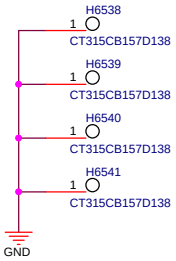


Hole D



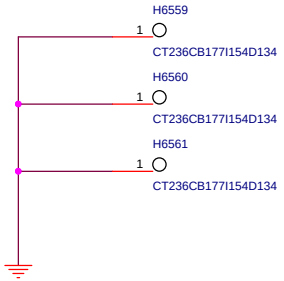
Hole E

Hole F



Hole G

*DGPU * 3*



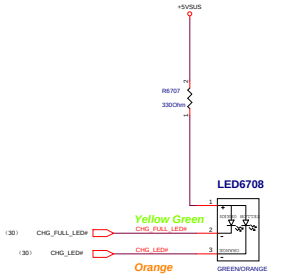
ASUSTeK COMPUTER INC.	Title : SCREW HOLE & NUT	
	Engineer: SZ_SYS2	
Size: A3	Project Name: X551CA	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 65 of 98	

<Core Design>

ASUSTek Computer Inc.	Title : DAU CONN	
	Engineer: C. A. Lai	
Size: A2	Project Name: X102MA_Bay Trail-M	Rev: 1.0G
Date: Friday, March 14, 2014	Sheet 66 of 98	

LED indicator

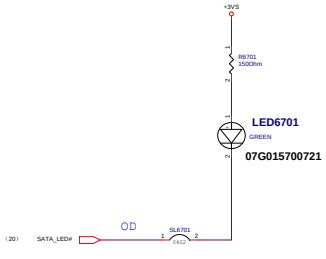
Charger LED



IF = 6~10.67mA
VF Min. = 1.7V
VF Max. = 2.4V

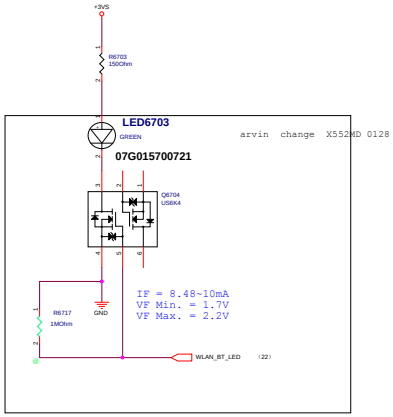
07G015701358

HDD LED



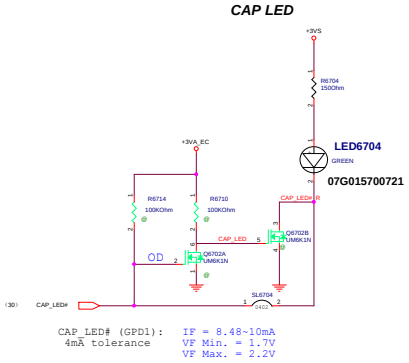
IF = 8.48~10mA
VF Min. = 1.7V
VF Max. = 2.2V

WIRELESS/ BT LED



IF = 8.48~10mA
VF Min. = 1.7V
VF Max. = 2.2V

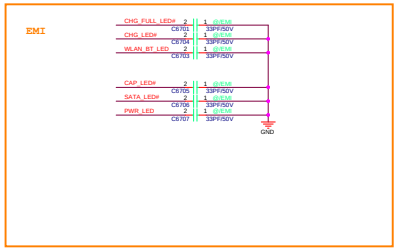
CAP LED



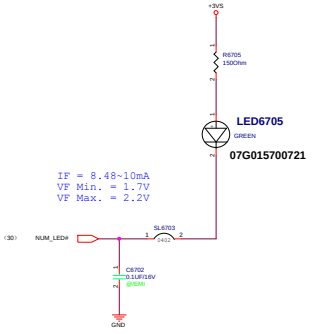
CAP_LED# (GPD1): 4mA tolerance

IF = 8.48~10mA
VF Min. = 1.7V
VF Max. = 2.2V

EMI

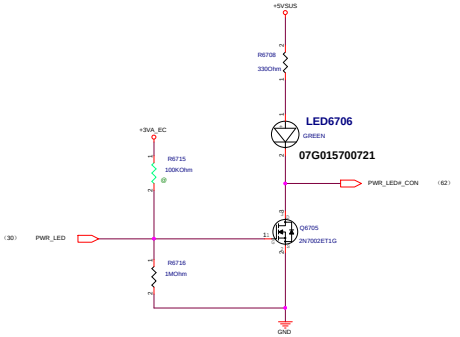


NUM LED

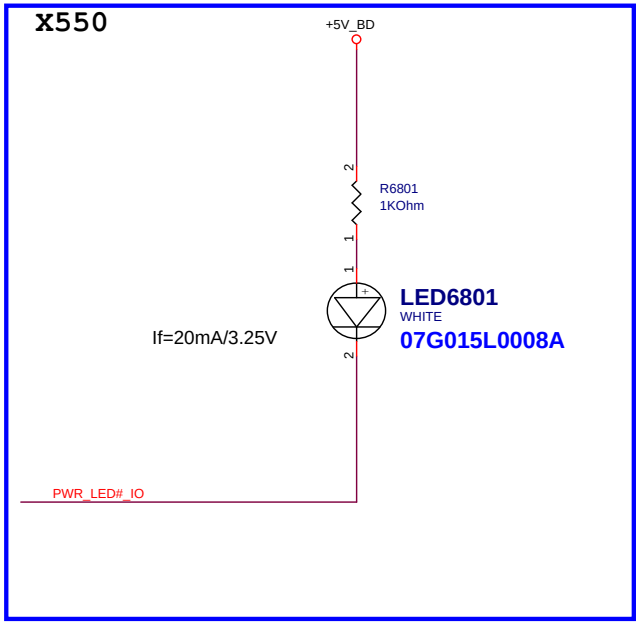


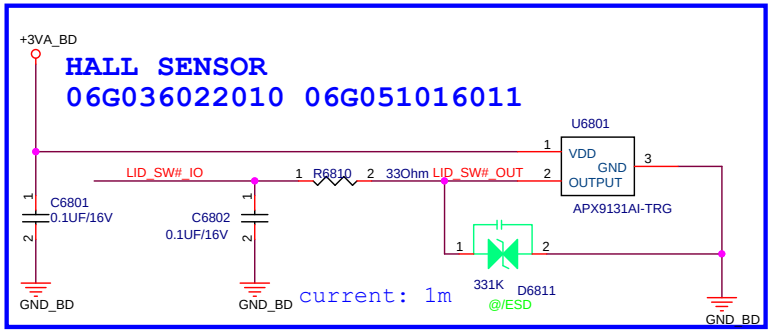
IF = 8.48~10mA
VF Min. = 1.7V
VF Max. = 2.2V

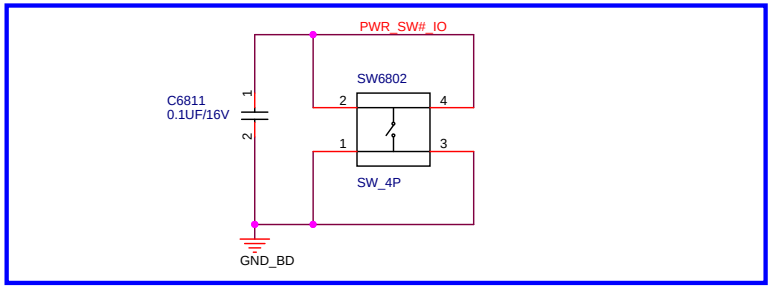
POWER LED

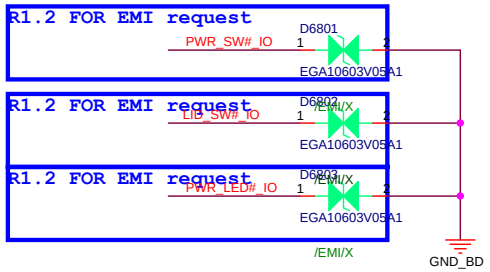


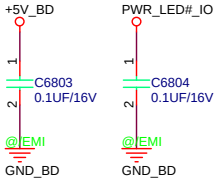
ASUSTeK COMPUTER INC.	Title : LED indicator		
	Engineer: SZ_SYS2		
Size: D	Project Name: X551CA		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 67 of 68		

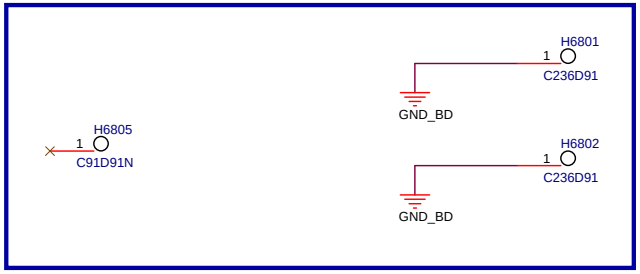


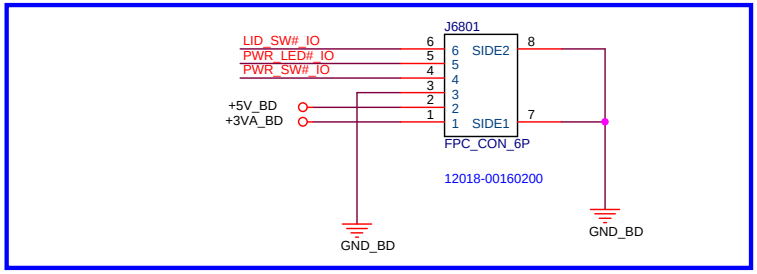












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ASUSTeK COMPUTER INC.

Title : PWR_SW&HALL_SW

Engineer: SZ2_Team3

Size	Project Name	Rev
B	X550LC	1.0

Date: Friday, March 14, 2014 Sheet 68 of 98

Title :	EMI
ASUSTeK COMPUTER INC.	Engineer: SZ_SYS2
Size: A	Project Name: X551CA
Rev: 1.0	
Date: Friday, March 14, 2014	Sheet 69 of 98

ARVIN CHANGE 0312

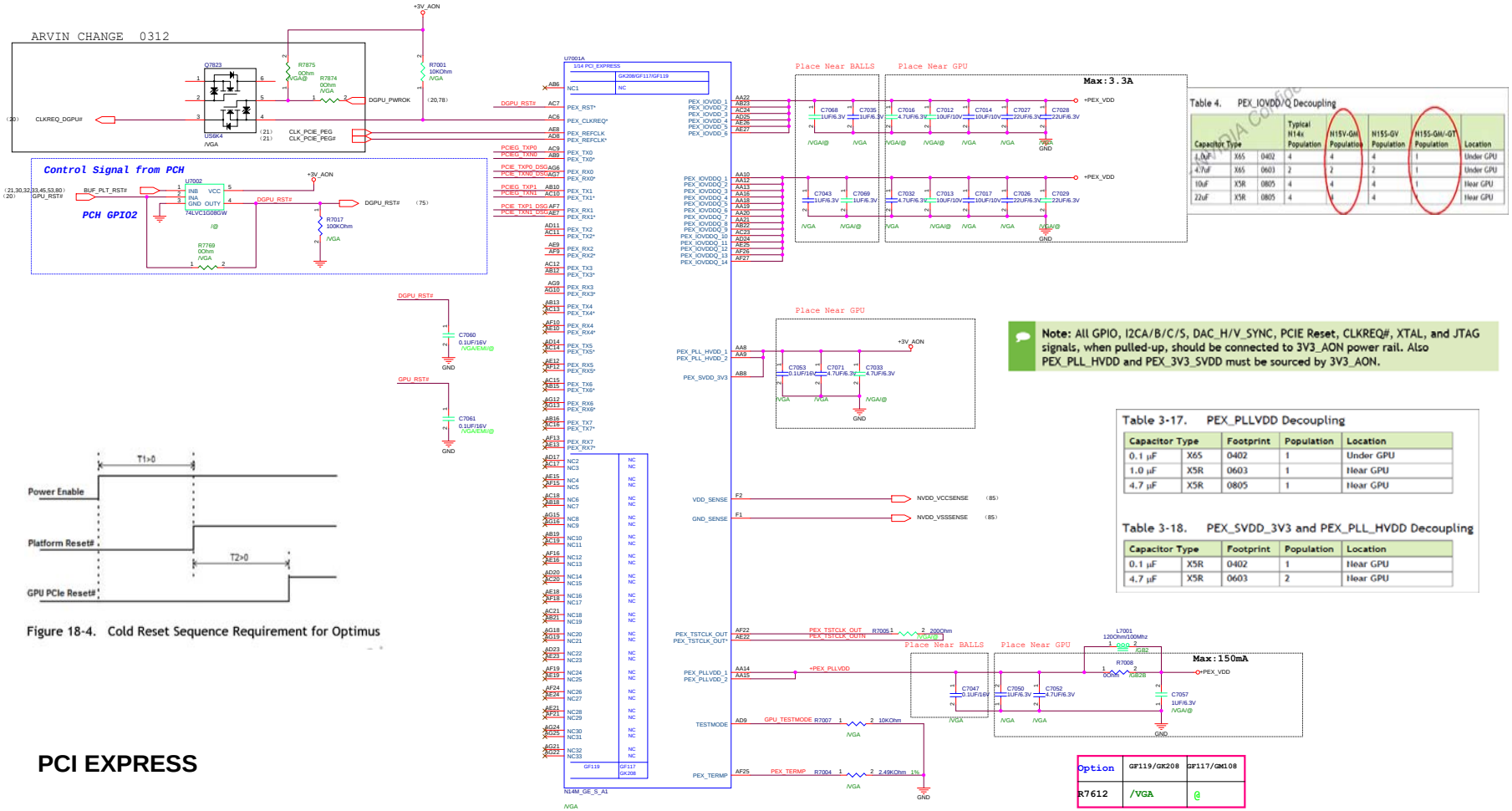


Table 4. PEX_IOVDD/Q Decoupling

Capacitor Type		Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
1.0uF	X6S 0402	4	4	4	1	Under GPU
4.7uF	X6S 0603	2	2	2	1	Under GPU
10uF	X5R 0805	4	4	4	1	Near GPU
22uF	X5R 0805	4	4	4	1	Near GPU

Note: All GPIO, I2CA/B/C/S, DAC_H/V_SYNC, PCIE Reset, CLKREQ#, XTAL, and JTAG signals, when pulled-up, should be connected to 3V3_AON power rail. Also PEX_PLL_HVDD and PEX_3V3_SVDD must be sourced by 3V3_AON.

Table 3-17. PEX_PLLVDD Decoupling

Capacitor Type	Footprint	Population	Location
0.1 µF X6S	0402	1	Under GPU
1.0 µF X5R	0603	1	Near GPU
4.7 µF X5R	0805	1	Near GPU

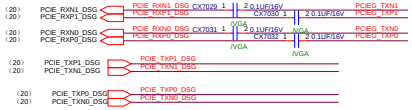
Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

Capacitor Type	Footprint	Population	Location
0.1 µF X5R	0402	1	Near GPU
4.7 µF X5R	0603	2	Near GPU

Figure 18-4. Cold Reset Sequence Requirement for Optimus

Option	GF119/GK208	GF117/GM108
R7612	/VGA	@

PCI EXPRESS



<Variant Name>

Title : VGA PCIE(1)

ASUSTek Computer Inc. Engineer: SZ_SYS2

Size: Custom | Project Name: X550 | Rev: 1.0

Date: Friday, March 14, 2014 | Sheet 70 of 98

GPU MEMORY INTERFACE: PARTITION A

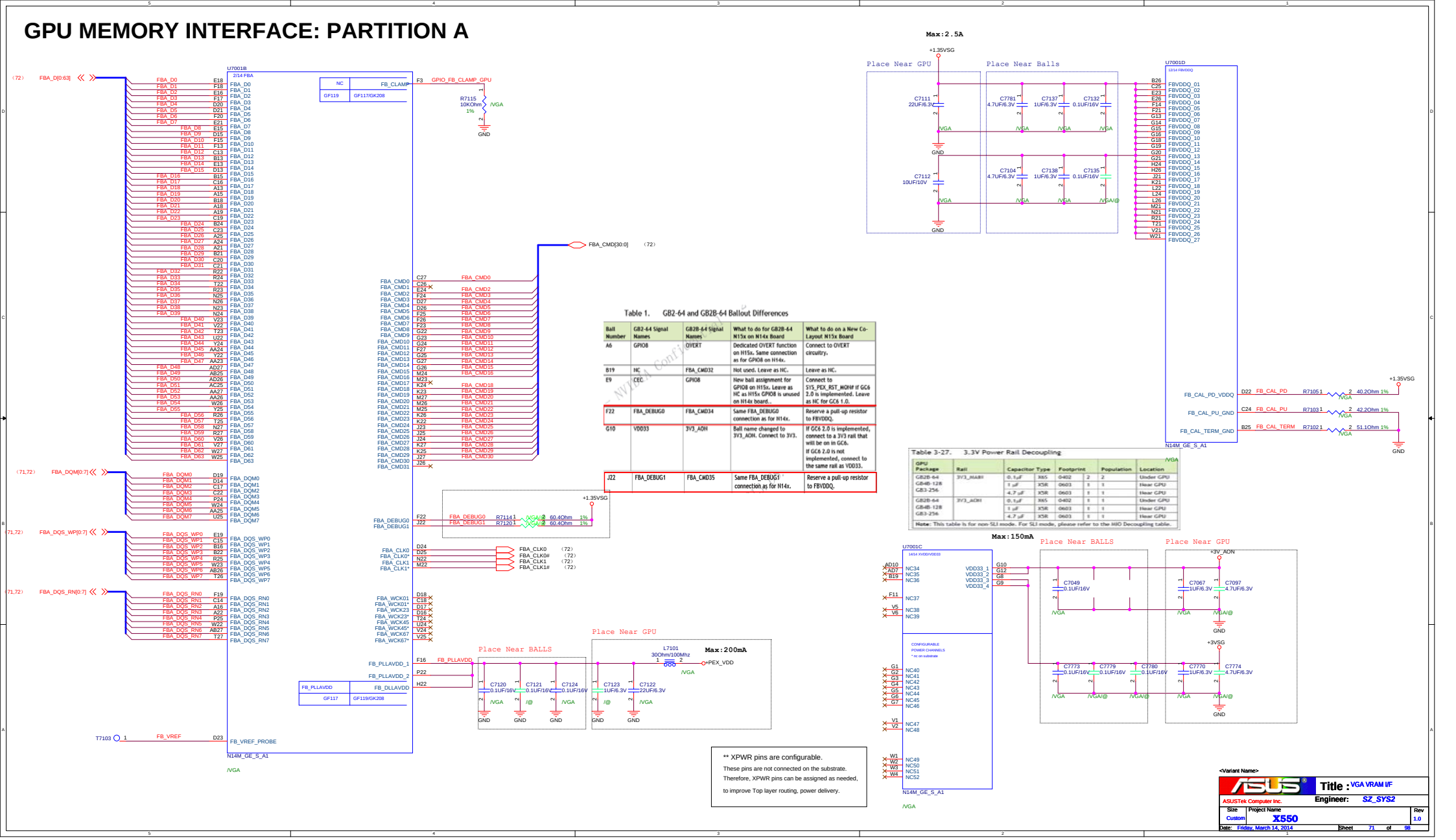


Table 1. GB2-64 and GB2B-64 Ballout Differences

Ball Number	GB2-64 Signal Names	GB2B-64 Signal Names	What to do for GB2B-64 N15x on N14x Board	What to do on a New Co-Layout N15x Board
A6	GPIO8	OVERT	Dedicated OVERT function on H15x. Same connection as for GPIO8 on H14x.	Connect to OVERT circuitry.
B19	NC	FBA_CMD32	Not used. Leave as NC.	Leave as NC.
E9	CEC	GPIO8	New ball assignment for GPIO8 on H15x. Leave as NC as H15x GPIO8 is unused on H14x board..	Connect to SYS_PEX_RST_MGHF if GC6 2.0 is implemented. Leave as NC for GC6 1.0.
F22	FBA_DEBUG0	FBA_CMD34	Same FBA_DEBUG0 connection as for H14x.	Reserve a pull-up resistor to FBVDDQ.
G10	VDD33	3V3_AON	Ball name changed to 3V3_AON. Connect to 3V3.	If GC6 2.0 is implemented, connect to a 3V3 rail that will be on in GC6. If GC6 2.0 is not implemented, connect to the same rail as VDD33.
J22	FBA_DEBUG1	FBA_CMD35	Same FBA_DEBUG1 connection as for H14x.	Reserve a pull-up resistor to FBVDDQ.

Table 3-27. 3.3V Power Rail Decoupling

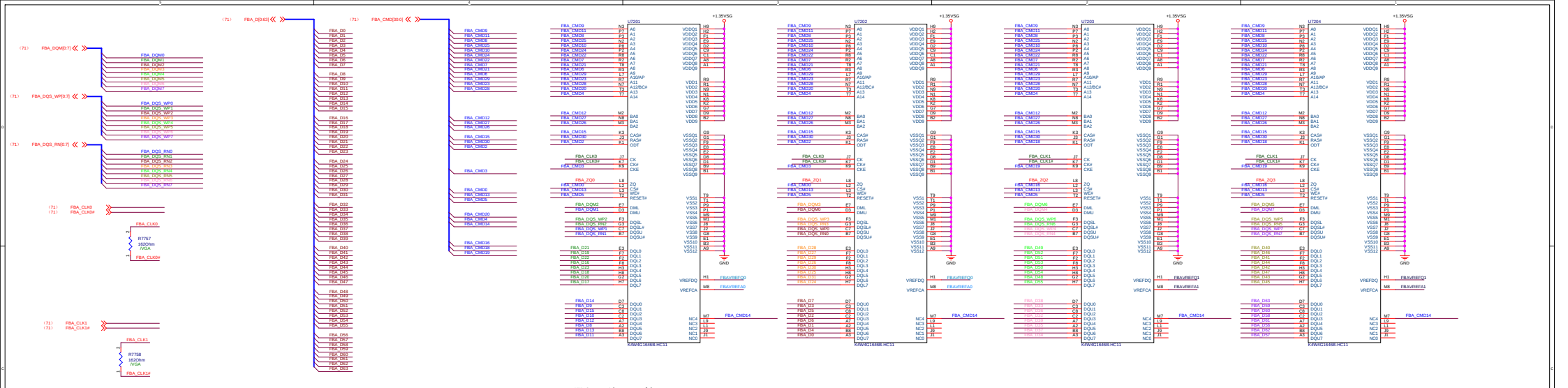
GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

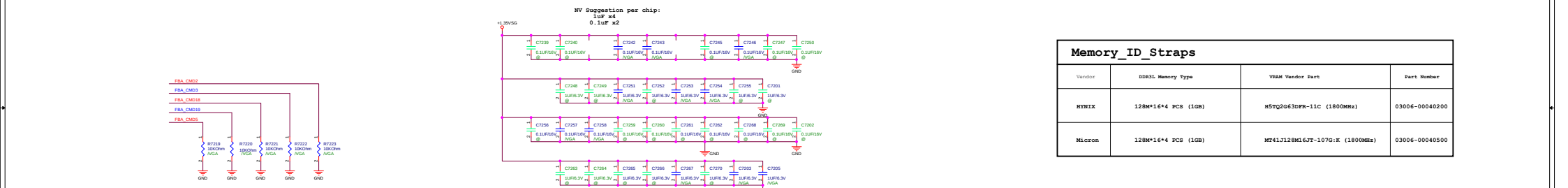
Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

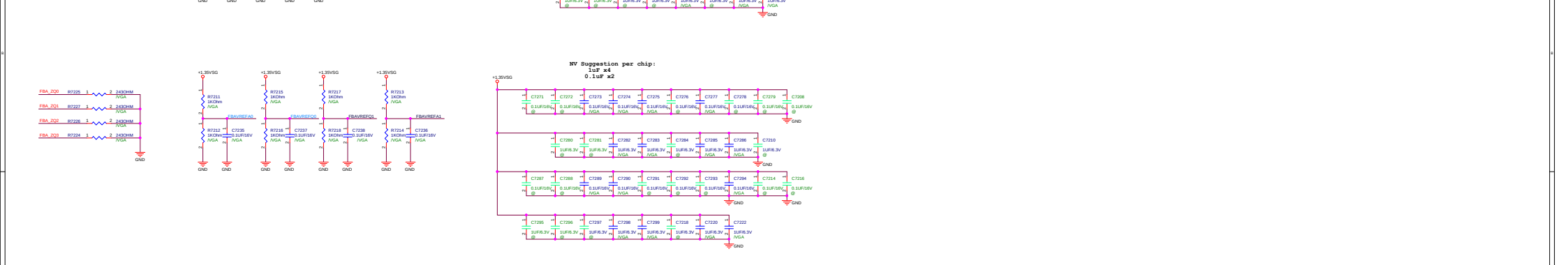
** XPWR pins are configurable.
These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

Title :	VGA VRAM I/F
Engineer:	SZ_SYS2
Project Name	X550
Size	Custom
Rev	1.0
Date:	Friday, March 14, 2014
Sheet	71 of 98

ASUSTek Computer Inc.







Memory_ID_Straps

Vendor	DDR3L Memory Type	VRAM Vendor Part	Part Number
HYNIX	128M*16*4 PCS (1GB)	H5TQ2G63DFR-11C (1800MHz)	03006-00040200
Micron	128M*16*4 PCS (1GB)	MT41J128M16JT-107G:K (1800MHz)	03006-00040500

<Variant Name>

Title : VGA VRAM CH_A1

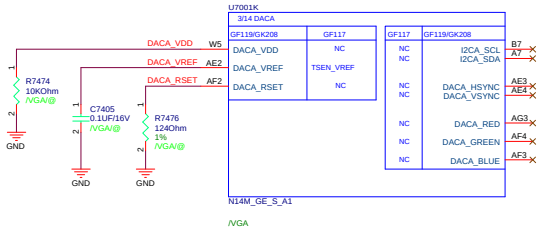
ASUSTek Computer Inc.

Engineer: SZ_SYS2

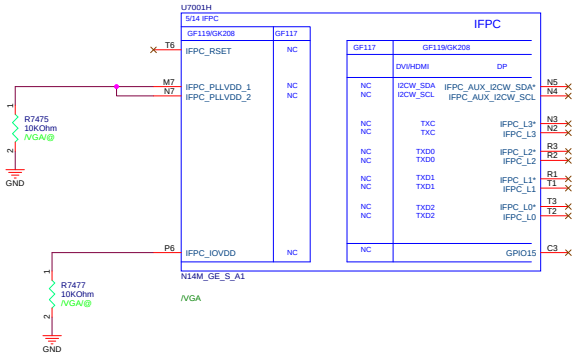
Size	Project Name	Rev
Custom	X550	1.0

Date: Friday, March 14, 2014 Sheet 73 of 98

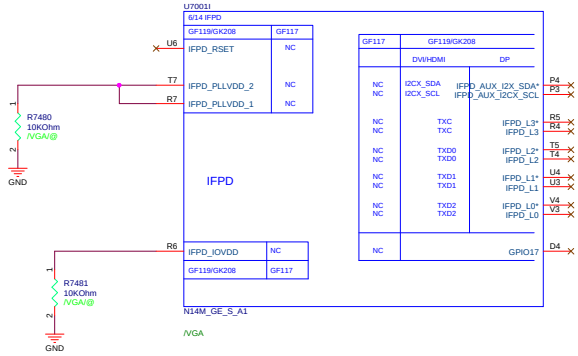
CRT DAC_A



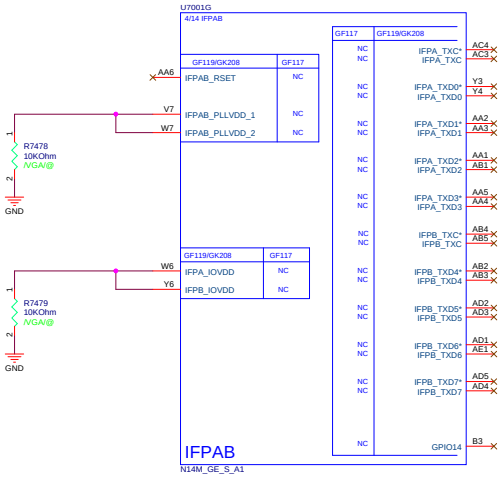
DP(link C)



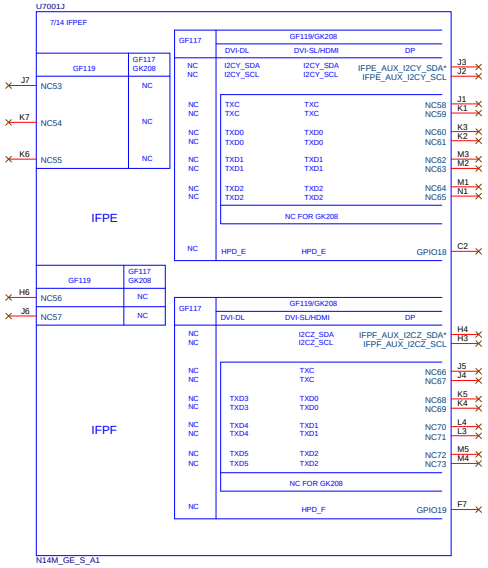
DVI(link D)



LVDS IFPA/B



LVDS IFPE/F



<Variant Name>

ASUSTek Computer Inc.

Title : VGA DAC/LVDS/HDMI

Engineer: SZ_SYS2

Size	Project Name	Rev
Custom	X550	1.0

Date: Friday, March 14, 2014 Sheet 74 of 98

Table 12-1. G82B-64 and G84B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MOH	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EN	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AON or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing	10K pull-up to 3V3_AON
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#*	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdrawn input	100K pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#*	O	GPU PCIe self-reset control	10K pull-up to 3V3_AON

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AON

Table 114. G82-64 and GB4-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MOH	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: Strap to boot FBVDD/Q
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 K pull-down
GPIO5	Reserved			
GPIO6	FB_CLAMP_TGL_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100 K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Catastrophic Over Temperature	100 K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100 K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdrawn input	100 K pull-up
GPIO13	PSI	O	Phase Shedding	PSI: 10k pull-up to enable two phase. - - -
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 73
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 73
GPIO16	FRM_LCK	O	JT Frame Lock signal	See Figure 73
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 73
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 73
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB used as DisplayPort	See Figure 73
GPIO20	Reserved			
GPIO21	Reserved			

• GPIO20 and GPIO21 are only available on N14M-LP/-GS/-IE/-IS & N14P-GV/-GV2
• The greyed out section of Table 107 indicates GPIOs that are not available for N14M-GE/-GL

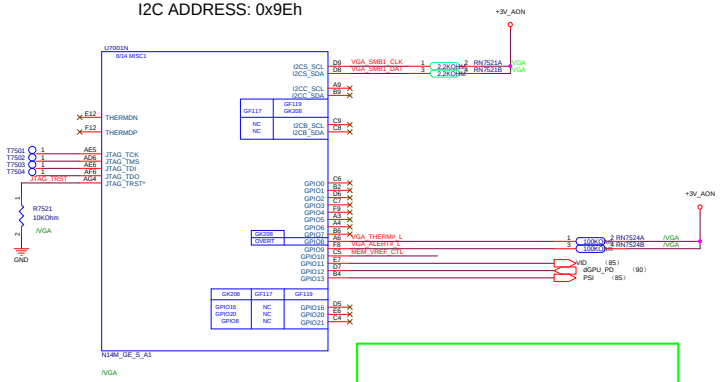
Table 7. GPIO Differences

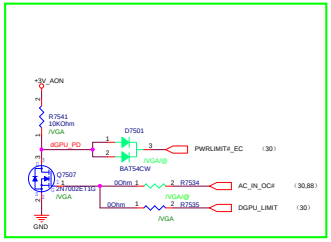
GPIO Pin	GPU	Normal Function	Comments
GPIO0	N15V-GM	RESERVED	Leave as NC
	N15S-GV	FB_CLAMP_MOH	Connect to FB_CLAMP_MOH circuitry.
	N15S-GM/-GT	FB_CLAMP_MOH in N14x systems; or GC6_FB_EN in N15x systems	If N15S-GM/-GT are designed into N14x motherboard with GC6 1.0, connect GPIO0 to FB_CLAMP_MOH circuitry. If N15S-GM/-GT are designed into N15x motherboard with GC6 2.0, use GPIO0 as the GC6_FB_EN function.
GPIO5	N15V-GM N15S-GV	RESERVED	Leave as NC
	N15S-GM/-GT	RESERVED in N14x systems; or 3V3_MAIN_EN in N15x systems	If N15S-GM/-GT are designed into N14x motherboard with GC6 1.0, leave GPIO5 as NC. If N15S-GM/-GT are designed into N15x motherboard with GC6 2.0, use GPIO5 as the 3V3_MAIN_EN function.
GPIO6	N15V-GM	RESERVED	Leave as NC
	N15S-GV	FB_CLAMP_TGL_REQ#	Connect to FB_CLAMP_TGL_REQ# circuitry.
	N15S-GM/-GT	FB_CLAMP_TGL_REQ# in N14x systems; or GPU_EVENT# in N15x systems.	If N15S-GM/-GT are designed into N14x motherboard with GC6 1.0, connect GPIO6 to FB_CLAMP_TGL_REQ# circuitry. If N15S-GM/-GT are designed into N15x motherboard with GC6 2.0, use GPIO6 as the GPU_EVENT# function.

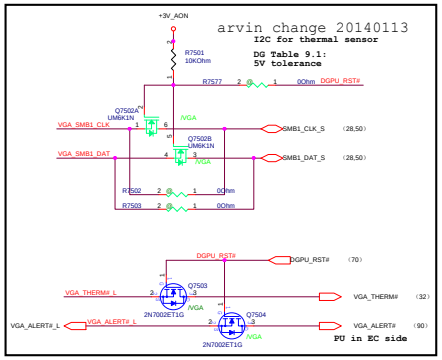
GPIO Pin	GPU	Normal Function	Comments
GPIO8	N15V-GM N15S-GV	OVERT	Connect to OVERT circuitry.
	N15S-GM/-GT	RESERVED in N14x systems; or SYS_PEX_RST_MON# in N15x systems	The OVERT function is provided on the dedicated OVERT pin on G82B-64, which is on the same pin as GPIO8 on G82-64. GPIO8 on G82B-64 is a system PEX reset monitor function for GC6 2.0. If N15S-GM/-GT are designed into N14x motherboard with GC6 1.0, leave GPIO8 as NC. If N15S-GM/-GT are designed into N15x motherboard with GC6 2.0, use GPIO8 as the SYS_PEX_RST_MON# function.
GPIO14, GPIO15, GPIO17, GPIO18, GPIO19	N15V-GM	N/A	Leave as NC
	N15S-GV N15S-GM/-GT	Display HPD	Leave as NC if HPD function is not required. See N15x Design Guide, DG-06803-001, for which IFP link should be paired with which GPIO pin for its HPD function.
GPIO16	N15V-GM	N/A	Leave as NC
	N15S-GV N15S-GM/-GT	RESERVED	Leave as NC
GPIO20	N15V-GM	N/A	Leave as NC
	N15S-GV N15S-GM/-GT	RESERVED	
GPIO21	N15V-GM	N/A	Leave as NC
	N15S-GV	RESERVED	Leave as NC
	N15S-GM/-GT	RESERVED in N14x systems; or GPU_PEX_RST_HOLD# in N15x systems	If N15S-GM/-GT are designed into N14x motherboard with GC6 1.0, leave GPIO21 as NC. If N15S-GM/-GT are designed into N15x motherboard with GC6 2.0, use GPIO21 as the GPU_PEX_RST_HOLD# function.

GPIO, TEMP SENSOR, JTAG

I2C ADDRESS: 0x9Eh







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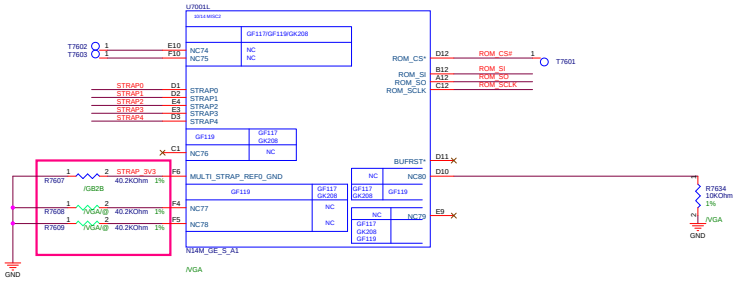
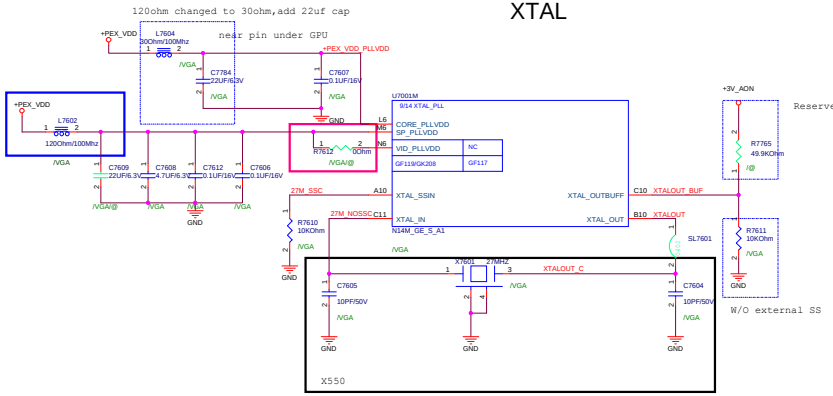
ASUSTek Computer Inc.	Title : VGA GPIO_THERM		
	Engineer: SZ_SYS2		
Size: Custom	Project Name: X550	Rev: 1.0	
Date: Friday, March 14, 2014	Sheet 75 of 86		

Option	GF119/GK208	GF117/GM108
R7612	/VGA	@

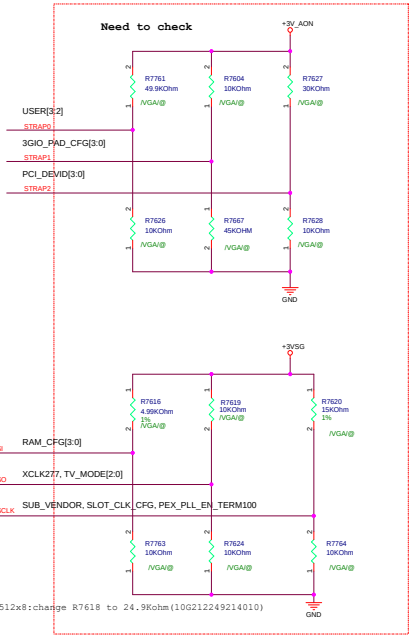


120ohm changed to 30ohm,add 22uf cap

near pin under GPU



	N14M-GE/-GL	Other N14x GPUs
Multi_Strap_Ref2_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref1_GND (Only on GB2-64 package)	No Connect	N/A
Multi_Strap_Ref0_GND	No Connect	40.2k 1% to GND
Strap Mode Selected	Binary	Multi-Lovol



DDR3 RAM_CFG

GPU SKU	GPU	VRAM Vendor	Type	F8VDD/ F8VDDQ	Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	Strap 3	Strap 2	Strap 1	Strap 0	Status
GF117	N15V-GM-B/S	Micron	DDR3	1.5V/1.5V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1234	0x1	PD 10K	PU 10K	PD 10K	PU 10K	Production ready
		Samsung	DDR3	1.5V/1.5V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x5	PD 10K	PU 10K	PD 10K	PU 10K	Production ready
		Hynix	DDR3	1.5V/1.5V	128Mx16	H5TC2G63FFR-11C	1000Mhz	NA	0XC	PU 10K	PU 10K	PD 10K	PU 10K	Production ready
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TC4G63AFR-11C	1000Mhz	NA	0x4	PD 10K	PU 10K	PD 10K	PD 10K	Production ready
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41J256M16HA-093G:E	1000Mhz	NA	0xD	PU 10K	PU 10K	PD 10K	PU 10K	Preliminary
		Hynix	DDR3L	1.35V/ 1.35V	128Mx16	H5TC2G63FFR-11C	900Mhz	NA	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Preliminary
		Micron	DDR3L	1.35V/ 1.35V	128Mx16	MT41K128M16JT-107G:K	900Mhz	NA	0x3	PD 10K	PD 10K	PD 10K	PU 10K	Preliminary
		Samsung	DDR3L	1.35V/ 1.35V	128Mx16	K4W2G1646E-BY11	900Mhz	NA	0x5	PD 10K	PU 10K	PD 10K	PU 10K	Preliminary
		Hynix	DDR3L	1.35V/ 1.35V	256Mx16	H5TC4G63AFR-11C	900Mhz	NA	0x4	PD 10K	PU 10K	PD 10K	PU 10K	Production ready
		Micron	DDR3L	1.35V/ 1.35V	256Mx16	MT41K256M16HA-107G:E	900Mhz	NA	0xD	PU 10K	PU 10K	PD 10K	PU 10K	Production ready
		Samsung	DDR3	1.5V/1.5V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x5	PD 10K	PU 10K	PD 10K	PU 10K	Production ready
		Micron	DDR3	1.5V/1.5V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1234	0x1	PD 10K	PU 10K	PD 10K	PU 10K	Production ready
		Hynix	DDR3	1.5V/1.5V	128Mx16	H5TC2G63DFR-PBC	1000Mhz	NA	0x6	PD 10K	PU 10K	PD 10K	PU 10K	Production ready
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41J256M16HA-093G:E	1000Mhz	NA	0xD	PU 10K	PU 10K	PD 10K	PU 10K	Production ready
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TC4G63AFR-11C	1000Mhz	NA	0x4	PD 10K	PU 10K	PD 10K	PU 10K	Production ready

DDR3 RAM_CFG

GPU SKU	GPU	VRAM Vendor	Type	F8VDD/ F8VDDQ	Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	ROM_SI	Status
GM108	N15S-GT/GM	Hynix	DDR3	1.5V/1.5V	128Mx16	H5TC2G63FFR-11C	1000Mhz	NA	0x6	PD 35K	Preliminary
		Micron	DDR3	1.5V/1.5V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1322	0x7	PD 45K	Preliminary
		Samsung	DDR3	1.5V/1.5V	128Mx16	K4W2G1646Q-BC1A	1000Mhz	NA	0x8	PU 5K	Preliminary
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TC4G63AFR-11C	1000Mhz	NA	0x0	PD 5K	Preliminary
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41J256M16HA-093G:E	1000Mhz	1322	0x1	PD 10K	Preliminary
		Samsung	DDR3	1.5V/1.5V	256Mx16	K4W4G1646D-HC1A	1000Mhz	NA	0x2	PD 15K	Preliminary
		DDR3L									
		Hynix	DDR3L	1.35V/ 1.35V	128Mx16	H5TC2G63FFR-11C	900Mhz	NA	0x9	PU 10K	Preliminary
		Micron	DDR3L	1.35V/ 1.35V	128Mx16	MT41J128M16JT-093G:K	900Mhz	1322	0xA	PU 15K	Preliminary
		Samsung	DDR3L	1.35V/ 1.35V	128Mx16	K4W2G1646Q-BC1A	900Mhz	NA	0xB	PU 20K	Preliminary
		Hynix	DDR3L	1.35V/ 1.35V	256Mx16	H5TC4G63AFR-11C	900Mhz	NA	0x3	PD 20K	Preliminary
		Micron	DDR3L	1.35V/ 1.35V	256Mx16	MT41J256M16HA-093G:E	900Mhz	1322	0x4	PD 25K	Preliminary
		Samsung	DDR3L	1.35V/ 1.35V	256Mx16	K4W4G1646D-HC1A	900Mhz	NA	0x5	PD 30K	Preliminary
		Dual Rank(Dual-Rank Layout with Single Rank Populated									
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TC4G63AFR-11C	1000Mhz	NA	0x0	PD 5K	Preliminary
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41J256M16HA-093G:E	1000Mhz	1322	0x1	PD 10K	Preliminary
		Samsung	DDR3	1.5V/1.5V	256Mx16	K4W4G1646D-HC1A	1000Mhz	NA	0x2	PD 15K	Preliminary
		Hynix	DDR3L	1.35V/ 1.35V	256Mx16	H5TC4G63AFR-11C	900Mhz	NA	0x3	PD 20K	Preliminary
		Micron	DDR3L	1.35V/ 1.35V	256Mx16	MT41J256M16HA-093G:E	900Mhz	1322	0x4	PD 25K	Preliminary
		Samsung	DDR3L	1.35V/ 1.35V	256Mx16	K4W4G1646D-HC1A	900Mhz	NA	0x5	PD 30K	Preliminary

<Variant Name>

Title : VGA XTAL

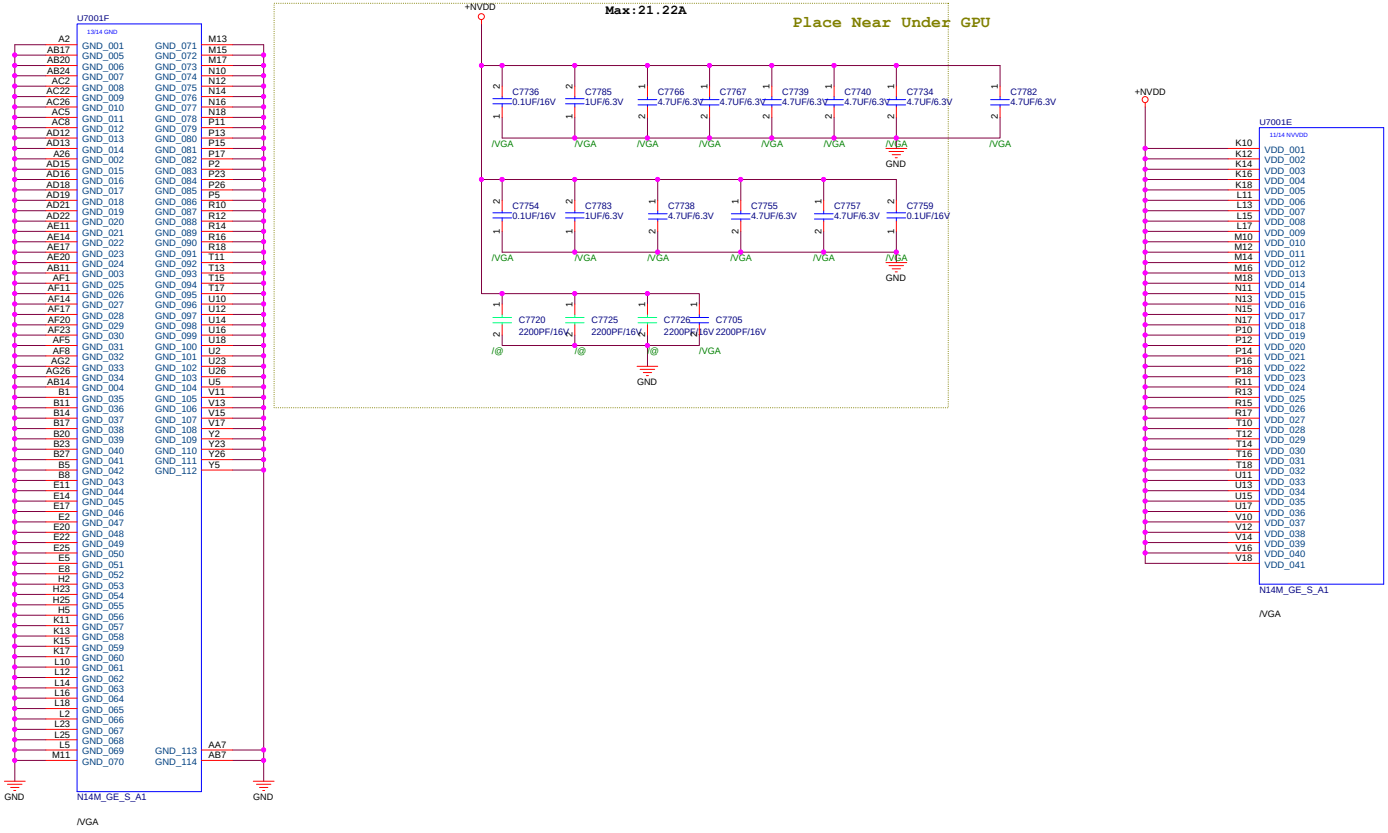
ASUSTek Computer Inc. Engineer: SZ_SYS2

Size: Custom | Project Name: X550 | Rev: 1.0

Date: Friday, March 14, 2014 | Sheet 76 of 98

NVVDD GROUND

NVVDD POWER AND DECOUPLING



<variant_name>

ASUSTek Computer Inc.

Title : VGA PWR_GND

Engineer: SZ_SYS2

Size	Project Name	Rev
C	X550	1.0

Date: Friday, March 14, 2014 Sheet 77 of 98

GPU IO Power Enable

D7705 BAT54CW /VGA

+1.05VS_PWRGD (84,87,91)

DGPU_PWR_EN (20) — **GPIO1 High Active**

R7012 2 /VGA 1 0Ohm — GPU_PWRON_3.3VSG_IO

R7723 100KOhm /VGA/@ — GND

+12VSUS

R7709 100KOhm /VGA

R7710 100KOhm /VGA — GPU_PWRON_3.3V_AON — GPU_PWRON_3.3V_AON

GPU_DSG — Q7810B UM6K1N /VGA

GPU_PWRON_3.3VSG_IO — Q7810A UM6K1N /VGA

C7721 0.01UF/16V /VGA — GND

GPU Power Good

GPU_PWRON_3.3VSG_IO — 0402 — SL7702 — GPU_PWRON_3.3VSG (85)

+1.8VS — 1SS355PT1 /VGA — 2D7001

R7014 1KOhm /VGA — C7010 0.01UF/16V /VGA — GND

X550MD R1.1 ARVIN CHANGE 0307

PCH_GPIO4 — DGPU_PWROK (20,70)

R7747 1 2 0Ohm /VGA — PGOOD_NVDD (85)

X550MD R1.1 ARVIN CHANGE 0312 follow X751MD

DGPU_PWROK

+3VS — R7871 0Ohm /X — R7872 100KOhm

+PEX_VDD — R7873 10KOhm /VGA

Q7808 PMBS3904 /VGA

Q7811A EM6K1-G-T2R /VGA — Q7811B EM6K1-G-T2R /VGA

C7805 0.22UF/10V /VGA — R7816 51KOhm /VGA — GND

GPU IO Power

+3VSG — +3V_AON

+3VSUS — +3V_AON

Q7701 SI3456DDV-T1-GE3 /VGA

D7701 1SS355PT /VGA

R7704 4.7KOhm 5% /VGA — GPU_PWRON_3.3V_AON

C7719 1000PF/50V N/A — GND

+1.35VSG — +1.35V

C7712 22UF/6.3V /VGA — C7710 22UF/6.3V /VGA — C7711 22UF/6.3V /VGA — CE7701 470uF/2V /@

C7775 0.1UF/16V /VGA/EMI/@ — C7776 0.1UF/16V /VGA/EMI/@ — C7777 0.1UF/16V /VGA/EMI/@ — C7778 0.1UF/16V /VGA/EMI/@ — C7787 0.1UF/16V /VGA/EMI/@ — C7789 0.1UF/16V /VGA/EMI/@ — C7790 0.1UF/16V /VGA/EMI/@

GND

+1.05VS — +PEX_VDD

Q7704 NTMFS4955NT1G /VGA

D7703 1SS355PT /VGA

Q7704_Gate — R7767 1% 100KOhm/VGA — GPU_PWRON_3.3V_AON

C7786 0.022UF/25V /VGA — GND

+1.35V — +1.35VSG

Q7703 NTMFS4955NT1G /VGA

1SS355PT — D7702 /VGA

R7701 150KOhm 1% /VGA — GPU_PWRON_3.3V_AON

C7709 0.022UF/25V /VGA — GND

DSG

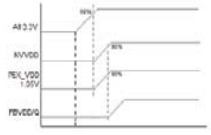
+NVDD — R7727 22Ohm /VGA — +VGA_CORE_DISCHRG — Q7802A UM6K1N /VGA

+3VSG — R7729 330Ohm /VGA — +3VSG_DISCHRG — Q7802B UM6K1N /VGA

+PEX_VDD — R7730 33Ohm /VGA — +PEX_VDD_DISCHRG — Q7803B UM6K1N /VGA

+1.35VSG — R7731 33Ohm /VGA — Q7803A UM6K1N /VGA

GPU_DSG



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Figure 3-6. Example of Power-up Sequencing Order

Note:
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.

<Variant Name>

ASUSTeK COMPUTER INC. — Title : GPU_Power_Sel — Engineer: SYS2-Team3

Size	Project Name	Rev
C	X550LC	4.0

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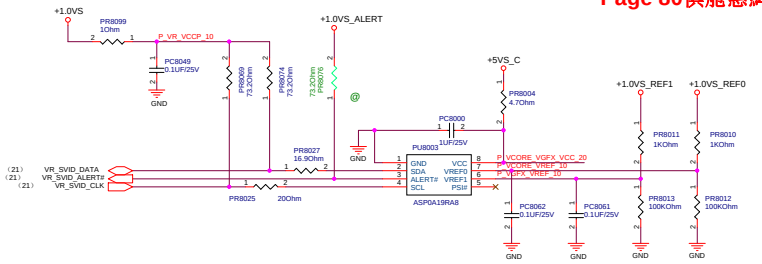
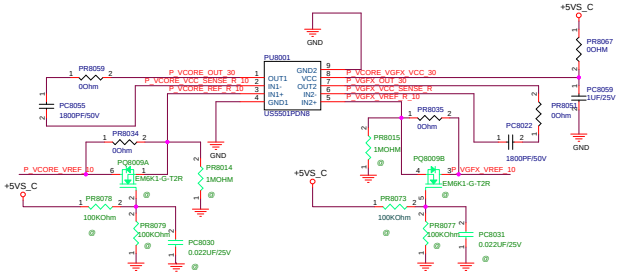
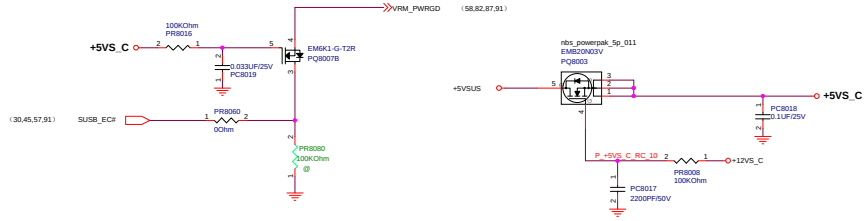
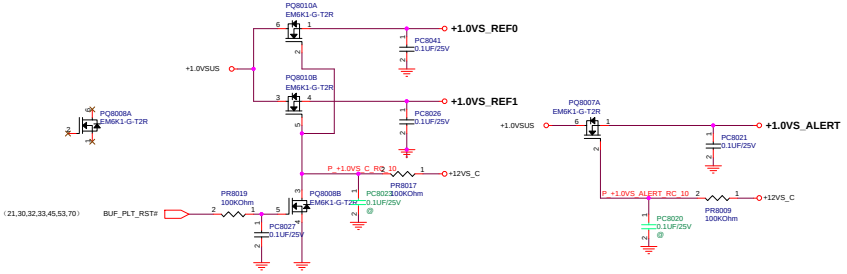
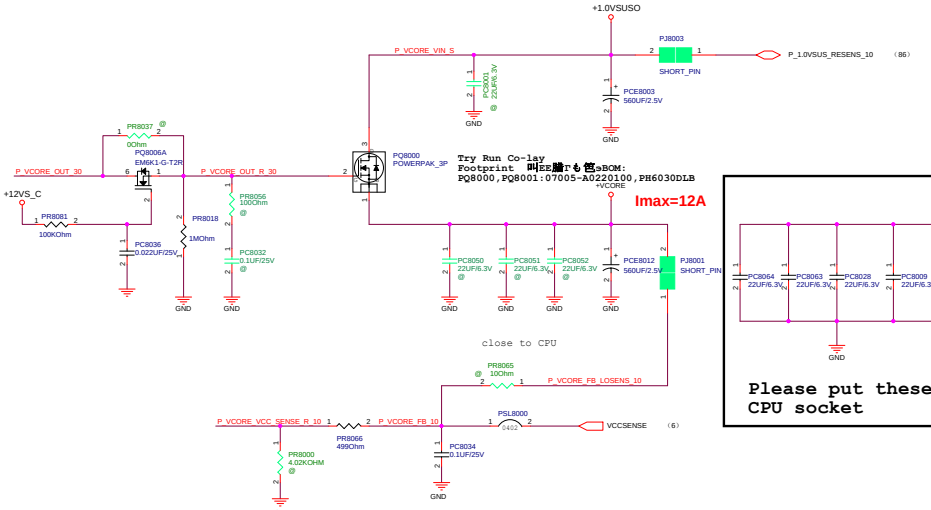
Title :	VGA_****
ASUSTeK COMPUTER INC.	Engineer: RD1_EE2-1
Size: C	Project Name: X102MA_Bay Trail-M
Rev: 1.0	
Date: Friday, March 14, 2014	Sheet 79 of 98

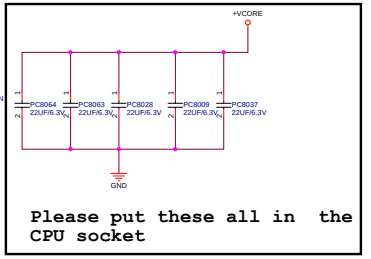


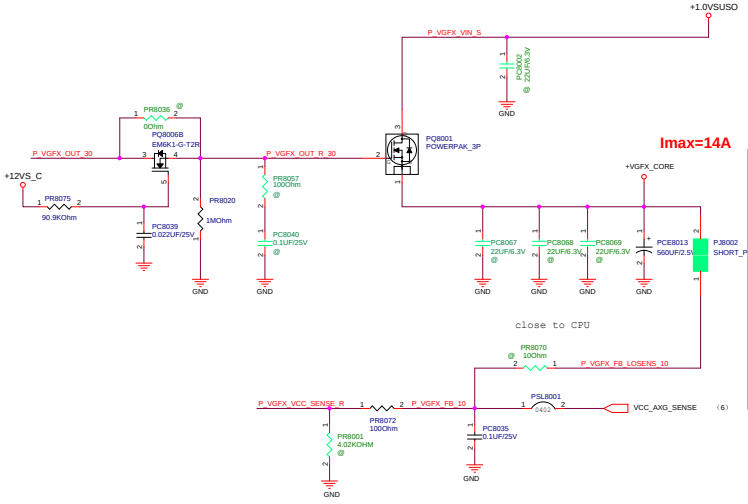


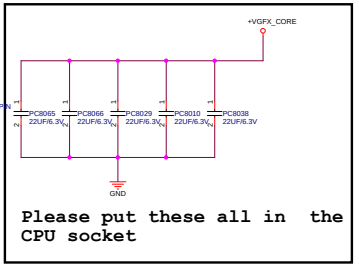






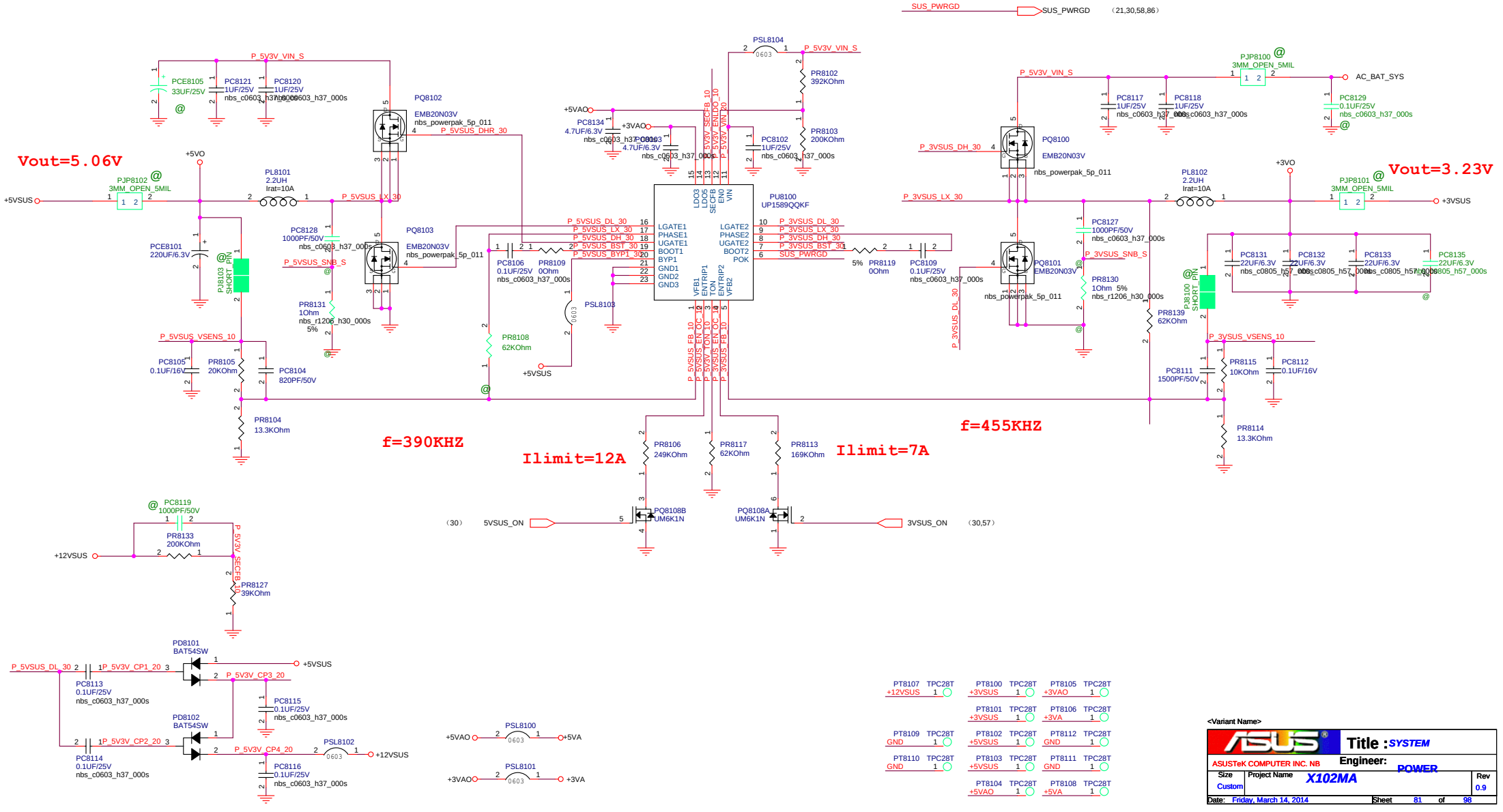




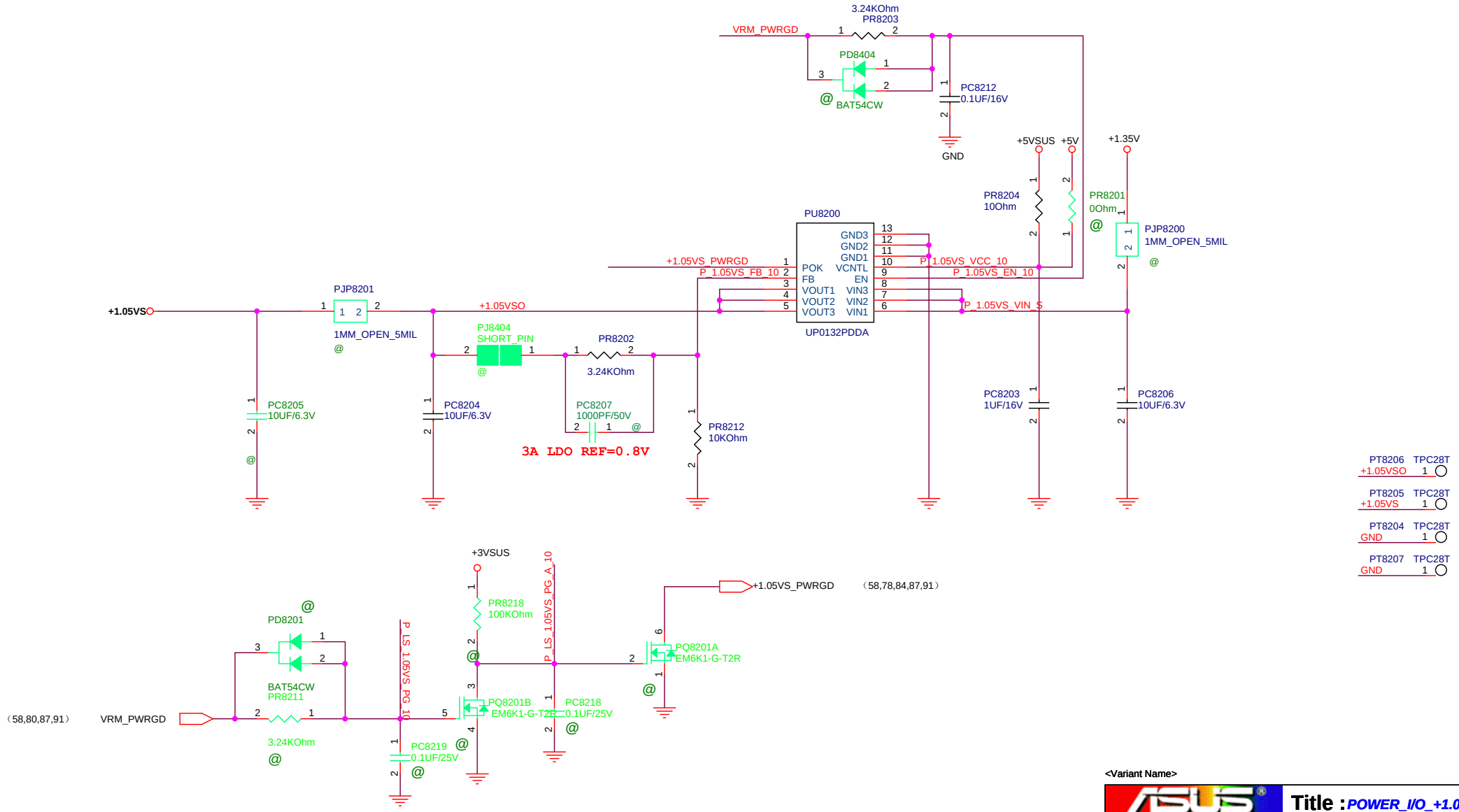


ASUSTeK COMPUTER INC.	Title : POWER_Vcore&Vgfx	
	Engineer: Power	
Size: Custom	Project Name: X102MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 80 of 86	

+3VSUS / +5VSUS [System Power]



+1.05VS POWER SUPPLY



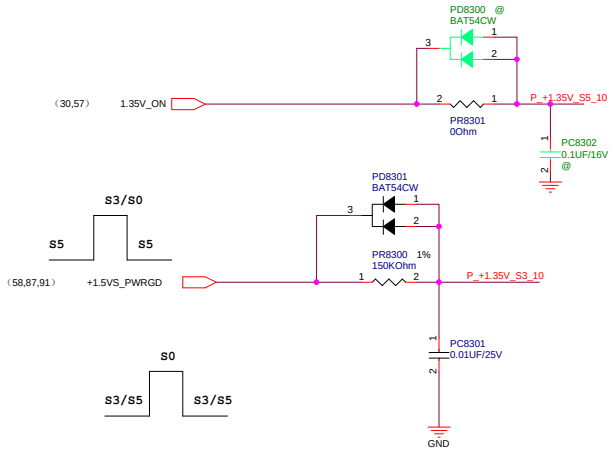
<Variant Name>

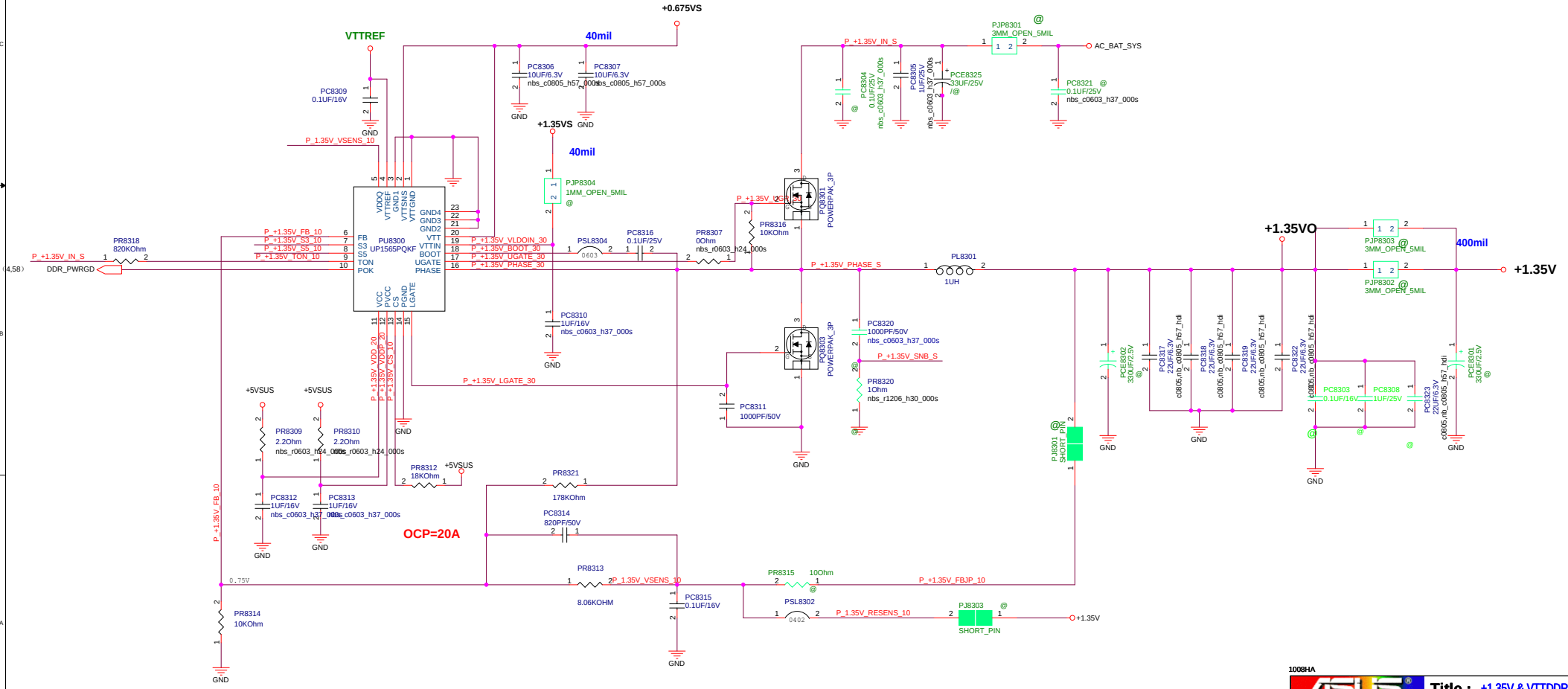
ASUSTeK COMPUTER INC.	Title : POWER_I/O_+1.05V	
	Engineer: Jeff Kao	
Size: Custom	Project Name: X102MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 82 of 98	

S3 And S5 Truth Table

State	S3	S5	VDDQ
S0	Hi	Hi	On
S3	Low	Hi	On
S4/S5	Low	Low	Off (Discharge)

State	VTTREF	VTT
S0	On	On
S3	On	Off(Hi-Z)
S4/S5	Off (Discharge)	Off (Discharge)





1008HA

ASUSTek Computer INC.

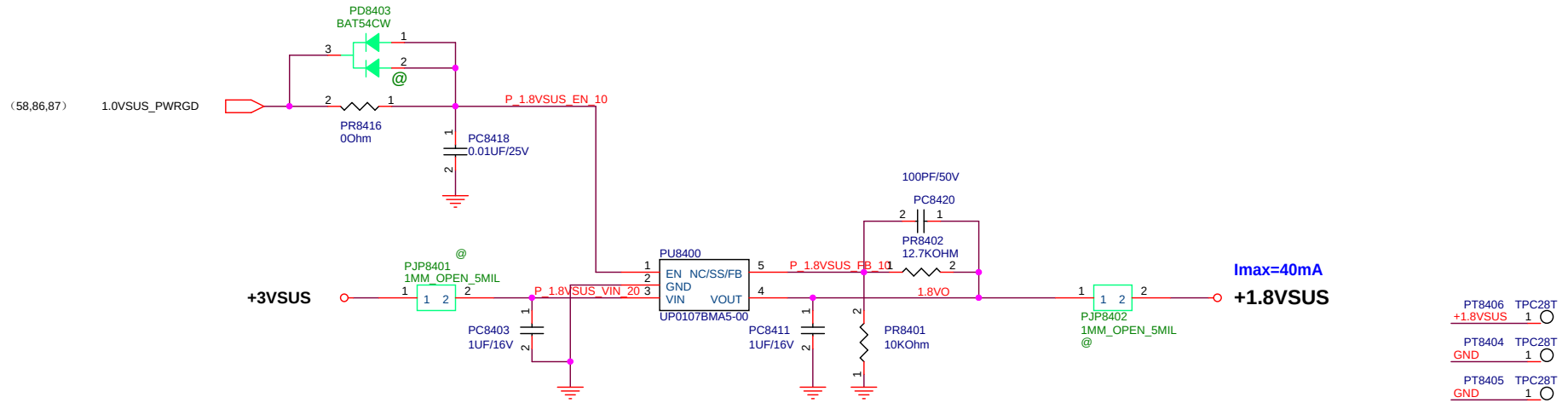
Title : +1.35V & VTTDDR

Engineer:

Size	Project Name	Rev
Custom	X102MA_Bay Trail-M	1.0

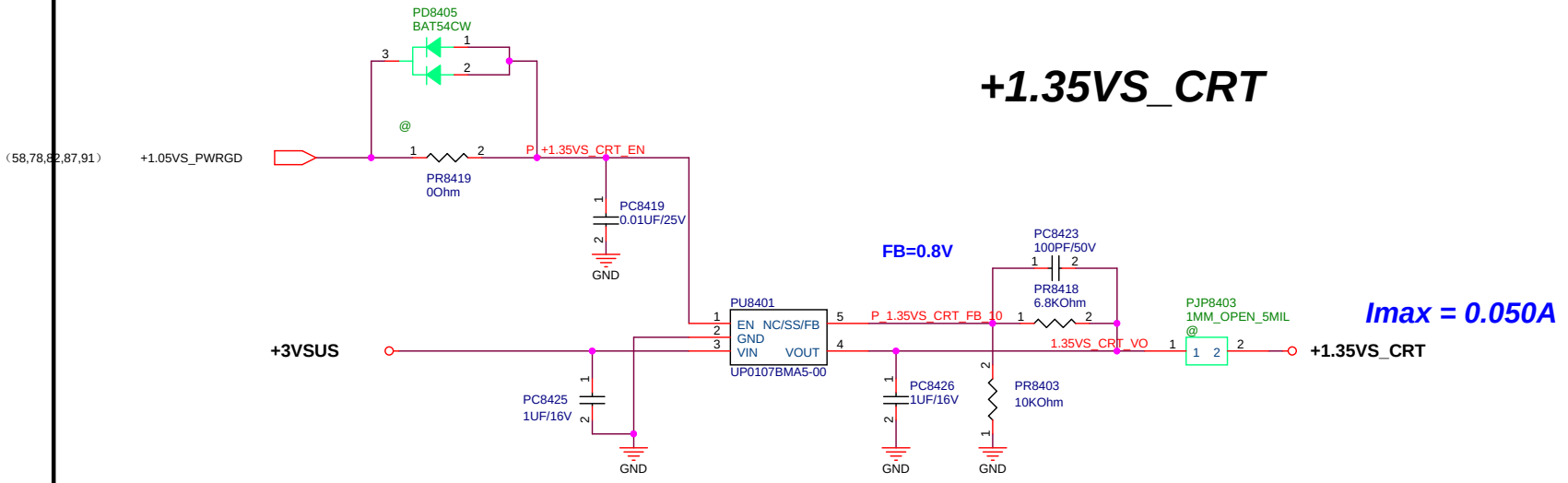
Date: Friday, March 14, 2014 Sheet 83 of 98

+1.8VSUS POWER SUPPLY

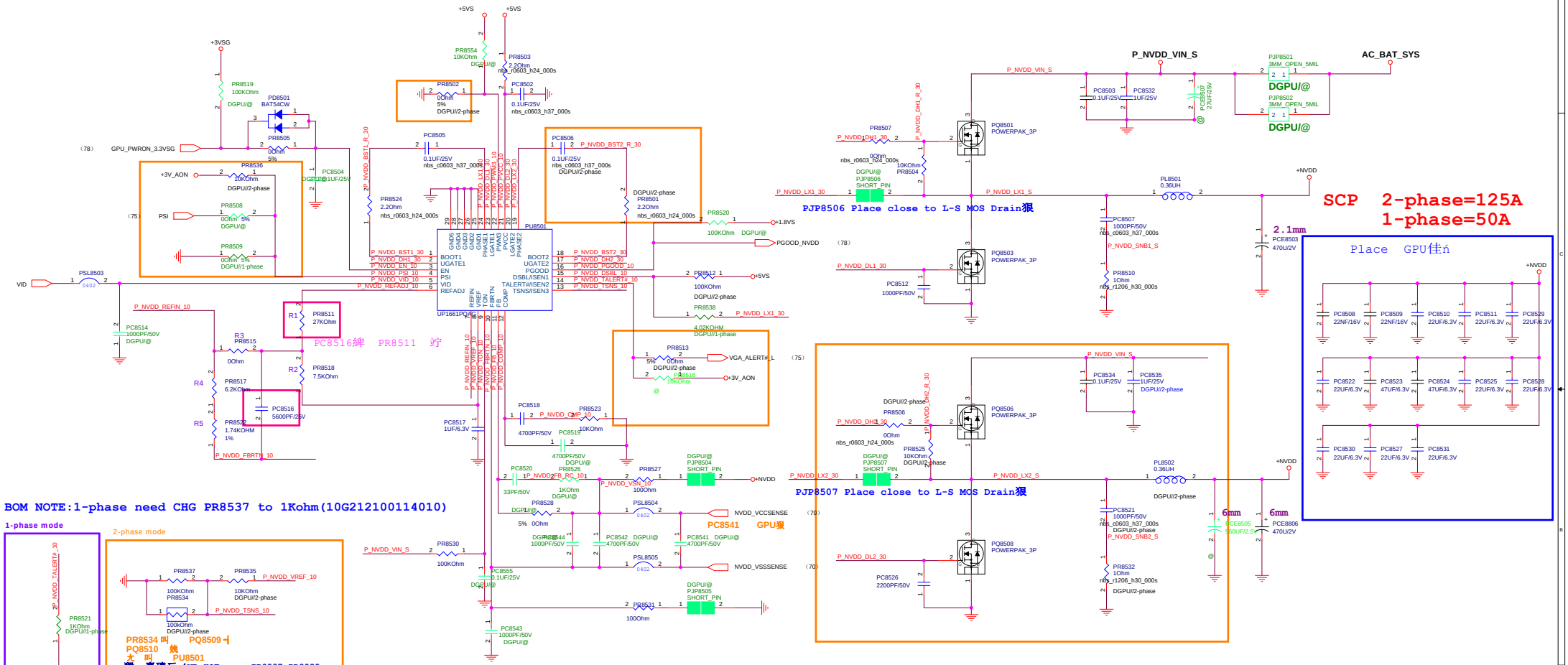


10.8

+1.35VS_CRT



ASUSTeK COMPUTER INC.	Title : PW_+1.8VA	
	Engineer:	
Size: Custom	Project Name: X200MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 84 of 98	



	Units	Config A	Config B	Config C	Config D
VBOOT	V	0.875	0.9	0.9	1.028
VMAX	V	1.2	1.2	1.15	1.15
VMIN	V	0.6	0.6	0.65	0.9
PR8511	Kohm	39	20	39	27
PR8518	Kohm	39	20	30	7.5
PR8515	Kohm	1.5	2	3	0
PR8517	Kohm	30	18	24	6.2
PR8522	Kohm	1.5	0	3	1.74
PC8516	nF	1.5	2.7	1.8	5.6

DGPU	Config
N14M-GE	C
N14M-LP	B
N14M-NS	B
N14M-GS	B
N14P-GV2	B
N14P-GV	B
N14P-LP	B
N14P-GS	B
N14P-GT	B

DGPU	Config
N15V-GM	D
N15S-GT	B

<Variant Name>

ASUSTeK COMPUTER INC.

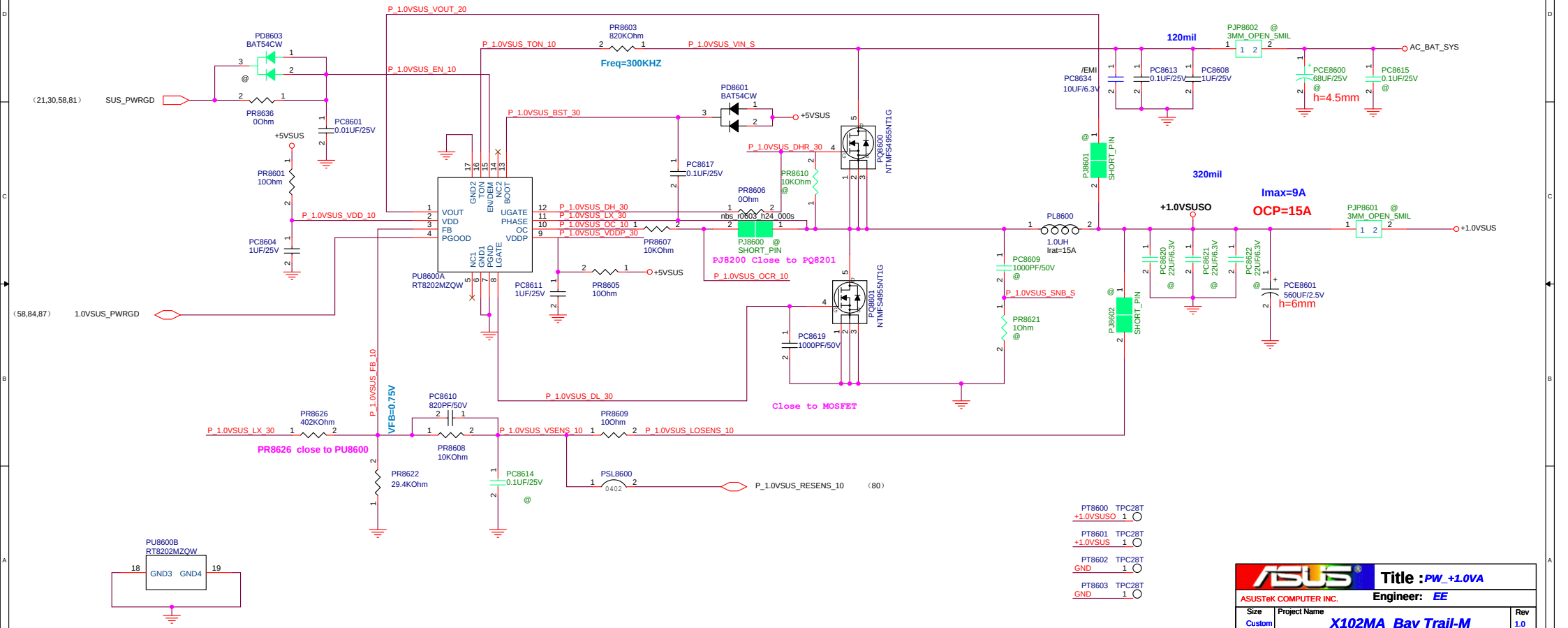
Title : NVDD

Engineer:

Size	Project Name	Rev
A2	KX_STD	R1.0

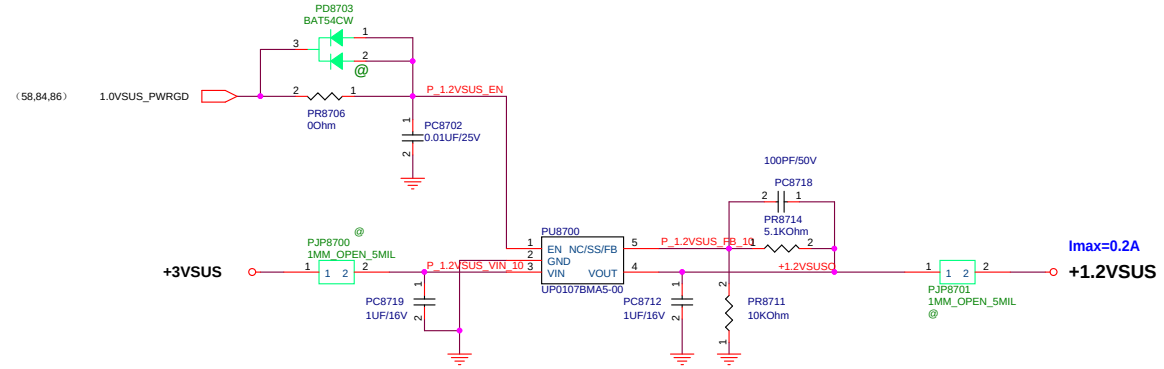
Date: Friday, March 14, 2014 Sheet 85 of 98

+1.0VSUS POWER SUPPLY



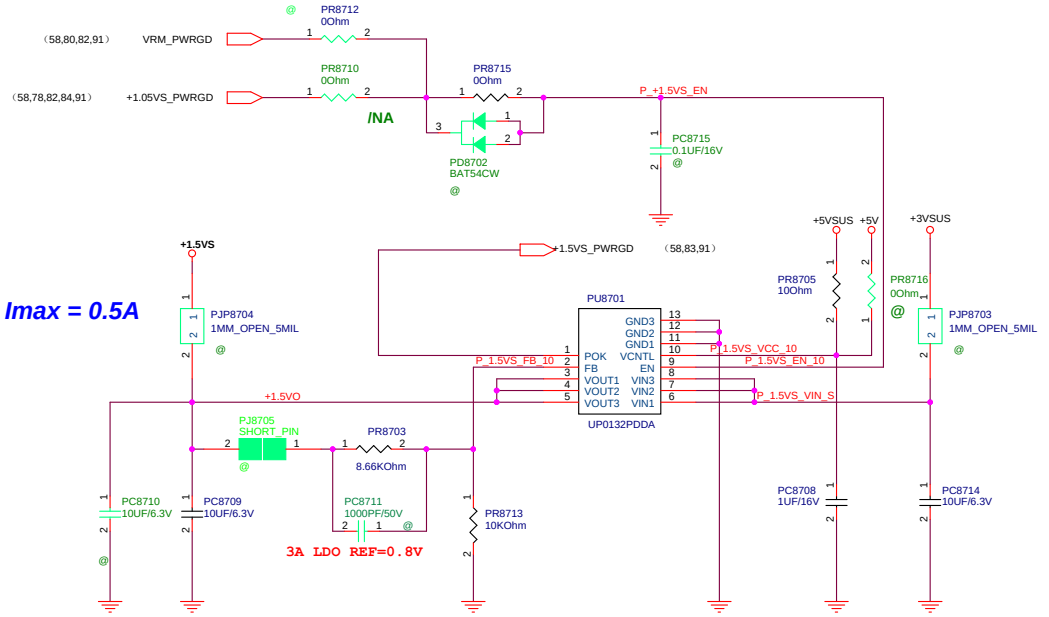
ASUSTeK COMPUTER INC.	Title : PW_+1.0VA		
	Engineer: EE		
Size: Custom	Project Name: X102MA_Bay Trail-M		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 86 of 98		

+1.2VSUS & +1.5VS POWER SUPPLY



PT8706 TPC28T +1.2VSUSO 1
PT8705 TPC28T +1.2VSUS 1
PT8704 TPC28T GND 1
PT8707 TPC28T GND 1

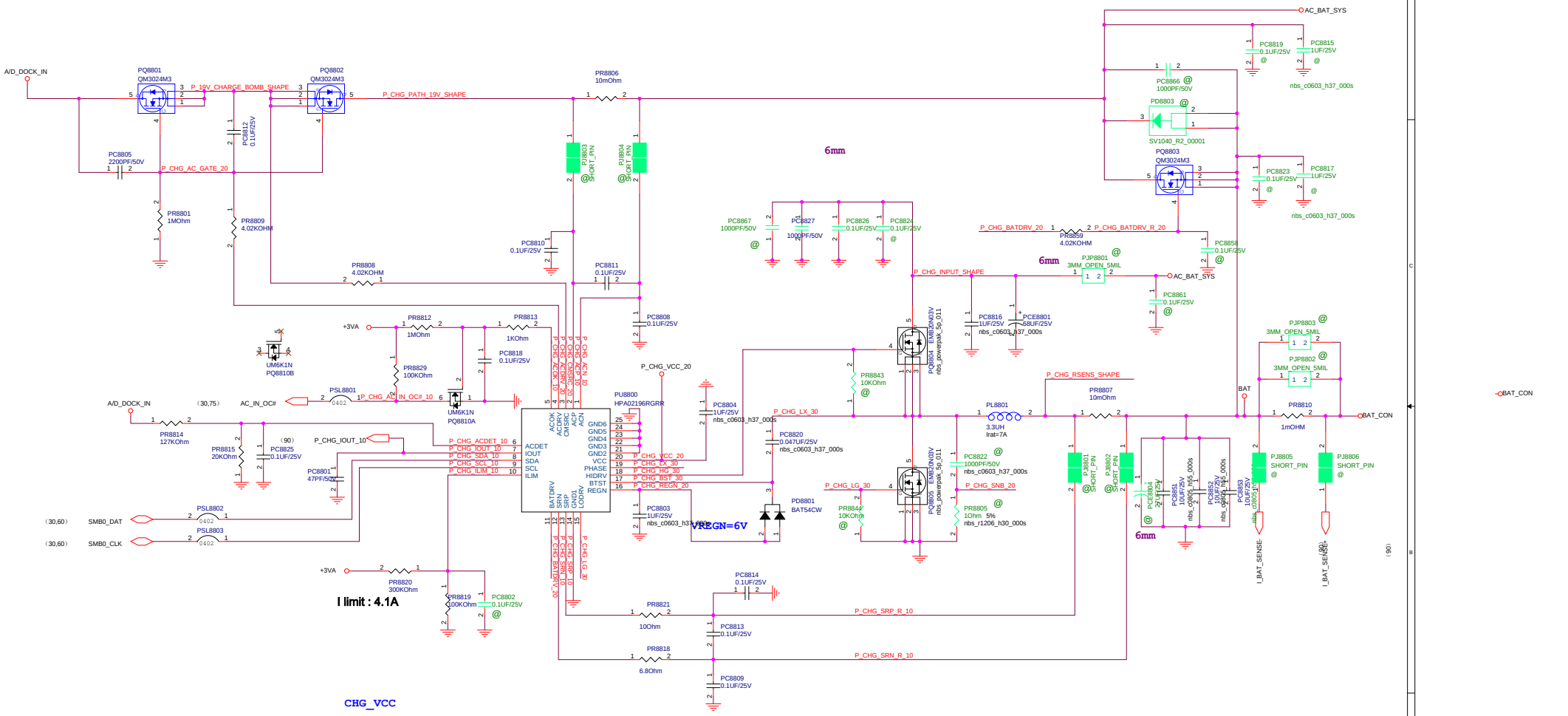
+1.5VS



PT8710 TPC28T +1.5VO 1
PT8709 TPC28T +1.5VS 1
PT8708 TPC28T GND 1
PT8711 TPC28T GND 1

<Variant Name>

ASUSTeK COMPUTER INC.	Title : PW_1.2VA&1.5VS	
	Engineer: EE	
Size: Custom	Project Name: X102MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 87 of 98	



<Variant Name>

ASUSTeK COMPUTER INC. NB3

Title : Charger

Engineer:

Size	Project Name	Rev
Custom	KX_STD	R1.2

Date: Friday, March 14, 2014 Sheet 88 of 98

<Variant Name>

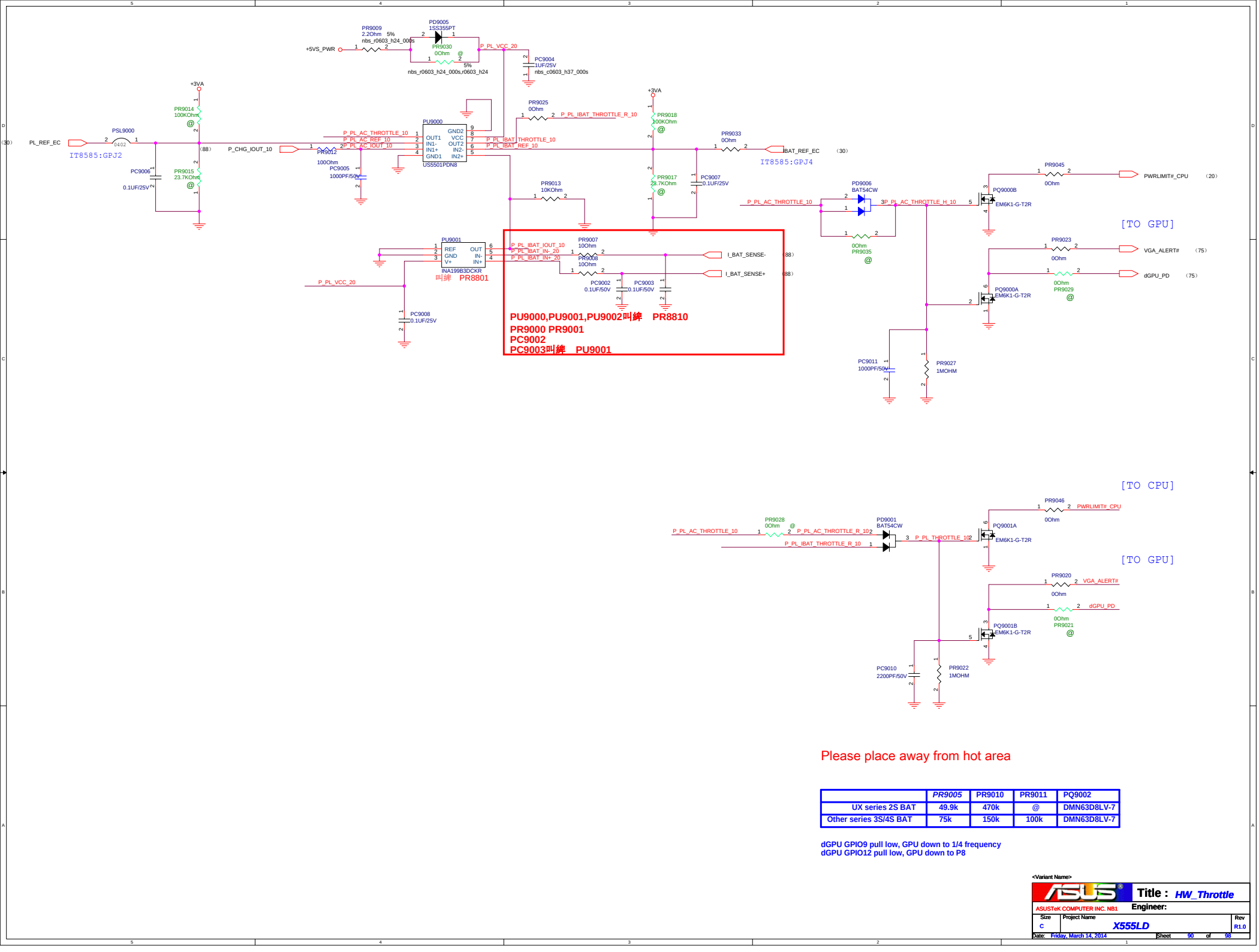
Title : POWER_+VGFX_CORE

ASUSTeK COMPUTER INC.

Engineer: RD1_EE3

Size	Project Name	Rev
Custom	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 89 of 98



Please place away from hot area

	PR9005	PR9010	PR9011	PQ9002
UX series 2S BAT	49.9k	470k	@	DMN63D8LV-7
Other series 3S/4S BAT	75k	150k	100k	DMN63D8LV-7

dGPU GPIO9 pull low, GPU down to 1/4 frequency
dGPU GPIO12 pull low, GPU down to P8

<Variant Name>

ASUSTeK COMPUTER INC. NB1

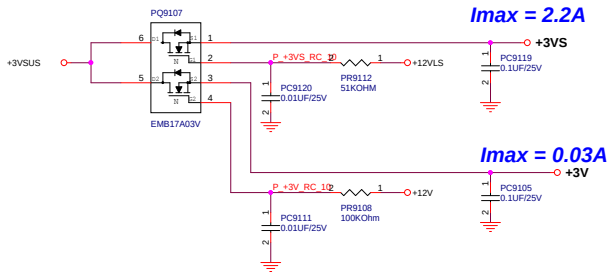
Title : HW_Throttle

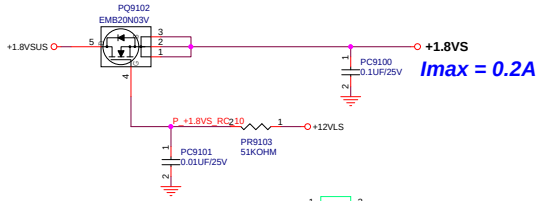
Engineer:

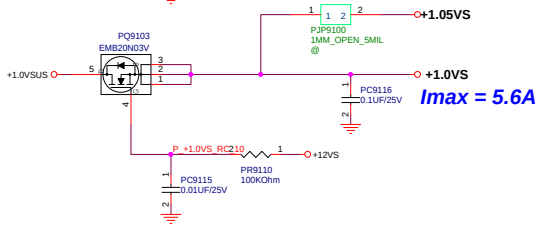
Size	Project Name	Rev
C	X555LD	R1.0

Date: Friday, March 14, 2014 Sheet 90 of 98

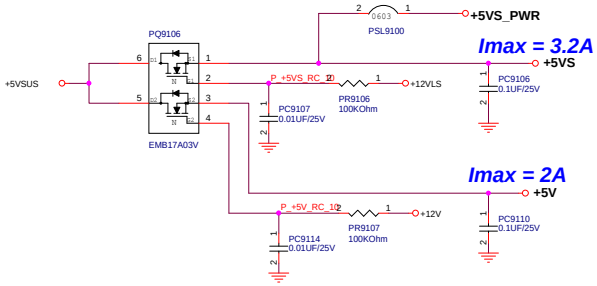
Load Switch

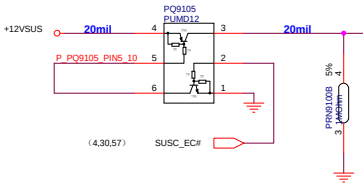


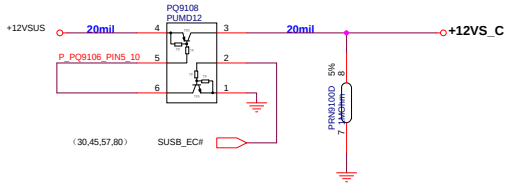


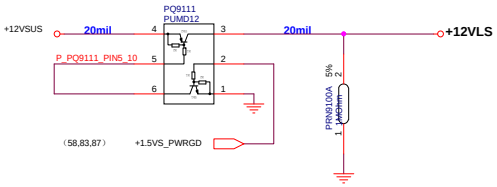


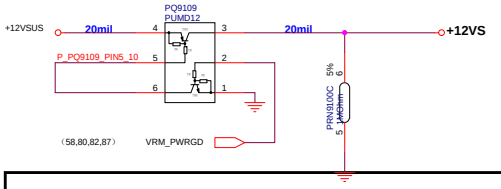
PSL9100 取代 PQ9106

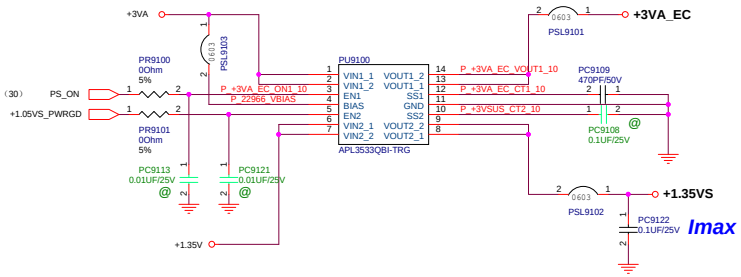


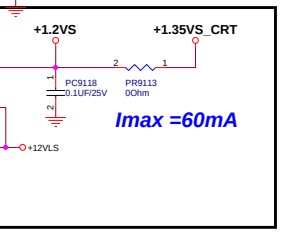








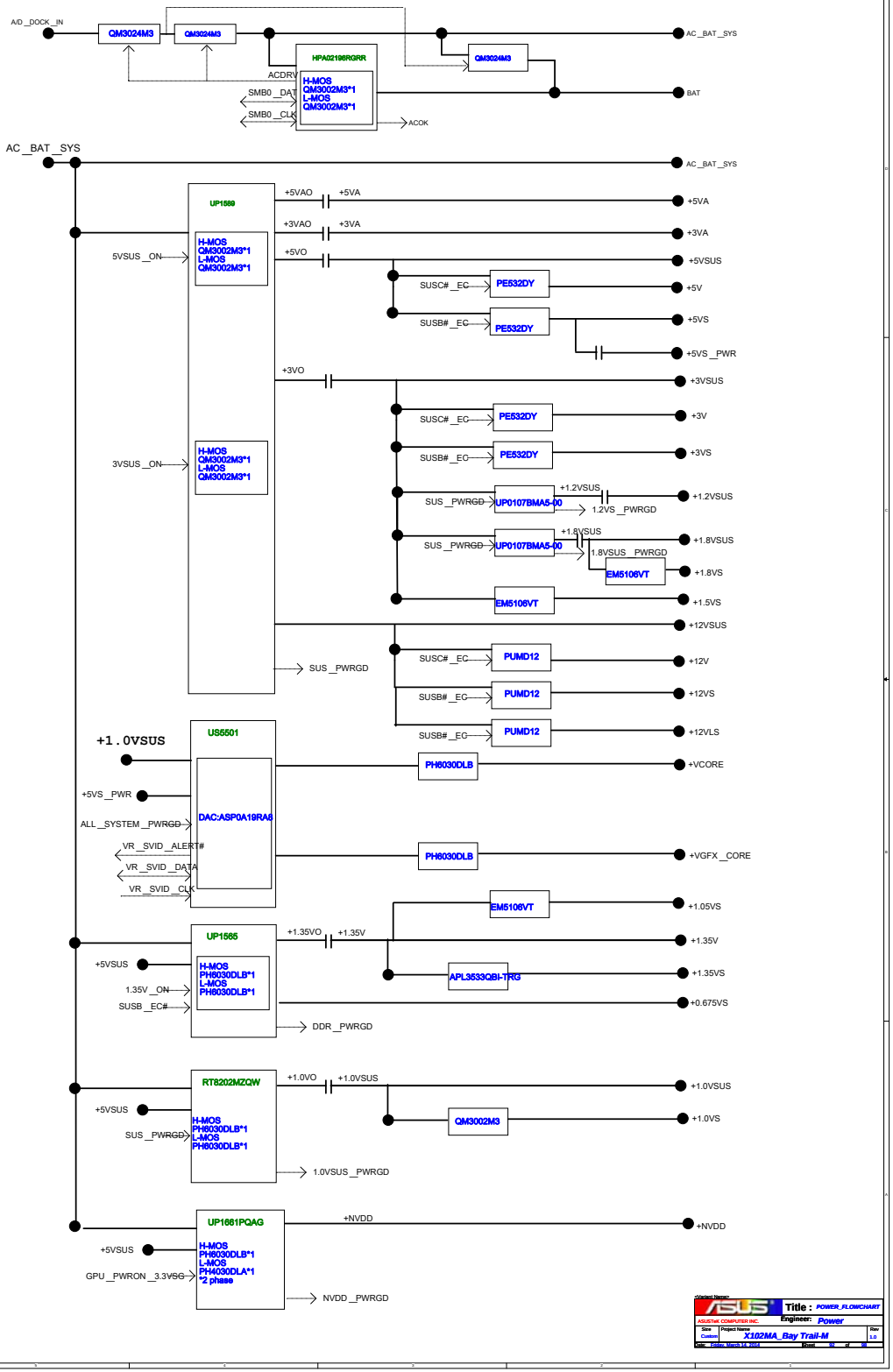




ARVIN CHANGE

<Variant Name>

ASUSTeK COMPUTER INC. NB	Title : Load Switch	
	Engineer:	
Size: Custom	Project Name: X102MA_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 91 of 98	


A/D_DOCK_IN
QM3024M3
QM3024M3
AC_BAT_SYS
HPA02196RGRR
QM3024M3
ACDRV
H-MOS
QM3002M3*1
L-MOS
QM3002M3*1
SMB0_DAT
SMB0_CLK
BAT
ACOK
AC_BAT_SYS
AC_BAT_SYS
UP1589
+5VAO
+5VA
+5VA
+3VAO
+3VA
+3VA
5VSUS_ON
H-MOS
QM3002M3*1
L-MOS
QM3002M3*1
+5VO
+5VSUS
SUSC#_EC
PE532DY
+5V
SUSB#_EC
PE532DY
+5VS
+5VS_PWR
+3VO
+3VSUS
SUSC#_EC
PE532DY
+3V
3VSUS_ON
H-MOS
QM3002M3*1
L-MOS
QM3002M3*1
SUSB#_EC
PE532DY
+3VS
SUS_PWRGD
UP0107BMA5-00
+1.2VSUS
+1.2VSUS
1.2VS_PWRGD
SUS_PWRGD
UP0107BMA5-00
+1.8VSUS
+1.8VSUS
1.8VSUS_PWRGD
EM5106VT
+1.8VS
EM5106VT
+1.5VS
+12VSUS
SUS_PWRGD
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
SUSB#_EC
PUMD12
+12VLS
+1.0VSUS
US5501
PH6030DLB
+VCORE
+5VS_PWR
DAC:ASP0A19RA8
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
PH6030DLB
+VGFX_CORE
EM5106VT
+1.05VS
UP1565
+1.35VO
+1.35V
+1.35V
+5VSUS
H-MOS
PH6030DLB*1
L-MOS
PH6030DLB*1
APL3533QBI-TRG
+1.35VS
1.35V_ON
SUSB_EC#
+0.675VS
DDR_PWRGD
RT8202MZQW
+1.0VO
+1.0VSUS
+1.0VSUS
+5VSUS
H-MOS
PH6030DLB*1
L-MOS
PH6030DLB*1
QM3002M3
+1.0VS
SUS_PWRGD
1.0VSUS_PWRGD
UP1661PQAG
+NVDD
+NVDD
+5VSUS
H-MOS
PH6030DLB*1
L-MOS
PH4030DLA*1
*2 phase
GPU_PWRON_3.3VSG
NVDD_PWRGD
Title : POWER_FLOWCHART
Engineer: Power
ASUSTeK COMPUTER INC.
Size
Custom
Project Name
X102MA_Bay Trail-M
Rev
1.0
Date: Friday, March 14, 2014
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ASUSTeK COMPUTER INC.

Title : POWER

Engineer:

Size: Custom | Project Name: Bay Trail-M | Rev: 1.0

Date: Friday, March 14, 2014 | Sheet 38 of 88

Rev	Date	Description
1.0	2012/10/22	First Release!
1.1	2014/03/07	1.Change EDP colay LVDS EDP signal 2.change R7014 100K TO 1k for DGPUPWOK sequence 3.ADD R3724 R3725 FOR headphone
1.1		
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Rev	Date	Description

ASUSTeK COMPUTER INC.

Title : SYSTEM HISTORY

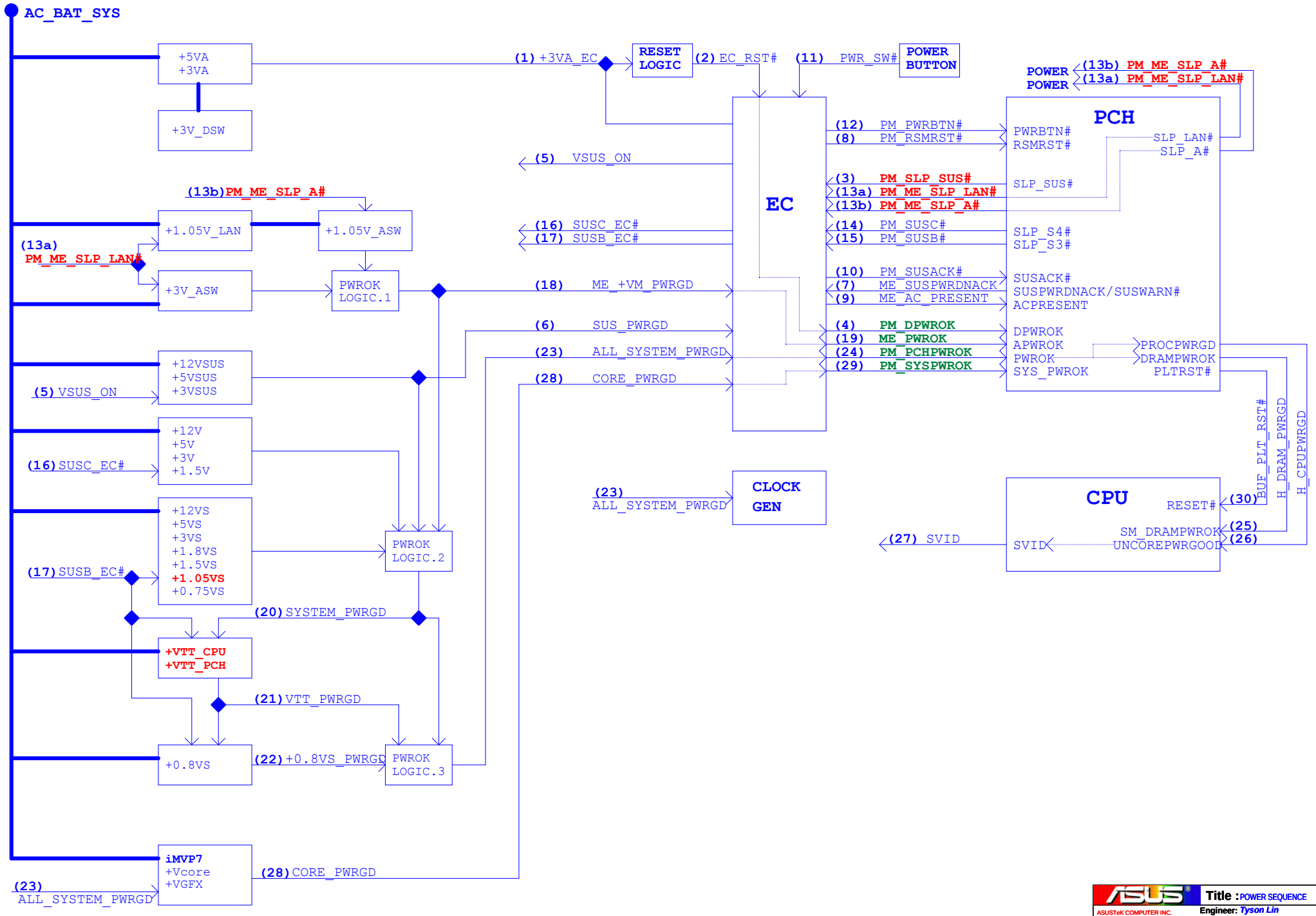
Engineer: Tyson Lin

Size	Project Name	Rev
C	S200T_Bay Trail-M	1.0

Date: Friday, March 14, 2014 Sheet 95 of 98

AC-IN Mode

U53 Power On Sequence Diagram Rev.0.14



ASUSTeK COMPUTER INC.

Title : POWER SEQUENCE

Engineer: Tyson Lin

Size	Project Name	Rev
C	S200T_Bay Trail-M	1.0

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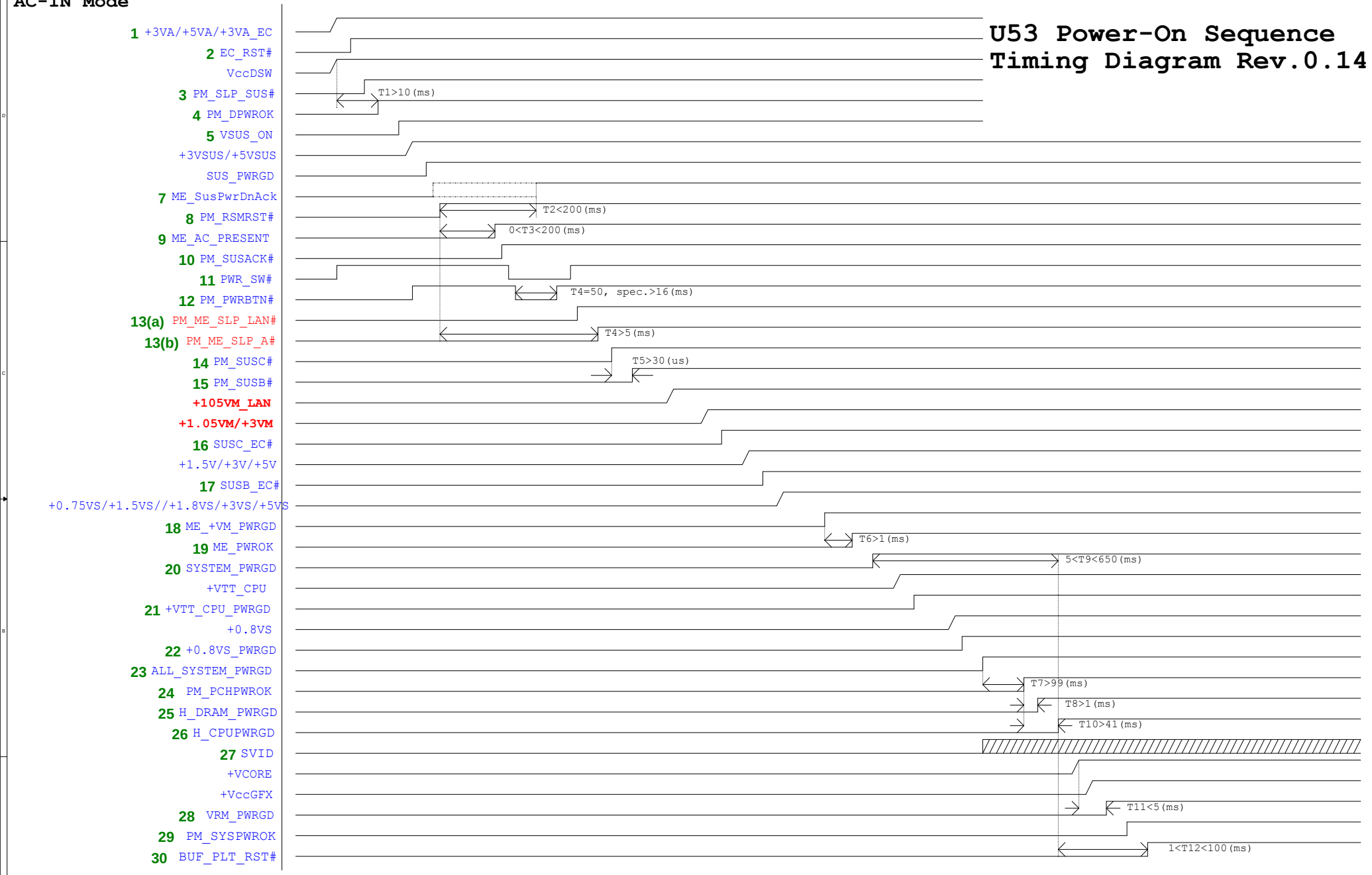
AC-IN Mode

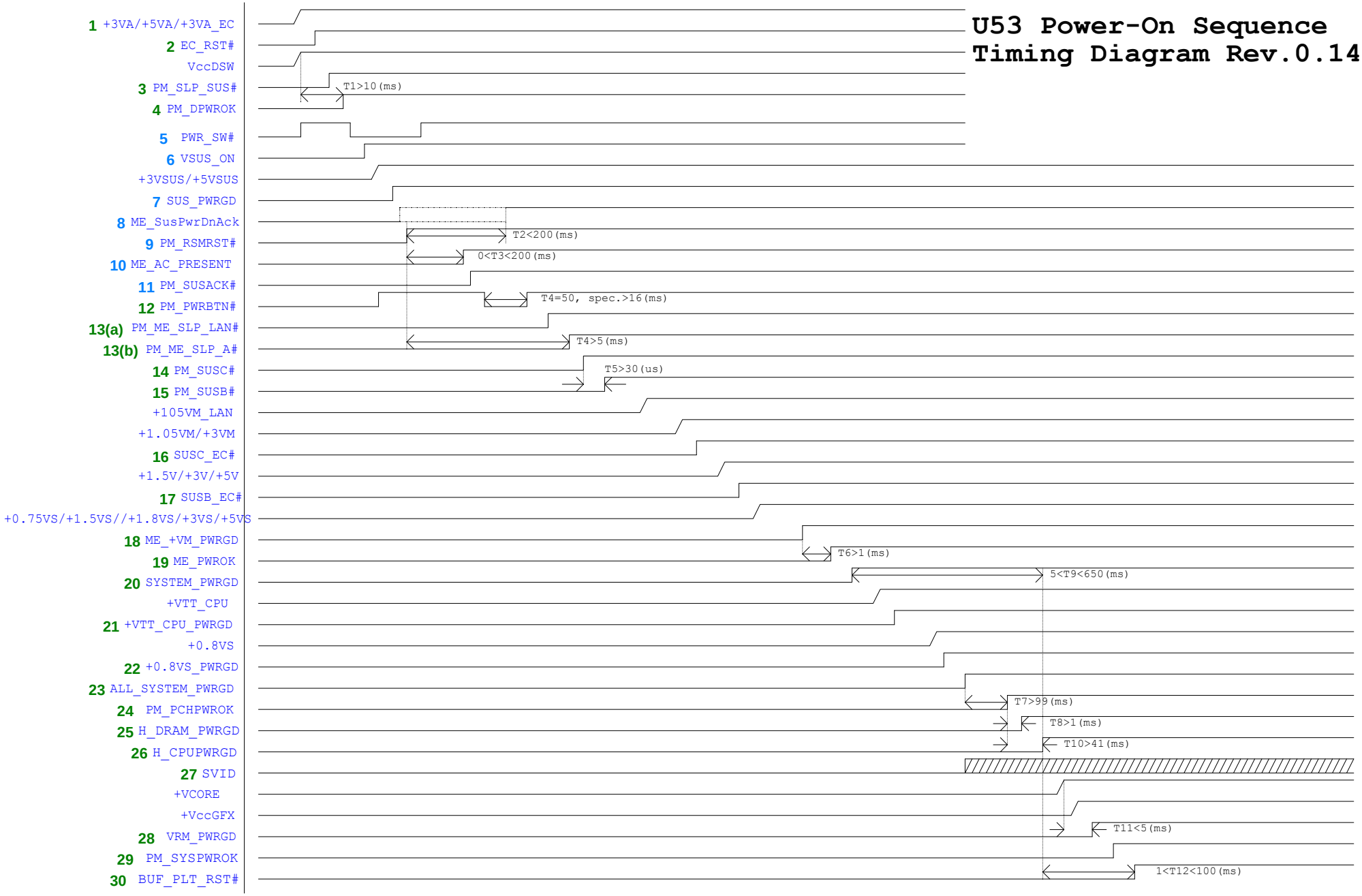
U53 Power-On Sequence Timing Diagram Rev.0.14



ASUSTeK COMPUTER INC.	Title : Power On Timing	
	Engineer: Tyson Lin	
Size: C	Project Name: S200T_Bay Trail-M	Rev: 1.0
Date: Friday, March 14, 2014	Sheet 97 of 98	

DC-IN Mode

U53 Power-On Sequence Timing Diagram Rev.0.14



ASUSTeK COMPUTER INC.	Title : Power On Timing		
	Engineer: Tyson Lin		
Size: C	Project Name: S200T_Bay Trail-M		Rev: 1.0
Date: Friday, March 14, 2014	Sheet 98 of 98		