COMPAL CONFIDENTIAL

MODEL NAME : CDP81

PCB NO : LA-E153P

BOM P/N :

GPIO MAP: Dell GPIO map EC16 062416 Compal Only

Breckenridge 15 DSC (non-TBT)

Kabylake H

2016-07-01

REV : 0.2 (X01)

@ : Nopop Component

EMI@ : EMI Component

@EMI@ : EMI Nopop Component

ESD@ : ESD Component

@ESD@ : ESD Nopop Component

RF@ : RF Component

@RF@ : RF Nopop Component

XDP@ : XDP Component

CONN@ : Connector Component

MB PCB

Part Number	Description
DAA000CN000	PCB 1SE LA-E153P REV0 MB DSC 1

Layout Dell logo

REV: X01
PWB: NJWXY

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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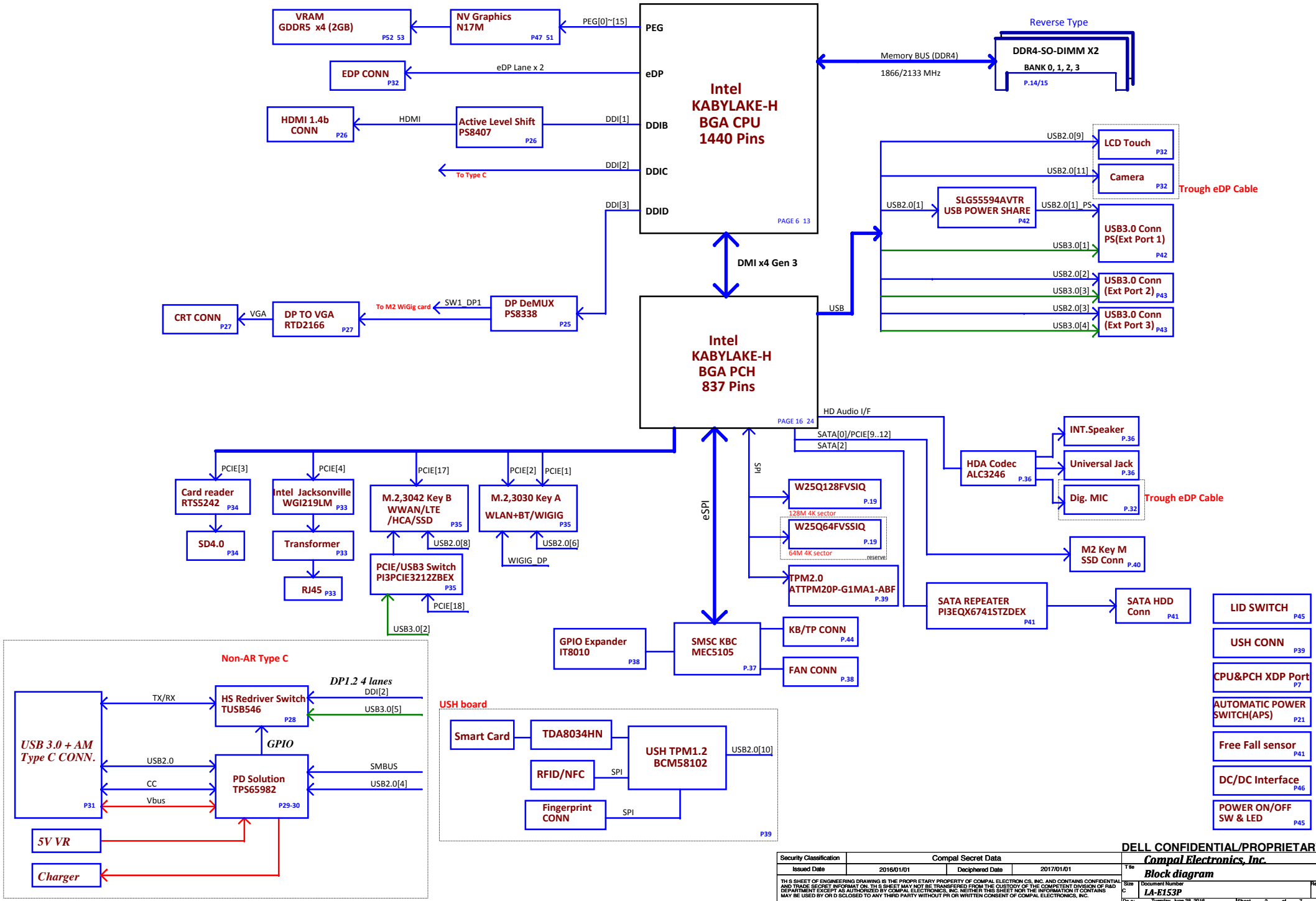
Title: Cover Sheet

Size: A | Document Number: LA-E153P | Rev: 0.2

Date: Friday, July 01, 2016 | Sheet 1 of 74

Breckenridge 15 DSC non-TBT Block Diagram



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Title: Block diagram

Size	Document Number	Rev
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_SUS +1.2V_MEM +1.0V_VCCST +2.5V_MEM	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.2V_RUN +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +1.8V_RUN
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

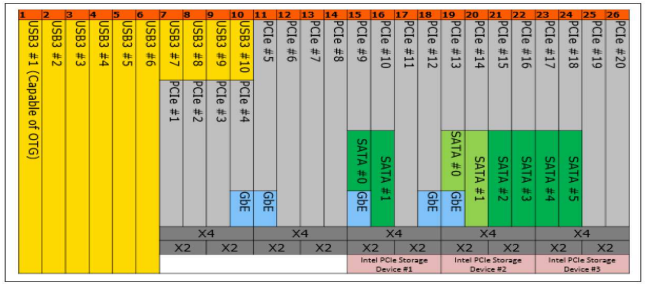
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB3-->Rear
USB3.0-2	SSIC-1			JNGFF2-->M2 3042(LTE)
USB3.0-3	SSIC-2			JUSB1-->Right
USB3.0-4				JUSB2-->Left
USB3.0-5				NA
USB3.0-6				NA
USB3.0-7		PCIE-1		JNGFF1-->M.2 3030(WIGIG)
USB3.0-8		PCIE-2		JNGFF1-->M.2 3030(WLAN)
USB3.0-9		PCIE-3		Card Reader
USB3.0-10		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		
		PCIE-7		
		PCIE-8		
		PCIE-9	SATA-0A	M.2 Socket 3 (Key M) M.2 2280 SSD (PCIex4 or SATA)
		PCIE-10	SATA-1A	
		PCIE-11		
		PCIE-12		
		PCIE-13	SATA-0B	NA
		PCIE-14	SATA-1B	NA
		PCIE-15	SATA-2	JSATA1-->HDD SATA
		PCIE-16	SATA-3	NA
		PCIE-17	SATA-4	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-18	SATA-5	M.2 3042 (HCA or QCA LTE) SSD Cache
		PCIE-19		NA
		PCIE-20		NA

USB PORT#	DESTINATION
1	JUSB3-->Rear
2	JUSB1-->Right
3	JUSB2 ->Left
4	Type C
5	NA
6	JNGFF1--> M.2 3030(BT)
7	NA
8	JNGFF2-->M2 3042(WWAN)
9	JEDP1-->Touch Screen
10	JUSH1-->USH
11	JEDP1-->Camera
12	NA

USH	H	BIO

VIDEO		DESTINATION
eDP		LCD
DDI-B		JHDMI1
DDI-C		Type-C
DDI-D	DeMux 1	M.2 3030 (WiGig)
		MB VGA

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.5
			Add Plating		
1	Top		Copper foil	0.5oz+plating	1.6
		3.8	Prepreg	1080	2.6
2	GND		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
3	IN 1		Copper foil	1oz	1.25
		3.7	Prepreg	2116H	4.3
4	GND/PWR		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
5	IN 2		Copper foil	1oz	1.25
		3.6	Prepreg	1080H x2 orPP2116HRC	4.2
6	IN 3		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
7	GND/PWR		Copper foil	1oz	1.25
		3.8	Prepreg	2116H	4.3
8	IN 4		Copper foil	1oz	1.25
		3.7	Core	4mil	3.87
9	GND		Copper foil	1oz	1.25
		3.8	Prepreg	1080	2.6
10	Bottom		Copper foil	0.5oz+plating	1.6
			Add Plating		
			SolderMask	IT-158	0.5
Overall Thickness (1.2mm ± 10%)					47.68000 1.211072



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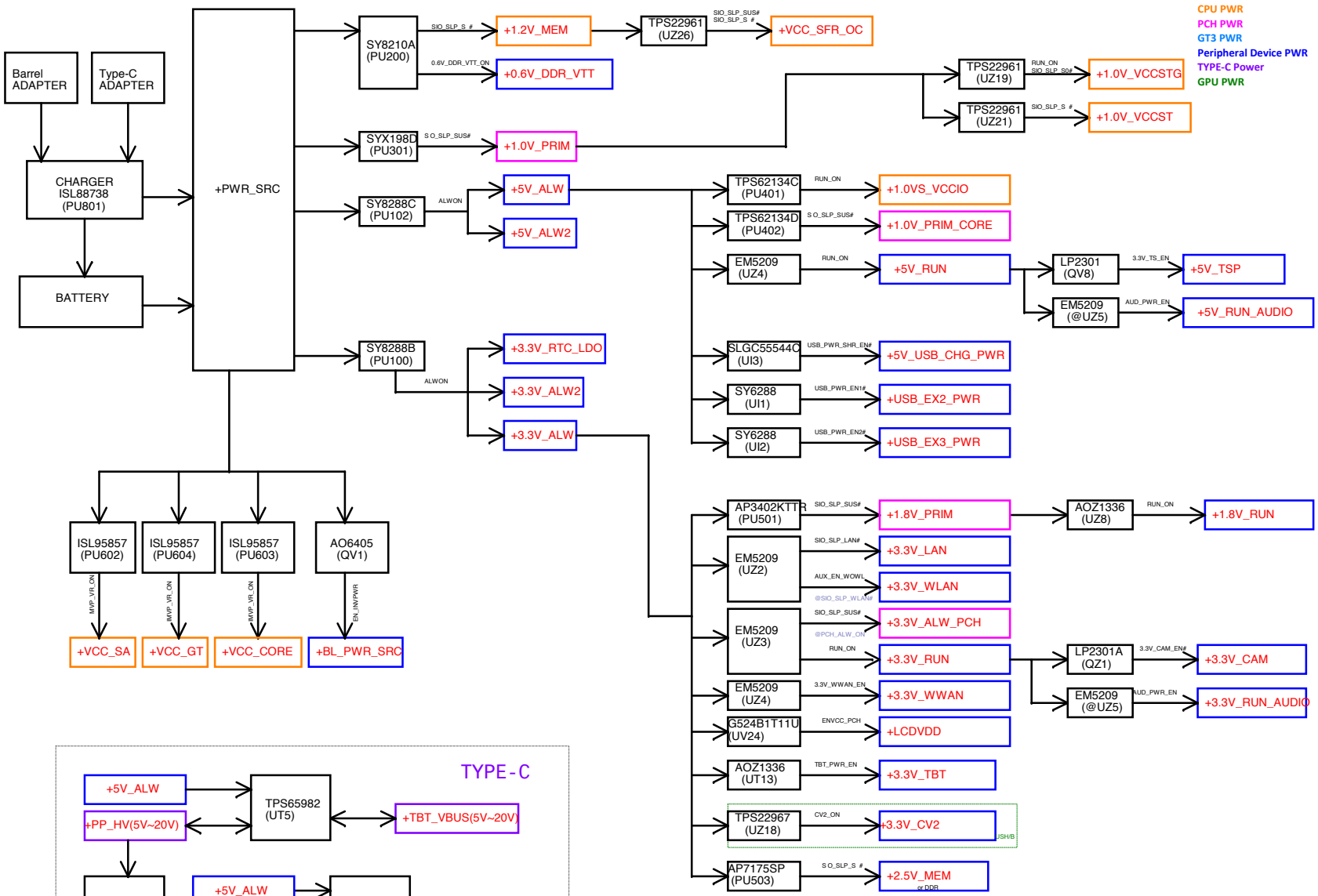
Title	Port Assignment		
Size A	Document Number LA-E153P		Rev 0.2
Date	Tuesday, June 28, 2016	Sheet 3 of 74	



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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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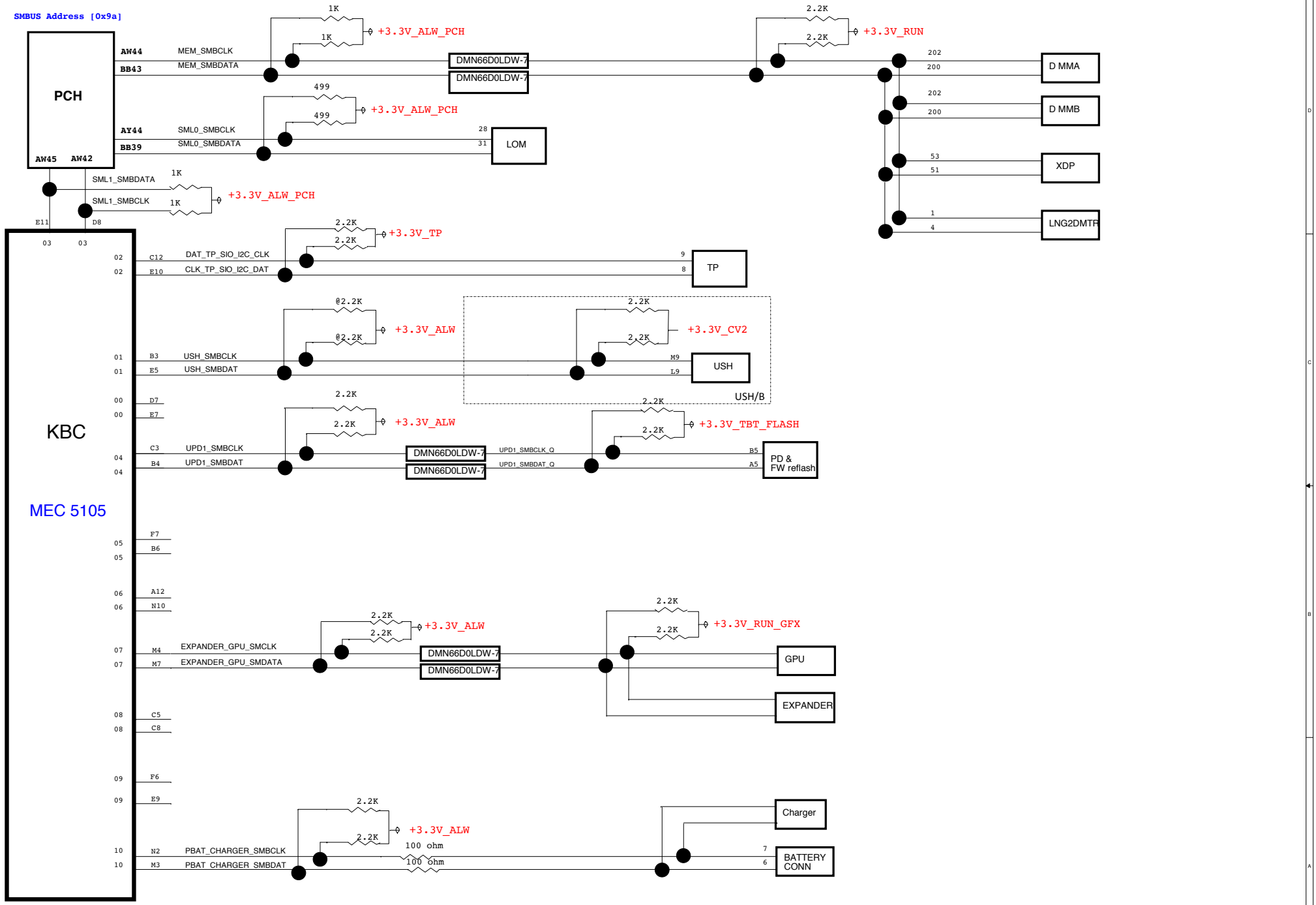
Title: Power Rails

Size	Document Number	Rev
C	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet of 7



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Title: SMbus Block Diagram

Size	Document Number	Rev
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PEG_CRX_GTX_P[0..15]
PEG_CRX_GTX_N[0..15]
PEG_CTX_C_GRX_P[0..15]
PEG_CTX_C_GRX_N[0..15]

1.0VS_VCCIO
RC2 1 2 PEG_COMP 24.9_0402_1%

Trace width=5 mils
,Spacing=15mil
Max length= 600 mils.

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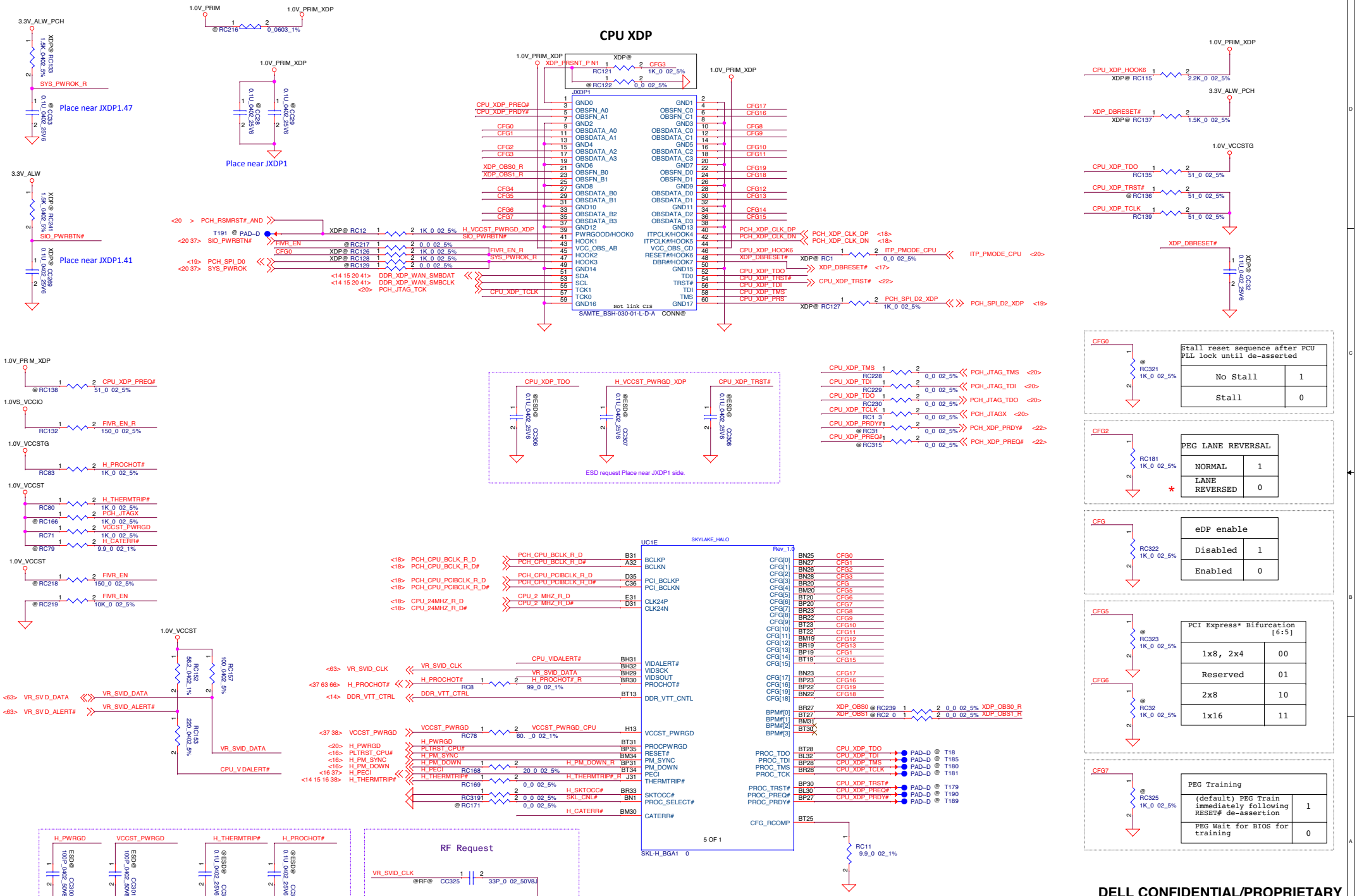
CPU XDP



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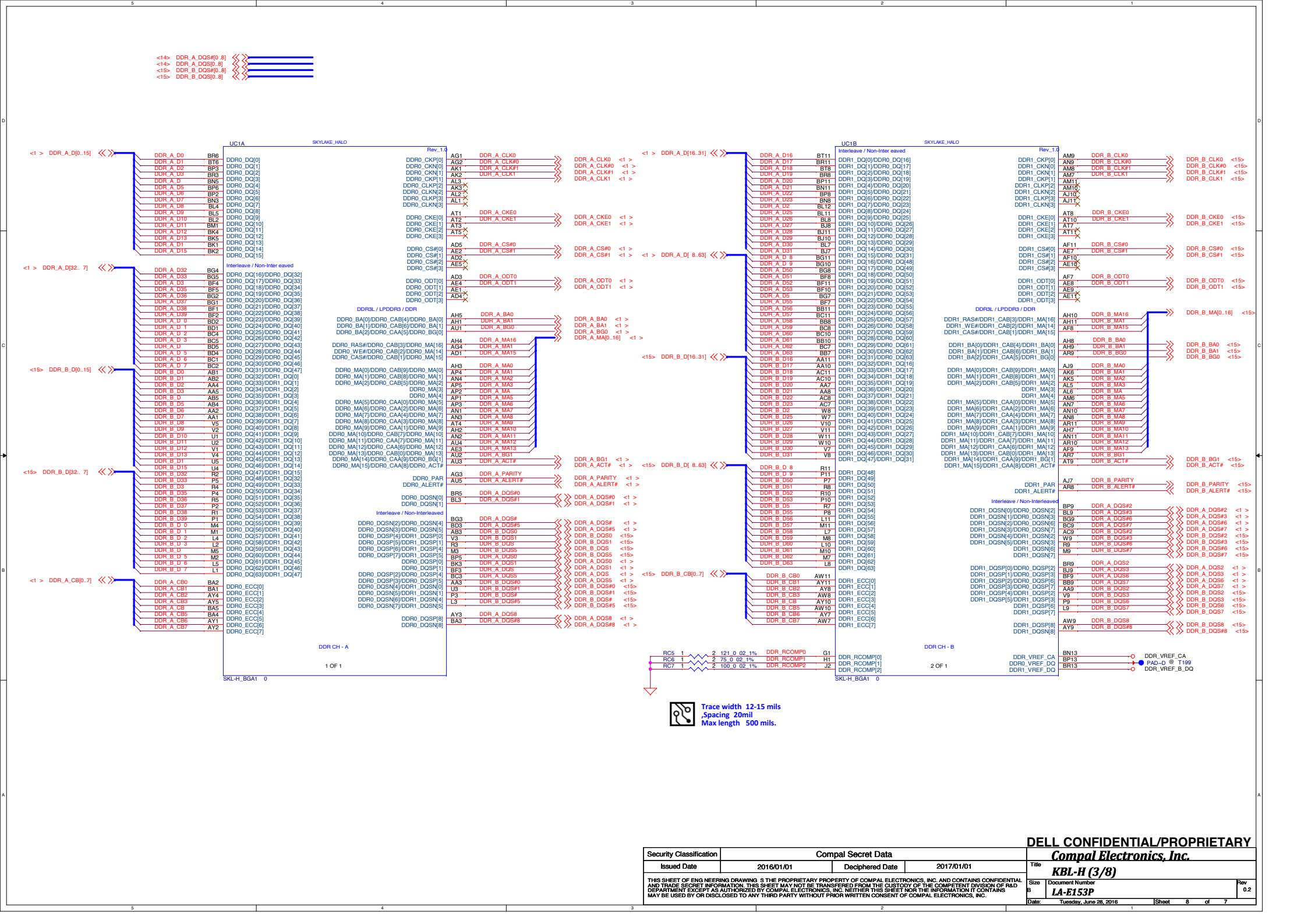

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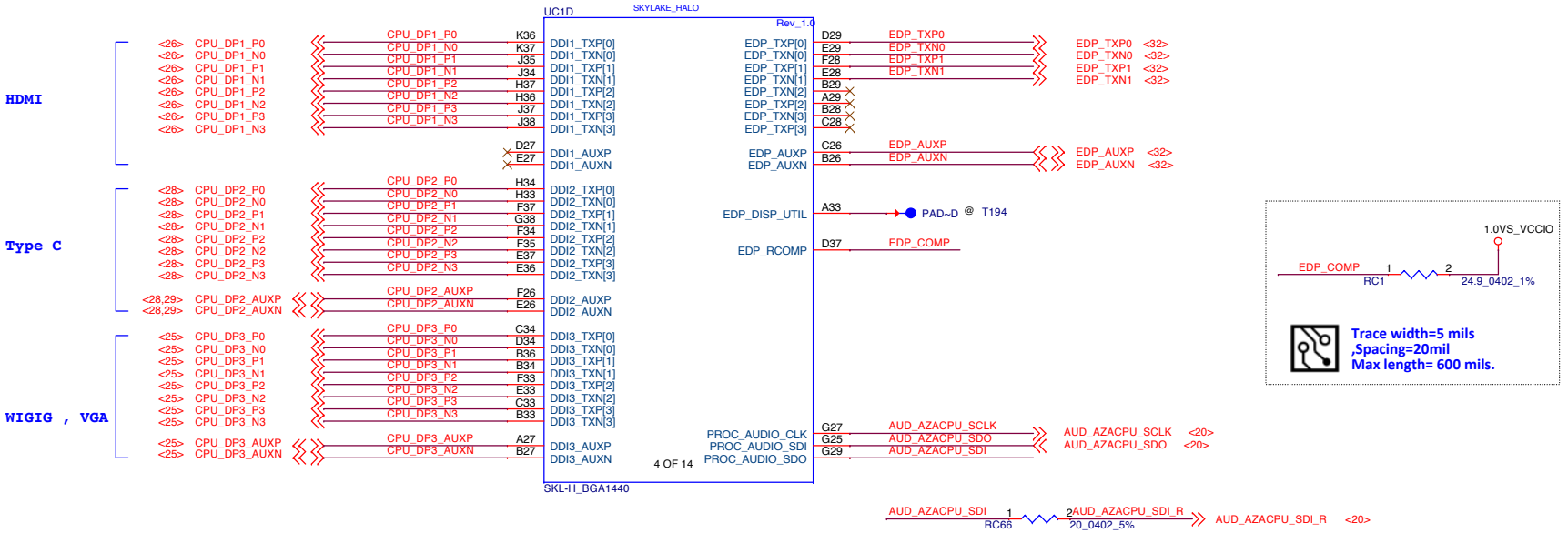

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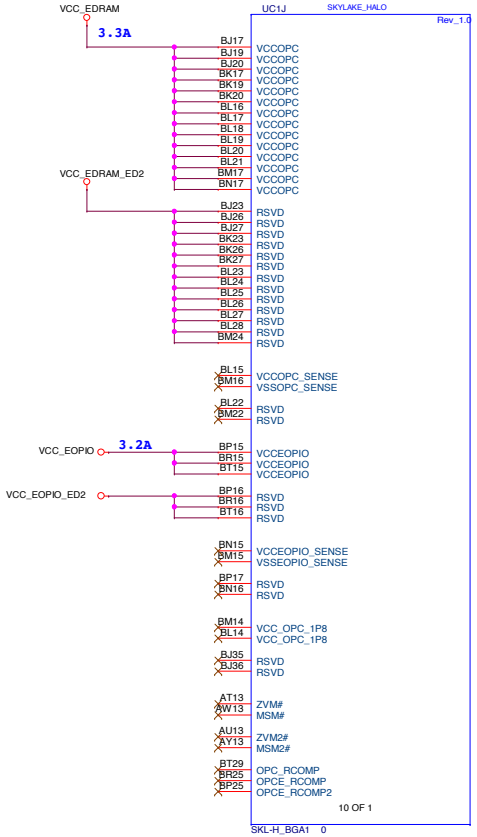

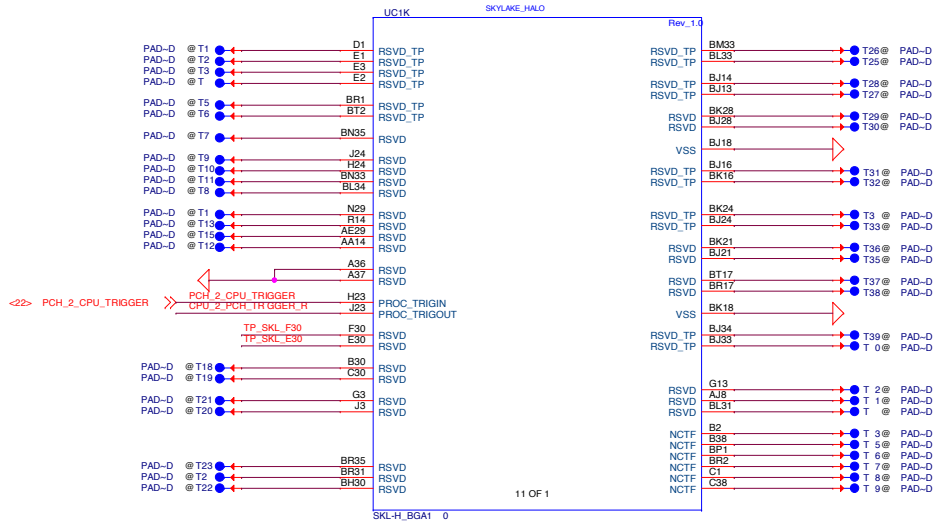

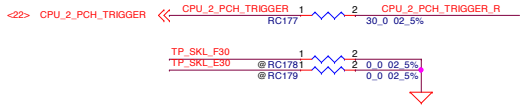

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Title: KBL-H (5/8)

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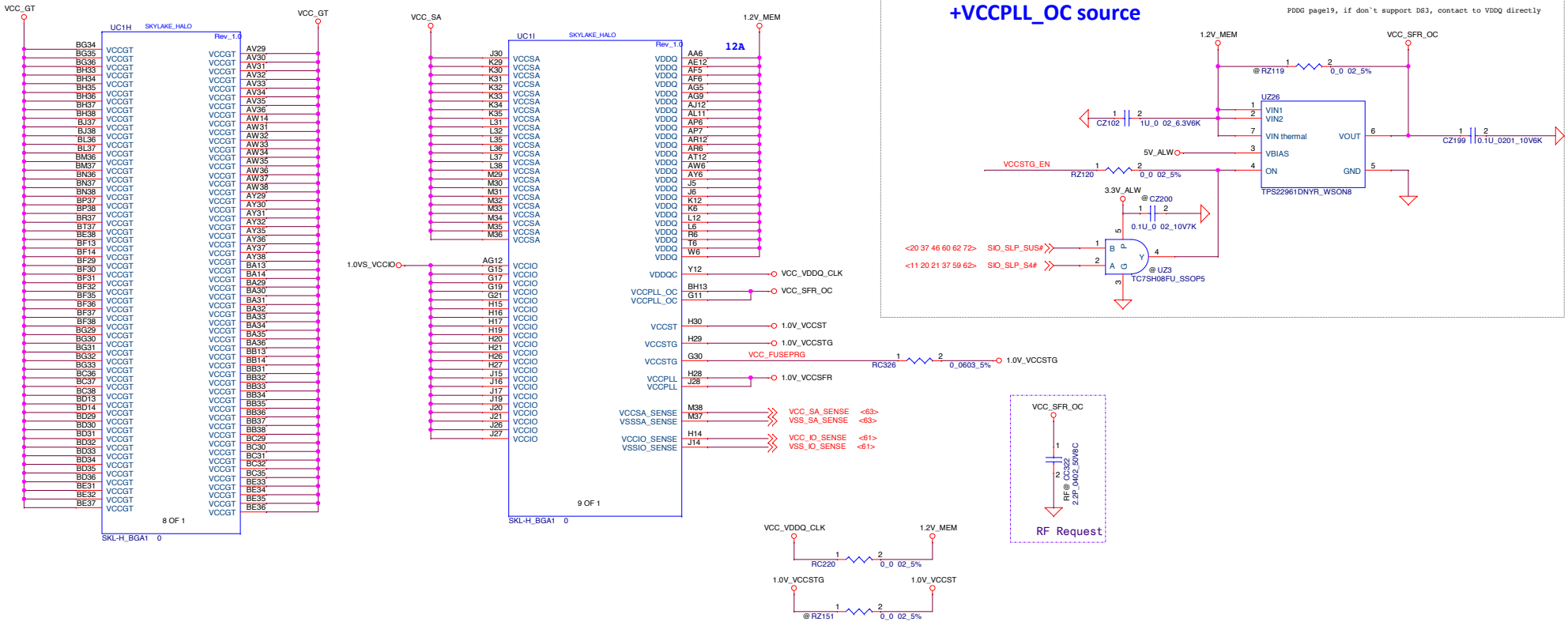
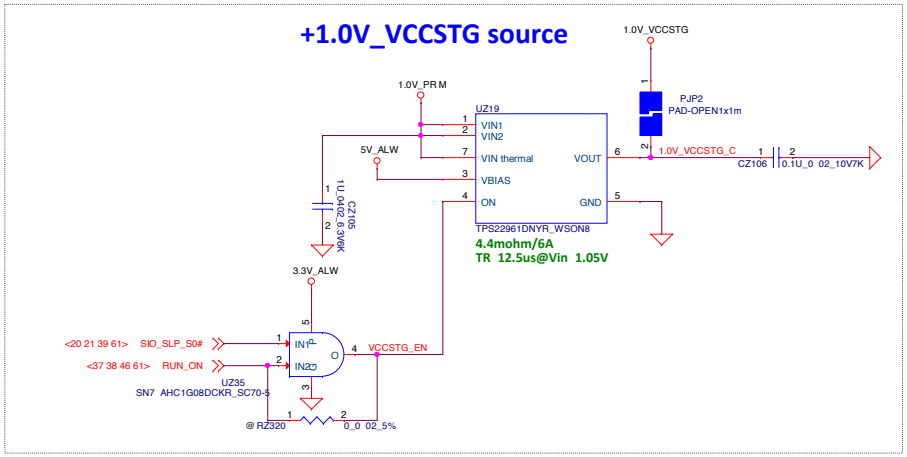


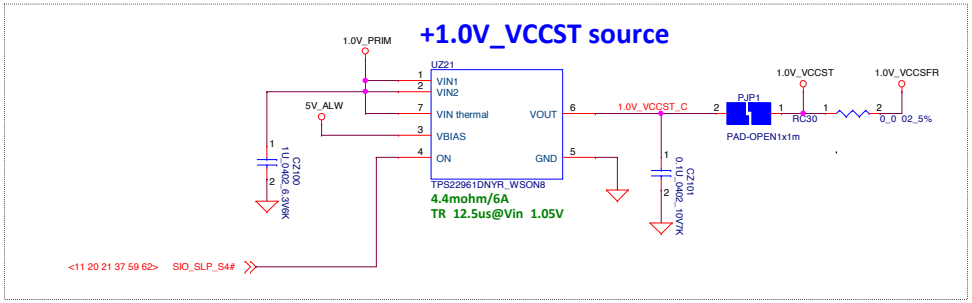
+VCCPLL_OC source

PDDG page19, if don`t support DS3, contact to VDDQ directly

+1.0V_VCCSTG source



+1.0V_VCCST source



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For SKL-H 4+2
Remove VCCOPC/VCCEOPIO/
VCCOPC_1P8 Cap

PLACE CAP BACKSIDE

VCC_VDDQ_CLK — 10U_0603_6.3V6M-D CC185
1.0V_VCCSTG — 1U_0402_6.3V6K CC186; 1U_0402_6.3V6K CC195
1.0V_VCCSFR — 1U_0402_6.3V6K CC192
1.0V_VCCST — 1U_0402_6.3V6K CC191
VCC_SFR_OC — 1U_0402_6.3V6K CC210; 1U_0402_6.3V6K CC208

1.0VS_VCCIO
PLACE CAP BACKSIDE
22U_0603_6.3V6M CC188; 22U_0603_6.3V6M CC187; 22U_0603_6.3V6M CC272

1.0V_VCCST
1U_0402_6.3V6K CC193; 1U_0402_6.3V6K CC194

Remove to Power (+VCC_SA cap)

1.2V_MEM
+1.2V_MEM DECOUPLING
PLACE CAP BACKSIDE
10U_0603_6.3V6M-D CC161; CC170; CC164; CC168; CC163; CC166; CC171; CC165; CC172; CC167
22U_0603_6.3V6M CC281; CC282; CC283; CC284

VCC_GT
UC1N SKYLAKE_HALO Rev_1.0
VCCGT: AJ29, AJ30, AJ31, AJ32, AJ33, AJ34, AJ35, AJ36, AK31, AK32, AK33, AK34, AK35, AK36, AK37, AK38, AL13, AL29, AL30, AL31, AL32, AL35, AL36, AL37, AL38, AM13, AM14, AM29, AM30, AM31, AM32, AM33, AM34, AM35, AM36, AN13, AN14, AN31, AN32, AN33, AN34, AN35, AN36, AN37, AN38, AP13, AP14, AP29, AP30, AP31, AP32, AP35, AP36, AP37, AP38, AR29, AR30, AR31, AR32, AR33, AR34, AR35, AR36, AT14, AT31, AT32, AT33, AT34, AT35, AT36, AT37, AT38, AU14, AU29, AU30, AU31, AU32, AU35, AU36, AU37, AU38
1 OF 1
SKL-H_BGA1 0

VCC_GTU
VCCGTX: AF29, AF30, AF31, AF32, AF33, AF34, AG13, AG14, AG3, AG32, AG33, AG34, AG35, AG36, AH13, AH14, AH29, AH30, AH31, AH32, AJ13, AJ14
Reserve for Soldering

VCCGT_SENSE, VSSGTX_SENSE, VSSGT_SENSE, VCCGTX_SENSE
AH38 → VCC_GT_SENSE <63>
AH35, AH37 → VSS_GT_SENSE <63>
AH36

VCC_CORE
UC1G SKYLAKE_HALO Rev_1.0
VCC: AA13, AA31, AA32, AA33, AA34, AA35, AA36, AA37, AA38, AB29, AB30, AB31, AB32, AB35, AB36, AB37, AB38, AC13, AC14, AC29, AC30, AC31, AC32, AC33, AC34, AC35, AC36, AD13, AD14, AD31, AD32, AD33, AD34, AD35, AD36, AD37, AD38, AE13, AE14, AE30, AE31, AE32, AE35, AE36, AE37, AE38, AF35, AF36, AF37, AF38, K13, K14, L13, N13, N14, N30, N31, N32, N35, N36, N37, N38, P13
VCC: V32, V33, V34, V35, V36, V37, V38, W13, W14, W29, W30, W31, W32, W35, W36, W37, W38, Y29, Y30, Y31, Y32, Y33, Y34, Y35, Y36, L14, P29, P30, P31, P32, P33, P34, P35, P36, R13, R31, R32, R33, R34, R35, R36, R37, R38, T29, T30, T31, T32, T35, T36, T37, T38, U29, U30, U31, U32, U33, U34, U35, U36, V13, V14, V31, P14
7 OF 1
SKL-H_BGA1 0

VCC_SENSE, VSS_SENSE
AG37 VCC_SENSE
AG38 VSS_SENSE
→ VCC_SENSE <63>, VSS_SENSE <63>

VCC_CORE
RC140 100_0402_1%
RC141 100_0402_1%

VSS_SENSE — 1 — 2 — VCC_SENSE
@ RC221 9.9_0 02_1%

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Title: KBL-H (7/8)			
Size: B	Document Number: LA-E153P		Rev: 0.2
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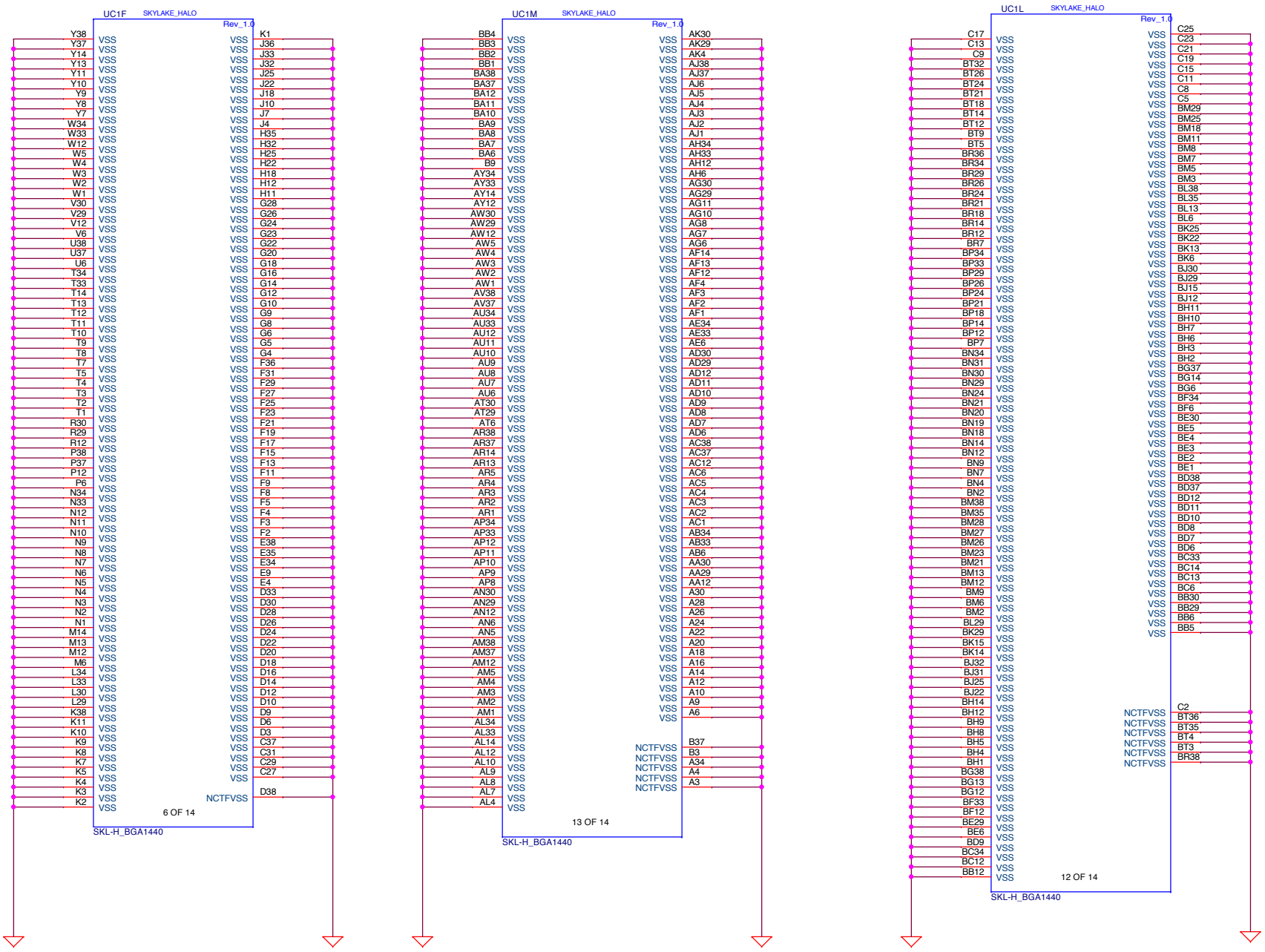

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A	LA-E153P	0.2

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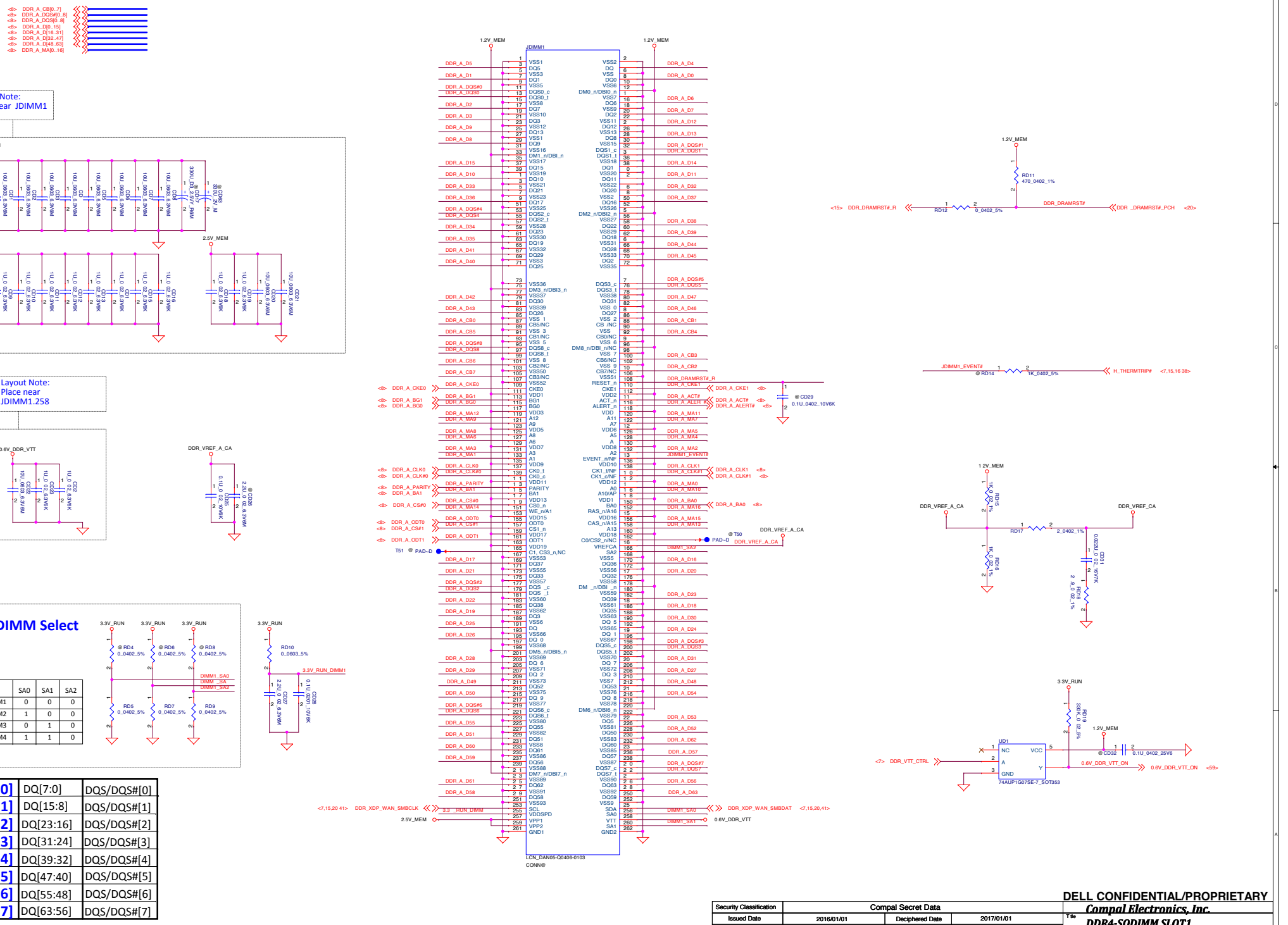

Byte[0]	DQ[7:0] DQS/DQS#[0]
Byte[1]	DQ[15:8] DQS/DQS#[1]
Byte[2]	DQ[23:16] DQS/DQS#[2]
* **Byte[3]**	DQ[31:24] DQS/DQS#[3]
Byte[4]	DQ[39:32] DQS/DQS#[4]
* **Byte[5]**	DQ[47:40] DQS/DQS#[5]
Byte[6]	DQ[55:48] DQS/DQS#[6]
Byte[7]	DQ[63:56] DQS/DQS#[7]

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: DDR4-SODIMM SLOT1

Size	Document Number	Rev
C	LA-E153P	0.2

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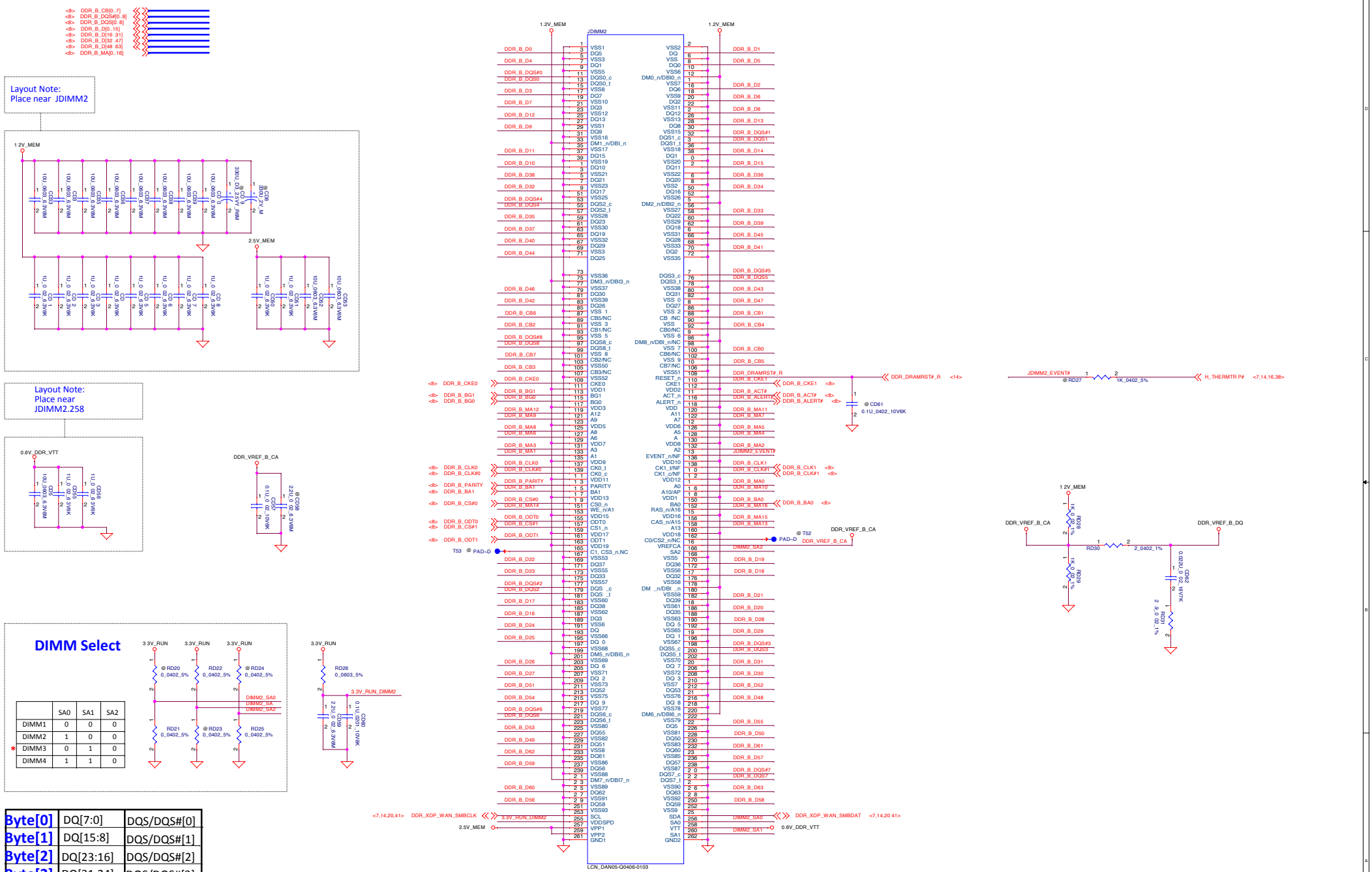

Byte[0]	DQ[7:0] DQS/DQS#[0]
Byte[1]	DQ[15:8] DQS/DQS#[1]
Byte[2]	DQ[23:16] DQS/DQS#[2]
* Byte[3]	DQ[31:24] DQS/DQS#[3]
Byte[4]	DQ[39:32] DQS/DQS#[4]
* Byte[5]	DQ[47:40] DQS/DQS#[5]
Byte[6]	DQ[55:48] DQS/DQS#[6]
Byte[7]	DQ[63:56] DQS/DQS#[7]

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Compal Electronics, Inc.

Title: DDR4-SODIMM SLOT2

Size: C | Document Number: LA-E153P | Rev: 0.2

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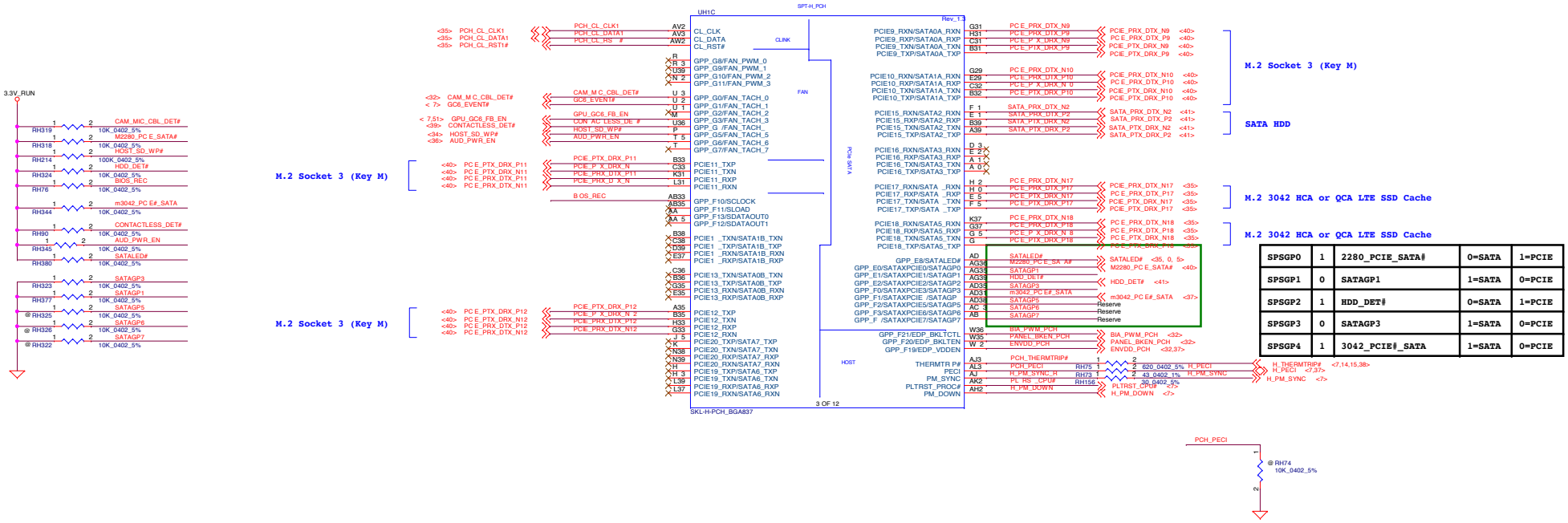

SPSGP0	1	2280_PCIE_SATA#	0=SATA	1=PCIE
SPSGP1	0	SATAGP1	1=SATA	0=PCIE
SPSGP2	1	HDD_DET#	0=SATA	1=PCIE
SPSGP3	0	SATAGP3	1=SATA	0=PCIE
SPSGP4	1	3042_PCIE#_SATA	1=SATA	0=PCIE

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: KABYLAKE PCH-H (1/9)

Size	Document Number	Rev
C	LA-E153P	0.2

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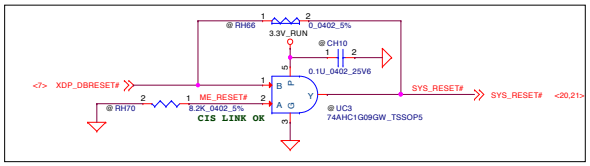

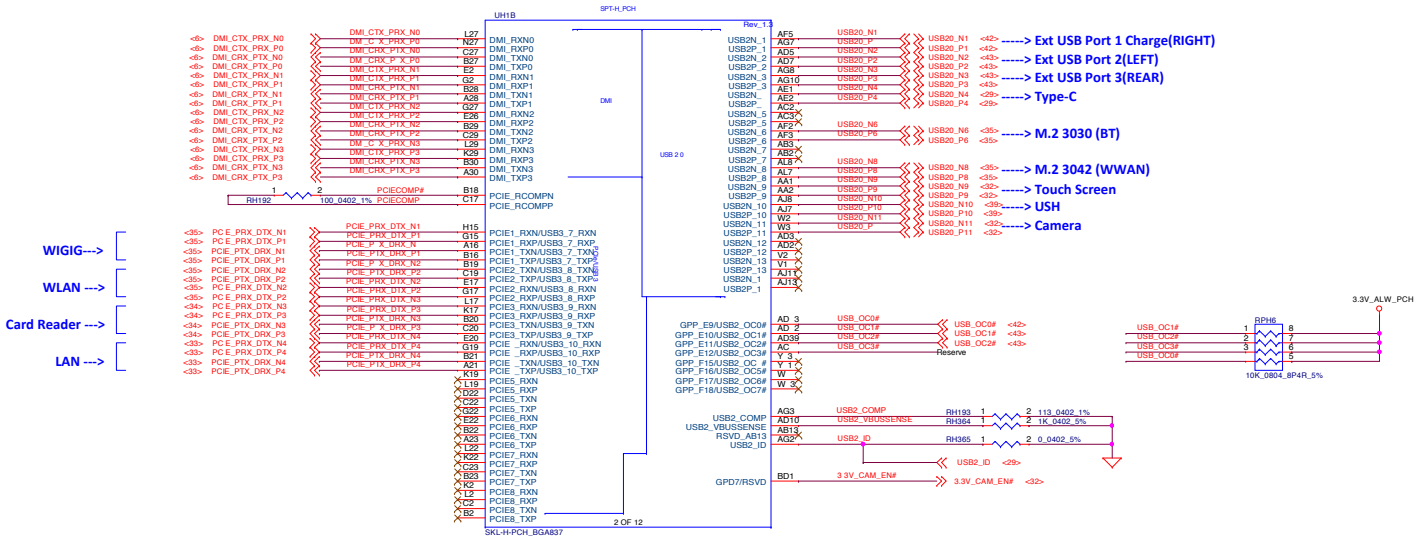

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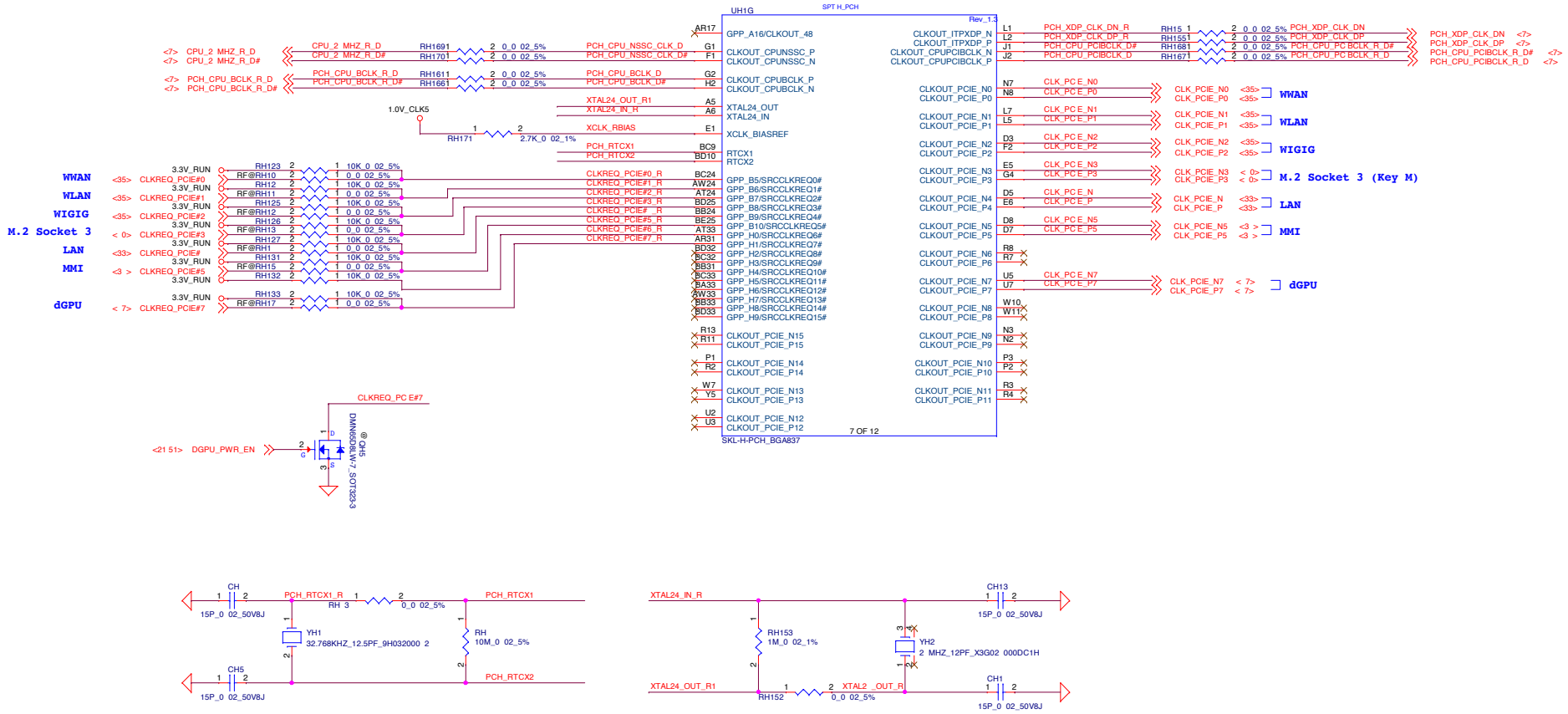
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: KABYLAKE PCH-H (2/9)

Size	Document Number	Rev
C	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet 17 of 74



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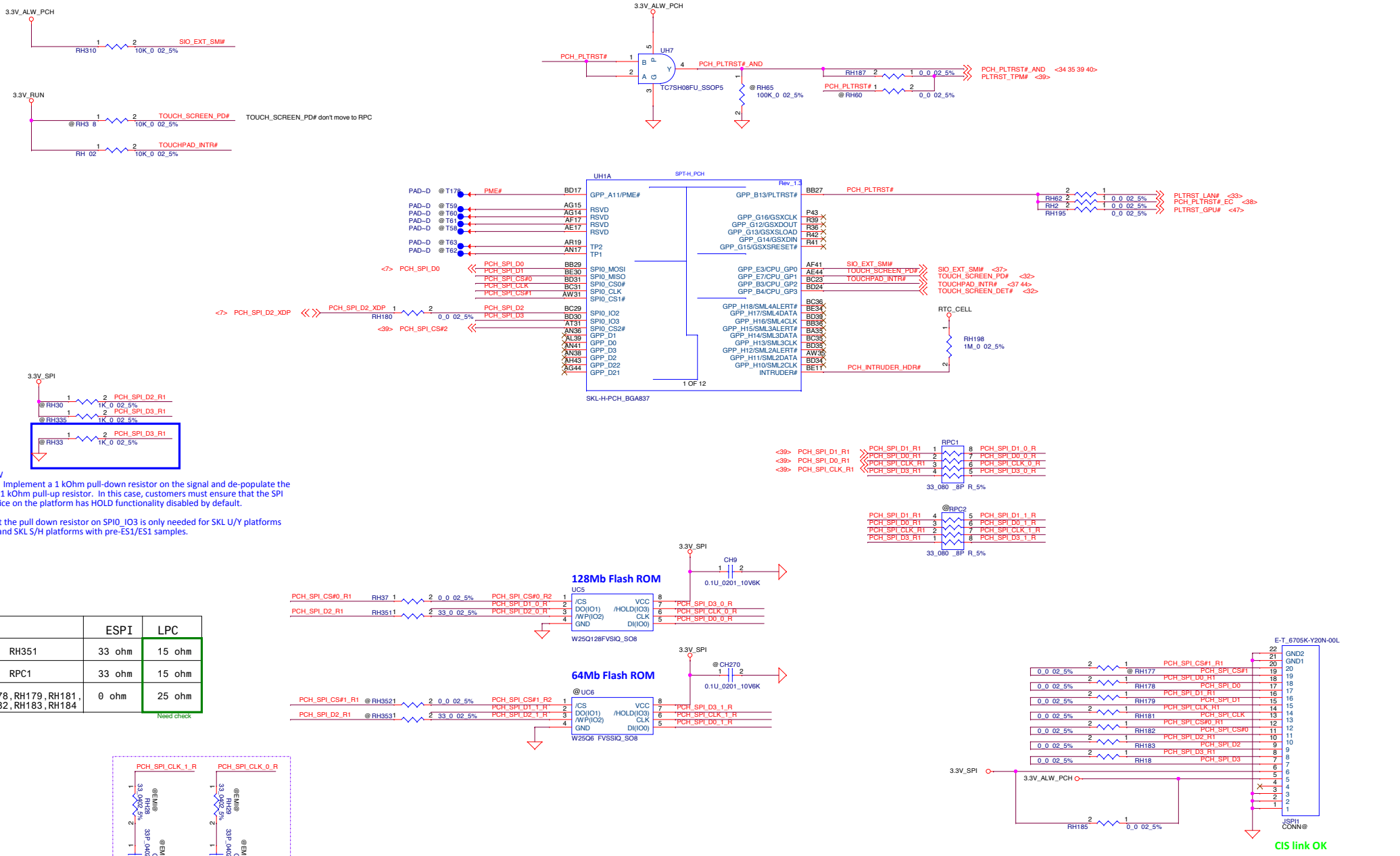
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: KABYLAKE PCH-H (3/9)

Size	Document Number	Rev
B	LA-E153P	0.2

Date: Thursday, June 30, 2016 | Sheet 18 of 7



9/5 MOW
Option 1 Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

	ESPI	LPC
RH351	33 ohm	15 ohm
RPC1	33 ohm	15 ohm
RH178,RH179,RH181, RH182,RH183,RH184	0 ohm	25 ohm

Need check

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Compal Electronics, Inc.

Title: *KABYLAKE PCH-H (4/9)*

Size	Document Number	Rev
B	*LA-E153P*	0.2

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Ext USB Port 1 Charge(RIGHT)

M.2 3042 (LTE)

Type C

Ext USB Port 2(LEFT)

Ext USB Port 3(REAR)

UH1F SPT-H_PCH Rev_1.3

SKL-H-PCH_BGA837

6 OF 12

UH1D SPT-H_PCH Rev_1.3

SKL-H-PCH_BGA837

OF 12

ESD Request place near PCH side

RF Request

Place close PCH side

EXI BOOT STALL BYPASS	
HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

Service Mode Switch
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

ME_FWP PCH has internal 20K PD. (suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW	ENABLE (DEFAULT) -->Pin1 & Pin3 short
HIGH	DISABLE (ME can update) -->Pin2 & Pin3 short

RH215	
POP	NO Support Deep sleep
DE-POP	Support Deep sleep

ESD request Place near PCH side.

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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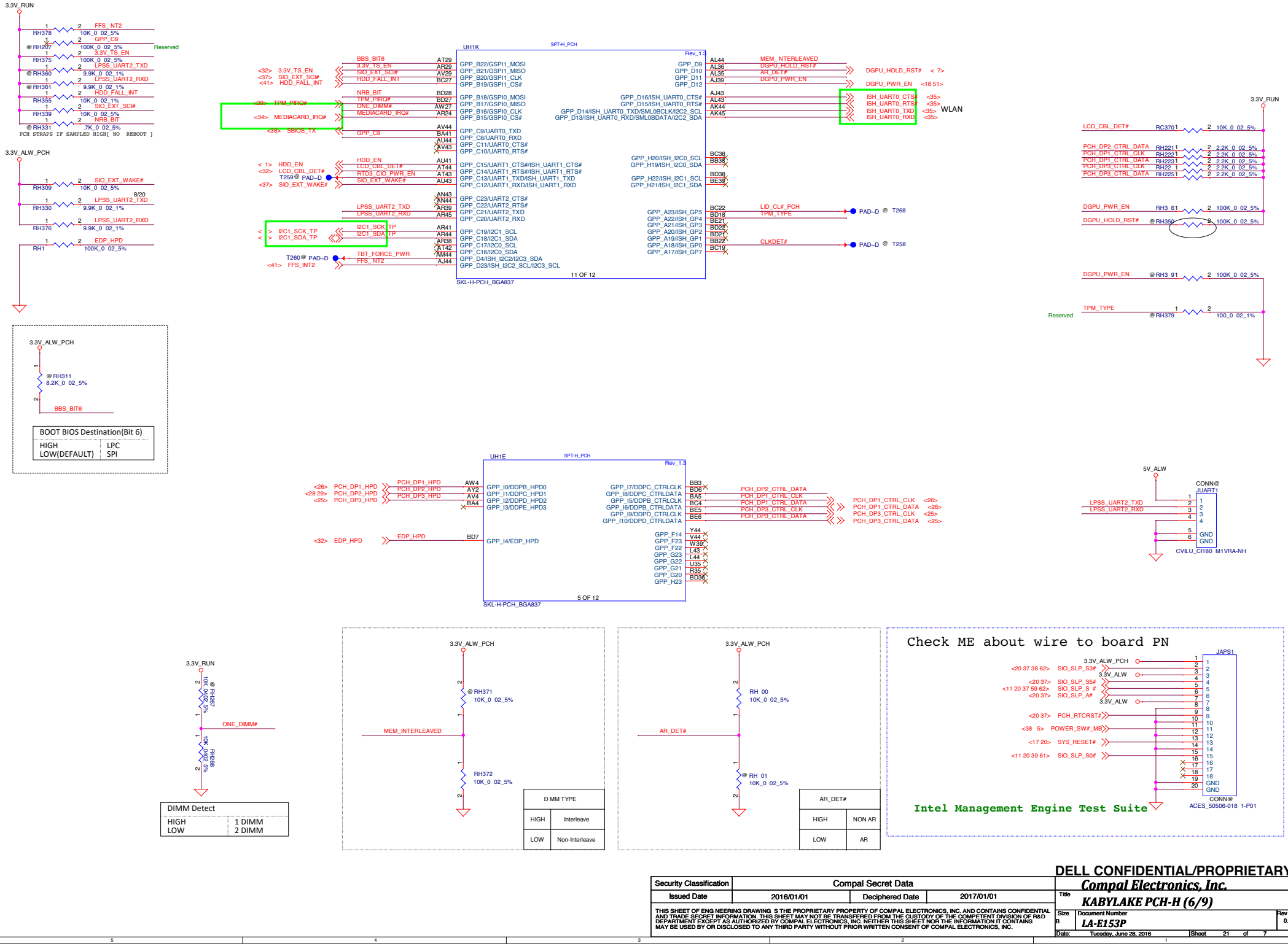
Title: KABYLAKE PCH-H (5/9)

Size	Document Number	Rev
B	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet 20 of 7



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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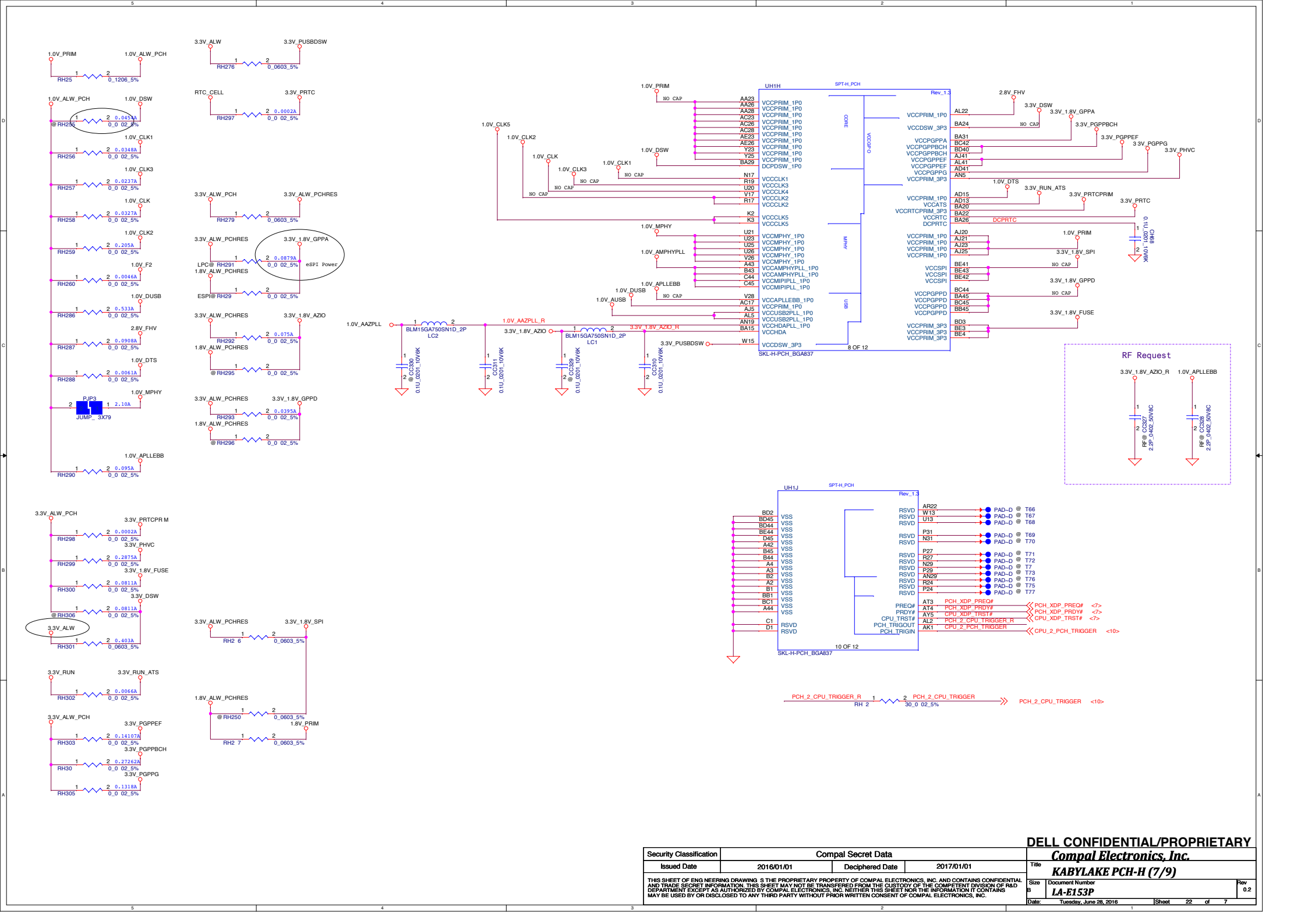
Compal Electronics, Inc.

Title: *KABYLAKE PCH-H (6/9)*

Size	Document Number	Rev
B	*LA-E153P*	0.2

Date: Tuesday, June 28, 2016 Sheet 21 of 7



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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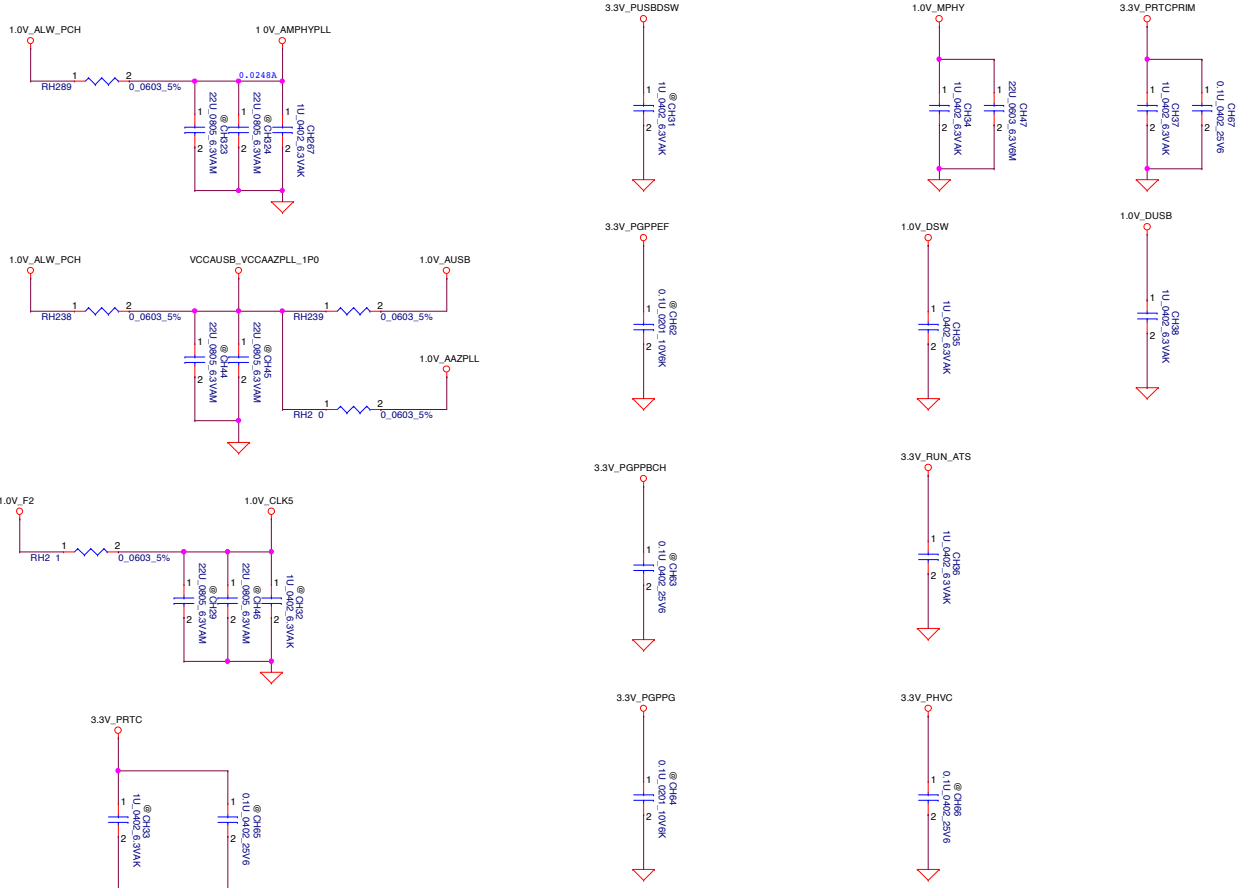
Compal Electronics, Inc.

Title: *KABYLAKE PCH-H (7/9)*

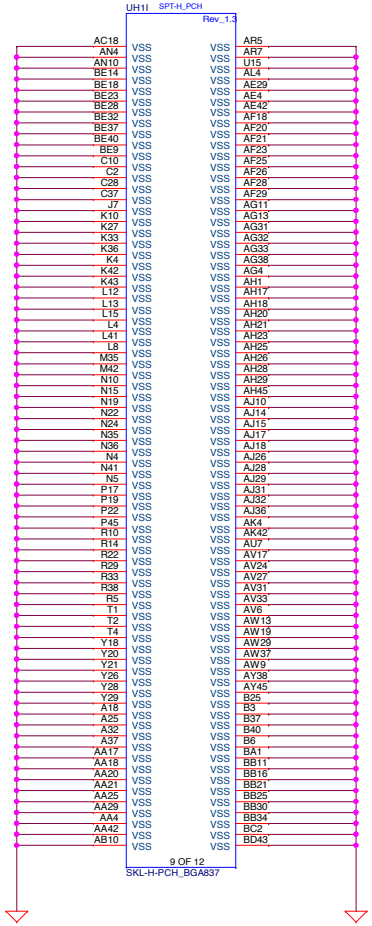
Size	Document Number	Rev
B	*LA-E153P*	0.2

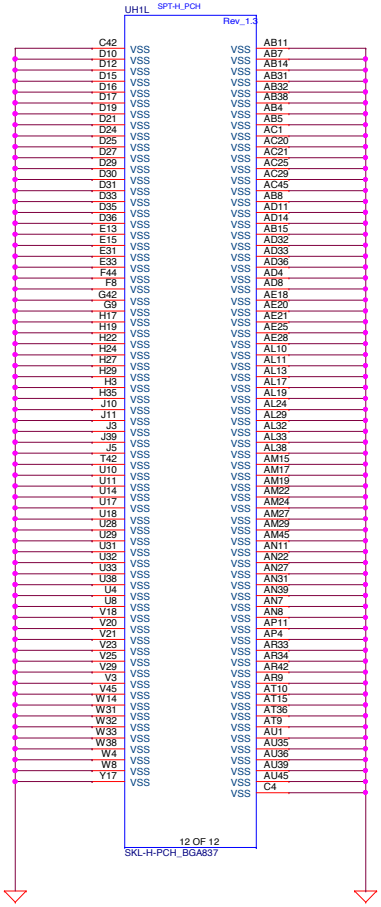
Date: Tuesday, June 28, 2016 | Sheet 22 of 7



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: KABYLAKE PCH-H (8/9)			
Size: B	Document Number: LA-E153P		Rev: 0.2
Date: Tuesday, June 28, 2016	Sheet 23 of 7		





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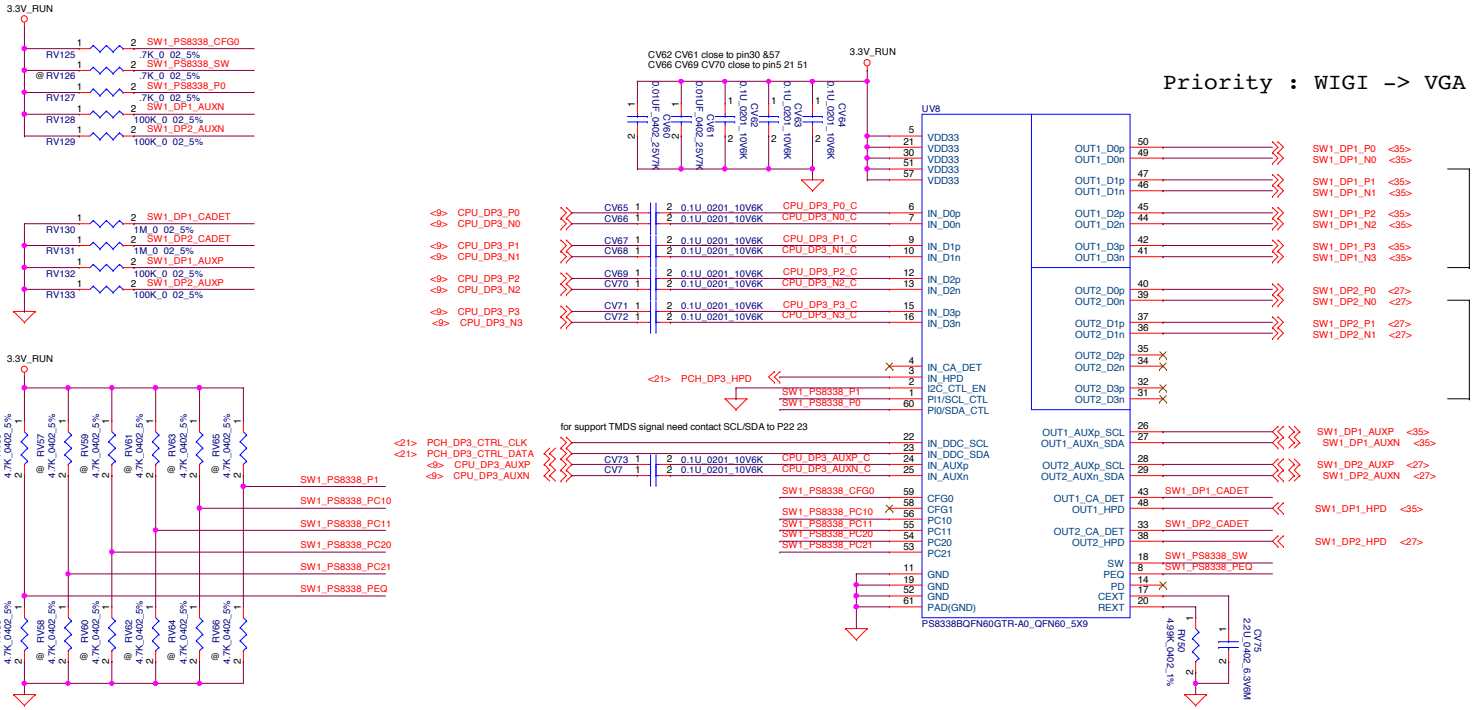
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: KABYLAKE PCH-H (9/9)		
Size: B	Document Number: LA-E153P	Rev: 0.2
Date: Tuesday, June 28, 2016	Sheet 2 of 7	



Port switching control or priority configuration Internal pull down ~150KΩ, 3 3V I/O
For Control Switching Mode (CFG0 = L)
SW = L Port1 is selected (default)
SW = H Port2 is selected
For Automatic Switching Mode (CFG0 = H)
SW = L Port1 has higher priority when both ports are plugged (default)
SW = H Port2 has higher priority when both ports are plugged

vender suggguest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3 3V I/O
PEQ =
L default,LEQ, compensate channel loss up to 11.5dB @HBR2
H HEQ, compensate channel loss up to 14.5dB @HBR2
M LLEQ, compensate channel loss up to 8.5dB @HBR2

PI0:Automatic EQ disable Internal pull down ~150K ohm 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *DP SW2 PS8338*

Size	Document Number	Rev
B	*LA-E153P*	0.2

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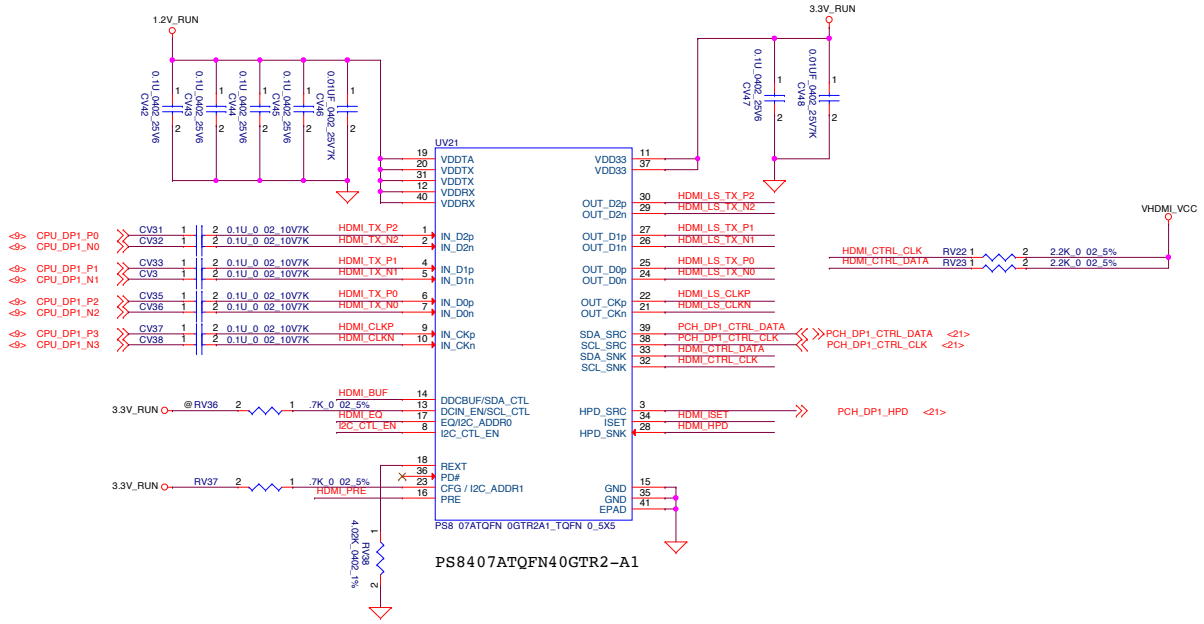
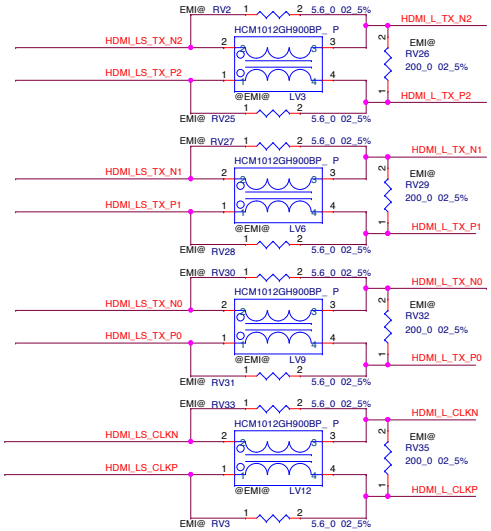
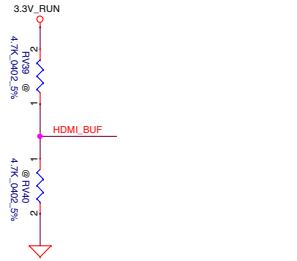
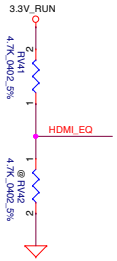
For Breckenridge 15



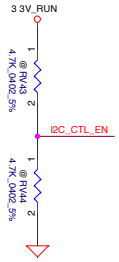




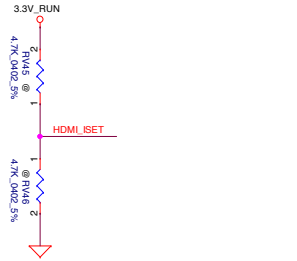
Enable active DDC buffer; Internal pull down at ~150KΩ, 3.3V I/O
L passive DDC pass-through(default)
H active DDC buffer with default threshold
M active DDC buffter without internal pull up resistor



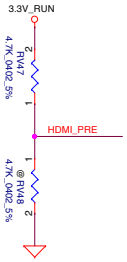
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L programmable EQ for channel loss up to 12.4dB(default)
H programmable EQ for channel loss up to 4.3dB
M programmable EQ for channel loss up to 8.6dB



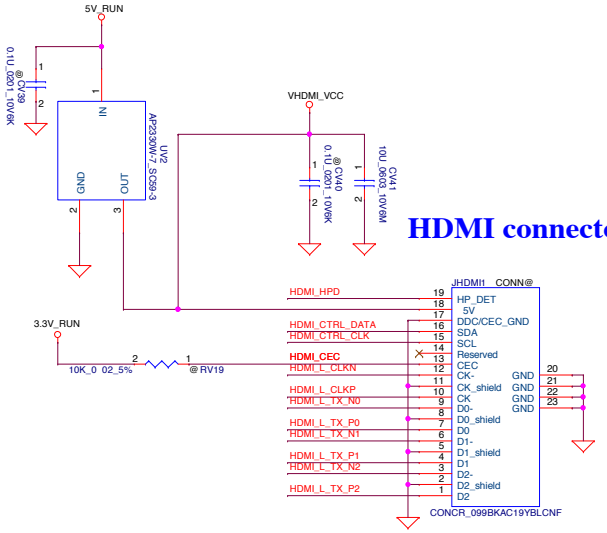
I2C Control enable Internal pull down at 150k 3.3V I/O
L Pin control is selected with auto jitter cleaning(default)
H I2C control is selected with default I2C address
M Pin control is selected with full jitter cleaning



TMDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
L default,1000mV
H increase +13%
M reduce -13%



Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L no pre-emphasis(default)
H 1.6dB pre-emphasis
M 2.5dB pre-emphasis



HDMI connector

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: HDMI CONN

Size	Document Number	Rev
B	LA-E153P	0.2

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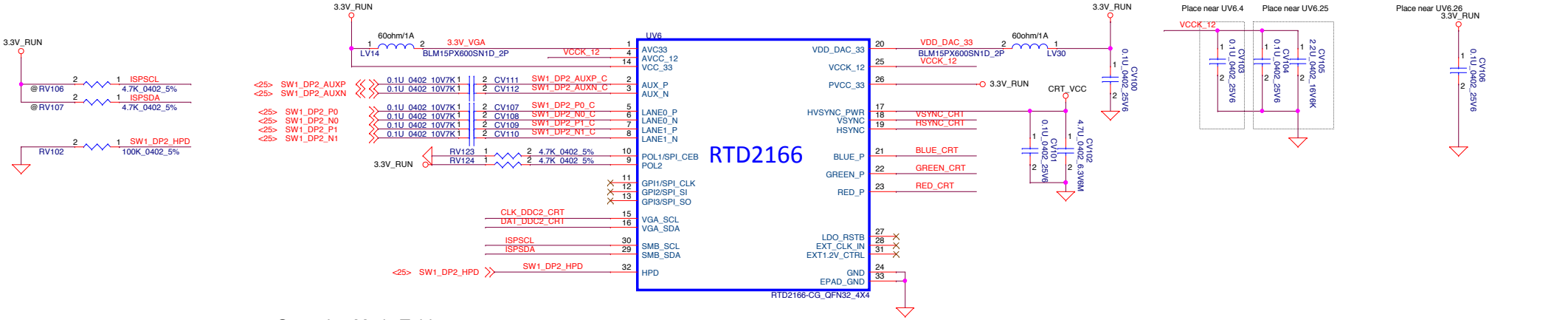
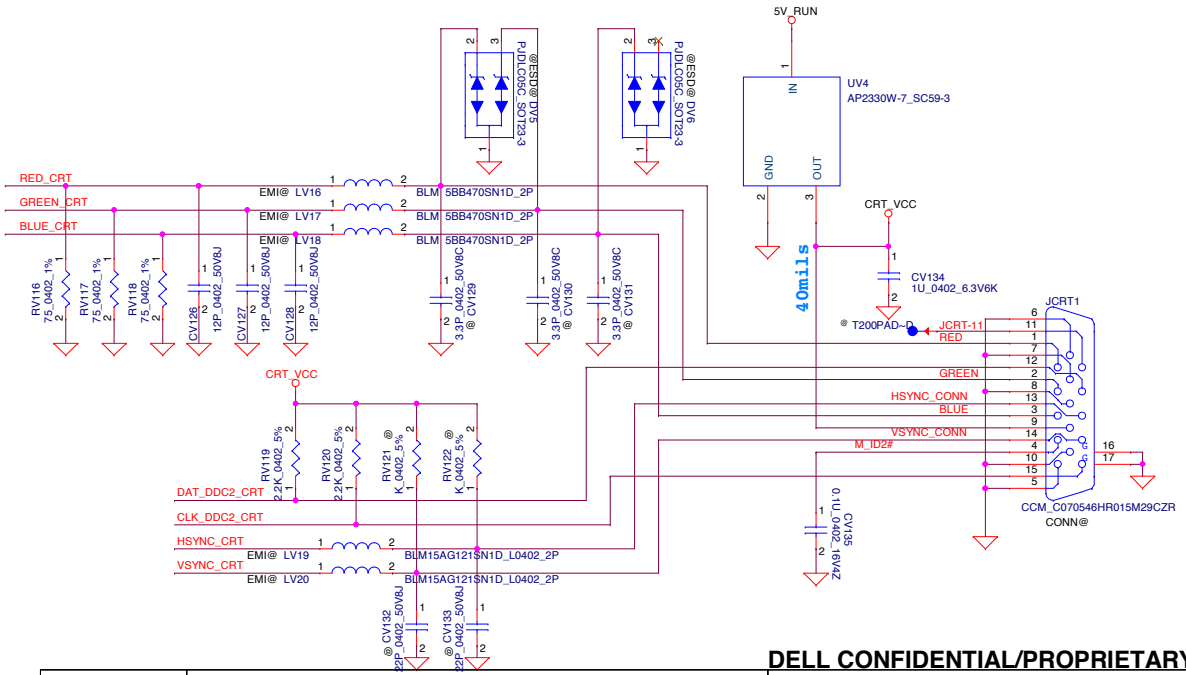
For TBT SW2_DP2
For non-TBT SW1_DP2

For Realtek Solution



Operation Mode Table

		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: DP to VGA & VGA Conn

Size: Custom | Document Number: LA-E153P | Rev: 0.2

Date: Tuesday, June 28, 2016 | Sheet 27 of 74

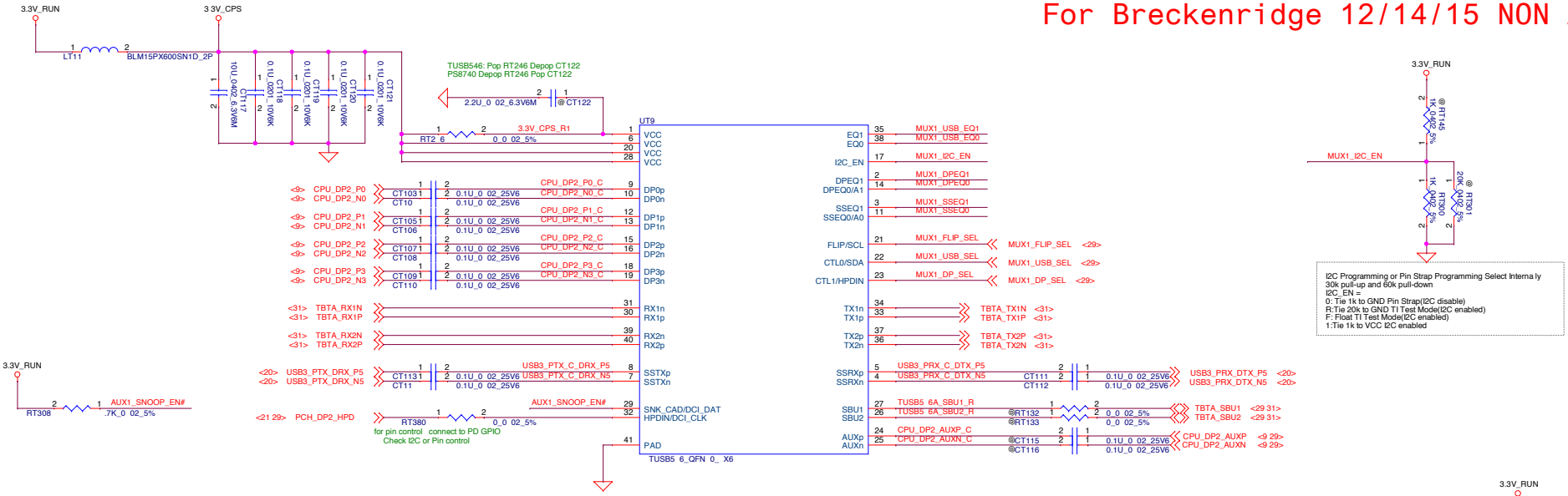


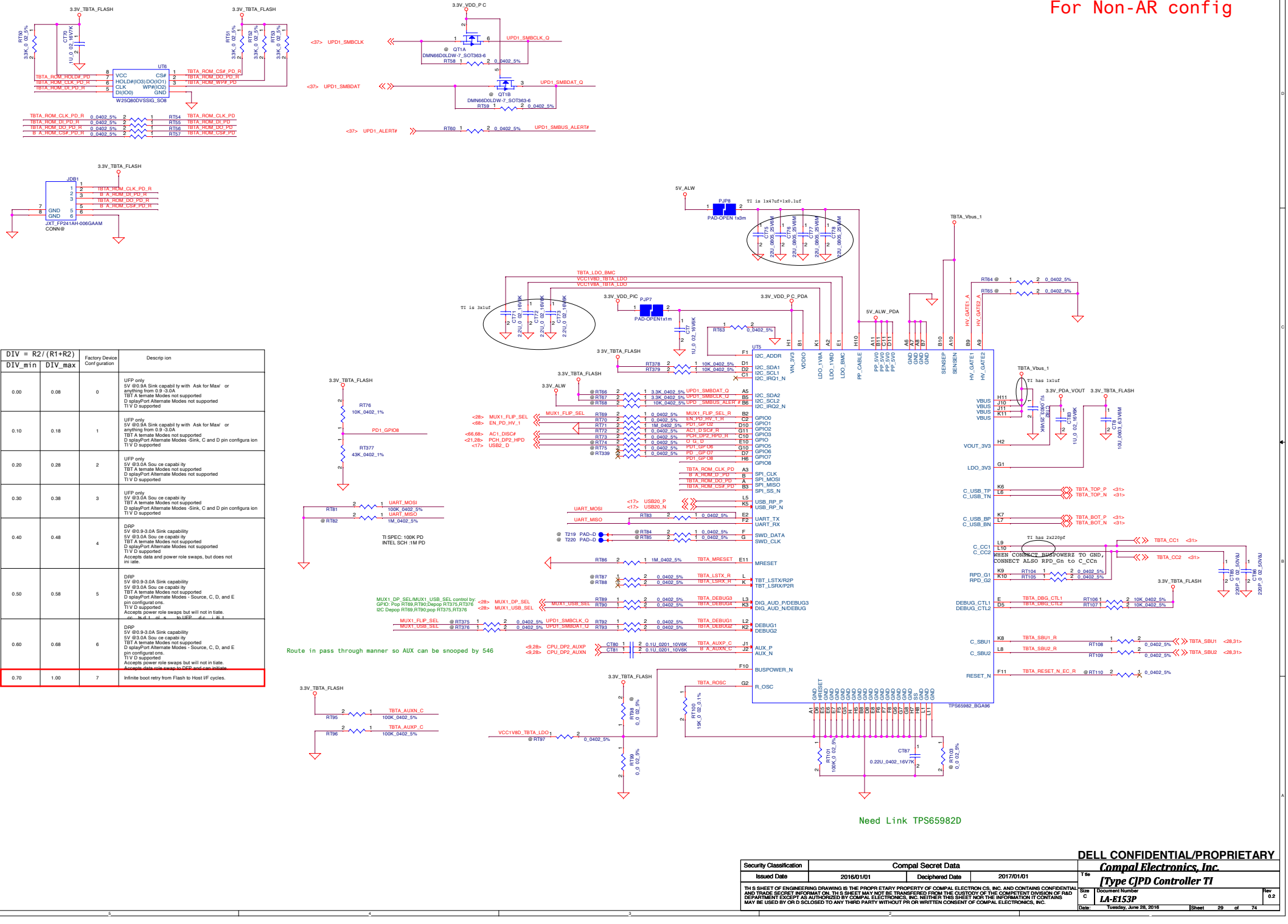
Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc.		
	DP/USB3 Repeater SW2 TUSB546		
Size B	Document Number LA-E153P		Rev 0.2
Date: Tuesday, June 28, 2016		Sheet 28 of 7	

For Non-AR config



DIV = R2/(R1+R2)		Factory Device Conf guration	Descrip ion
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capabil ty with Ask for Max/ or anything from 0.9 -3.0A TBT A temate Modes not supported D splayPort Alternate Modes not supported Ti V D supported
0.10	0.18	1	UFP only 5V @0.9A Sink capabil ty with Ask for Max/ or anything from 0.9 -3.0A TBT A temate Modes not supported D splayPort Alternate Modes -Sink, C and D pin configura ion Ti V D supported
0.20	0.28	2	UFP only 5V @3.0A Sou ce capabi ity TBT A temate Modes not supported D splayPort Alternate Modes not supported Ti V D supported
0.30	0.38	3	UFP only 5V @3.0A Sou ce capabi ity TBT A temate Modes not supported D splayPort Alternate Modes -Sink, C and D pin configura ion Ti V D supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Sou ce capabi ity TBT A temate Modes not supported D splayPort Alternate Modes not supported Ti V D supported Accepts data and power role swaps, but does not ini iate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Sou ce capabi ity TBT A temate Modes not supported D splayPort Alternate Modes - Source, C, D, and E pin configurat ons. Ti V D supported Accepts power role swaps but will not in tiate. cc ts d i ol s to UFP d c i ai t
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Sou ce capabi ity TBT A temate Modes not supported D splayPort Alternate Modes - Source, C, D, and E pin configurat ons. Ti V D supported Accepts power role swaps but will not in tiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

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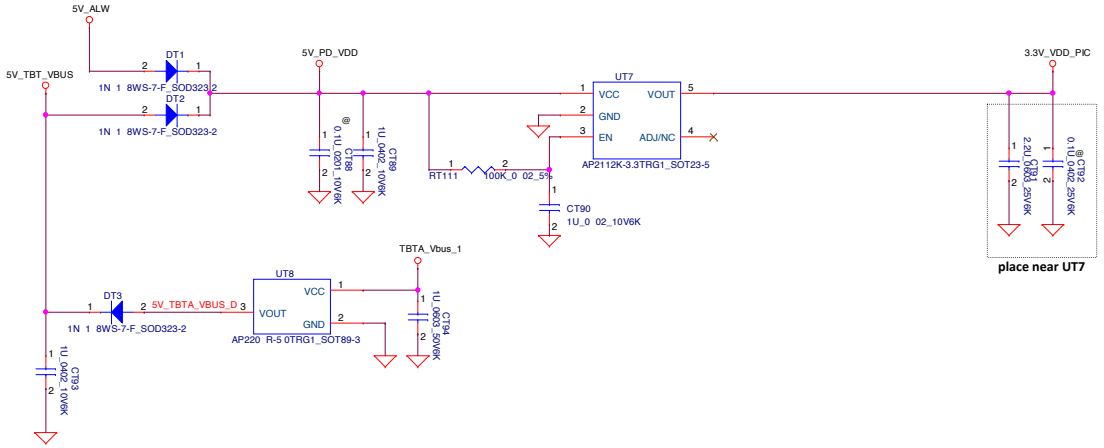
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: [Type CJPD Controller TI

Size: C | Document Number: LA-E153P | Rev: 0.2

Date: Tuesday, June 28, 2016 | Sheet 29 of 74



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

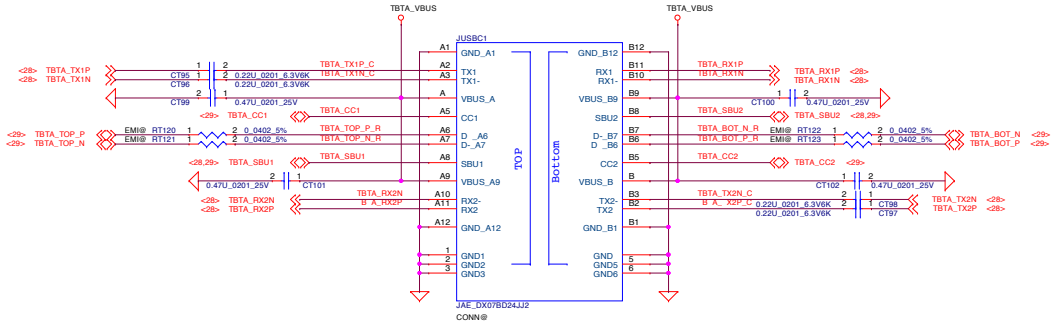
Compal Electronics, Inc.

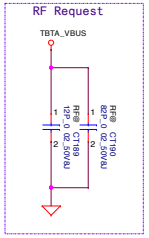
Title: [Type C]PD Power

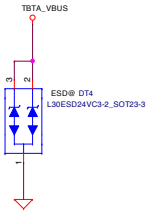
Size	Document Number	Rev
B	LA-E153P	0.2

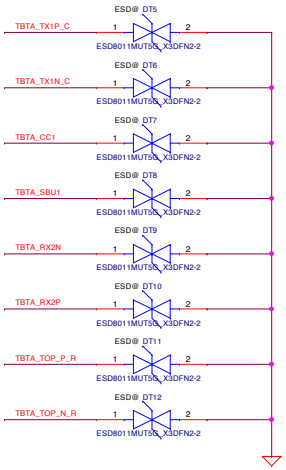
Date: Tuesday, June 28, 2016 | Sheet 30 of 7

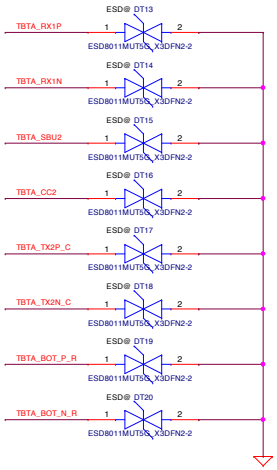
For NON AR Config

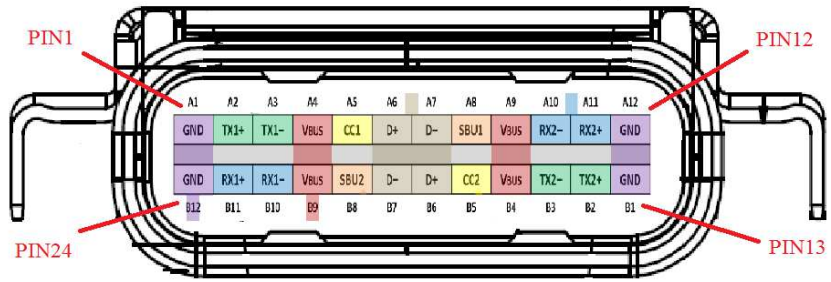








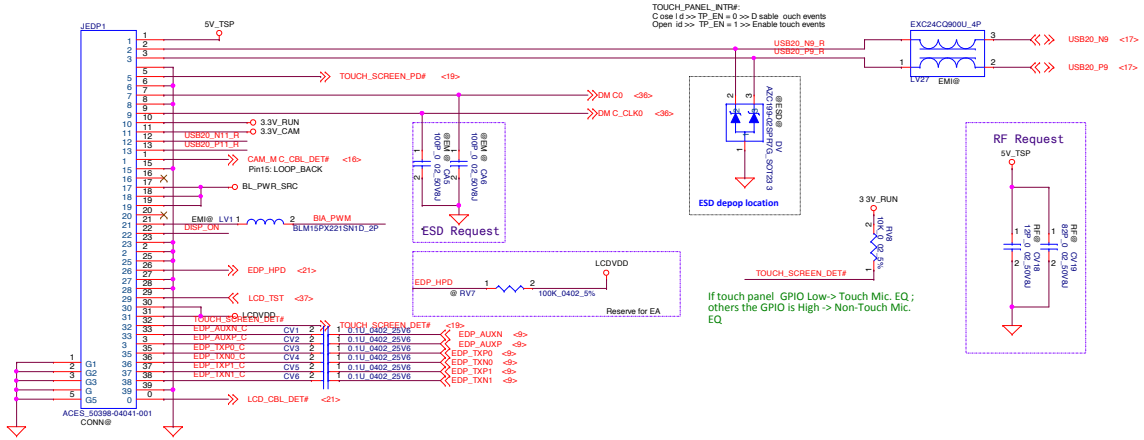


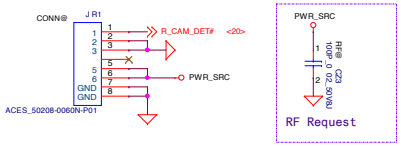


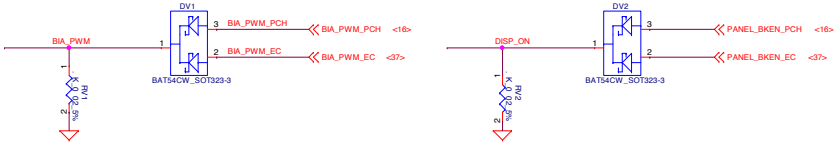
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

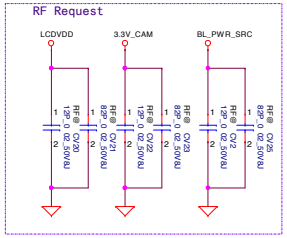
Compal Electronics, Inc.			
Title	USB 3.0 CONN TYPE C		
Size C	Document Number LA-E153P		Rev 0.2
Date: Tuesday, June 28, 2016	Sheet 31 of 74		

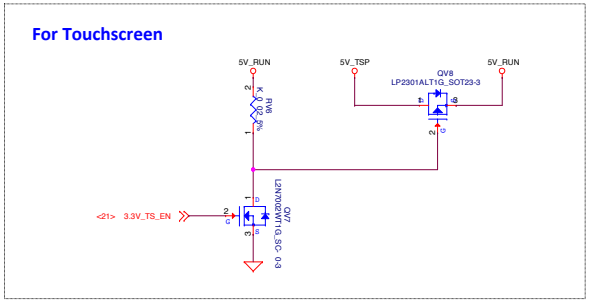
For Breckenridge 14

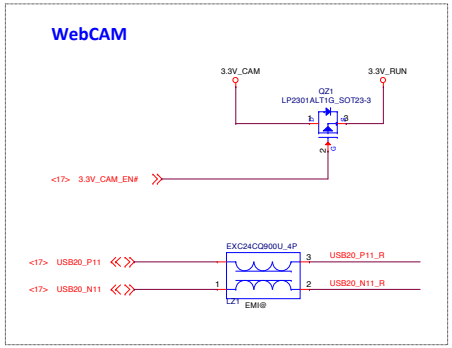


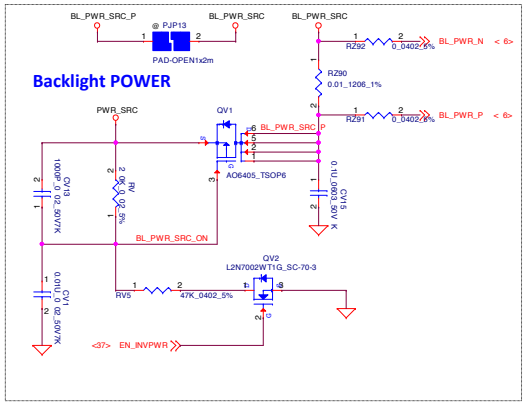


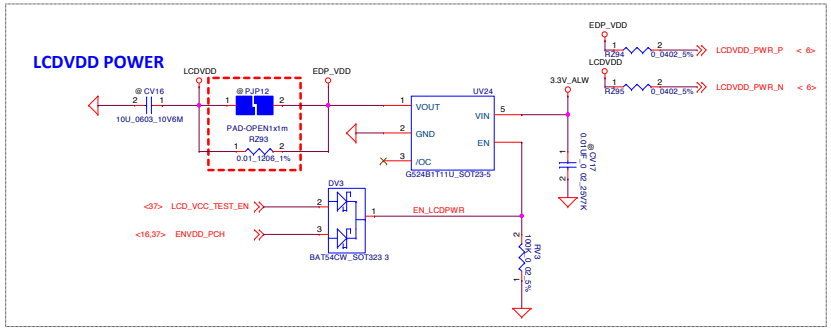












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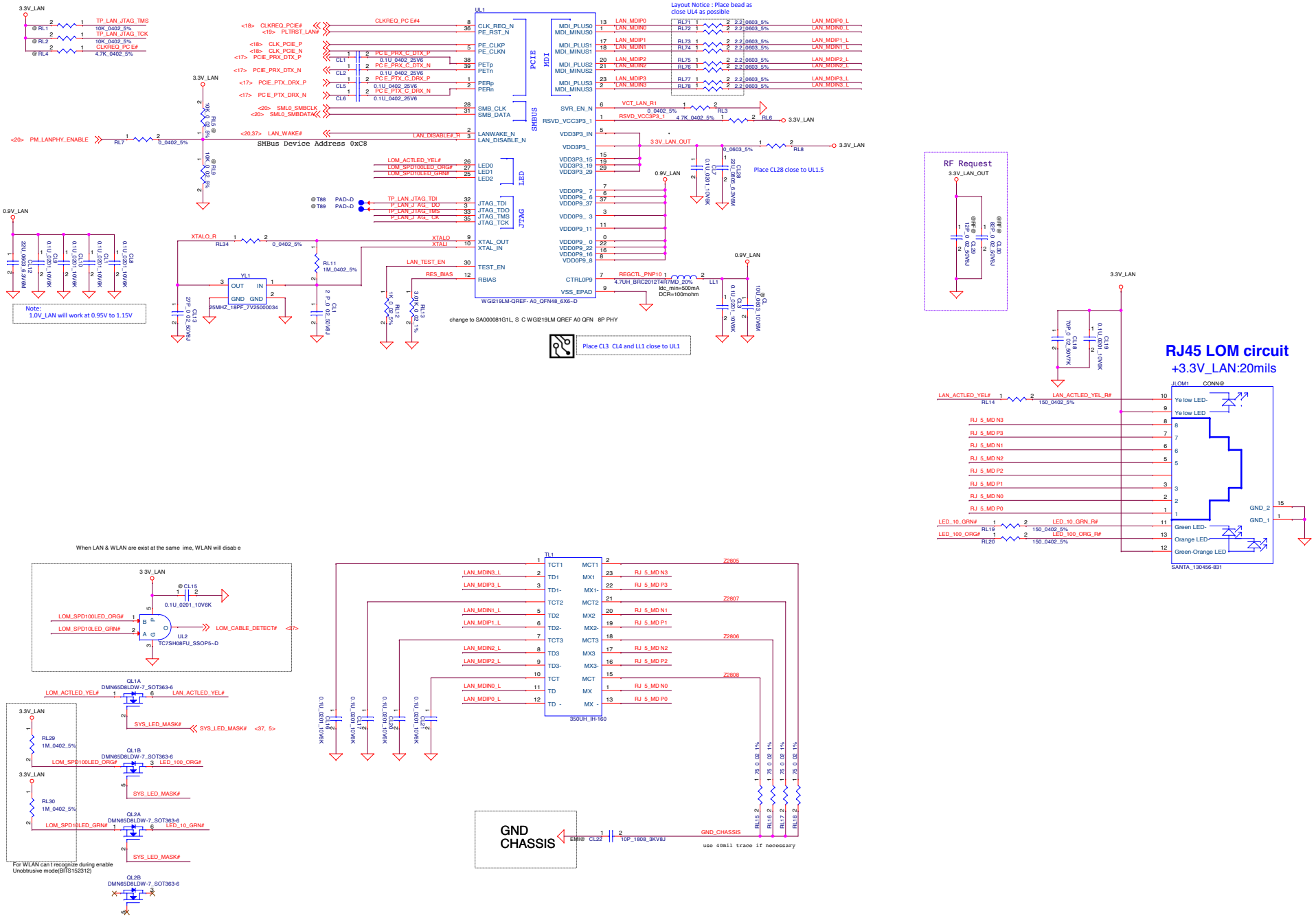
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: eDP CONN & Touch screen

Size	Document Number	Rev
C	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet 32 of 74



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc.		
	LAN Clarkvillie & RJ45		
Size	Document Number		Rev
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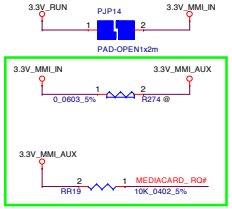
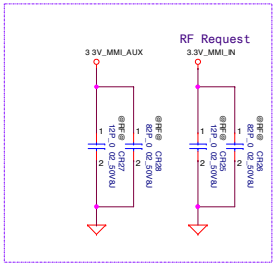
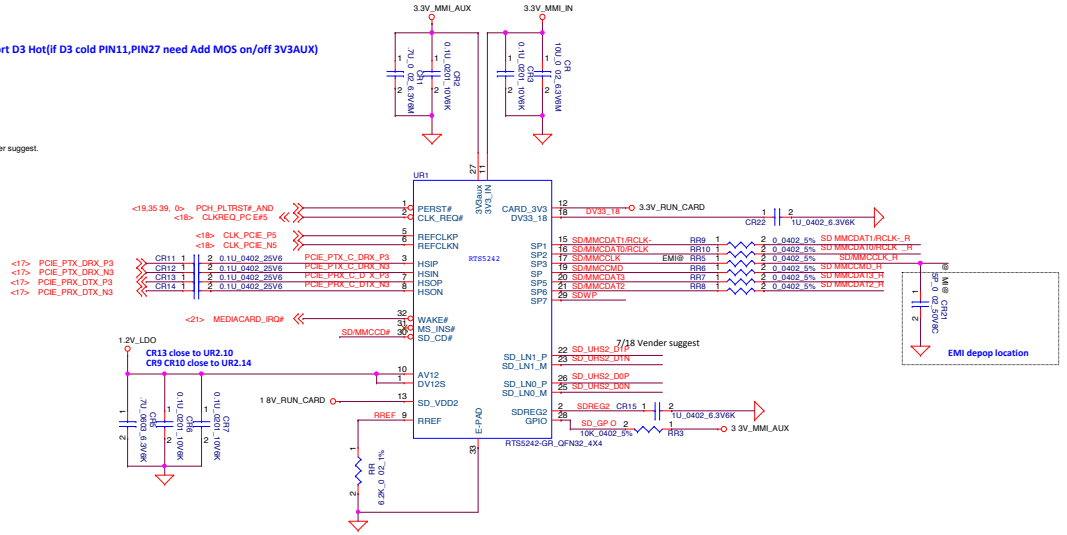
For PCIE Interface



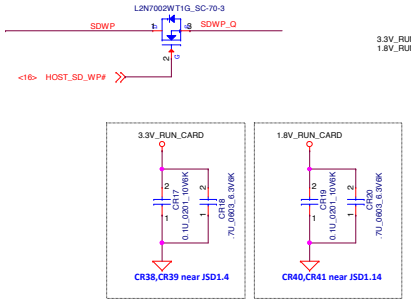
support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

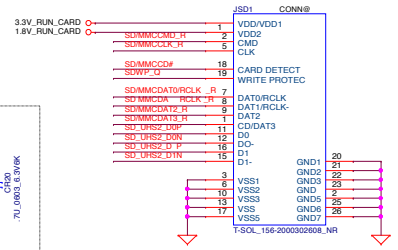
7/18 Vender suggest.





HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)





LINK SP070011U00 DONE

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc.		
	Card Reader		
Size	Document Number		Rev
C	LA-E153P		0.2
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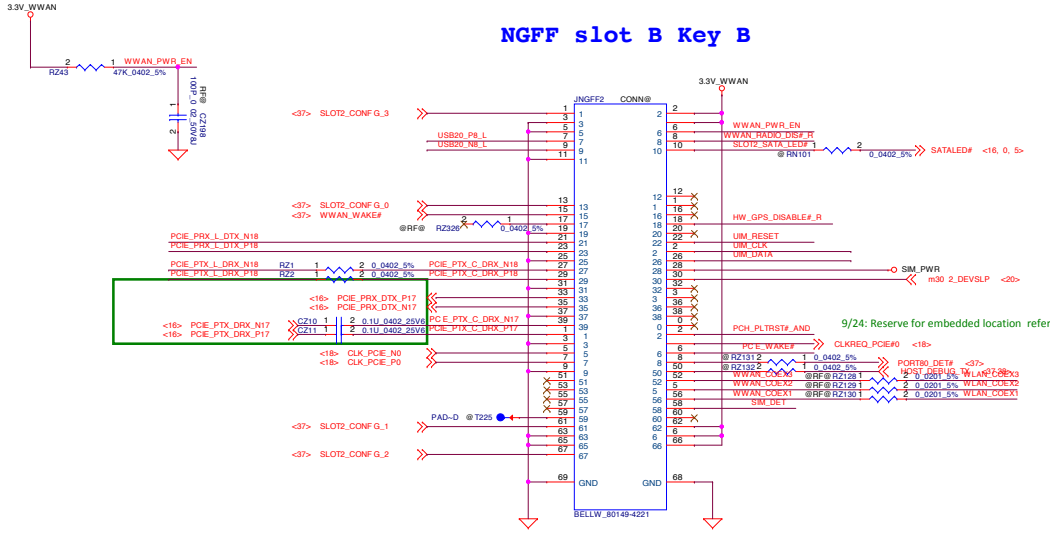
for Brekenridge 12/14/15 UMA

NGFF slot B Key B

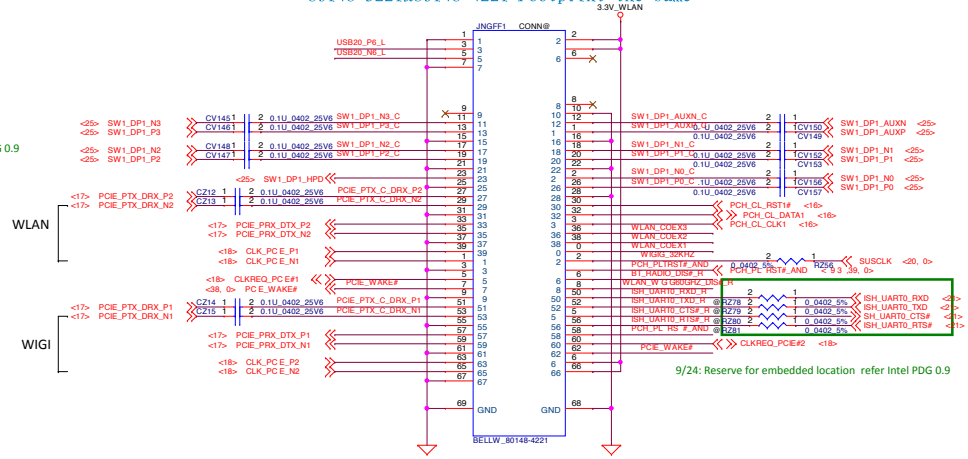


9/24: Reserve for embedded location refer Intel PDG 0.9

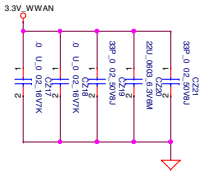
For TBT SW2_DP1
For non-TBT SW1_DP1

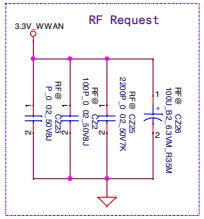
NGFF slot A Key A

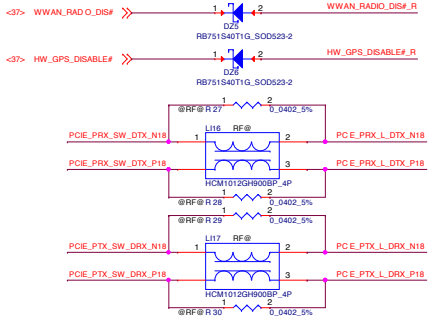
80148-3221&80148-4221 Footprint the same

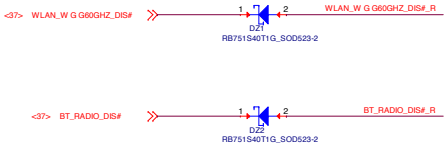


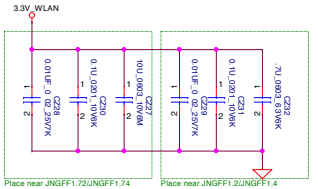
9/24: Reserve for embedded location refer Intel PDG 0.9





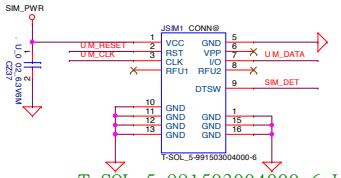




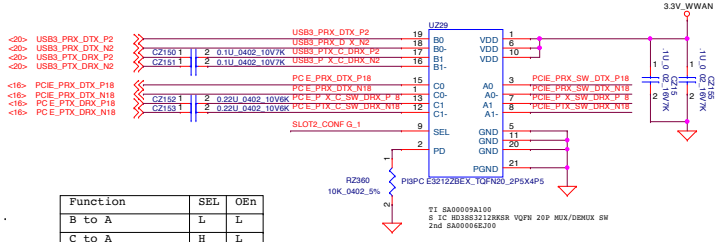


STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	m3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	H gh
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

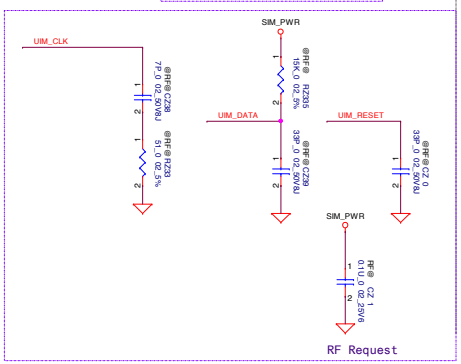
SIM Card Push-Push

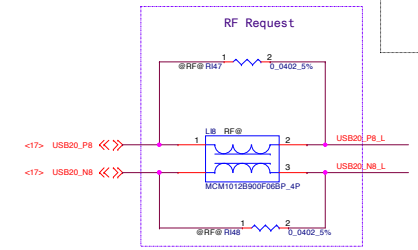


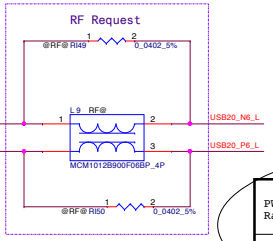
T-SOL_5-991503004000-6 LINK DONE

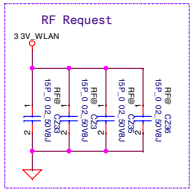


Function	SEL	OEn
B to A	L	L
C to A	H	L
All ports Hi-Z, IC power down	X	H









Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	NGFF Card		
Size	Document Number		Rev
Custom	LA-E153P		0.2
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1W x 1ch, ohm (Transducer spec is 8Ohm 0.5Watt per unit, there are two transducer un ts in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1

ACES_50278-00401-001

Close to UA1

Close to UA1 pin6

HDA_BIT_CLK_R

DMIC_CLK0

place close to UA1 pin3

Place closely to Pin 13.

AUD_SENSE_A

AUD_HP_NB_SENSE

Add for solve pop noise and detect issue

place at AGND and DGND plane

PJP19

PAD-OPEN1x1m

CLASS-D POWER DOWN CONTROL CIRCUIT

AUD_NB_MUTE#

HDA_RST#_R

HDA_Link`s 3.3V,no need level sh ft circuit

RB751S40T1G_SOD523-2

PD#

RE313@one control line f DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

EM5209VF_SON14_2X3

2.5A

500mA

Place CA29 close to Codec

ALC3246-CG_MQFN48_6X6

Add this Fi ter o avo d other components/chips be influenced

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Global Headset

Universal Jack

SINGA_2SJ3095-059111F

Normal

Open

Only BR15U UMA use LA2,LA3,because 6L

RF Request

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: Codec ALC3246

Size	Document Number	Rev
C	LA-E153P	0.2

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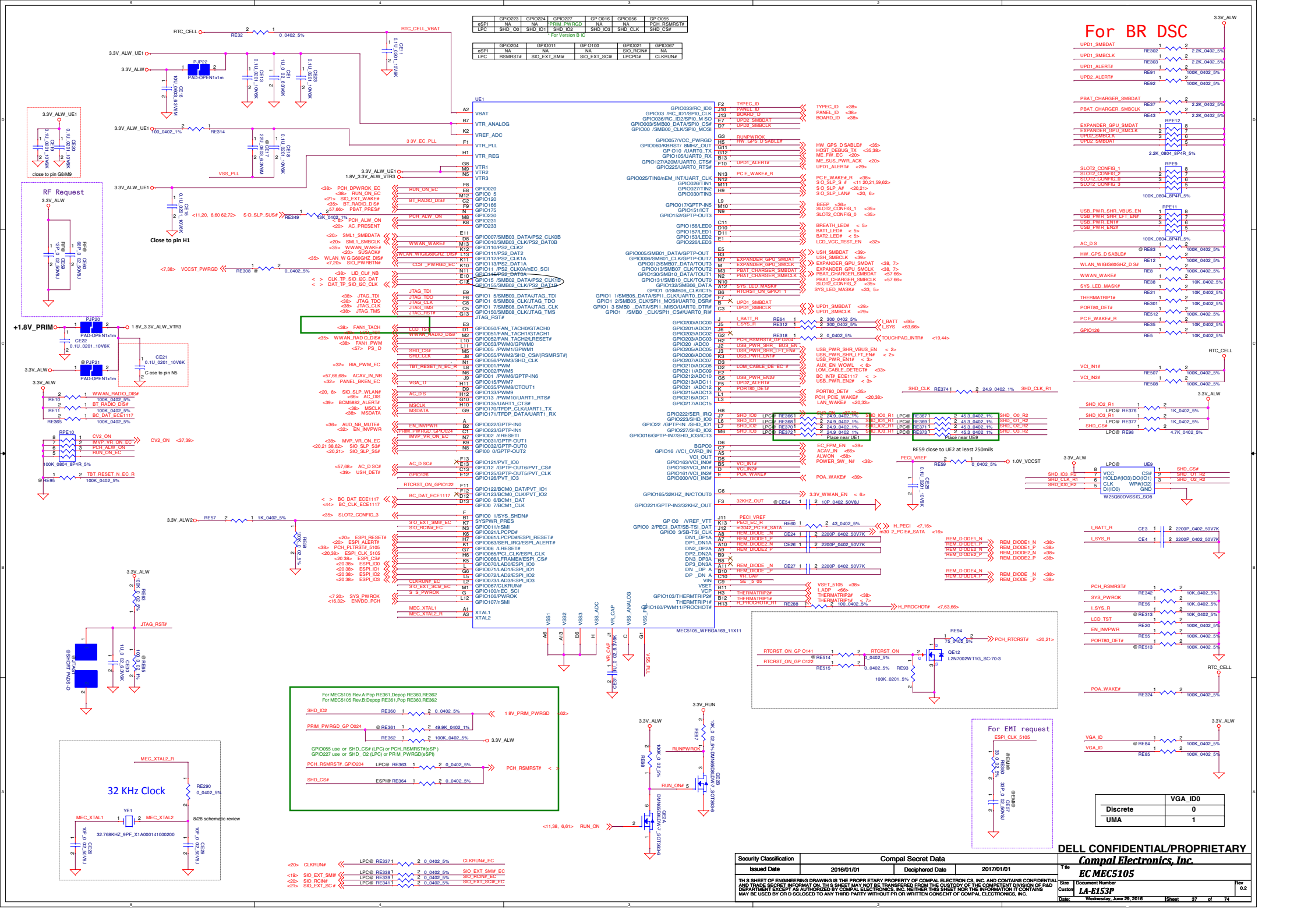
For BR DSC
RF Request
32 KHz Clock
For EMI request
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
EC MEC5105
Security Classification
Compal Secret Data
Issued Date
2016/01/01
Deciphered Date
2017/01/01
Size
Custom
Document Number
LA-E153P
Rev
0.2
Date:
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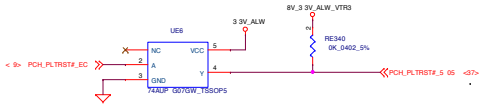
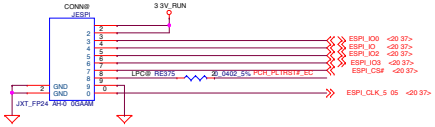
Sheet
37
of
74
VGA_ID0
Discrete
0
UMA
1

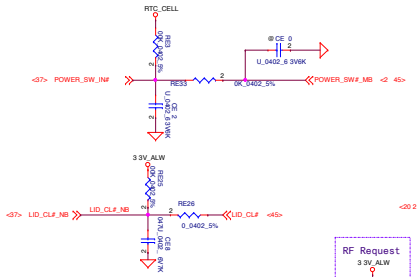
For BR DSC

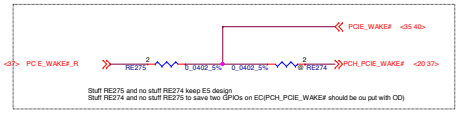


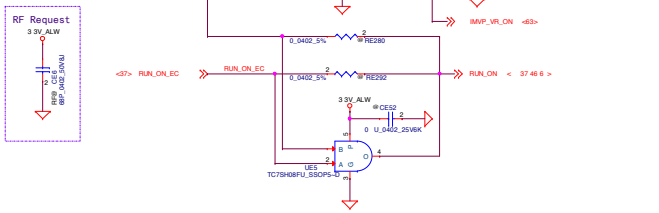


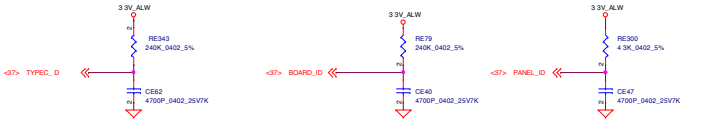
PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3 3V_RUN	+3 3V_RUN
2	+3 3V_RUN	+3 3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK









RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR w/o AR)
4.3K	4700p	,
2K	4700p	
1K	4700p	

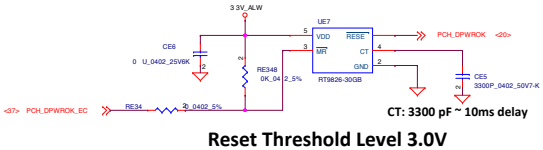
RE79	CE40	REV
* 240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	BR15 H
* 4.3K	4700p	BR15 P

PD_ACE_DET# rise time is measured from 5% 68%.

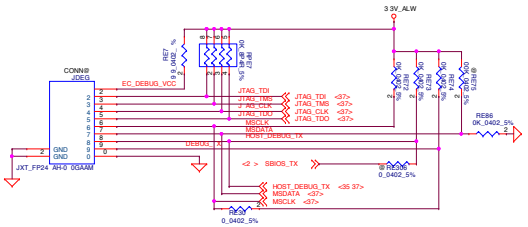
BOARD_ID rise time is measured from 5% 68%.

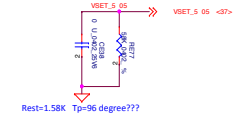
PANEL_ID rise time is measured from 5% 68%.

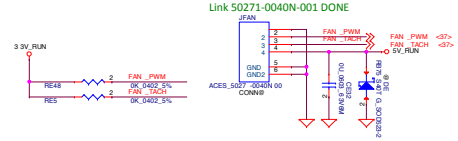


CT: 3300 pF ~ 10ms delay

Reset Threshold Level 3.0V





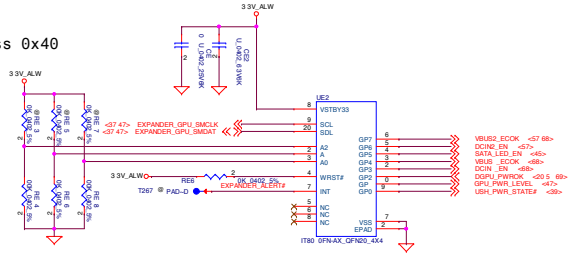


Control Byte

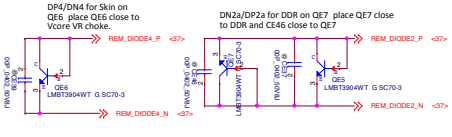
0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Wire
R/W = 1 = Read

SMBus address 0x40



5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



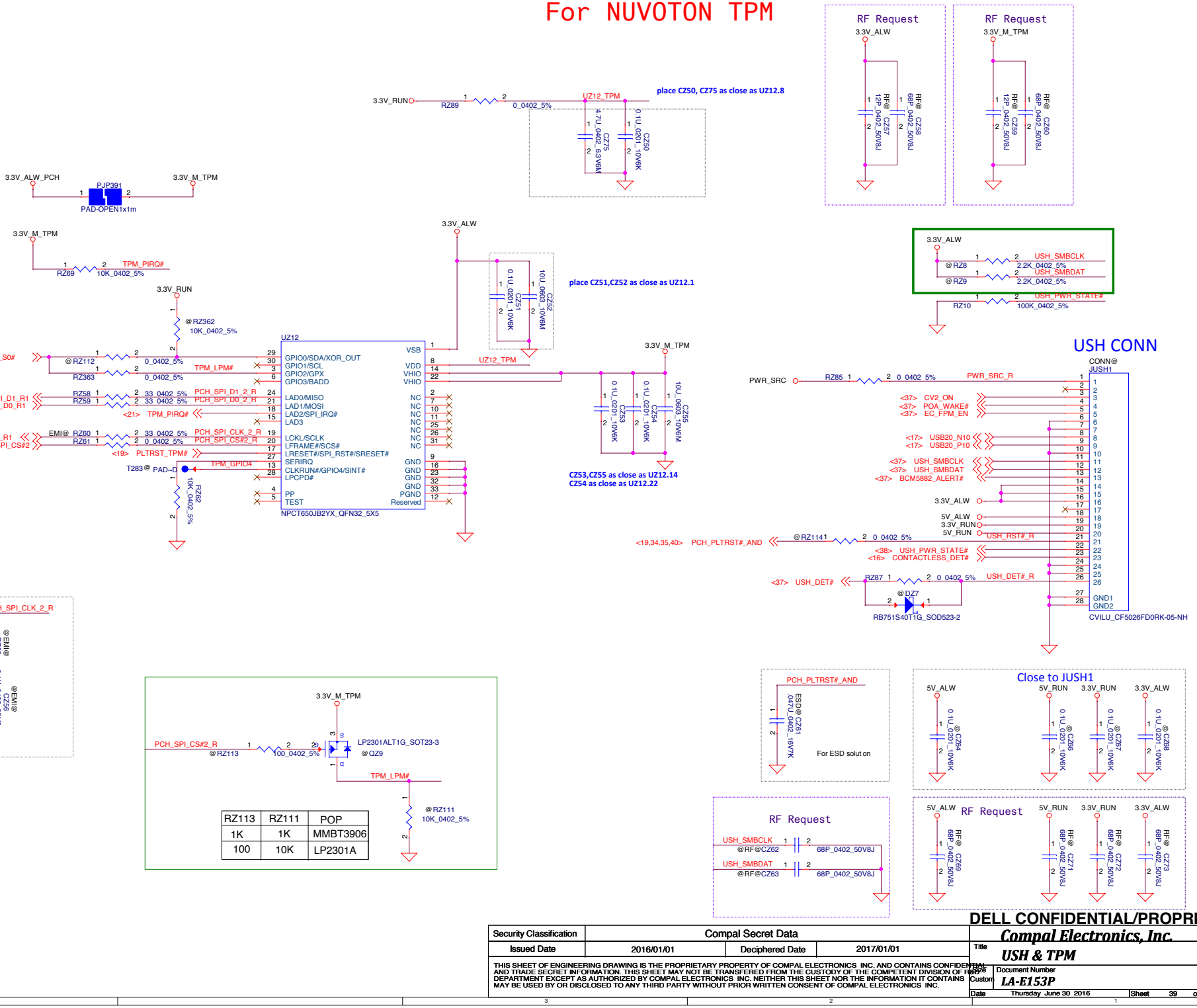
Security Classi ication	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017 01/01

Compal Electronics, Inc.

MEC5105 SUPPORT

Size	Document Number	Rev
Custom	LA-E153P	0.2
Date	Tuesday, June 28, 20 6	Sheet 38 of 74

For NUVOTON TPM



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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: USH & TPM

Size: Custom | Document Number: LA-E153P | Rev: 0.2

Date: Thursday, June 30, 2016 | Sheet 39 of 74

For Breckenridge 15

RF Request

3.3V_HDD_M2

@RH@ CN60 68P_0402_50V8J

3.3V_HDD_M2

@CN61 0.1U_0201_10V6K

CN62 0.1U_0201_10V6K

CN63 22U_0603_6.3V6M

CN64 22U_0603_6.3V6M

Place near HDD CONN

3.3V_RUN

@RZ100 0_0_02_5% HDD_PWR_P <41 46>

3.3V_HDD_M2

@RZ101 0_0_02_5% HDD_PWR_N <41 46>

2280 SSD

NGFF slot C Key M

3.3V_HDD_M2

@RN37 M2280_DEVSLP 10K_0_02_5%

if signal is PCIE GEN3/SATA GEN3 maybe change C value or no need for DG0.9 SATA EXPRESS HDD

RZ99 0.01_1206_1%

2.8A

3.3V_RUN

@PJP31 PAD-OPEN1x3m

JNGFF3 CONN@

1	GND	2	3.3VAUX
3	GND	4	3.3VAUX
5	PERn3	6	N/C
7	PERp3	8	N/C
9	GND	10	DAS/DSS#
11	PETn3	12	3.3VAUX
13	PETp3	14	3.3VAUX
15	GND	16	3.3VAUX
17	PERn2	18	3.3VAUX
19	PERp2	20	N/C
21	GND	22	N/C
23	PETn2	24	N/C
25	PETp2	26	N/C
27	GND	28	N/C
29	PERn1	30	N/C
31	PERp1	32	N/C
33	GND	34	N/C
35	PETn1	36	N/C
37	PETp1	38	DEVSLP
39	GND	40	N/C
41	PERn0/SATA B	42	N/C
43	PERp0/SATA B-	44	N/C
45	GND	46	N/C
47	PETn0/SATA A-	48	N/C
49	PETp0/SATA A	50	PERST#
51	GND	52	CLKREQ#
53	REFCLKn	54	PEWake#
55	REFCLKp	56	N/C
57	GND	58	N/C
67	N/C	68	SUSCLK
69	PEDET	70	3.3VAUX
71	GND	72	3.3VAUX
73	GND	74	3.3VAUX
75	GND		
77	MTG77	76	MTG76

LCN_DAN05-67356-0103

<16> PC E_PRX_DTX_N12
<16> PC E_PRX_DTX_P12
CN65 0.22U_0_02_10V6K PCIE_PTX_C_DRX_N12
CN66 0.22U_0_02_10V6K PCIE_PTX_C_DRX_P12
<16> PCIE_PTX_DRX_N12
<16> PCIE_PTX_DRX_P12
<16> PC E_PRX_DTX_N11
<16> PC E_PRX_DTX_P11
CN67 0.22U_0_02_10V6K PCIE_PTX_C_DRX_N11
CN68 0.22U_0_02_10V6K PCIE_PTX_C_DRX_P11
<16> PCIE_PTX_DRX_N11
<16> PCIE_PTX_DRX_P11
<16> PCIE_PRX_DTX_N10
<16> PCIE_PRX_DTX_P10
CN69 0.22U_0_02_10V6K PCIE_PTX_C_DRX_N10
CN70 0.22U_0_02_10V6K PCIE_PTX_C_DRX_P10
<16> PC E_PTX_DRX_N10
<16> PC E_PTX_DRX_P10
<16> PCIE_PRX_DTX_P9
<16> PCIE_PRX_DTX_N9
CN71 0.22U_0_02_10V6K PCIE_PTX_C_DRX_N9
CN72 0.22U_0_02_10V6K PCIE_PTX_C_DRX_P9
<16> PCIE_PTX_DRX_N9
<16> PCIE_PTX_DRX_P9
<18> CLK_PCIE_N3
<18> CLK_PCIE_P3
<16> M2280_PCIE_SATA#

NVME_LED# @RN100 0_0_02_5% SATALED# <16 35 45>

M2280_DEVSLP <20>

PCH_PLTRST#_AND <19 3 35 39>

PCIE_WAKE# CLKREQ_PCIE#3 <18>

PC E_WAKE# <35 38>

SUSCLK_R RN99 0_0_02_5% SUSCLK <20 35>

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: M2 2280 Socket

Size: B | Document Number: LA-E153P | Rev: 0.2

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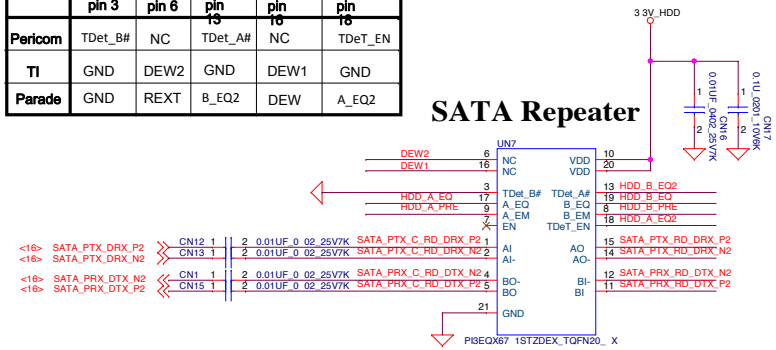
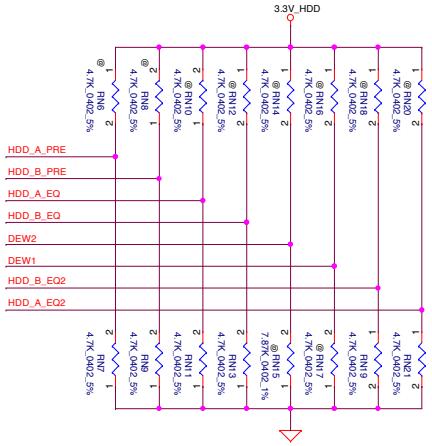
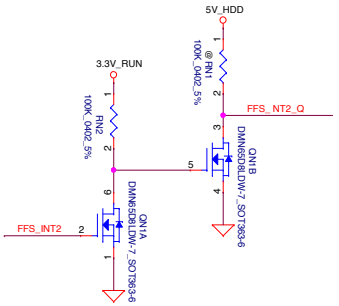
	pin 3	pin 6	pin 15	pin 16	pin 18
Pericom	TDet_B#	NC	TDet_A#	NC	TDeT_EN
TI	GND	DEW2	GND	DEW1	GND
Parade	GND	REXT	B_EQ2	DEW	A_EQ2

SATA Repeater



	HDD_A_EQ PIN17	HDD_B_EQ PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
Pericom PI3EQX6741ST	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC	NC	PD (RN9)	PD (RN11)
TI SN75LVCP601	PD (RN13)	NC	PD (RN83)	PD (RN23)	NC (IPU)	NC (IPU)	PH (RN8)	PH (RN10)
Parade PS8527C	PD (RN13)	PD (RN16)	PD (RN83)	PD (RN23)	NC (1/2 VDD)	PD (RN19)	NC (1/2 VDD)	NC (1/2 VDD)

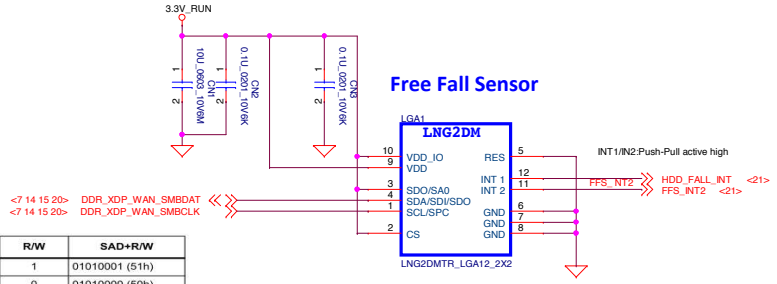




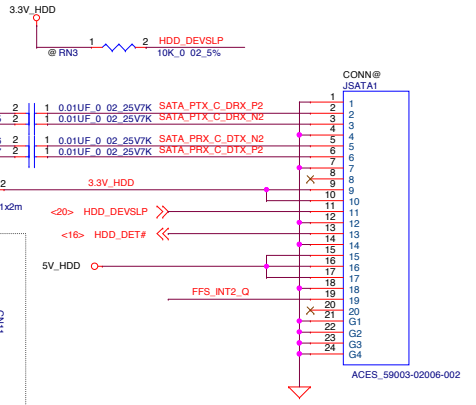
			A_EQ	B_EQ		A_EM	B_EM
Main	Pericom	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
2nd	TI	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
3rd	Parade	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	A_EQ 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	B_EQ 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 M 1	A_EM 0dB -3.5dB -1.5dB	B_EM 0dB -3.5dB -1.5dB

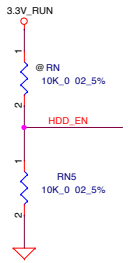
* red color is current setting

Free Fall Sensor

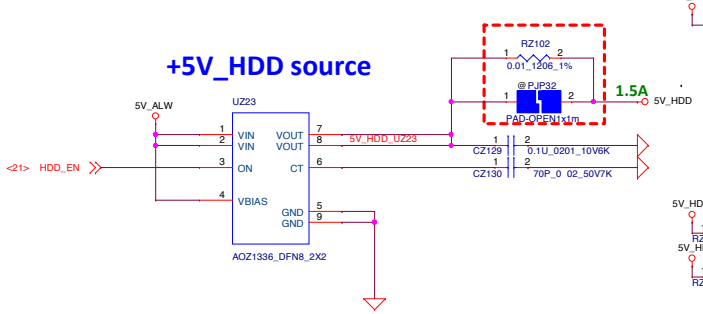


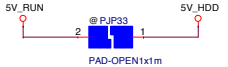
Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

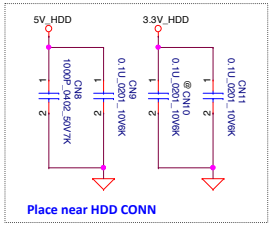


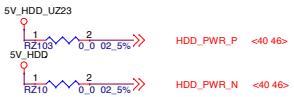


+5V_HDD source









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Security Classification	Compal Secret Data	
Issued Date	2016/01/01	Deciphered Date 2017/01/01

Compal Electronics, Inc.

Title: HDD CONN

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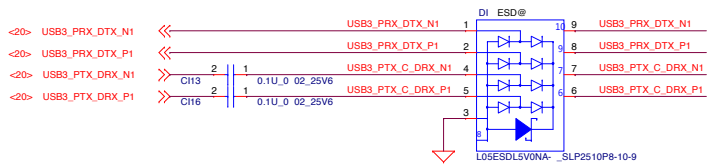
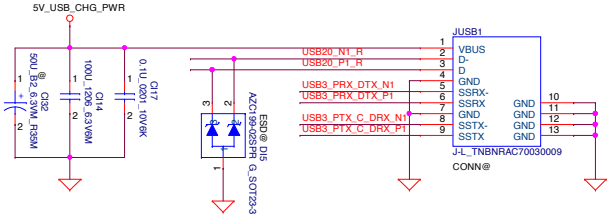
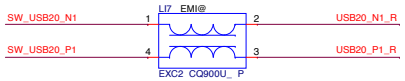
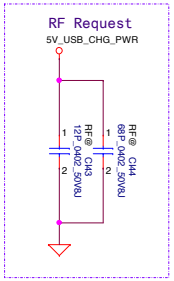
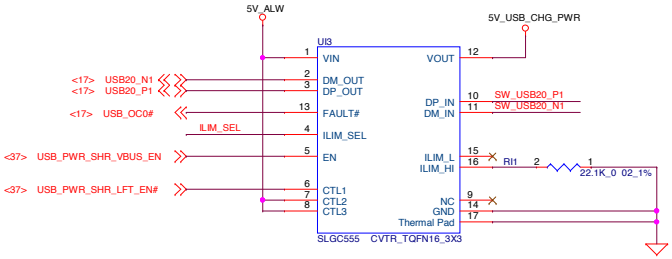
For PWR SW + Charger combine IC

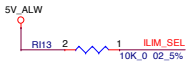


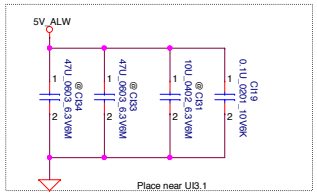












Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title	*USB SW*	
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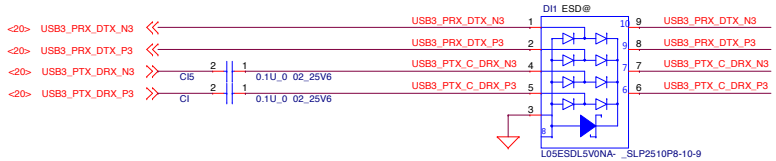
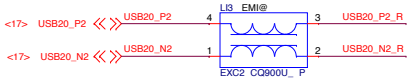
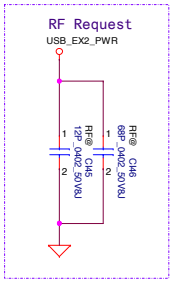
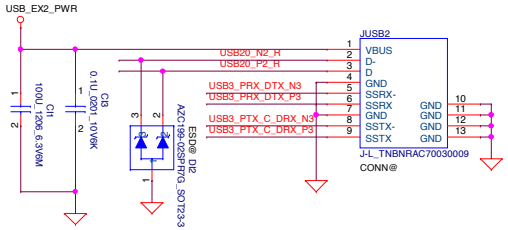
For Breckenridge 14&15/Steamboat 14

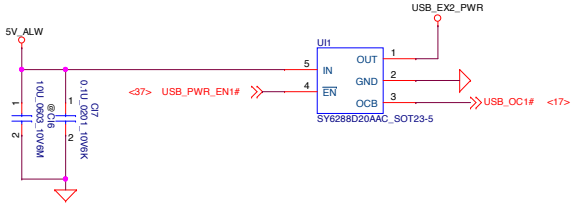


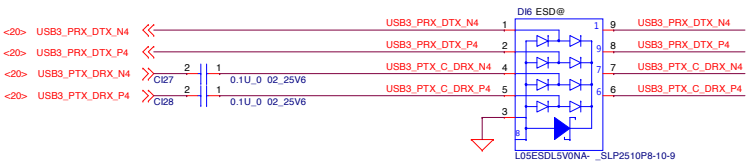


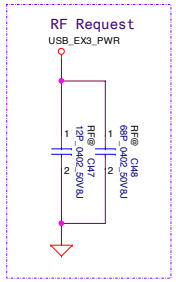
DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm

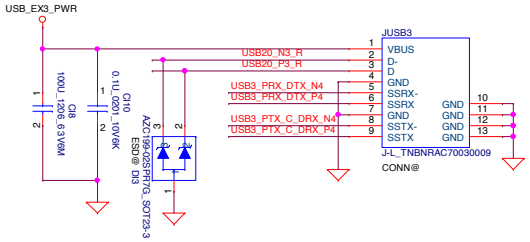


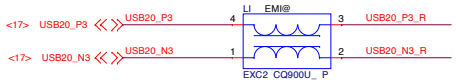


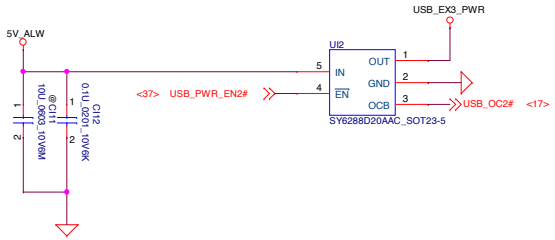












Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc.

Title: *JUSB2&JUSB3*

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B	*LA-E153P*	0.2

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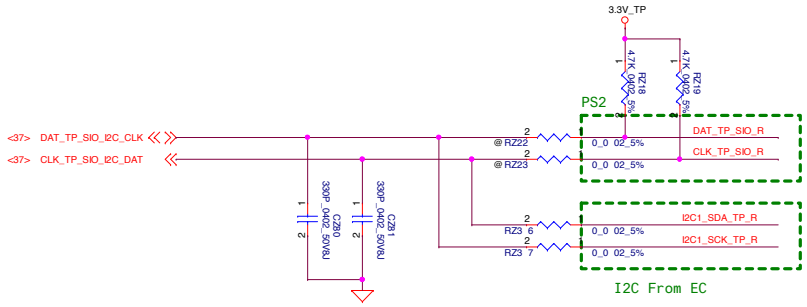
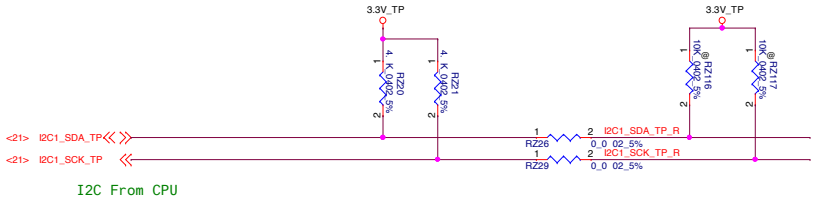
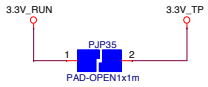
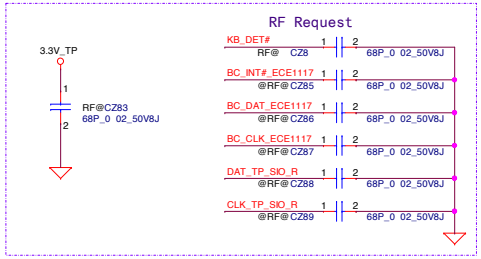
Touch Pad



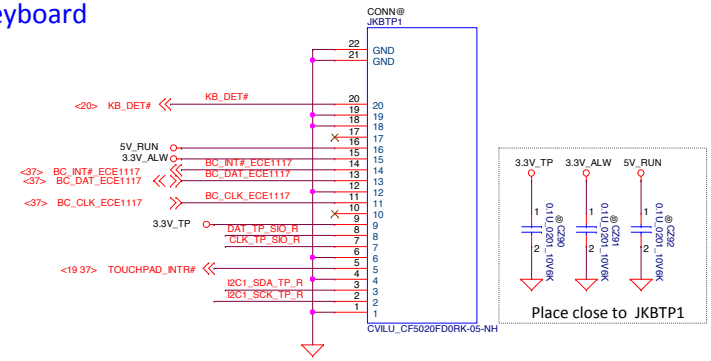


Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will u ilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC w ll control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan f I2C has issues

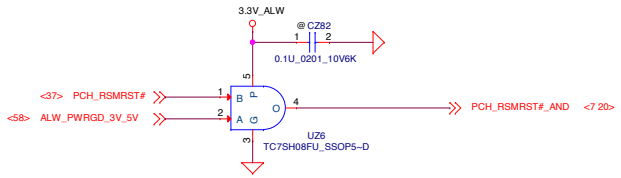




Keyboard



RSMRST circuit



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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

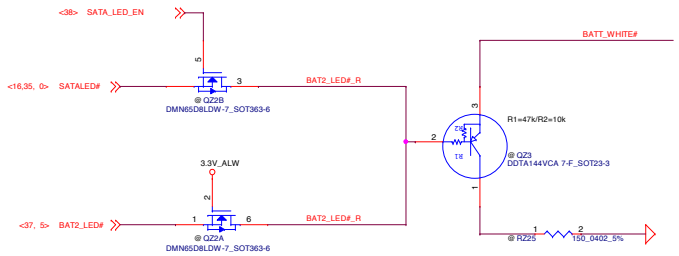
Title: Keyboard

Size	Document Number	Rev
B	LA-E153P	0.2

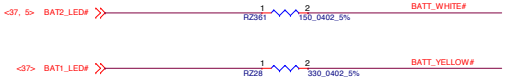
Date: Tuesday, June 28, 2016 Sheet of 7

HDD LED MUX

means EC can sw tch ba tery white led and HDD LED by hot key Fn H

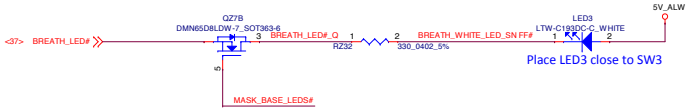


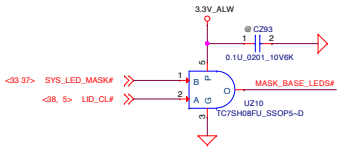
Battery LED



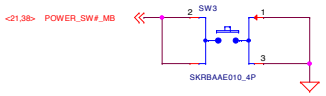
Breath LED

LED P/N change to SC50000FL00 from SC50000BA00

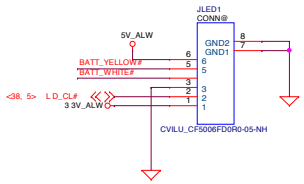




POWER & INSTANT ON SWITCH



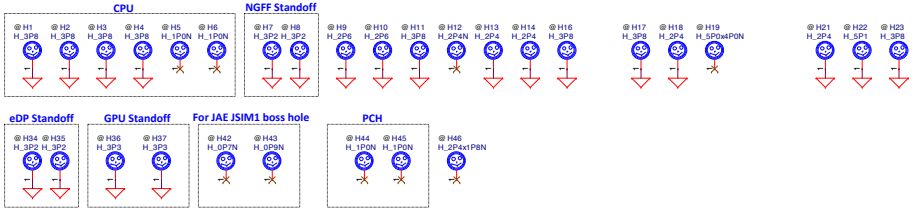
LED board CONN



Fiducial Mark

@ FD1 F DUCIAL MARK~D
@ FD2 F DUCIAL MARK~D
@ FD3 F DUCIAL MARK~D
@ FD4 F DUCIAL MARK~D

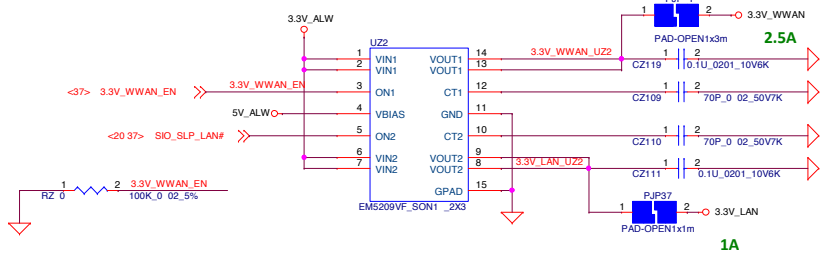
LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



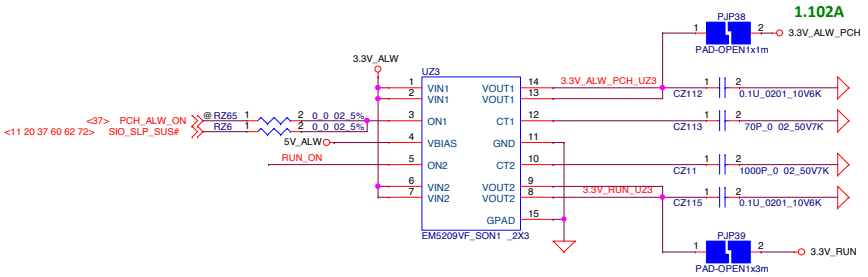
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	PAD, LED		
Size C	Document Number LA-E153P		Rev 0.2
Date: Tuesday, June 28, 2016		Sheet 45 of 74	

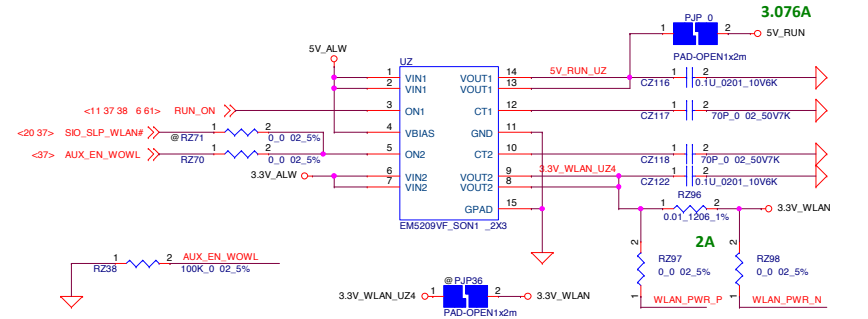
+3.3V_WWAN/+3.3V_LAN source



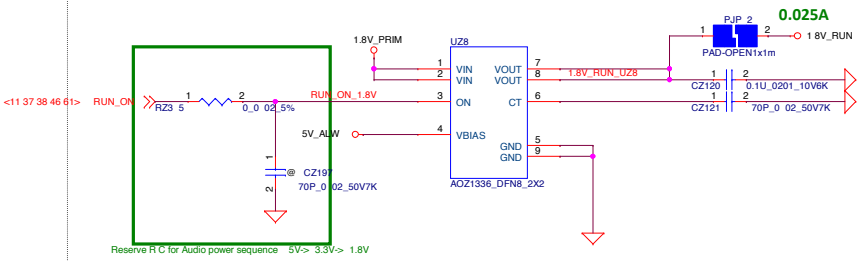
+3.3V_ALW_PCH/+3.3V_RUN source



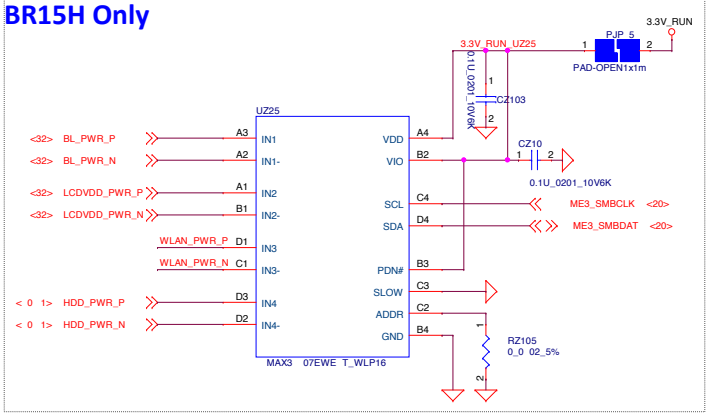
+5V_RUN/+3.3V_WLAN source



+1.8V_RUN source

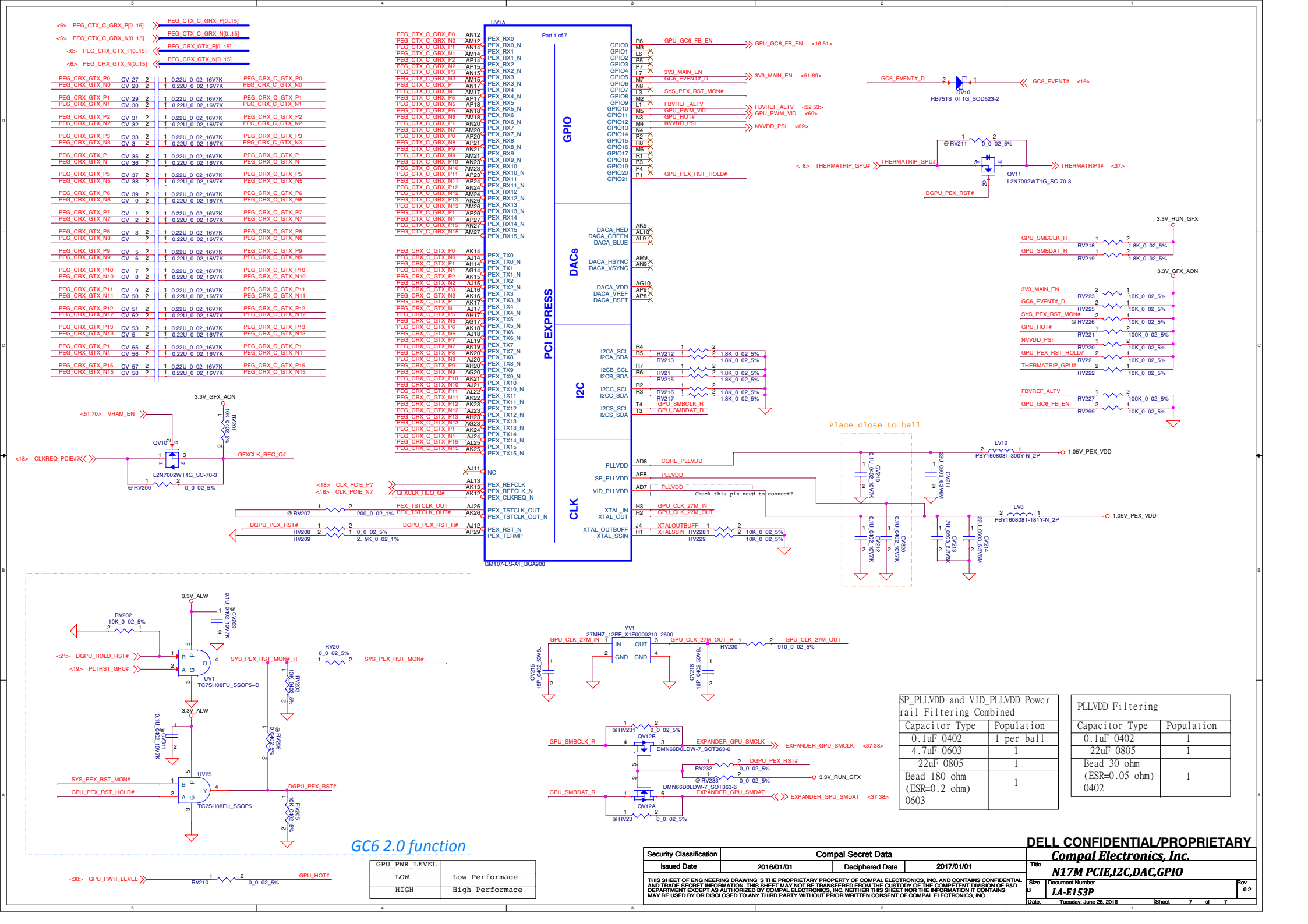


BR15H Only



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title	Compal Electronics, Inc.		
	Power control		
Size B	Document Number LA-E153P		Rev 0.2
Date: Tuesday, June 28, 2016		Sheet 6 of 7	



SP_PLLVDD and VID_PLLVDD Power rail Filtering Combined	
Capacitor Type	Population
0.1uF 0402	1 per ball
4.7uF 0603	1
22uF 0805	1
Bead 180 ohm (ESR=0.2 ohm) 0603	1

PLLVDD Filtering	
Capacitor Type	Population
0.1uF 0402	1
22uF 0805	1
Bead 30 ohm (ESR=0.05 ohm) 0402	1

GPU_PWR_LEVEL	
LOW	Low Performace
HIGH	High Performace

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: **N17M PCIE,I2C,DAC,GPIO**

Size	Document Number	Rev
B	LA-E153P	0.2

Date: Tuesday, June 28, 2016 | Sheet 7 of 7

I2CS Slave Address

SMBUS_ALT_ADDR	Description
0	0x9E(Default)
1	0x9C(Multi-GPU usage)

VGA_DEVICE Setting

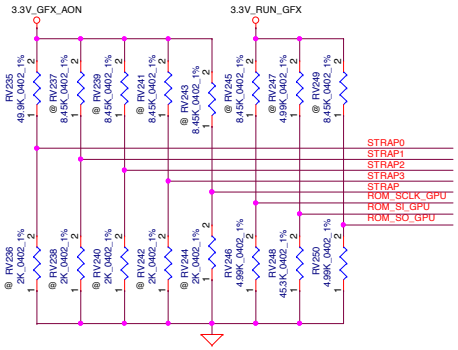
VGA_DEVICE	Description
0	Non-Primary 3D Acceleration Device(Class Code 302h)
1	Primary Display or VGA Device(Class Code 300h)

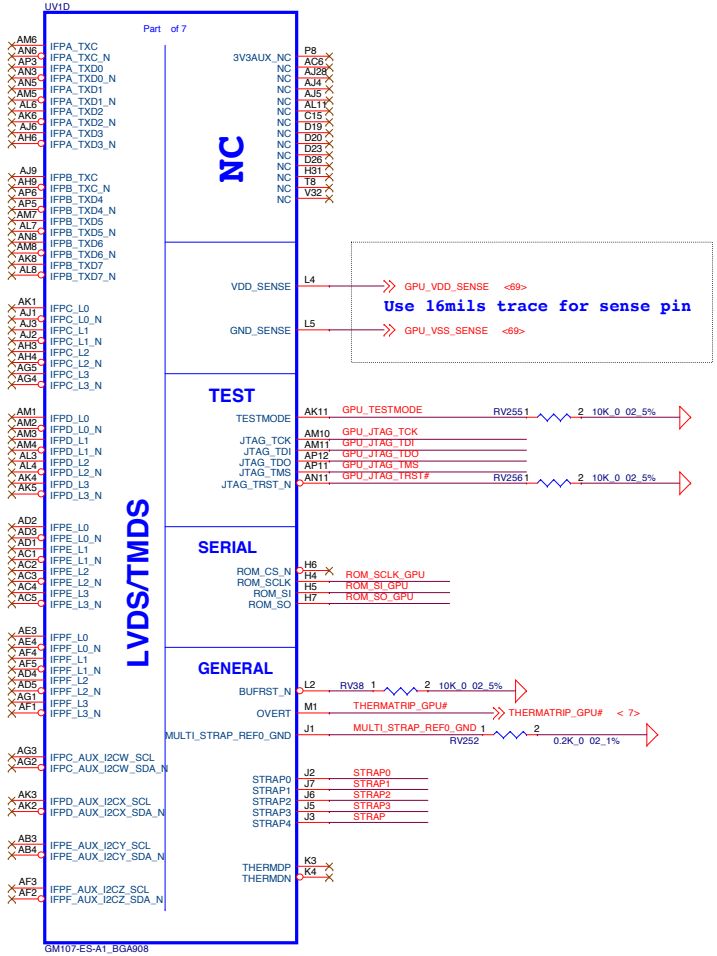
Resistance Mapping to Hex Values

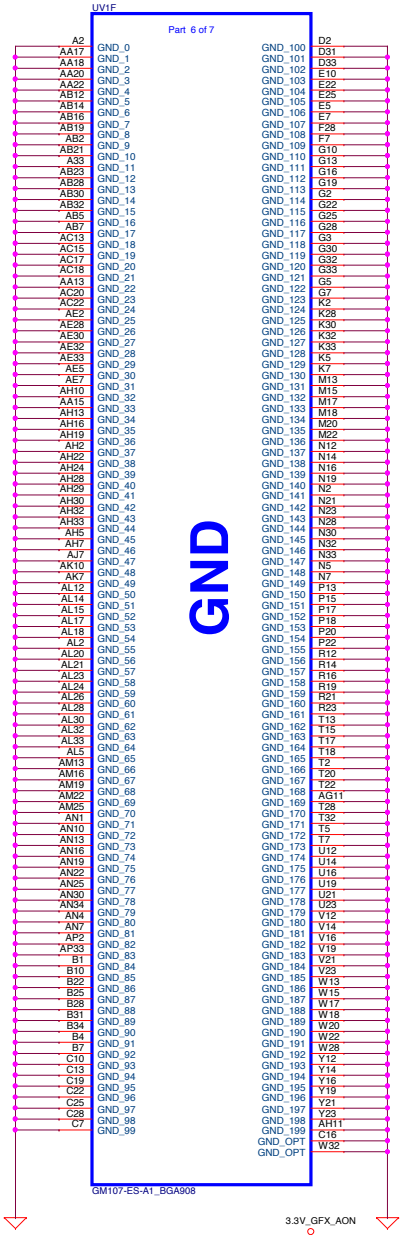
Resistor Value	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

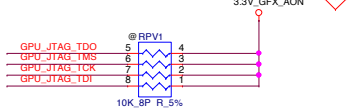
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
4 Gb	128Mx32	1.35V	Samsung	K4G41325FE-HC28	E-die	0x7	5 Gbps	N/A	Full	Production candidate
			Micron	EDW4032BABG-60-F	A-die	0x4	5 Gbps	N/A	Full	Production candidate

Decive ID change to 0x1056









For N17M-Q3 [2GB – GDDR5 4Gbit technology 4pcs x 32]

VENDER	STRAP	Part Number	Note(ROM_SI)
Samsung	0x7	K4G41325FE-HC28 SA00009TT0L	RV248 45.3k PD
Micron	0x4	EDW4032BABG-60-F SA00009E30L	RV248 24.9k PD

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0	Note
ROM_SCLK	SOR3_EXPOSED->0	SOR2_EXPOSED->0	SOR1_EXPOSED->0	SOR0_EXPOSED->0	ROM_SCLK pull-down RV246 4.99k to GND
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	ROM_SI pull-down RV248 24.9k to GND
ROM_SO	DEVID_SEL->0(default)	PCIE_CFG->0(defual)	SMB_ALT_ADDR->0(default)	VGA_DEVICE->0	ROM_SO pull-down RV250 4.99k to GND
STRAP0	Keep pull up to 3V3_AON and pull-down to GND footprint and stuff 50k ohm pull up				STRAP0 pull up RV235 50k to 3.3V_GFX_AON
STRAP1 STRAP2 STRAP3 STRAP4	Reserve				

DEVID_SEL/PCIE_CFG defaul set 0 need refer Platform Update Notification for the latest configuration

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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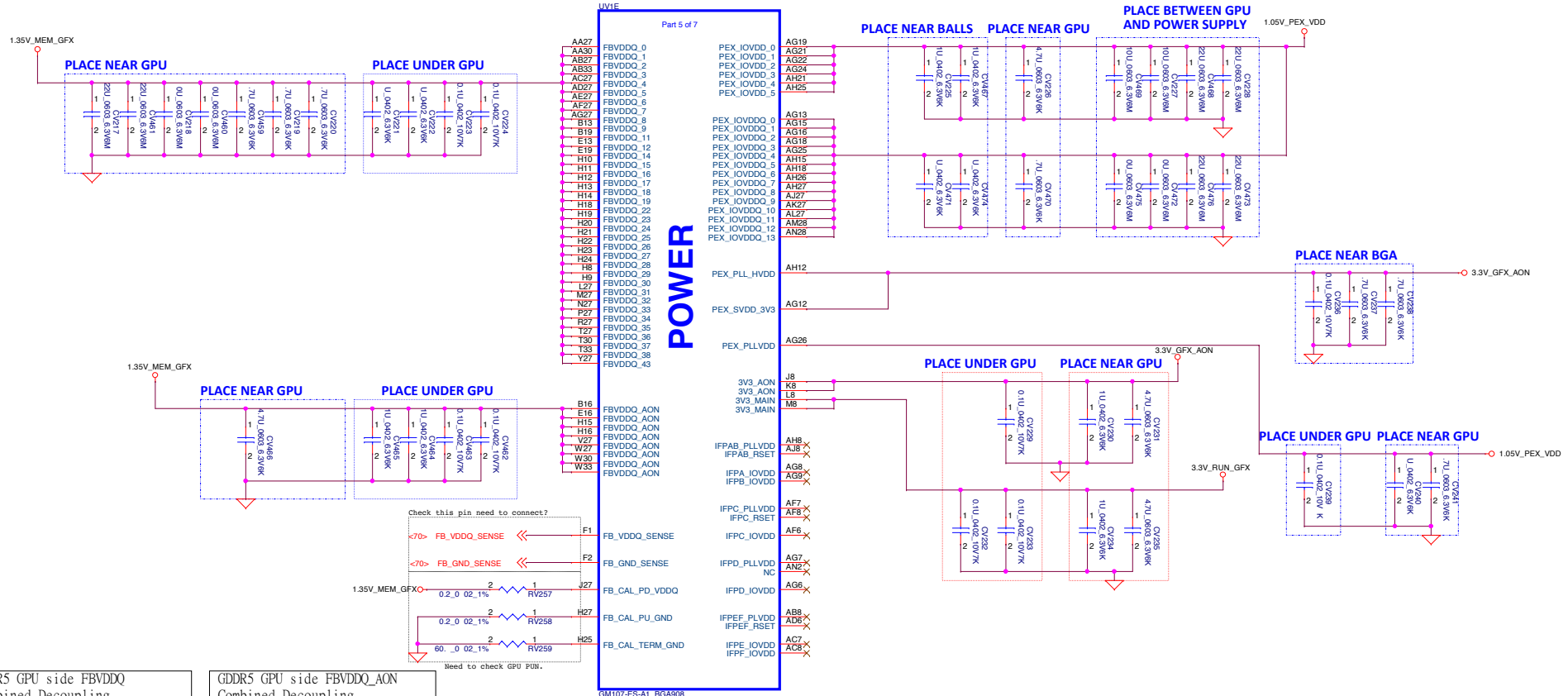
Compal Electronics, Inc.

Title: N17M DP, STRAP, GND

Size	Document Number	Rev
B	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet 8 of 7



GDDR5 GPU side FBVDDQ Combined Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	3
10uF 0805	2
22uF 0805	2

GDDR5 GPU side FBVDDQ_AON Combined Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1.0uF 0603	2
4.7uF 0603	1

Power Supply Rail		N17M-Q3
	(V)	(A)
GPU_Core	-	26
GPU_FBIO	1.5/1.35	TBD
PEX_IOVDD/Q	1.05	TBD
PEX_PLLVDD	1.05	TBD
FBA_PLL_AVDD	1.05	TBD
FBA_DLL_AVDD	1.05	TBD
PLL_VDD	1.05	TBD
SP_PLLVDD	1.05	TBD
1.05V Total	1.05	TBD
VDD33+3V3AON	3.3	TBD
PEX_SVDD_3V3	3.3	TBD
PEX_PLL_HVDD	3.3	TBD
3.3V Total	3.3	TBD

PEX_PLLVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0805	1

PEX_SVDD/PEX_PLL_HVDD Decoupling	
Capacitor Type	Population
0.1uF 0402	1
4.7uF 0603	2

3V3_MAIN Decoupling	
Capacitor Type	Population
0.1uF 0402	2
1uF 0603	1
4.7uF 0603	1

3V3_AON Decoupling	
Capacitor Type	Population
0.1uF 0402	1
1uF 0603	1
4.7uF 0603	1

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: *N17M Power*

Size: B | Document Number: *LA-E153P* | Rev: 0.2

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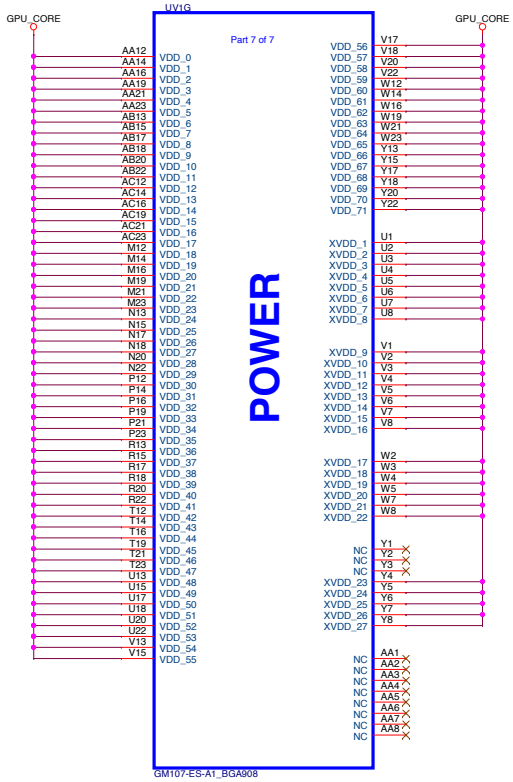
Caps on Power Side
1UX8 4.7UX15 under GPU
4.7UX5 22UX7 330UX1 near GPU



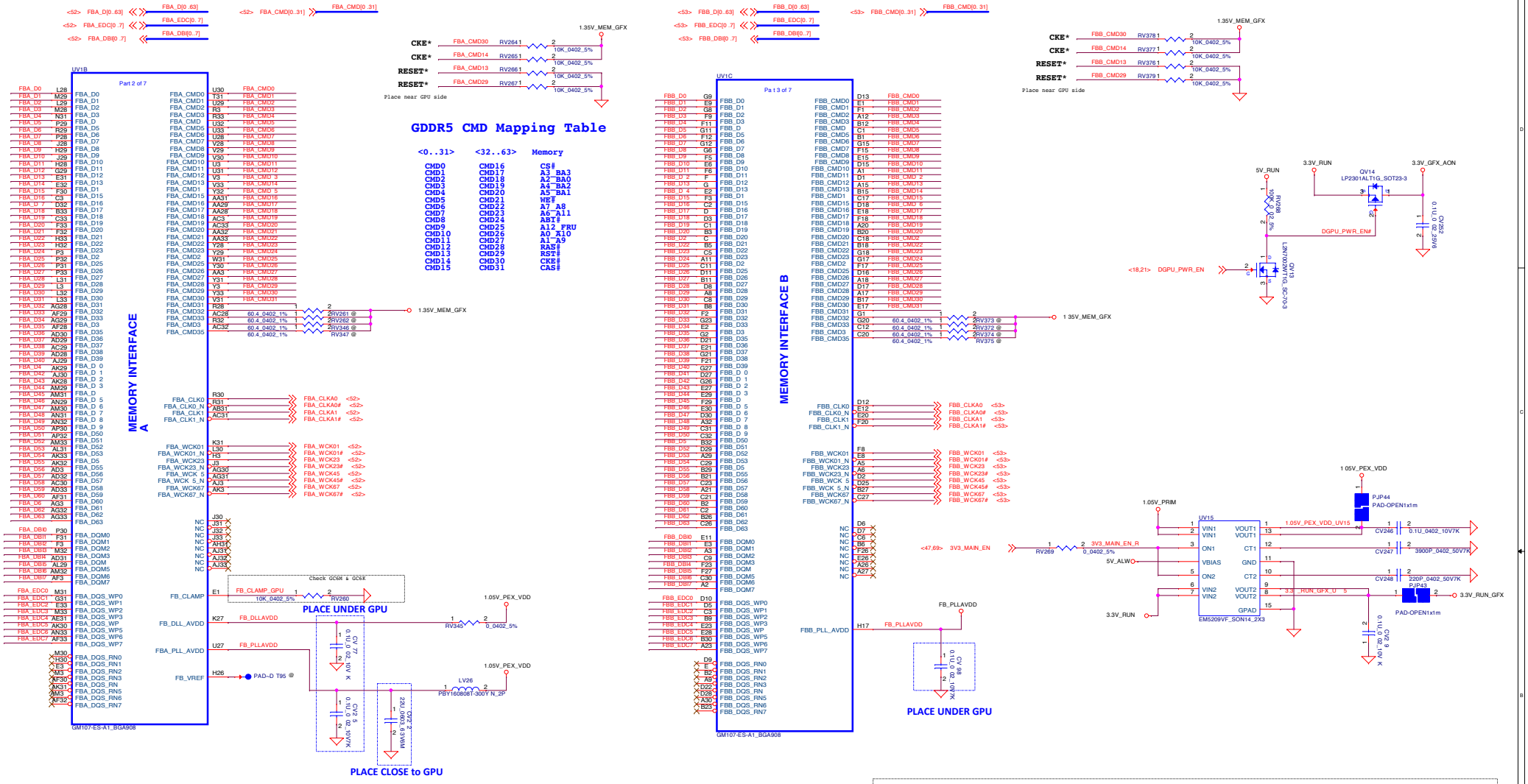
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: *N17M Power GFX Core*

Size	Document Number	Rev
B	*LA-E153P*	0.2

Date: Tuesday, June 28, 2016 | Sheet 50 of 7



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title: N17M Memory			
Size: C	Document Number: LA-E153P		Rev: 0.2
Date: Tuesday, June 28, 2016		Sheet 51 of 74	

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD0	CMD16	CS#
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_FRU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

NORMAL

UV17

K4G41325FE-HC28_FBGA170-D

170-BALL SGRAM GDDR5

MIRROR

UV18

K4G41325FE-HC28_FBGA170-D

170-BALL SGRAM GDDR5

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc

Title: GDDR5 VRAM A

Size	Document Number	Rev
C	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet 52 of 74

GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD0	CMD16	CS#
CMD1	CMD17	A3_BA3
CMD2	CMD18	A2_BA0
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD5	CMD21	WE#
CMD6	CMD22	A7_A8
CMD7	CMD23	A6_A11
CMD8	CMD24	ABI#
CMD9	CMD25	A12_FRU
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD12	CMD28	RAS#
CMD13	CMD29	RST#
CMD14	CMD30	CKE#
CMD15	CMD31	CAS#

NORMAL

MIRROR

BYTE0 BYTE1 BYTE2 BYTE3 BYTE4 BYTE5 BYTE6 BYTE7

UV19 K4G41325FE-HC28_FBGA170-D

UV20 K4G41325FE-HC28_FBGA170-D

170-BALL SGRAM GDDR5

1.35V_MEM_GFX

FBA_VREFD_H FBA_VREFC_H FBVREF_ALTV

QV9 2N7002KW_SOT323-3

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc

Title: GDDR5 VRAM B

Size: C | Document Number: LA-E153P | Rev: 0.2

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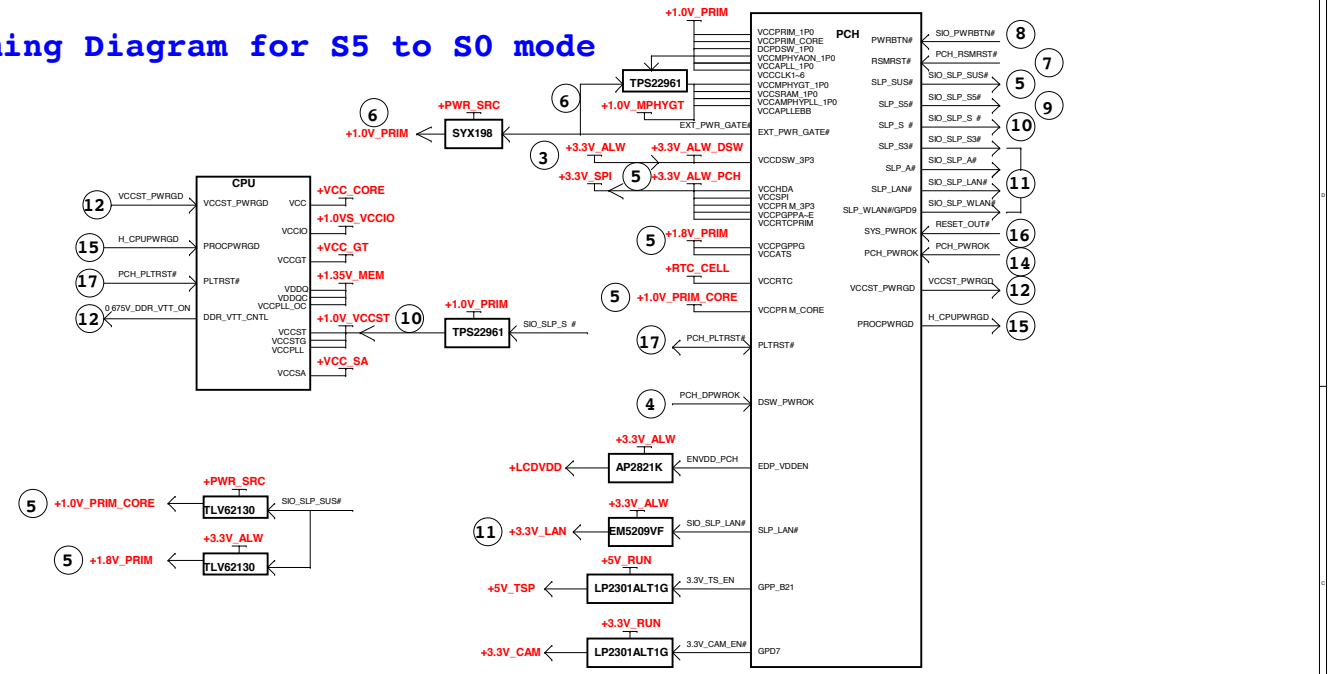
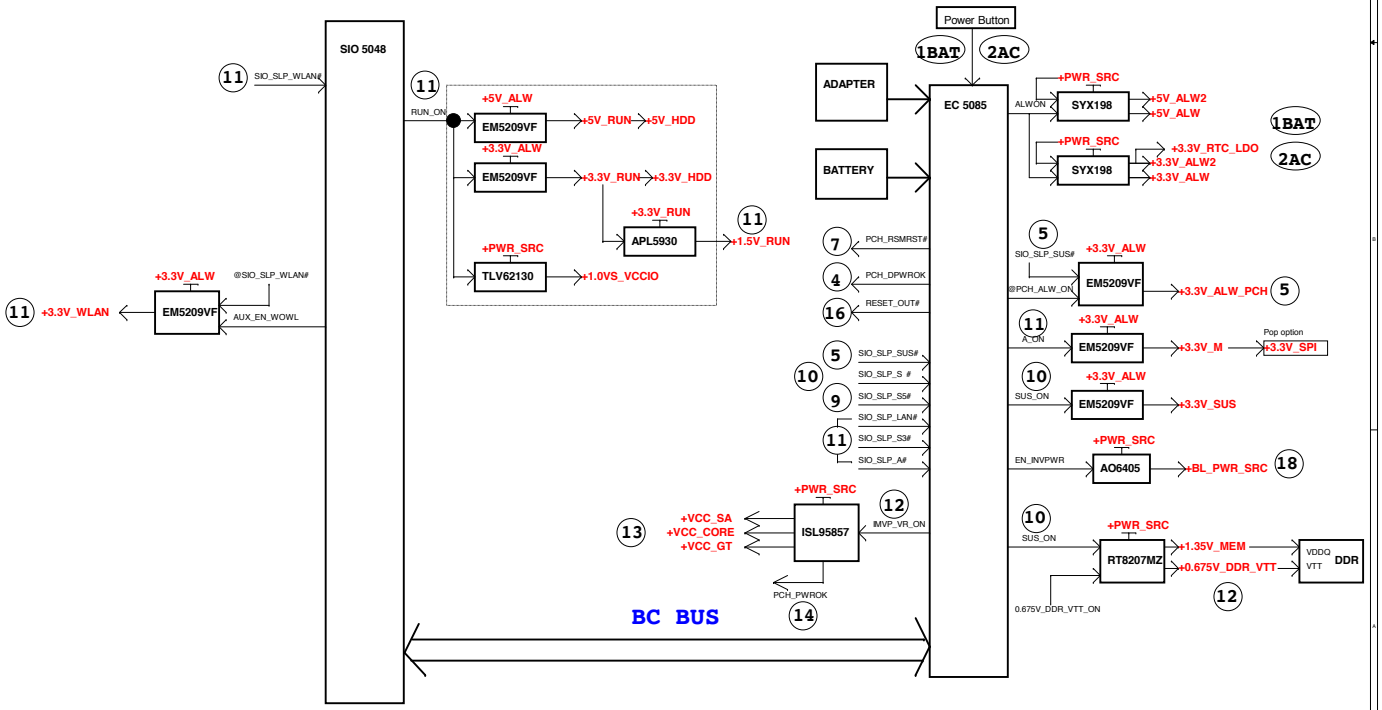
Timing Diagram for S5 to S0 mode





Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Compal Electronics, Inc

Title: Power Sequence

Size: Document Number: LA-E153P Rev: 0.2

Date: Sheet 54 of 74

For power common schemati

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: **Power common schematic**

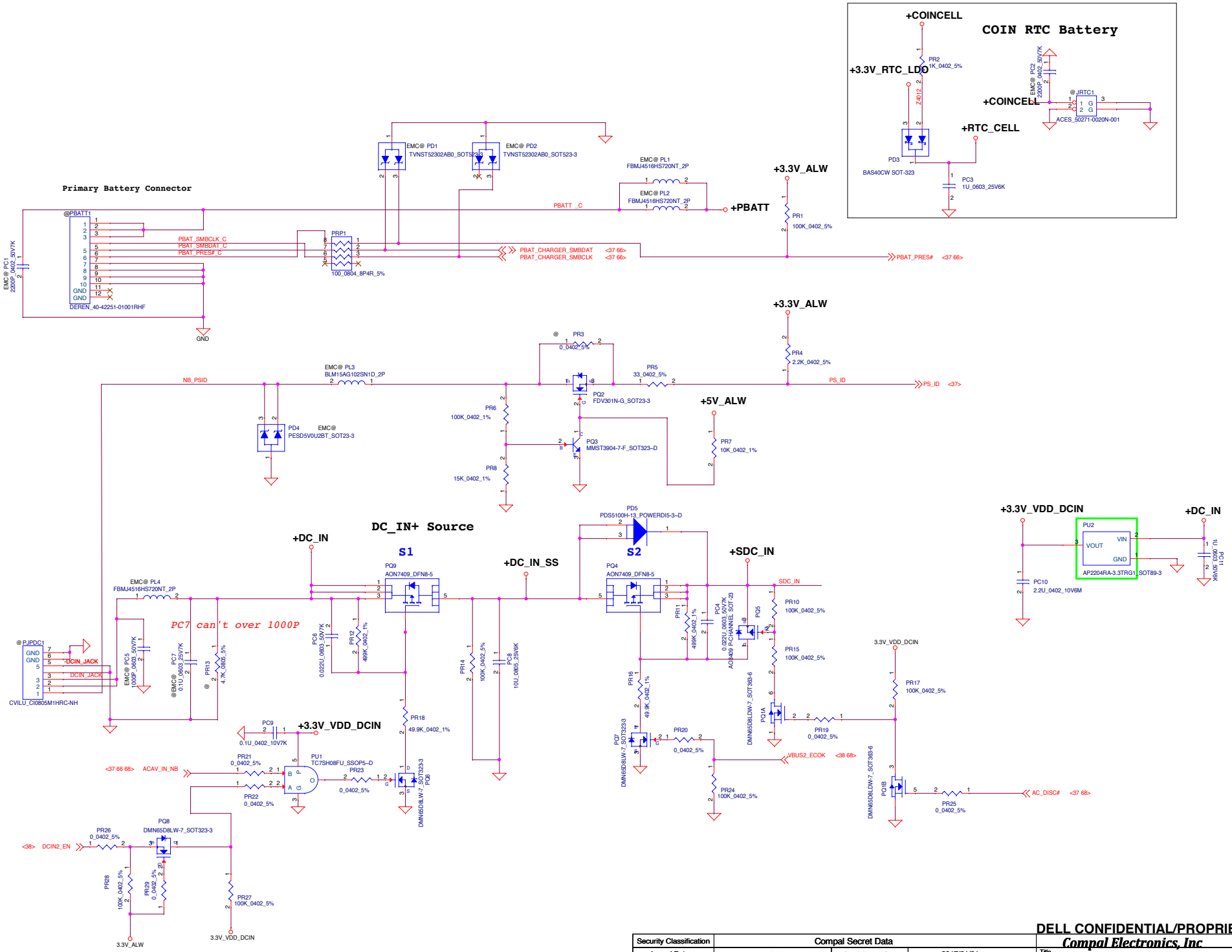
Size	Document Number	Rev
A	LA-E153P	0.2

Date: Tuesday, June 28, 2016 | Sheet 55 of 74

For power common schemati

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.		
Title: Power common schematic		
Size: A	Document Number: LA-E153P	Rev: 0.2
Date: Tuesday, June 28, 2016	Sheet 56 of 74	



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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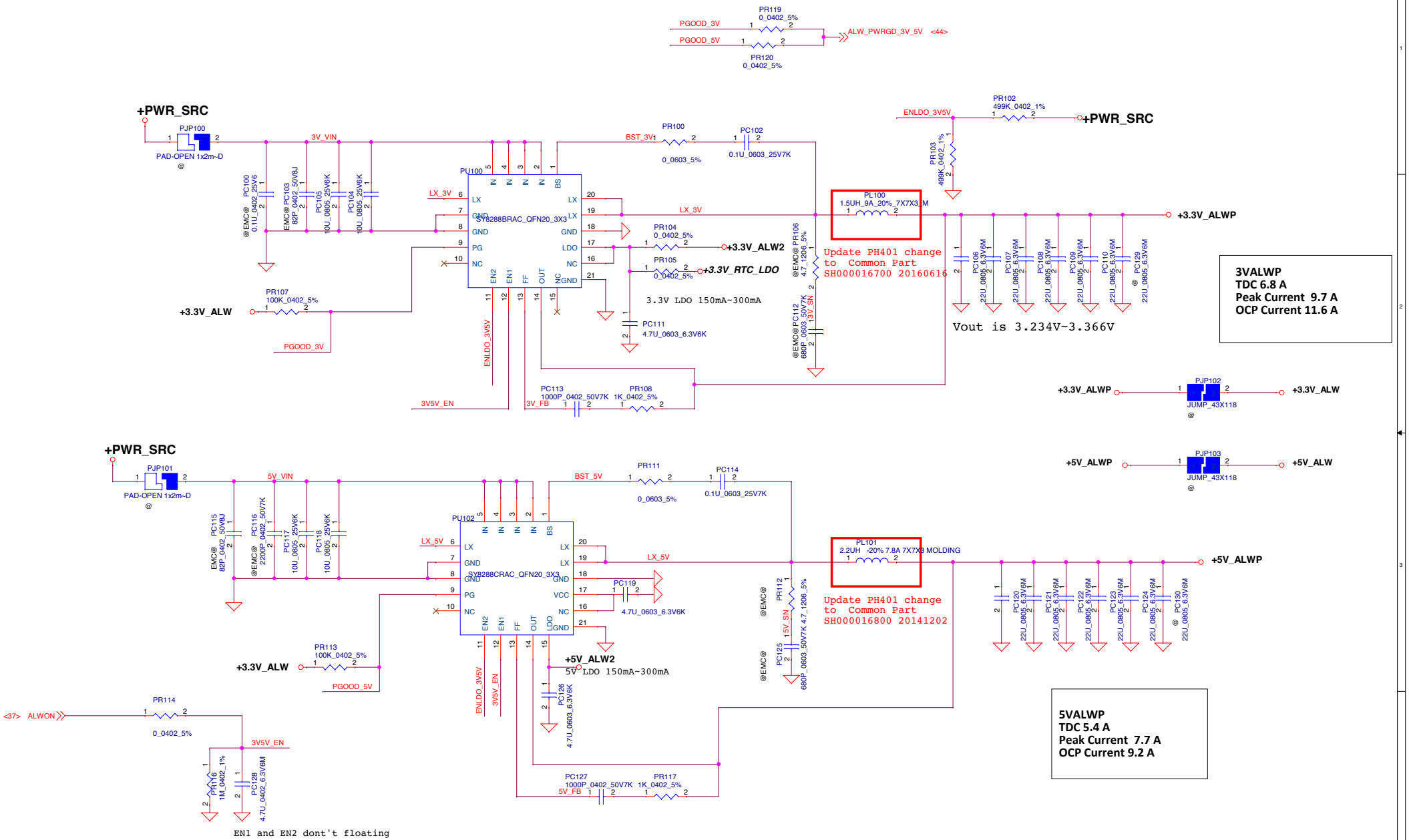
Compal Electronics, Inc

Title	+DCIN		
Size C	Document Number LA-E153P		Rev 0.2
Date: Tuesday, June 28, 2016		Sheet 57 of 74	



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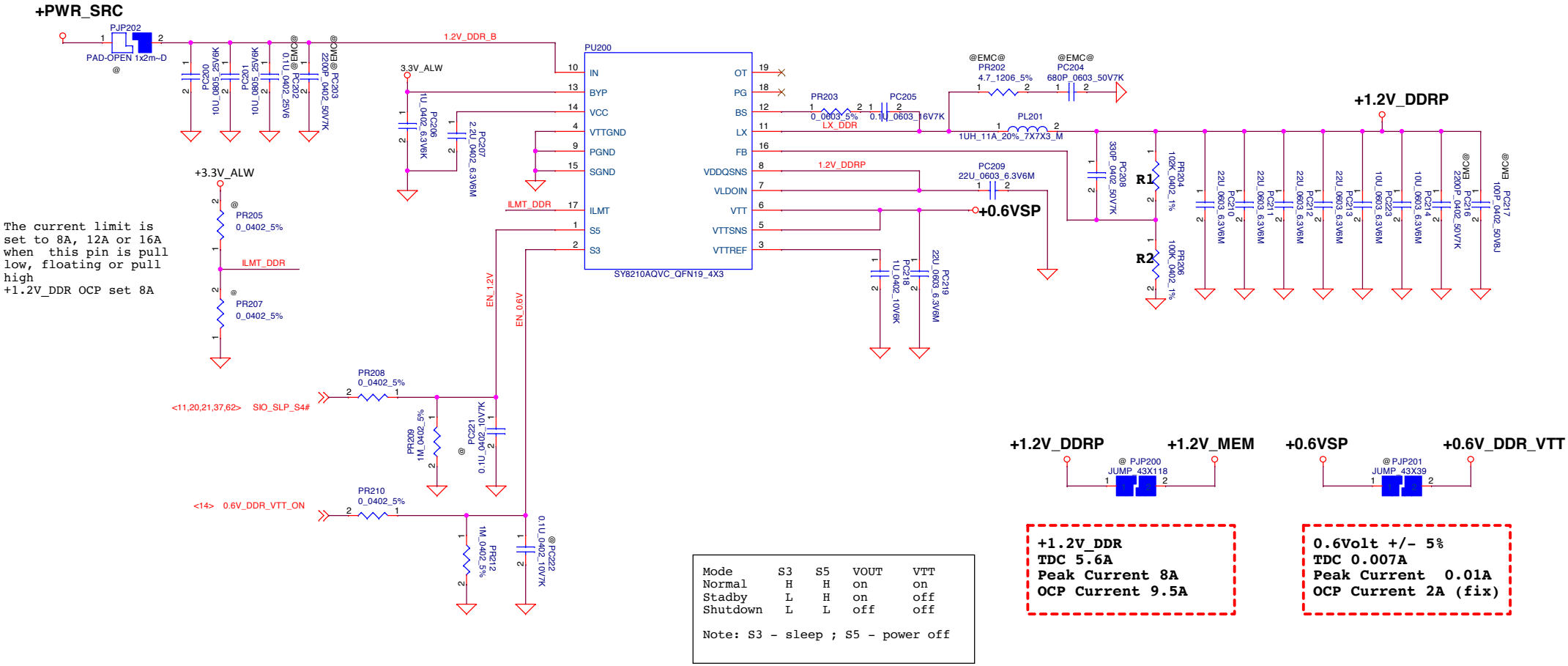
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

Size: Custom | Document Number: LA-E153P | Rev: 0.2

Date: Tuesday, June 28, 2016 | Sheet 58 of 74



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 8A

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 5.6A
Peak Current 8A
OCP Current 9.5A

0.6Volt +/- 5%
TDC 0.007A
Peak Current 0.01A
OCP Current 2A (fix)

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: +1.2V_MEN/+0.6V_DDR_VTT

Size	Document Number	Rev
Custom	LA-E153P	0.2

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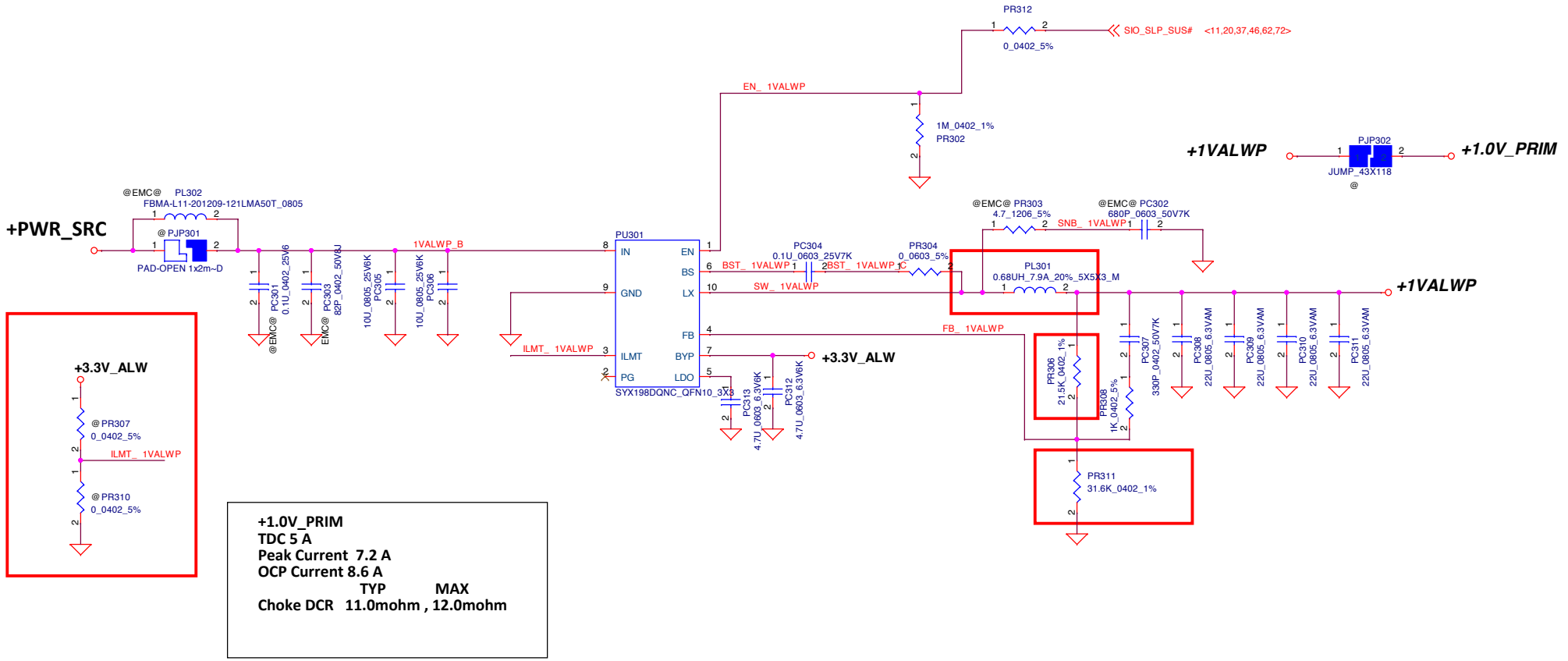


+1.0V_PRIM
TDC 5 A
Peak Current 7.2 A
OCP Current 8.6 A

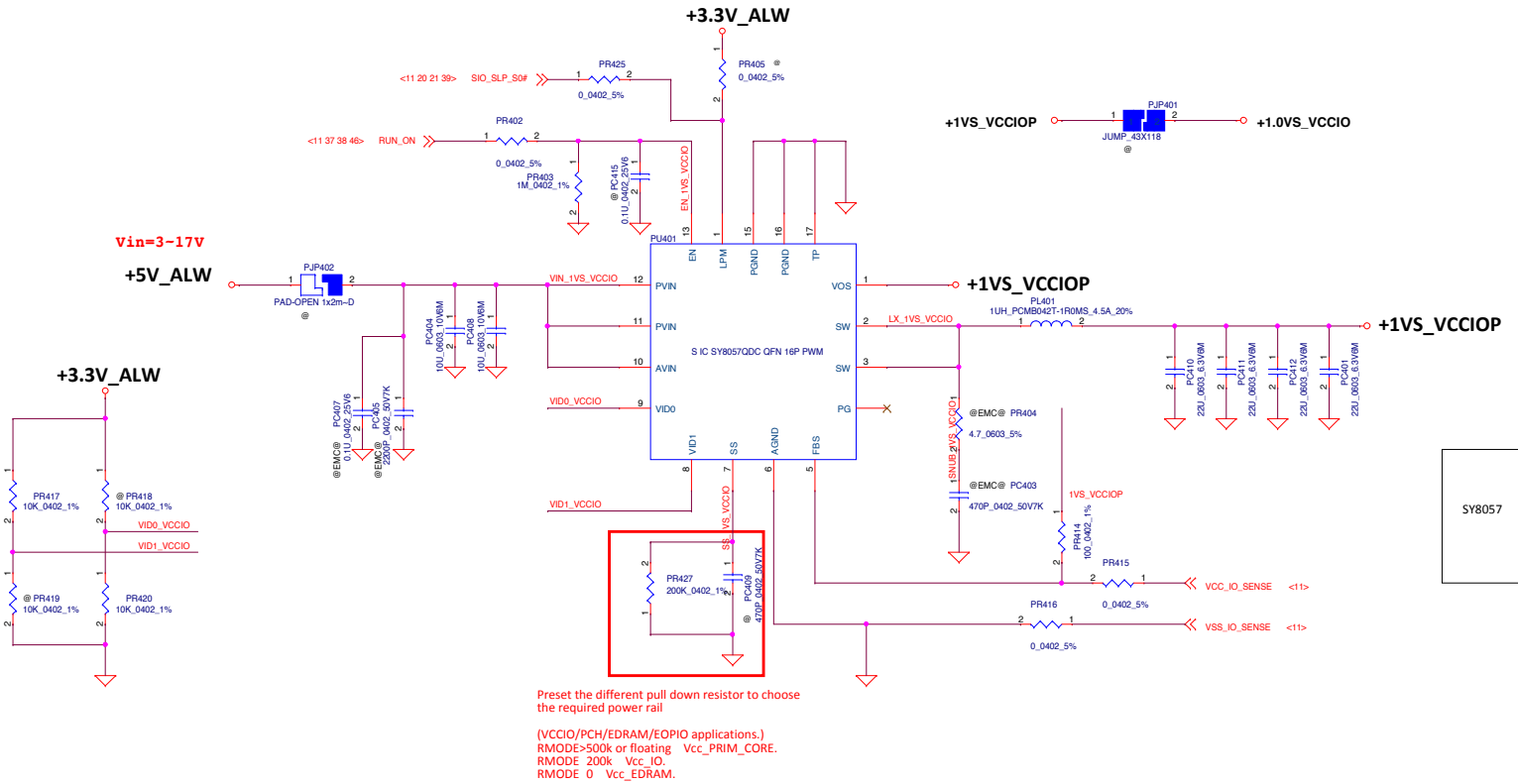
	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title	+1VALWP		
Size	Document Number		Rev
Custom	LA-E153P		0.2
Date	Tuesday, June 28, 2016	Sheet	60 of 74



Preset the different pull down resistor to choose the required power rail

(VCCIO/PCH/EDRAM/EOPIO applications.)
RMODE>500k or floating Vcc_PRIM_CORE.
RMODE 200k Vcc_IO.
RMODE 0 Vcc_EDRAM.

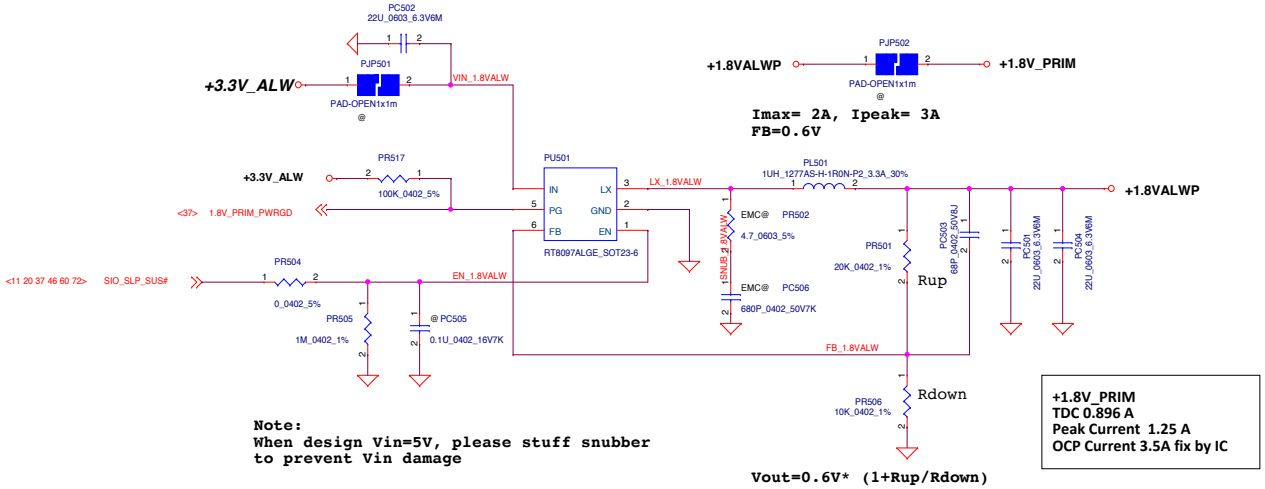
+1.0VS_VCCIO
TDC 3.9A
Peak Current 5.5 A
OCP Current 6.6 A Fix by IC

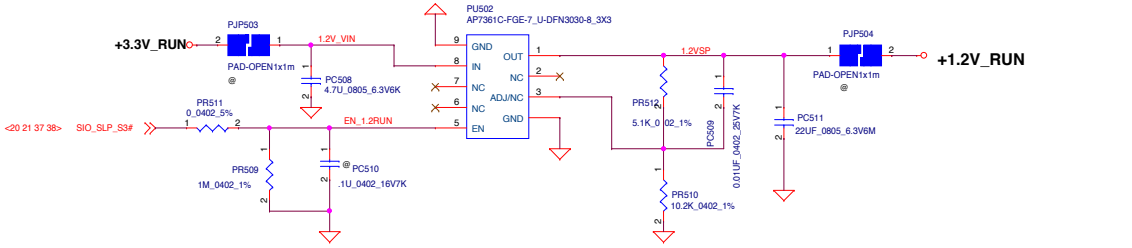
	TYP	MAX

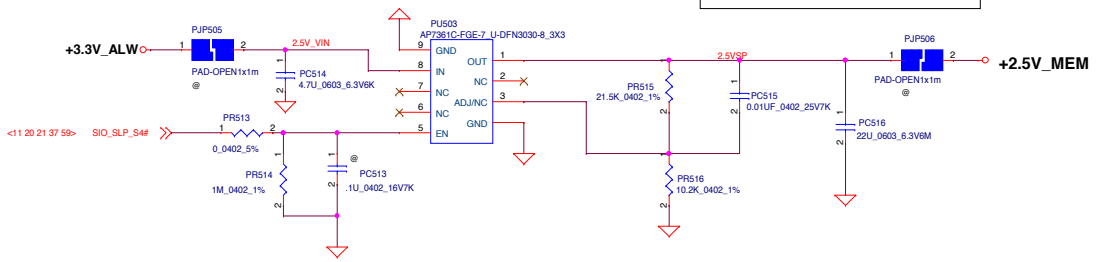
	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
SY8057	0	X	X	0(LPM)
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc
Title: +1VS_VCCIO
Size: C | Document Number: LA-E153P | Rev: 0.2
Date: Tuesday, June 28, 2016 | Sheet 61 of 74







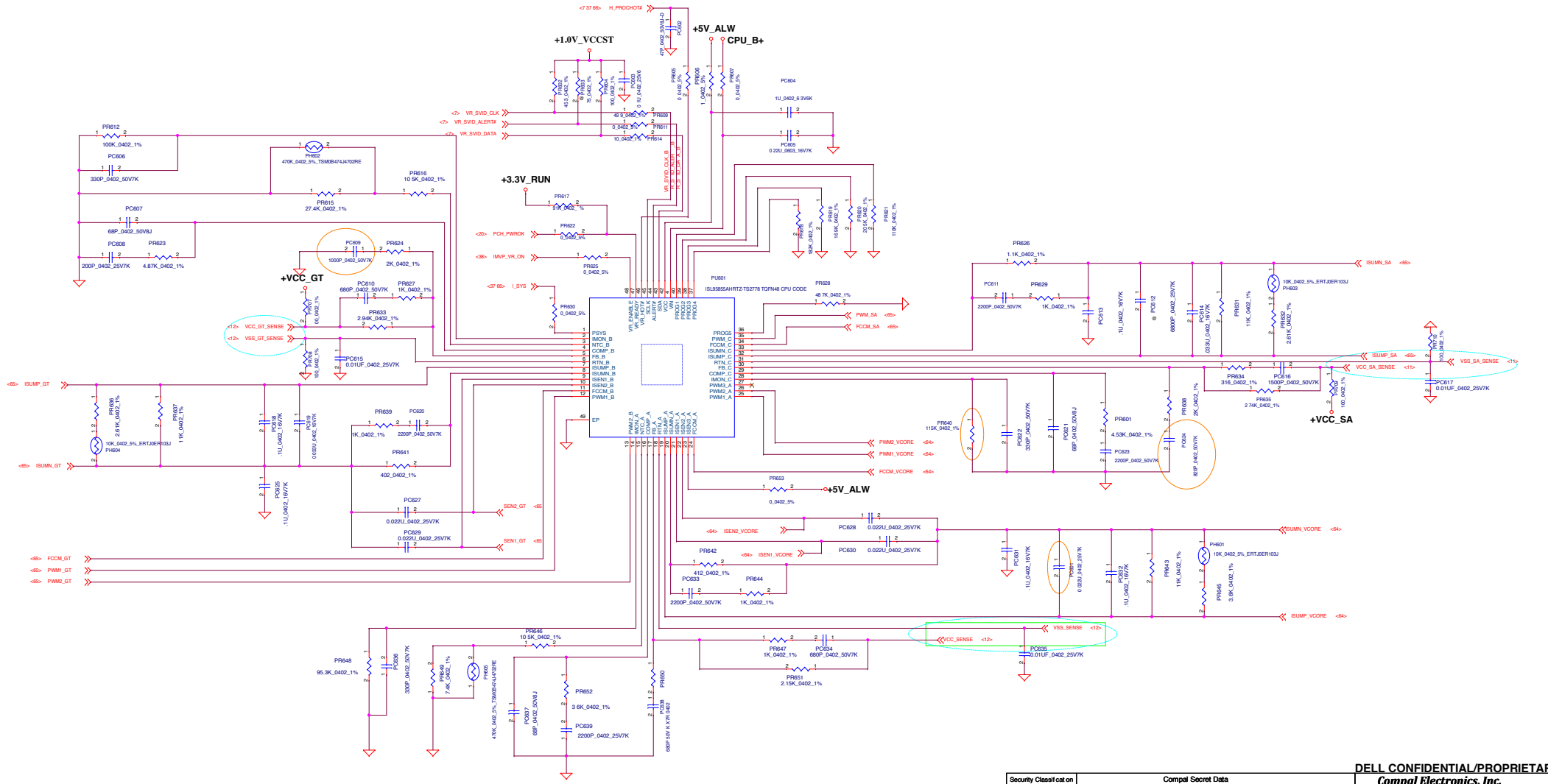
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc

Title: +1.8VALWP/+1.5VSP/2.5V_MEN

Size	Document Number	Rev
C	LA-E153P	0.2

Date: Tuesday, June 28, 2016 Sheet 62 of 74



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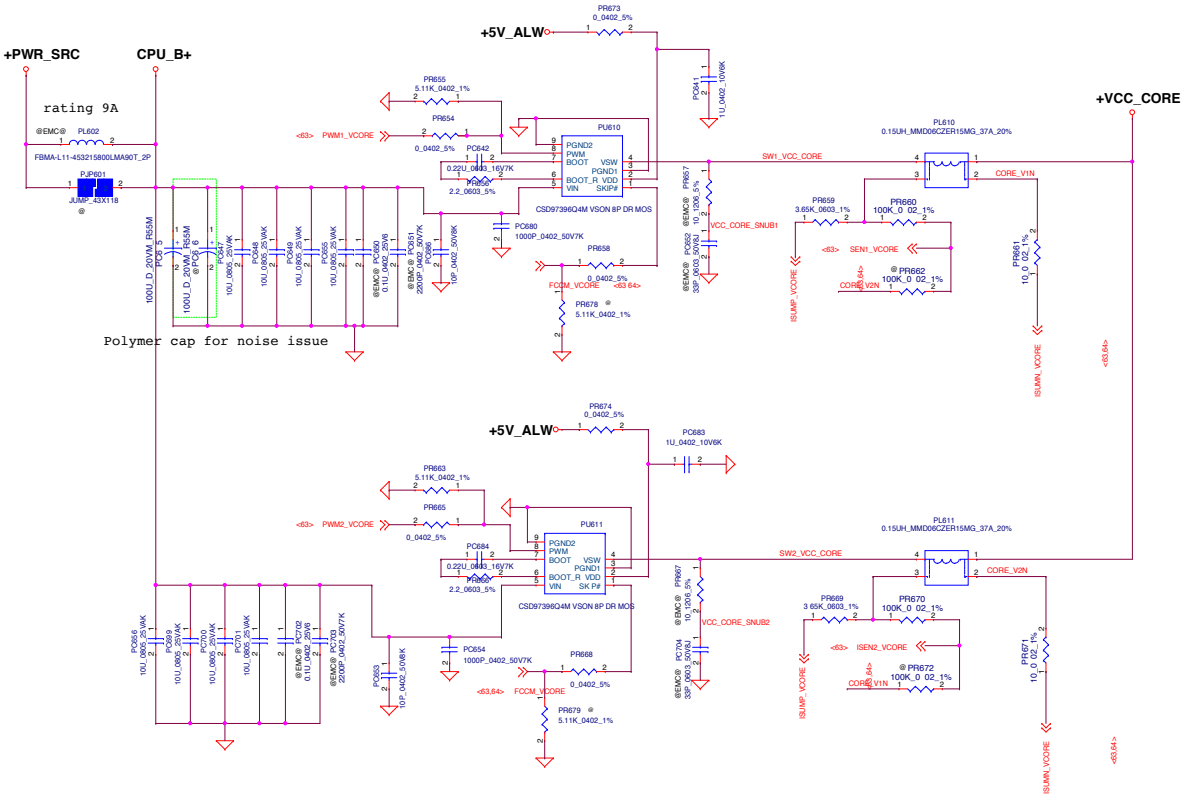
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title	VCORE_ISL95855		
Size	Document Number		Rev
Custom	LA-E153P		0.2
Date	Tuesday, June 28, 2016	Sheet	63 of 74

VCC_core
TDC 50A
Peak Current 68A
OCP current 81.6A
Choke DCR 0.9 +-7%m ohm



Security Classification	Compal Secret Data		
Issued Date	2016/01 01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: VCORE

Size: Custom | Document Number: LA-E153P | Rev: 0.2

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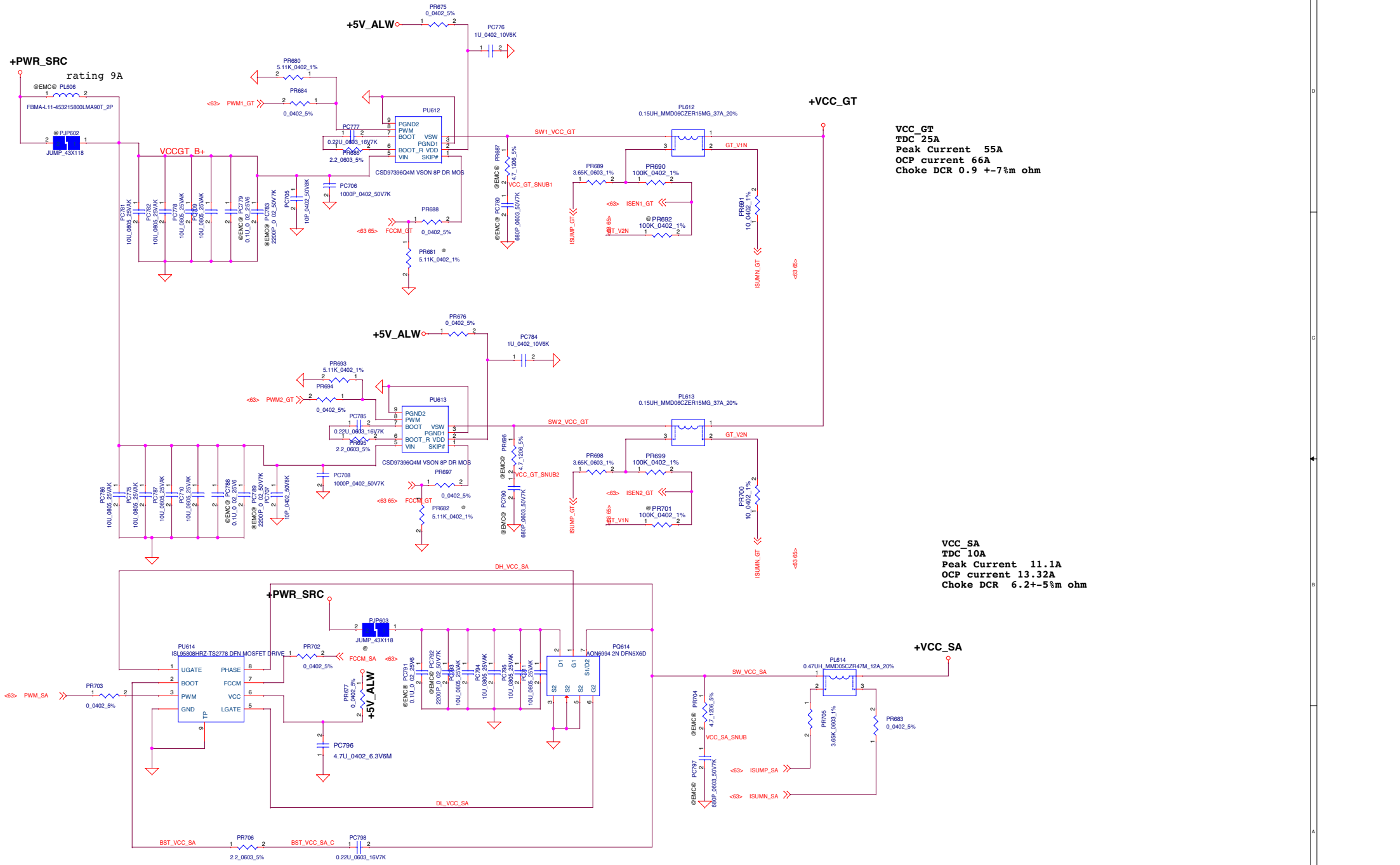

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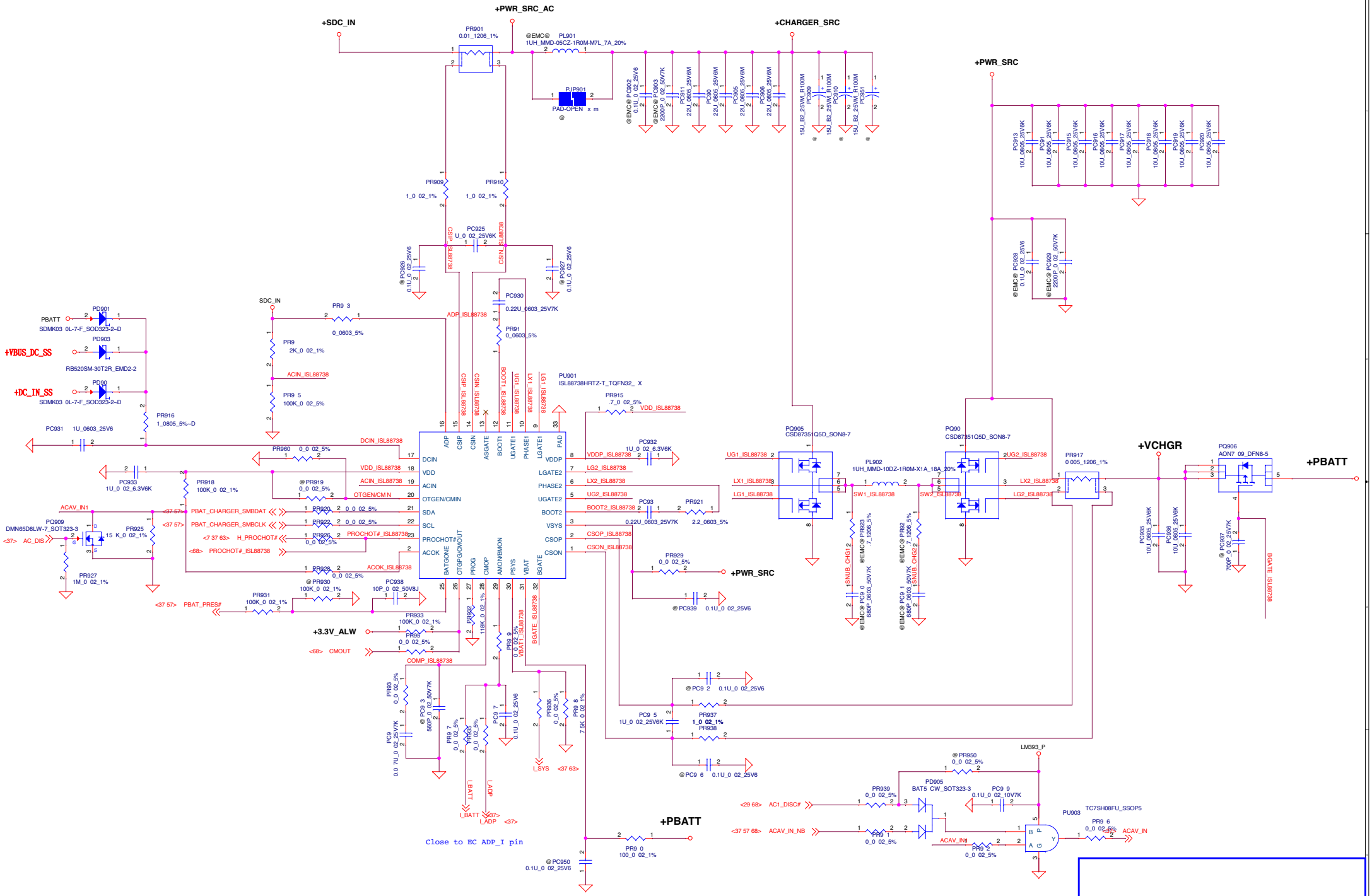
Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc

Title	VGT_VSA		
Size C	Document Number LA-E153P		Rev 0.2
Date: Tuesday, June 28, 2016	Sheet 65 of 74		



Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Decphered Date	2017/01/01

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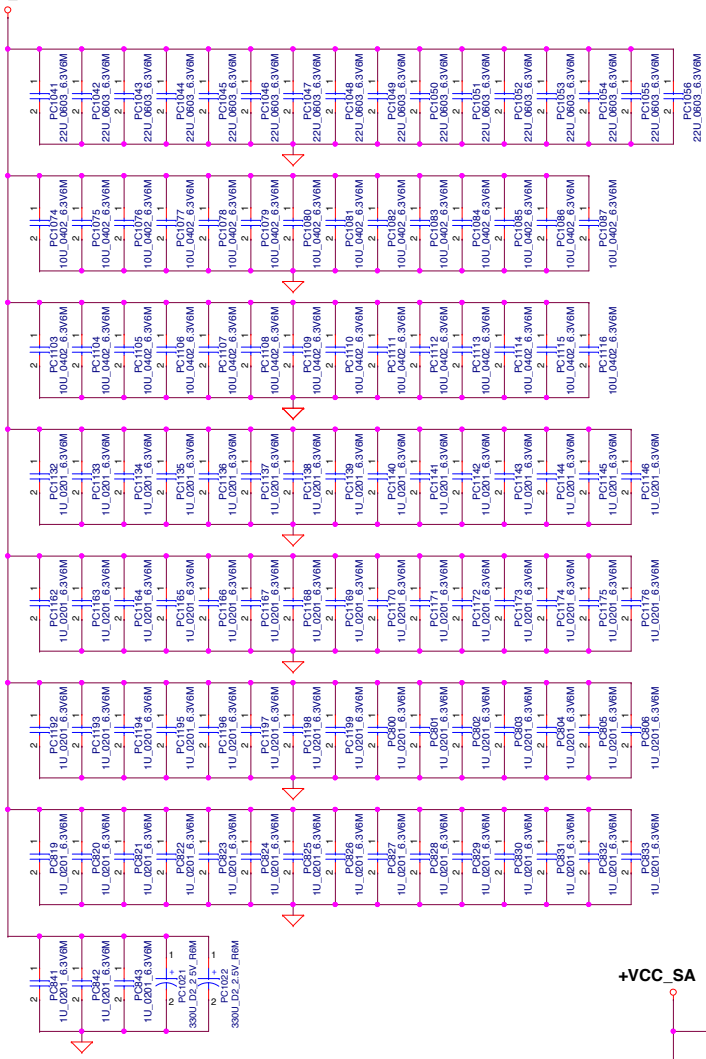
Compal Electronics, Inc.

Title: PWR_CHARGER_ISL9237 (Colay)

Size	Document Number	Rev
Custom	LA-E153P	0.2
Date: Tuesday, June 28, 2016	Sheet 66 of 7	

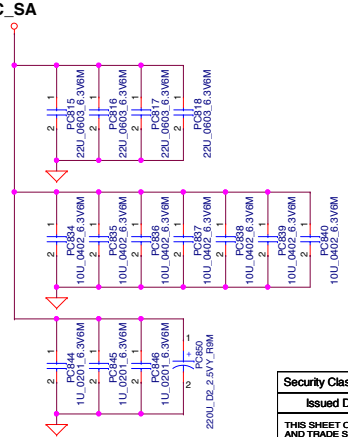
VCC_CORE Place on CPU
Back Side.
22U_0603 * 8 pcs + 10U_0402*28 pcs + 1U_0201*35 pcs
Primary Side.
22U_0603 * 8 pcs+330u_D2*2 pcs

+VCC_CORE



VCC_SA Place on CPU
Back Side.
22U_0603 * 2 pcs + 10U_0402*7 pcs + 1U_0201*3 pcs
Primary Side.
22U_0603 * 2 pcs + 220u_D2*1 pcs

+VCC_SA



VCC_GT Place on CPU
Back Side.
22U_0603 * 8 pcs +10U_0402*35 pcs +1U_0201*68 pcs
Primary Side.
22U_0603 * 12 pcs +470u_D2*2 pcs

+VCC_GT

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

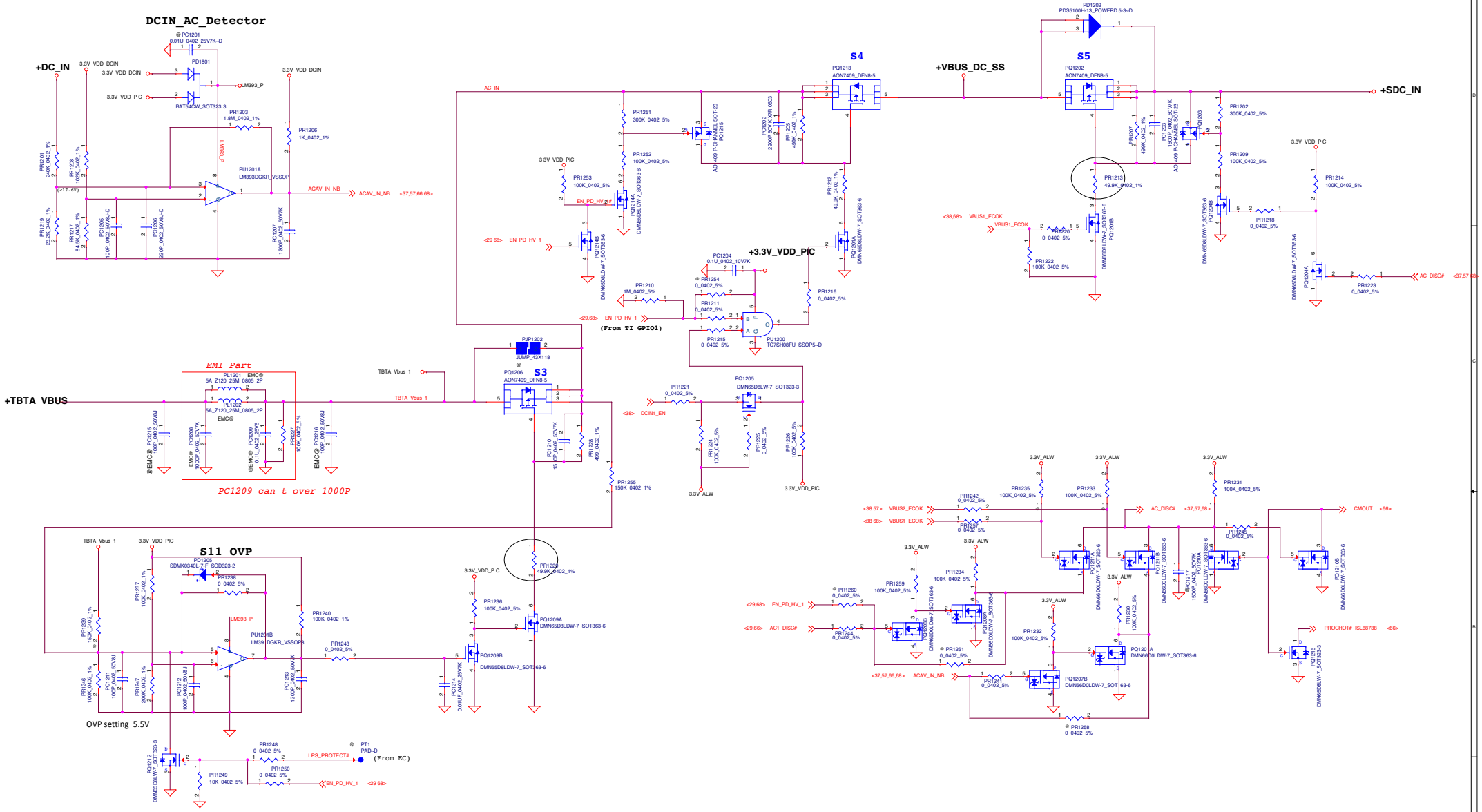
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

Size	Document Number	Rev
Custom	LA-E153P	0.2

Date: Tuesday, June 28, 2016 | Sheet 67 of 7



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Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title	ParkCity_TypeC_PD		
Size	Document Number		Rev
Custom	LA-E153P		0.2
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Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR9	39K	20K	39K
Rref1	PR5	39K	20K	30K
Rboot	PR8	1.5K	2K	3K
Rref2=PR10+PR12	PR10	30K	18K	24K
	PR12	1.5K	0	3K
C	PC8	1.5nf	2.7nf	1.8nf

Module model information:
RT8813A_V1A for IC module
RT8813A_V1B for SW module

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

OCP=54A/2=27A per phase
Ivalley=27A-7.811A/2=23.1A

H-side MOS:TPCA8065
Rds(on):
11.7mohm@Vgs=10V
9.4mohm@Vgs=4.5V
Id :16A@Ta=25 degC

L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

Choke: 0.36uH (Size:10*10*4)
Rdc=1.1mohm +-5%
Heat Rating Current=30A
Saturation Current=50A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

Operation phase Number with DEM	PSI Voltage setting
1 phase with CCM	0.8V to 1.2V
Active phase with CCM	1.8V to 5.5V

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14P-GV2	N14M-GS	N14M-LP	N14P-LP	N14P-GE	N14P-GS	N14P-GT
OpenVReg Configurations	Config B	Config B	Config B	Config B	Config B	Config B	Config B	Config B
Rated TDP	18W	25W	18W	13W	18.9W	25W	25.6W	35.5W
Power at Tj=102C								
Boosted GPU Total at Tj 102C	25W	32W	25W	20W	23W	N/A	30W	40W
EDP-Continuous at Tj=102C	24A	32A	26A	22A	25A	27A	38A	45A
EDP-Peak at Tj 102C	35A	55A	45A	35A	35A	40A	60A	75A
Istep max (Evaluation)	15A	27A	25A	20A	14A	12A	31.5A	35A
OCP Setting Current	42A	66A	54A	42A	42A	48A	72A	90A
Rocset	8.96K	12.45K	10.7K	8.96K	8.96K	9.83K	8.3K	9.39K
Recommendation	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H1L	2phase 1H2L	2phase 1H2L
Polymer Cap (330uF)	6mohm * 2	9mohm * 3	9mohm * 3	6mohm * 2	6mohm * 2	6mohm * 2	6mohm * 3 (L=0.22uH)	4.5mohm * 3 (L=0.15uH)
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	10mohm * 3	NULL	NULL

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

PSI Pull high on HW side

Pull high on HW side

Reserve Location

Place close HW side RH373

1. VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms (PC616 pop)

2. Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=304.89Khz

3. Thermal monitoring:
(VGPU_VREF-VTSNS)/PR620=VTSNS/Rth

	T_min	T_typica	T_max
PR620=18.	K96.73C	100C	103.1C
PR620=13K	106.38C	110C	113.4C

+VGA_CORE(N16S-GT1-KA)
TDC 26.5 A
Peak 53 A
OCP 63.6 A

SH00000OY00 Main
SH00000UF00 2nd

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Title: +GPU_CORE
Size: C | Document Number: LA-E153P | Rev: 0.2
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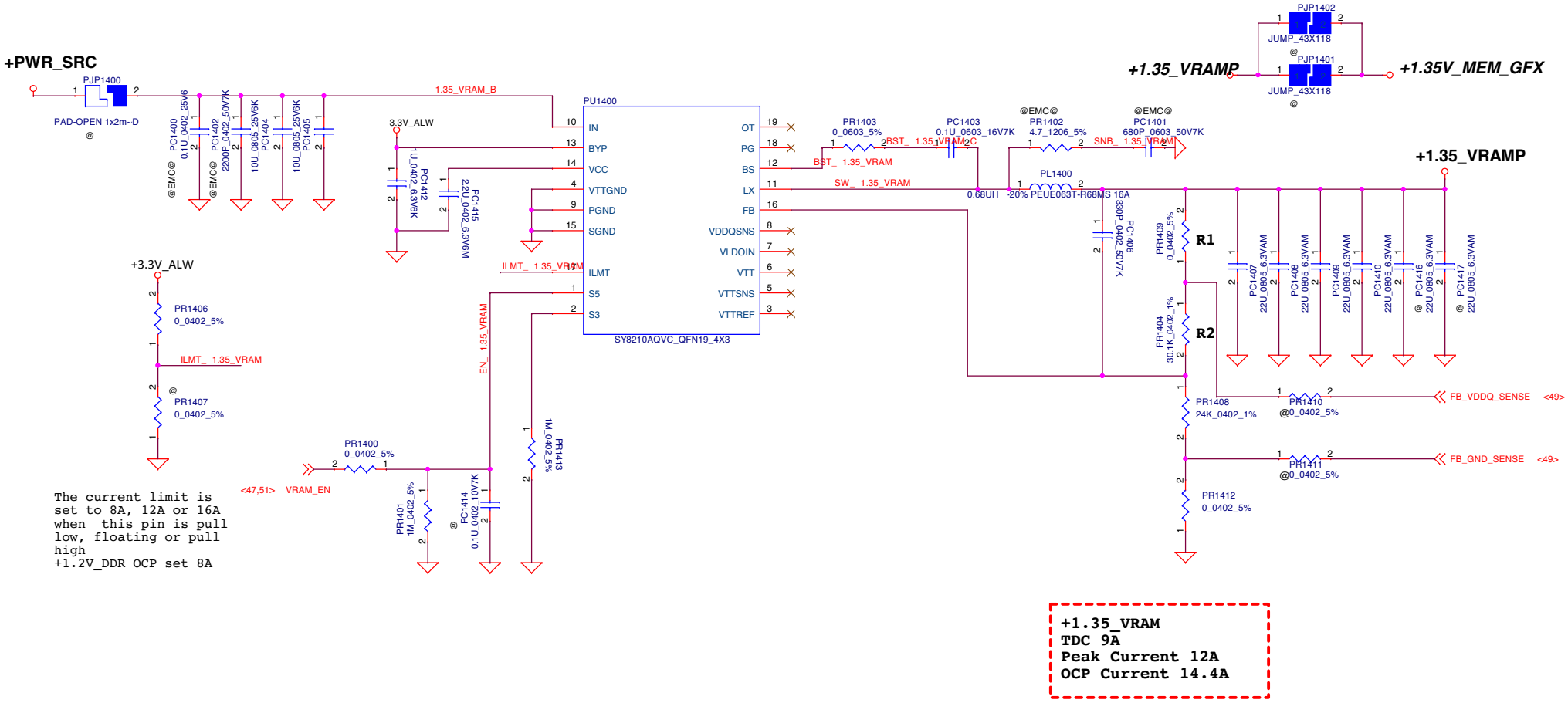

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Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	GPU_VRAM(SYX198D)		
Size	Document Number		Rev
Custom	LA-E153P		0.2
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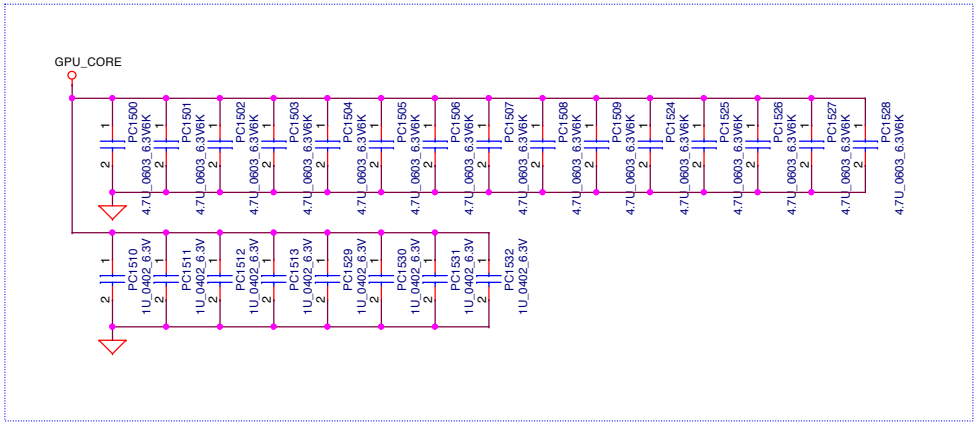
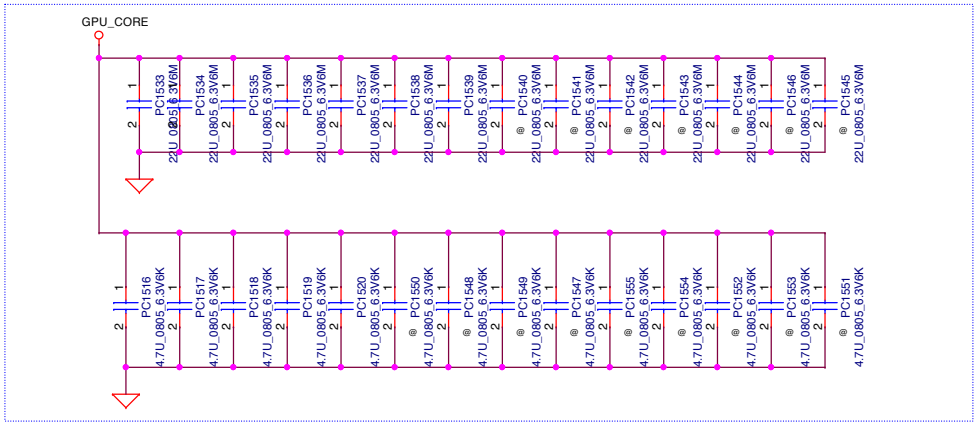


nVidia GB4B-128 package
Under GPU
4.7uF 0603 * 15
1uF 0402 * 8



nVidia GB4B-128 package
Near GPU
22uF 0805 *7
4.7uF 0805 *5

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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Title: PROCESSOR DECOUPLING

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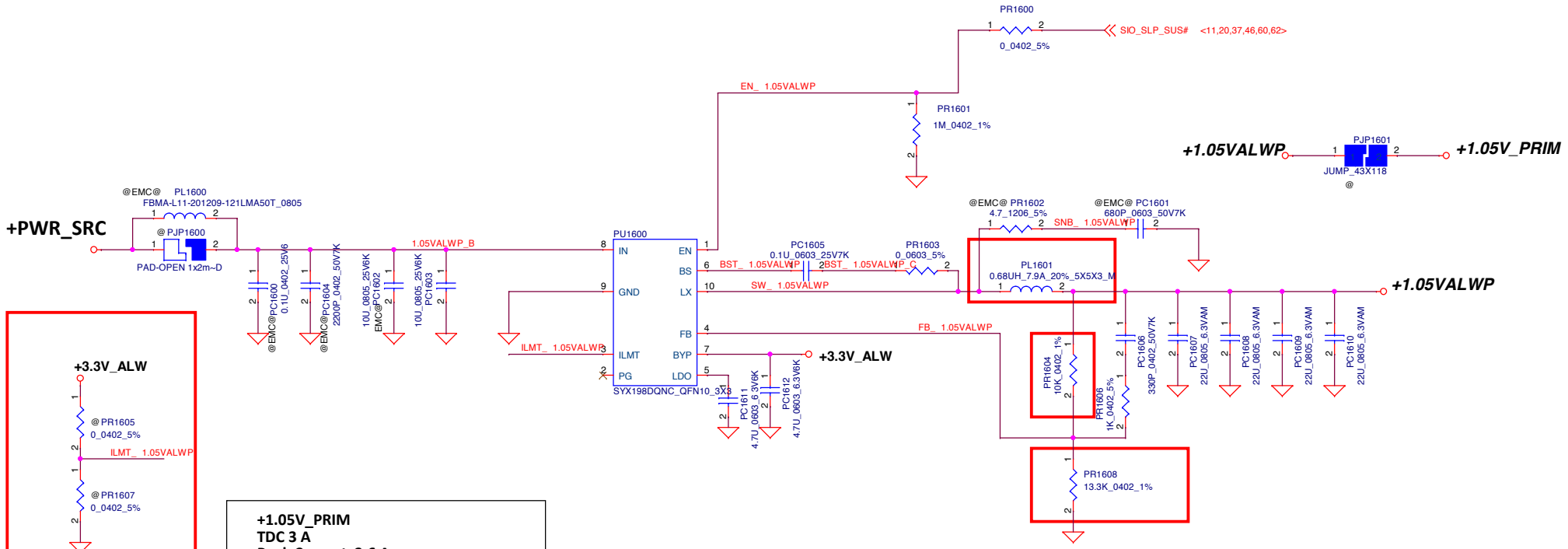

+1.05V_PRIM
TDC 3 A
Peak Current 3.6 A
OCP Current 4.32 A

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

Vo=0.6*(1+R1/R2)

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title	+1VALWP		
Size	Document Number		Rev
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Date	Tuesday, June 28, 2016	Sheet	72 of 74

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
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10							
11							
12							
13							
14							

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.			
Title	PWR P.I.R		
Size: Custom	Document Number: LA-E153P		Rev: 0.2
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	2016/5/27	COMPAL	S0ix(modern standy) support for VCCPLL_OC	Pop RZ120 and Depop UZ34 Add net name VCCSTG_EN(UZ19.4) and connect to RZ120.1	0.2(X01)
2	37	HW	2016/5/27	COMPAL	Reserve PORT80_DET# PD resistance	Reserve RE513 100k (SD028100380) to GND	0.2(X01)
3	35	HW	2016/6/1	COMPAL	Intel schematics reivew modify item	CZ28,CZ29 change from 0.047uF to 0.01uF CZ27 change from 0.1uF(@)_0201 to 10uF_0603	0.2(X01)
4	45	HW	2016/6/1	COMPAL	JLED1 pin define error	JLED1 pin definition change	0.2(X01)
5	39	HW	2016/6/1	COMPAL	TPM change to NUVOTON	Change TPM from Atmel to NUVOTON.	0.2(X01)
6	35	HW	2016/6/1	COMPAL	Intel reviwe result (WWAN Coex feature support)	Add RZ128 0 ohm connect WWAN_COEX3 and WLAN_COEX3 Add RZ129 0 ohm connect WWAN_COEX2 and WLAN_COEX2 Add RZ130 0 ohm connect WWAN_COEX1 and WLAN_COEX1	0.2(X01)
7	35	HW	2016/6/7	COMPAL	Debug card reserve	Add RZ131, RZ132 for PORT80_DET# and HOST_DEBUG_TX	0.2(X01)
8	37	HW	2016/6/7	COMPAL	For MEC5105K-D1-TN setting	1. Change UE1 to SA00009GL00 2. POP RE360,RE362 3. De-POP RE361	0.2(X01)
9	35,32	HW	2016/6/16	COMPAL	For EMC request	De-pop RZ131, RZ132. CL22 change to 10pf , POP CA7,CZ1 (100P),CH268 modify from 22p to 47p and POP,Change LV1 to SM01000NY00	0.2(X01)
10	41	HW	2016/6/16	COMPAL	BITS284924-HDD is still working after press power button into S5 during POST.	POP RN5	0.2(X01)
11	39	ME	2016/6/17	COMPAL	Connector change	1. JKBTP1 change to CVILU_CF5020FD0RK-05-NH 2. JUSH1 change to CVILU_CF5026FD0RK-05-NH 3. JIR1 change to ACES_50208-0060N-P01	0.2(X01)
12	36	HW	2016/6/20	COMPAL	Vender suggest	RA7,RA8 change to 16.2ohm	0.2(X01)
13	37	HW	2016/6/22	COMPAL	The posibility of GPIO map update	Add RE514,RE515 for RTCRST_ON	0.2(X01)
14	41	HW	2016/6/22	COMPAL	BITS283552 - [BR_CSLP] FFS AP no function when execute FF generator or shake SU	FFS VDD_IO change to +3.3V_RUN	0.2(X01)
15	28	HW	2016/6/22	COMPAL	TypeC USB Rx EQ change 1dB can PASS USB RSG test	depop RT144, pop RT304	0.2(X01)

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

Compal Electronics, Inc.

Title: EE P.I.R (1/6)

Size: Custom | Document Number: LA-E153P | Rev: 0.2

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