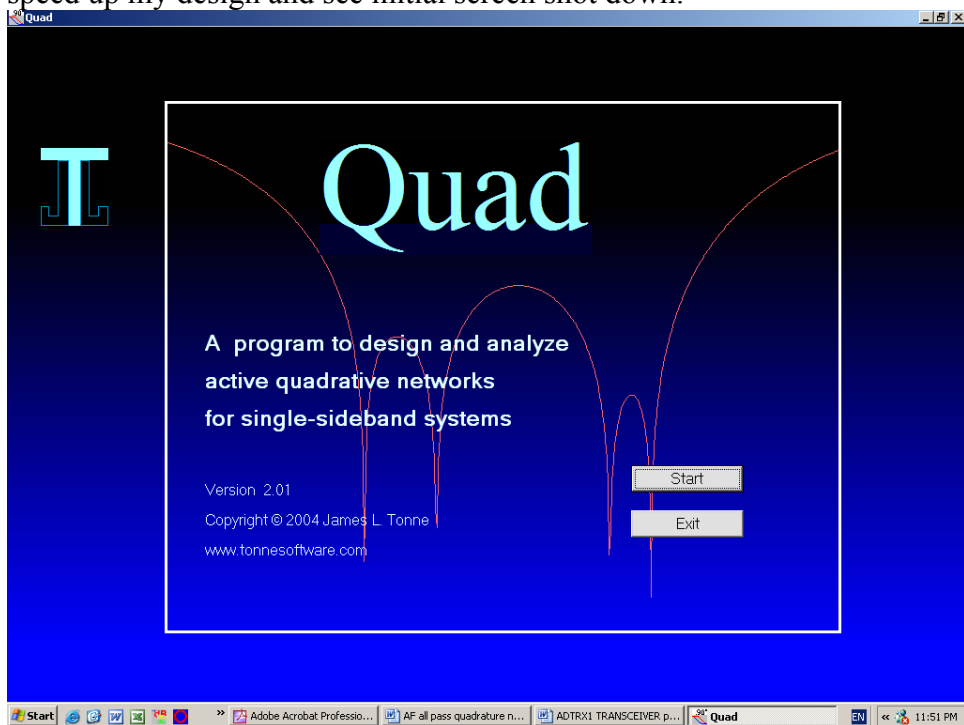


An AF All pass Quadrature Networks Practical Approach old Technique Revised

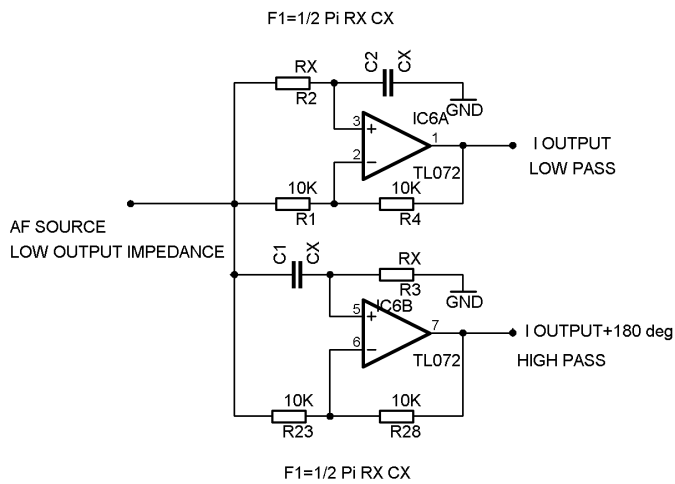
Dipl. Ing . Tasić Siniša –Tasa YU1LM/QRP

An all pass audio quadrature networks as subject was in focus of mine interest few years ago when I was dealing with image rejection direct conversion receivers design. Some results and how it can be realized them I publish in article "***Renaissance of HF DC receivers***" on this site. Article contains 30 pages collected materials about DC receivers with schematics, useful formulas for calculations, PCBs and complete receivers made or design by author. I apologize that this materials are written on Serbian language but schematics, formulas and PCBs are useful for everyone who is in the touch with the direct conversion receivers. I would like to design an SDR transceiver contest grade quality. I was waiting long time to obtain some freeware SB (sound card) software for SDR transceiver but still stay only hope. We still haven't free transmission programs for SSB/CW....In meanwhile I made HF SDR transceiver called ADTRX1 (analog + digital).Upper limit for ADTRX1 is 35 MHz and leak of adequate transmission software I solved with hardware realization. First I started with the CW operation. Solution for CW is a very simple and easy and contains only one audio frequency, audio sub carrier, with quadrature outputs I/Q (90 DEG). Audio sub carrier frequency region between 4-10 kHz was obtaining from the board B2 dividing few MHz oscillator inside IC 4060 with binary divider and filtered with AF LP(low pass) network I connected very clear sinusoidal signal to the two stage all pass phase shift network realized with OP AMP . Adjusting I/Q outputs was very easy and my SDR transceiver was now ready to go on the air. Opposite side band rejection was satisfied and with careful adjustment reached 50 dB and more. A broadband result was better than 40 dB. This result was good for the simple network with one IC TL084 with 4 OP AMP inside. After that I decided to try digital modes and useful audio range have to be much wider than one kHz or more compared to single frequency for the CW. Experimenting with networks I find on INTERNET very interesting free software www.tonnesoftware.com which help me to improve and speed up my design and see initial screen shot down.

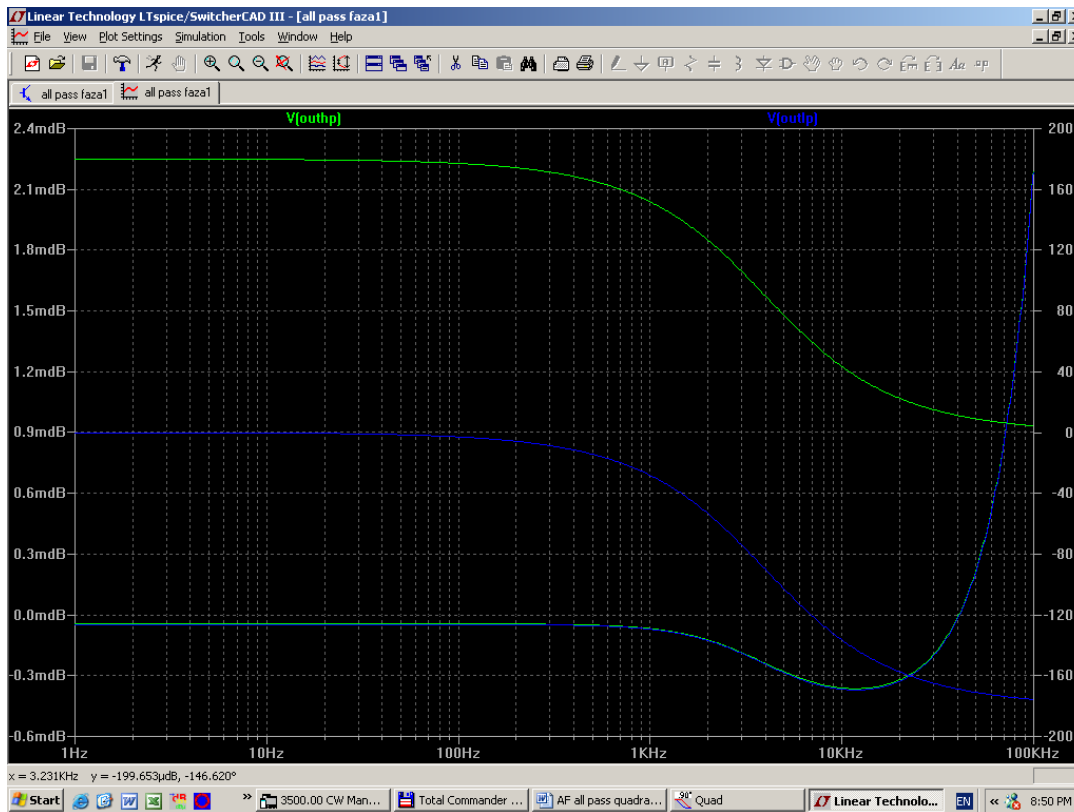


The design/simulation was now really very easy and determinations components variation spread up and their influence to the final result was new light for me. It was possible for me to obtain similar results in some CAD but

adding this Monte Carlo part took to much time and I don't like it if it is necessary. Program is for modulators and demodulator circuits realization as HP (high pass) network but I am using complementary (dual) circuit see schematic and simulation for both networks are down. From results it is evident that it isn't important HP or LP realization only component values.

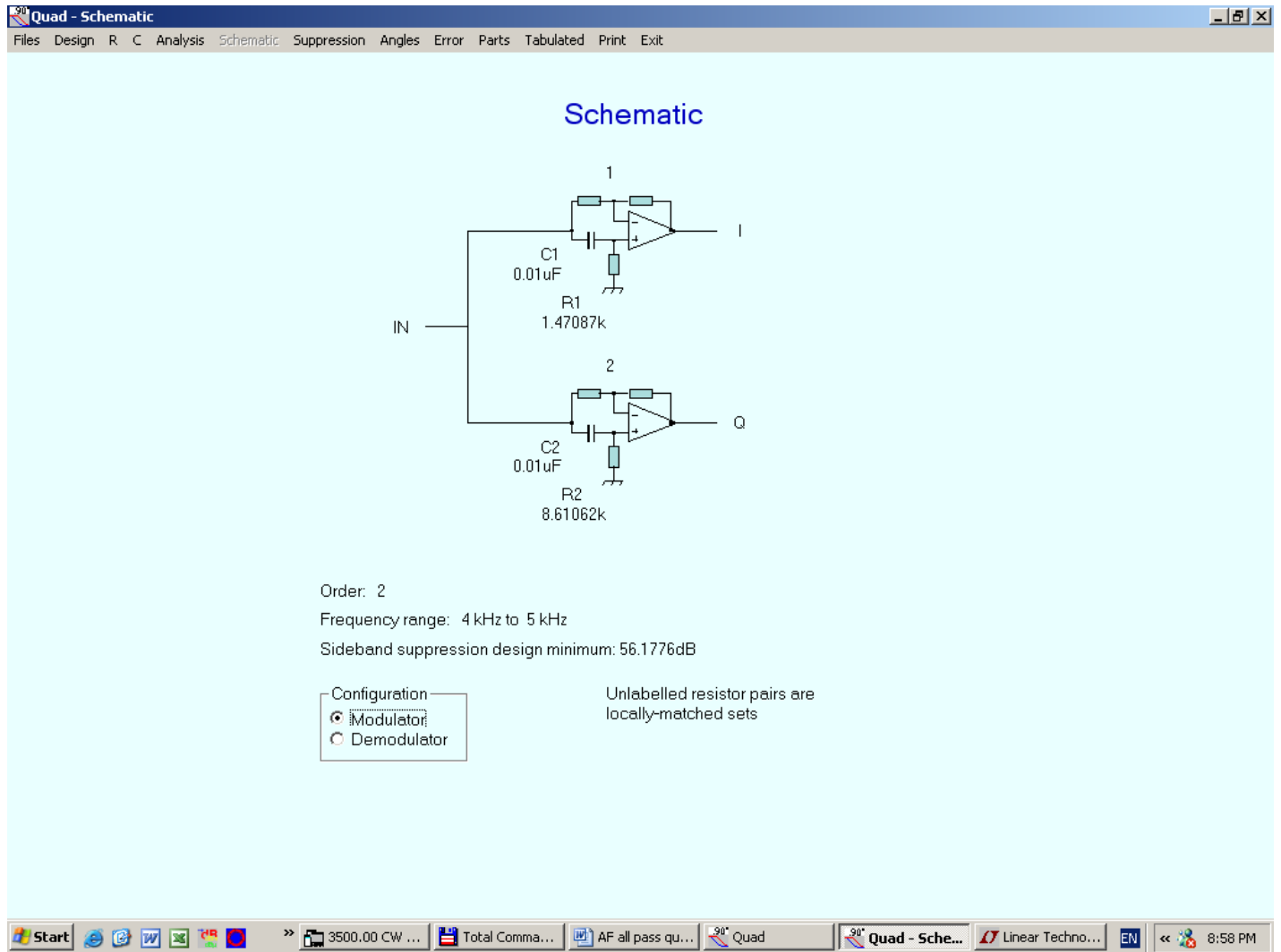


SCHEMATIC AS ILLUSTRATION 2 POSSIBILITY FOR AF SHIFT NETWORKS LOW PASS AND HIGH PASS VERSIONS

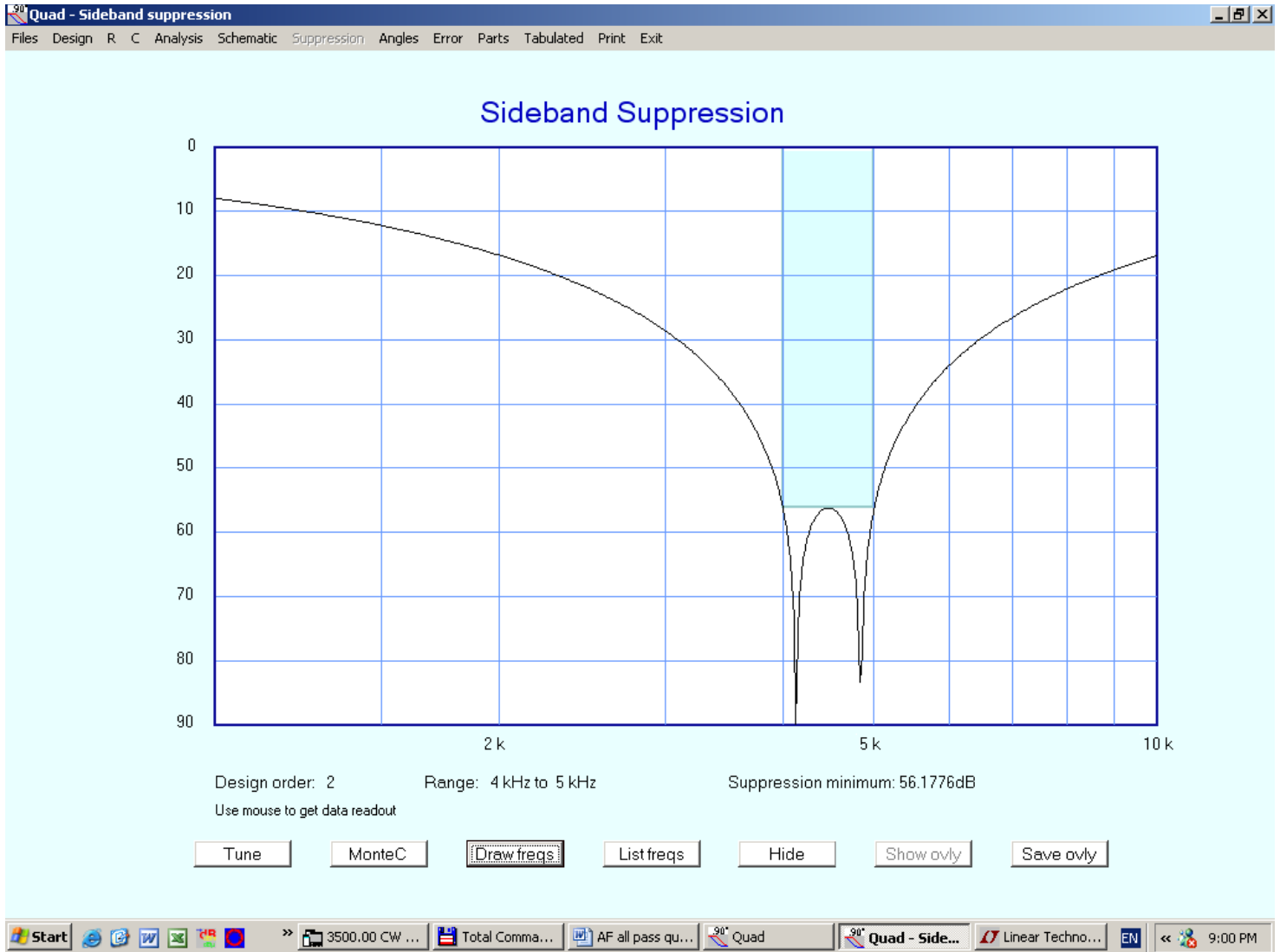


All design are with low pass networks original schematics from QUAD CAD is high pass components values are the same except that R and C have to change places in networks which is connected to the + input OP AMP. C in all networks is 10 nF 1% tolerances.

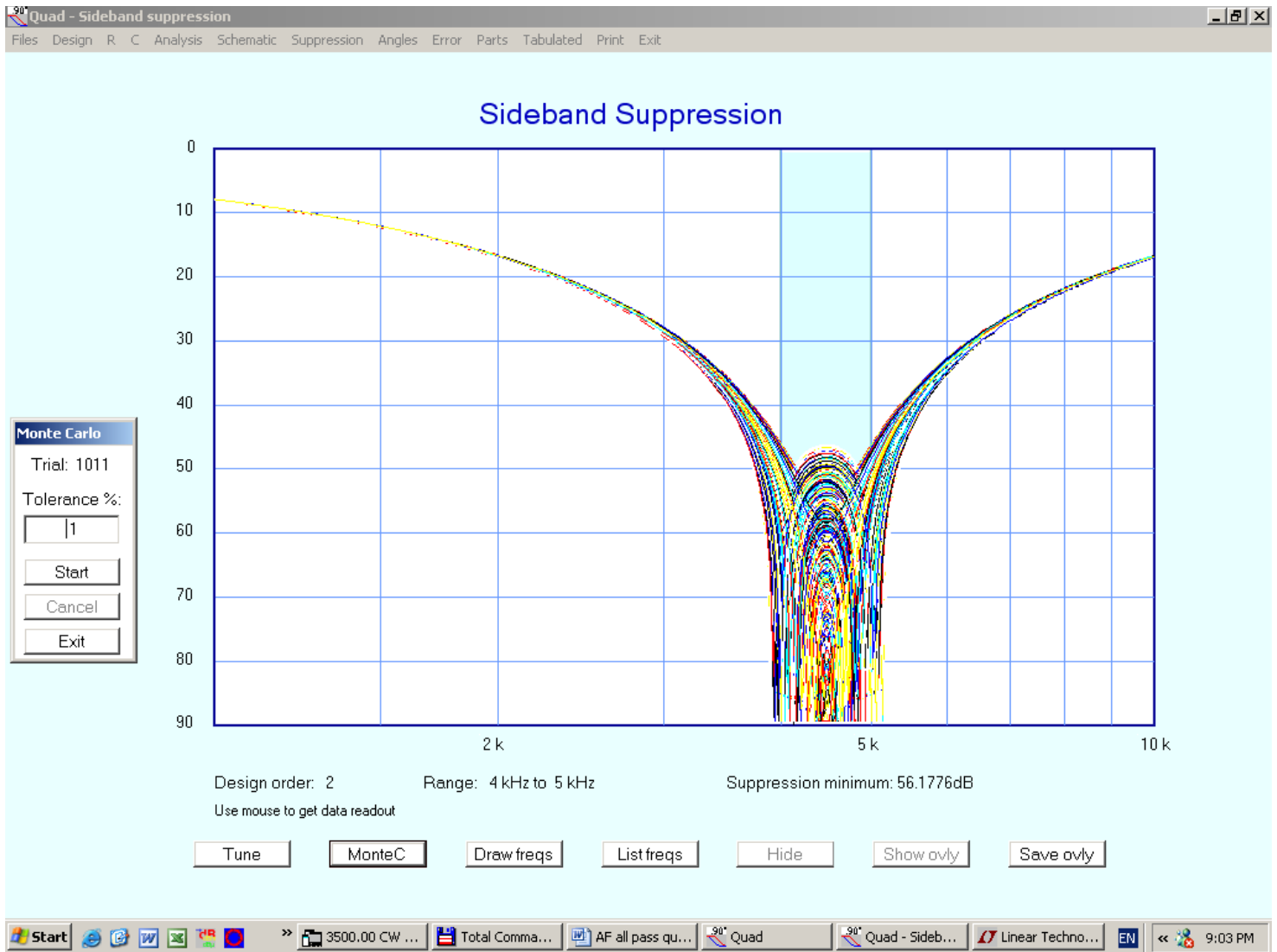
1. CW sub carrier 4-5 KHz I/Q phase shift networks is second order with one TL 072 FET OP AMP.



Ideal theoretical situation with opposite side suppression.

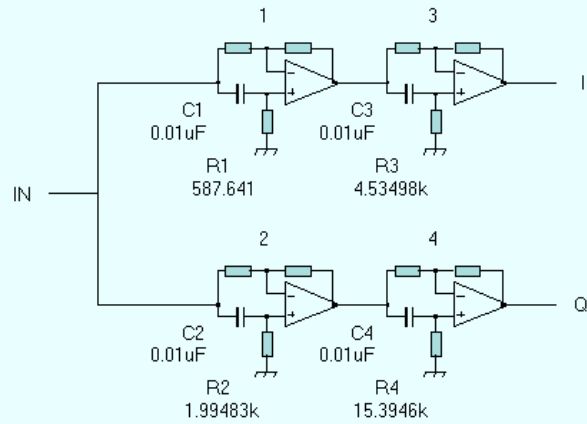


Influence of component tolerances to the final results and results which we can really expect with practical realization.



The same situation but with 4 order networks one TL084

Schematic



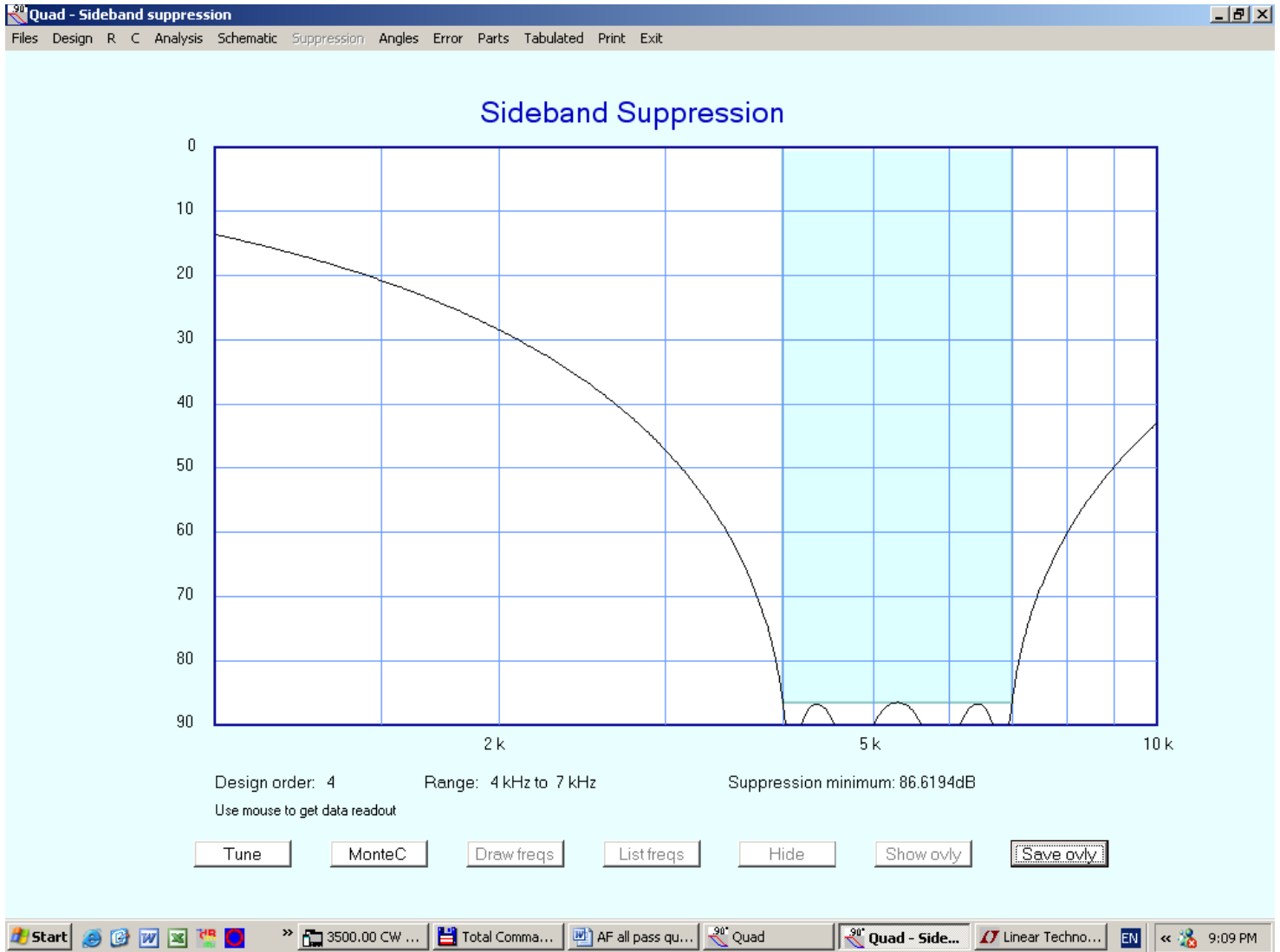
Order: 4
Frequency range: 4 kHz to 7 kHz
Sideband suppression design minimum: 86.6194dB

Configuration

- Modulator
- Demodulator

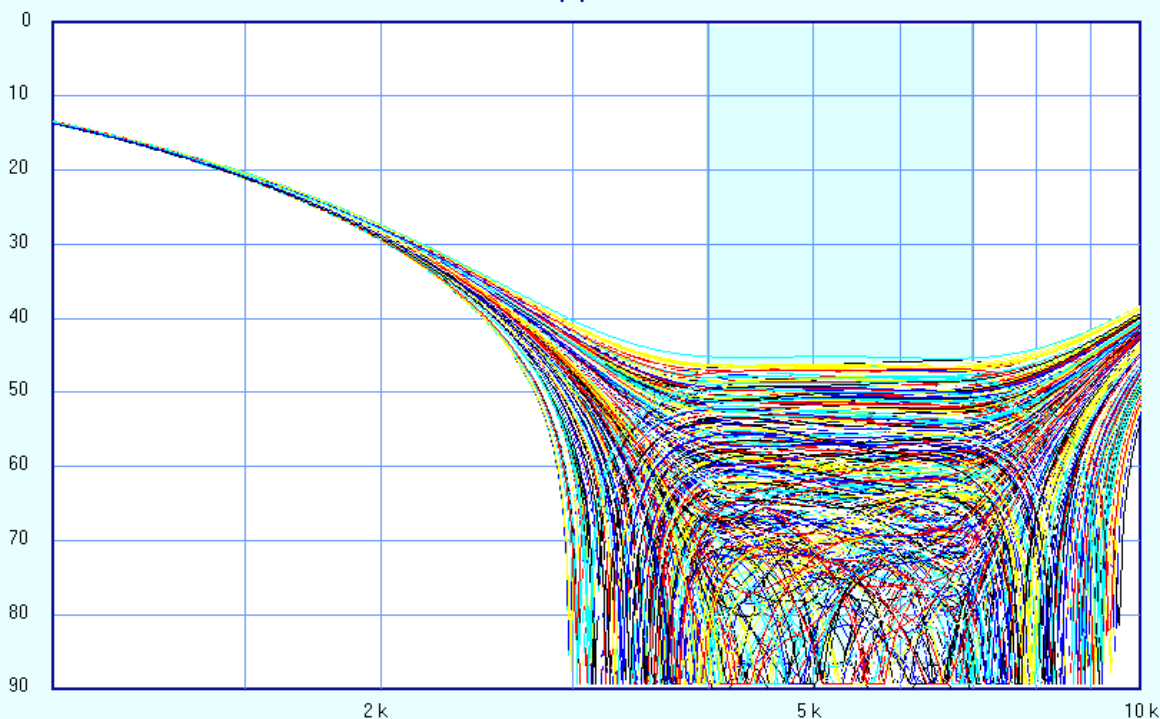
Unlabelled resistor pairs are locally-matched sets

Ideal situation with sideband suppression



Component tolerances influence to the final results and results which we can really expect in practice

Sideband Suppression

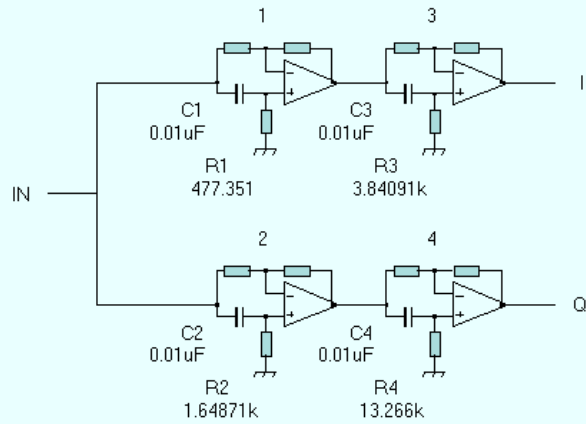


Monte Carlo
Trial: 1027
Tolerance %:

Design order: 4 Range: 4 kHz to 7 kHz Suppression minimum: 86.6194dB
Use mouse to get data readout

-
-
-
-
-
-
-

Schematic



Order: 4

Frequency range: 4 kHz to 10 kHz

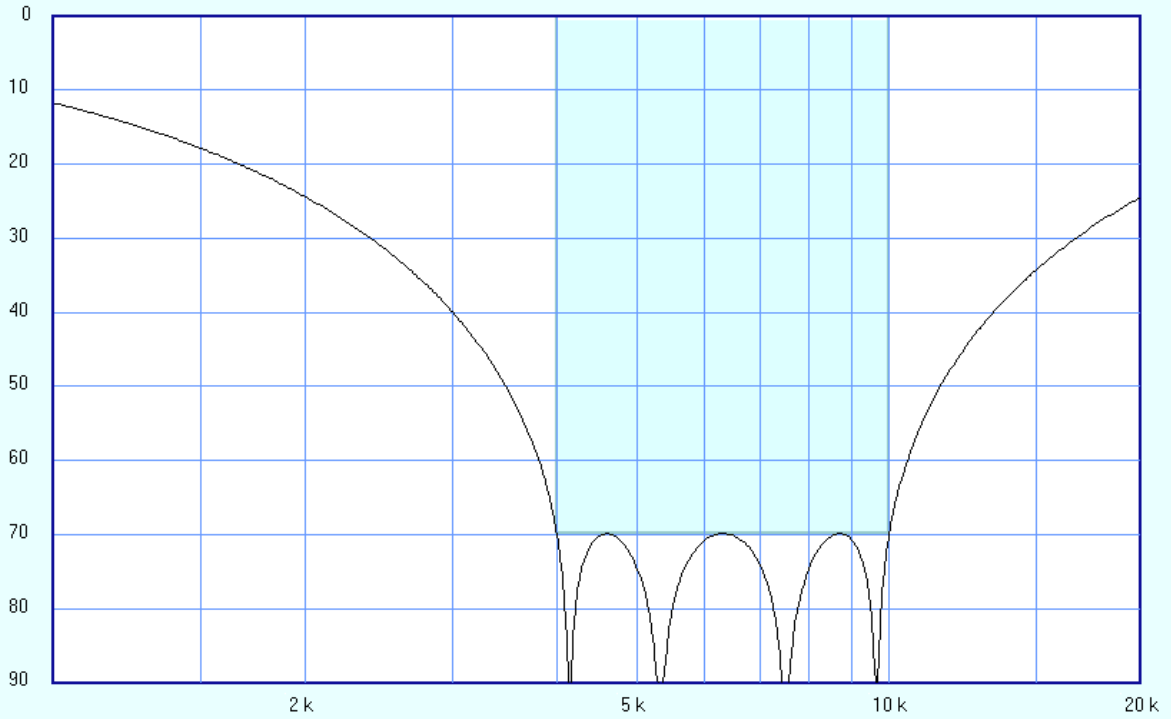
Sideband suppression design minimum: 69.8531 dB

Configuration

- Modulator
- Demodulator

Unlabelled resistor pairs are locally-matched sets

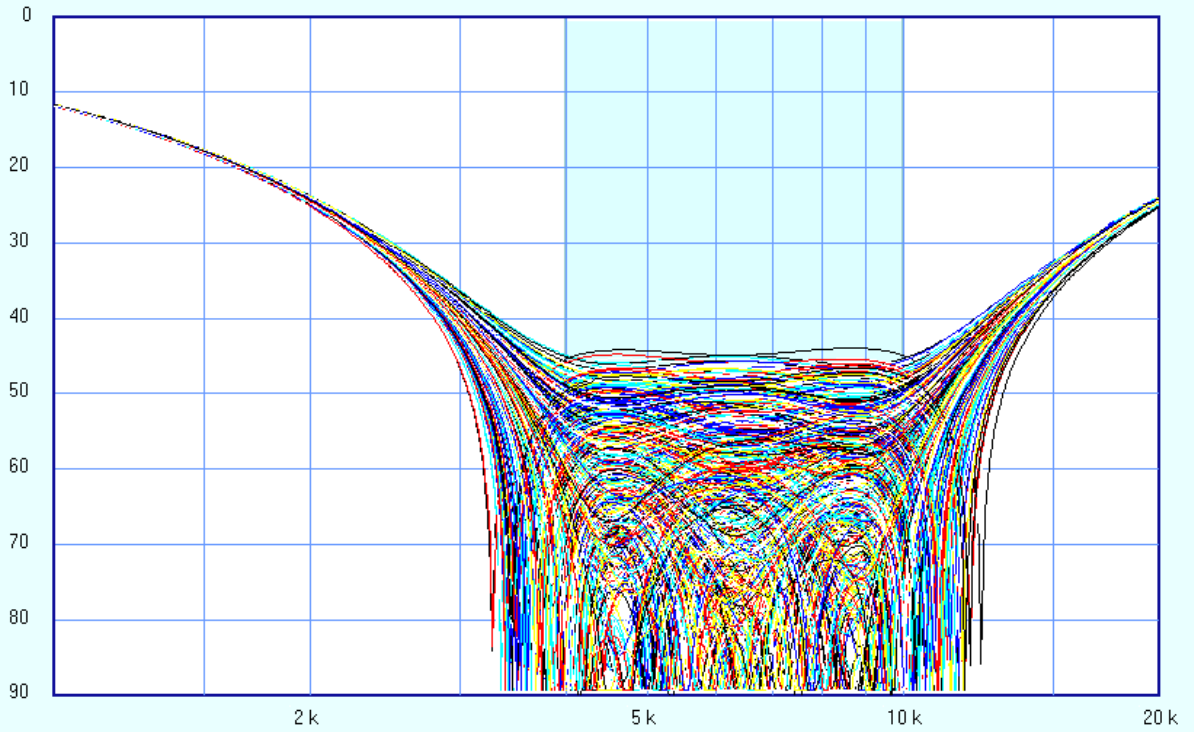
Sideband Suppression



Design order: 4 Range: 4 kHz to 10 kHz Suppression minimum: 69.8531 dB
Use mouse to get data readout

Tune MonteC Draw freqs List freqs Hide Show ovly Save ovly

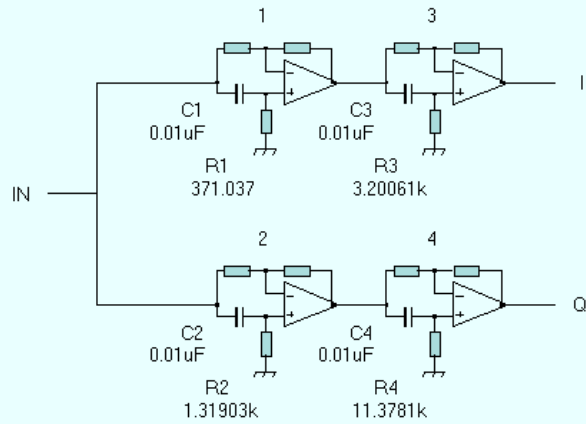
Sideband Suppression



Monte Carlo
Trial: 1034
Tolerance %:

Design order: 4 Range: 4 kHz to 10 kHz Suppression minimum: 69.8531dB

Schematic

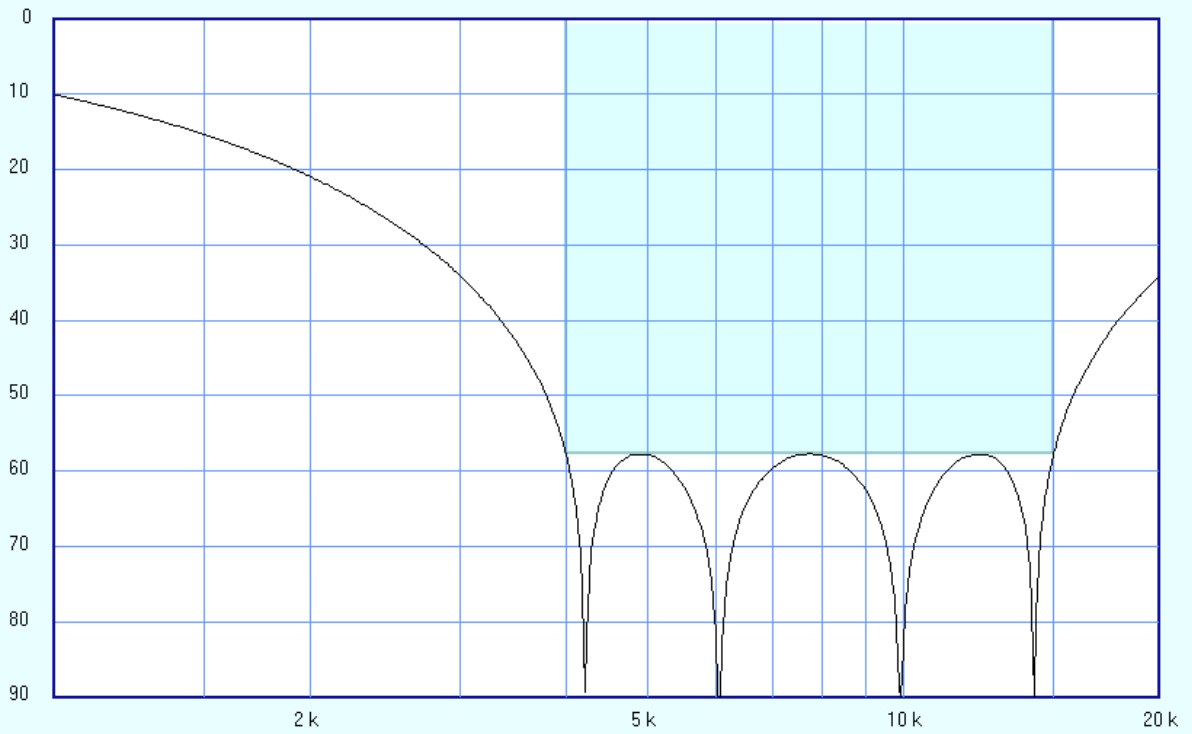


Order: 4
Frequency range: 4 kHz to 15 kHz
Sideband suppression design minimum: 57.7226dB

- Configuration
- Modulator
 - Demodulator

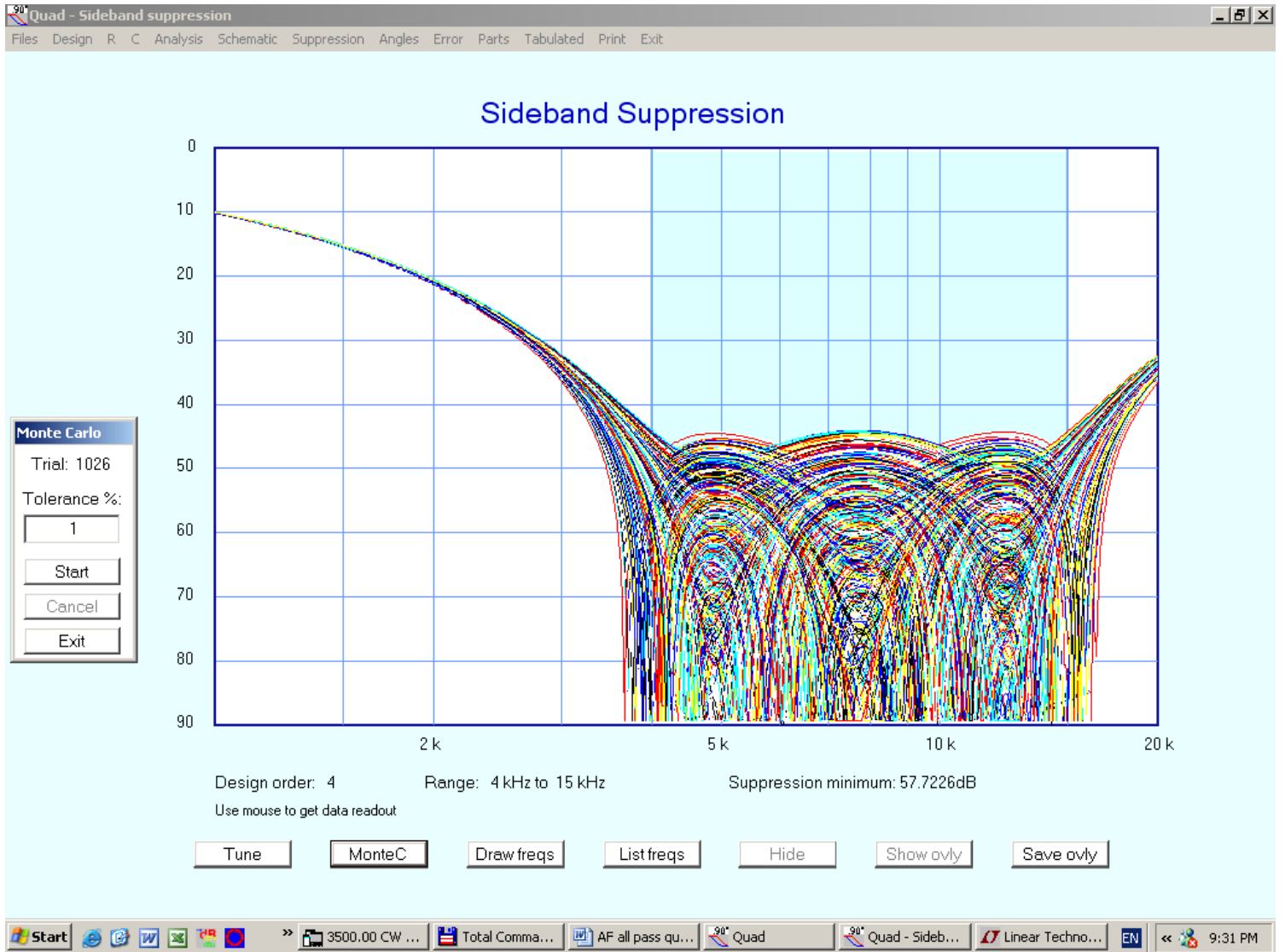
Unlabelled resistor pairs are locally-matched sets

Sideband Suppression



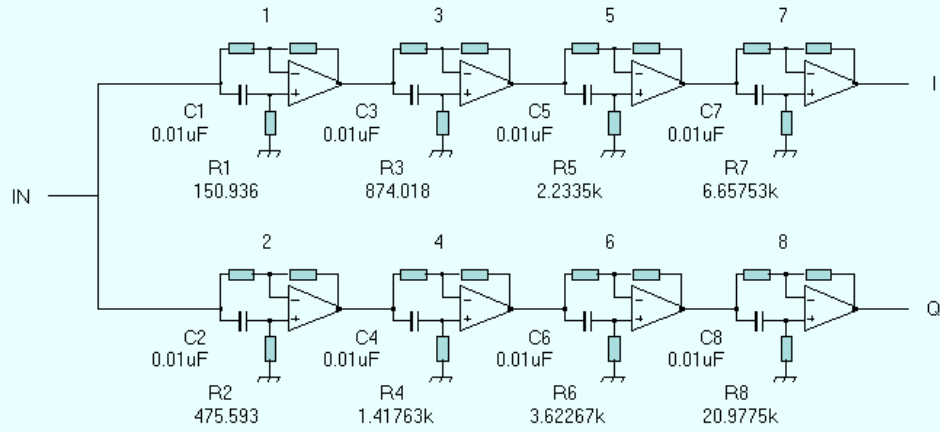
Design order: 4 Range: 4 kHz to 15 kHz Suppression minimum: 57.7226dB
Use mouse to get data readout

Tune MonteC Draw freqs List freqs Hide Show only Save only



The same situation but with 8 order networks realized with two TL084 FET OP AMP.

Schematic

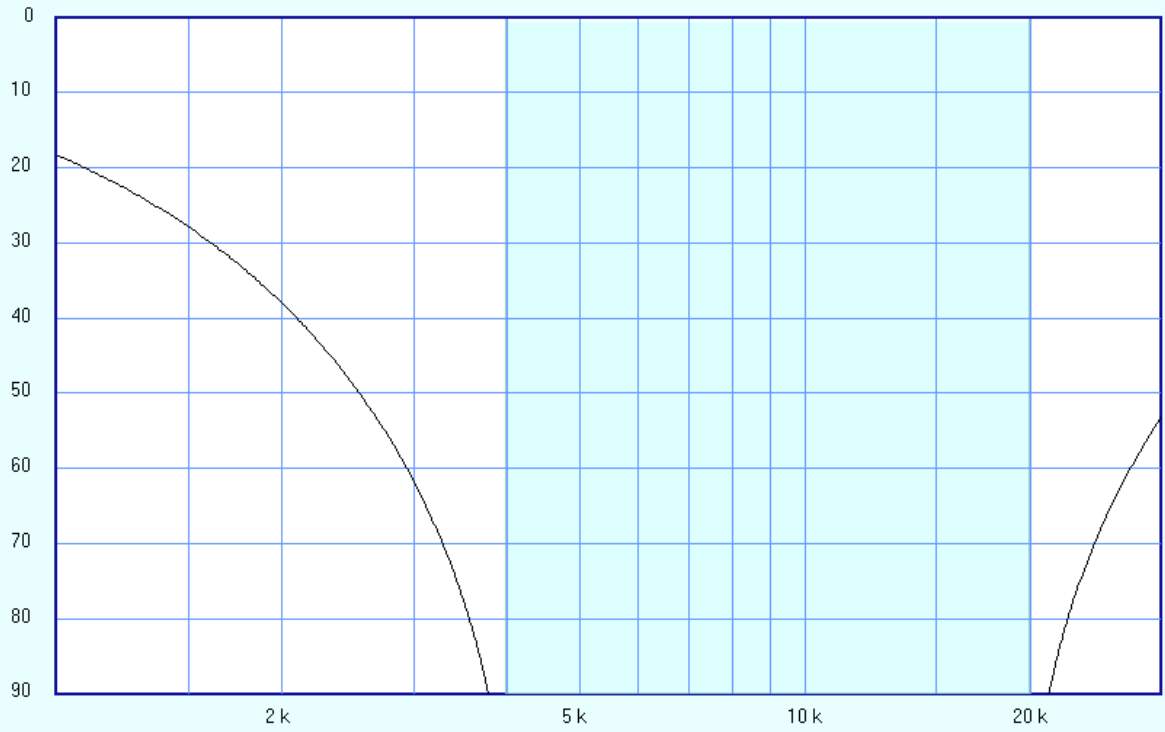


Order: 8
Frequency range: 4 kHz to 20 kHz
Sideband suppression design minimum: 108.834dB

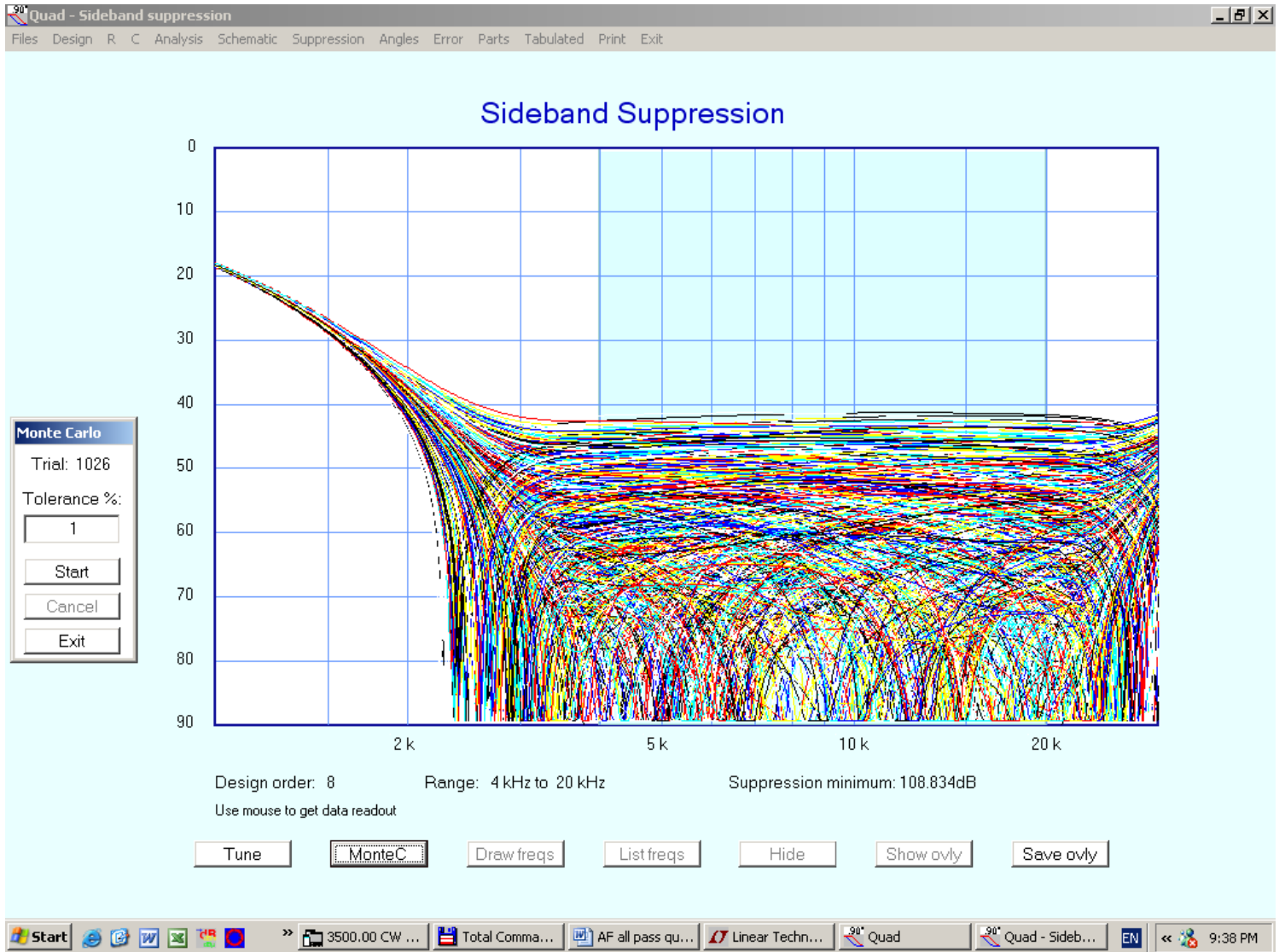
- Configuration
- Modulator
 - Demodulator

Unlabelled resistor pairs are locally-matched sets

Sideband Suppression

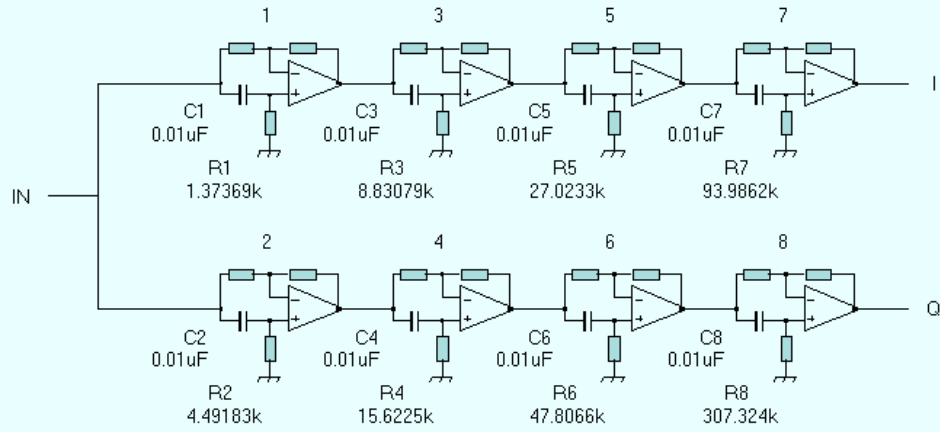


Design order: 8 Range: 4 kHz to 20 kHz Suppression minimum: 108.834dB
Use mouse to get data readout



All pass network realization for SSB transmission audio frequency band between 200 Hz to 3 kHz and 8 order networks with 2 FET OP AMP TL084.

Schematic

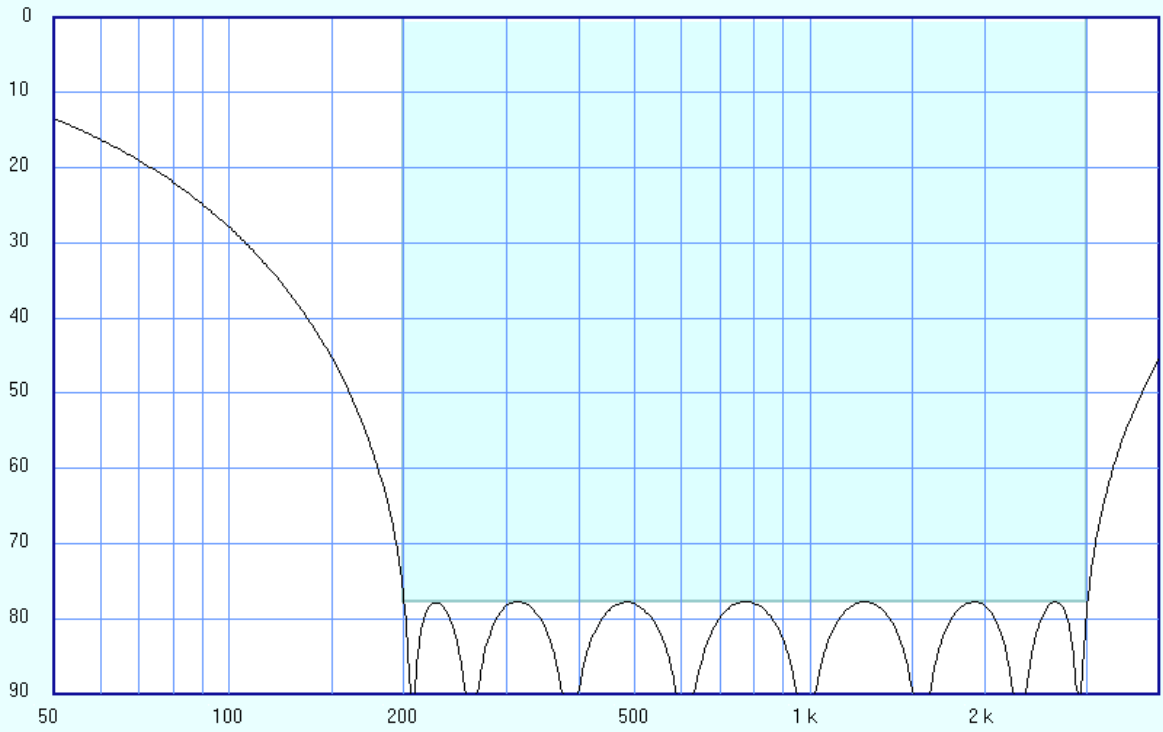


Order: 8
Frequency range: 200 Hz to 3 kHz
Sideband suppression design minimum: 77.7531 dB

- Configuration
- Modulator
 - Demodulator

Unlabelled resistor pairs are locally-matched sets

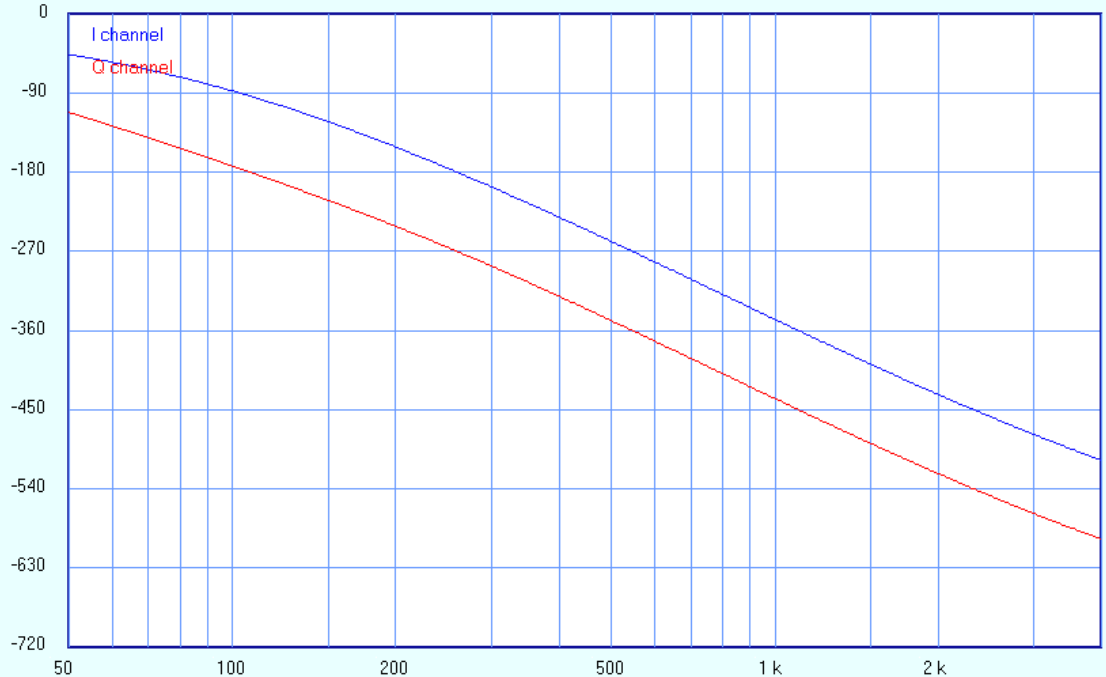
Sideband Suppression



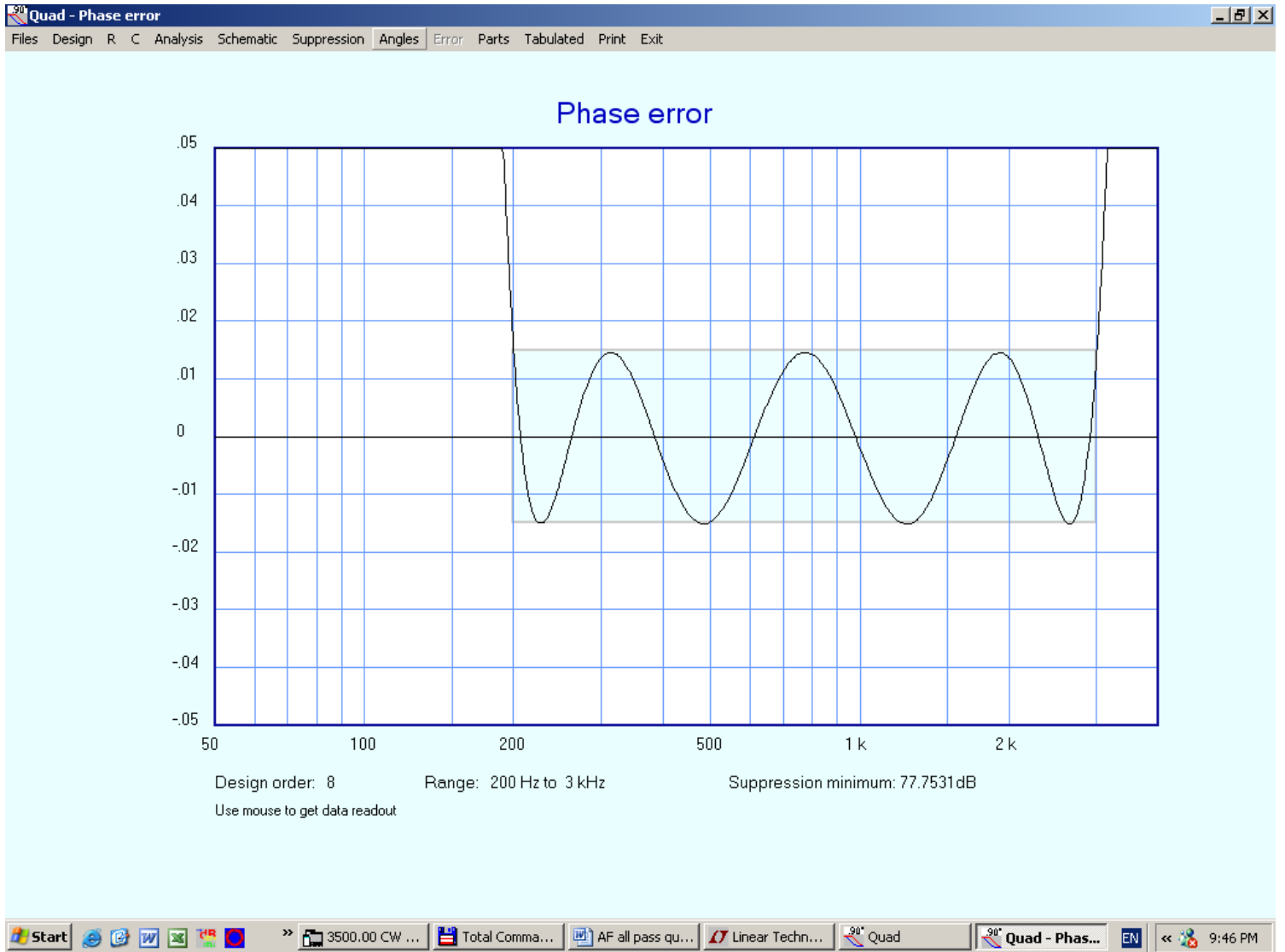
Design order: 8 Range: 200 Hz to 3 kHz Suppression minimum: 77.7531 dB
Use mouse to get data readout

Tune MonteC Draw freqs List freqs Hide Show ovly Save ovly

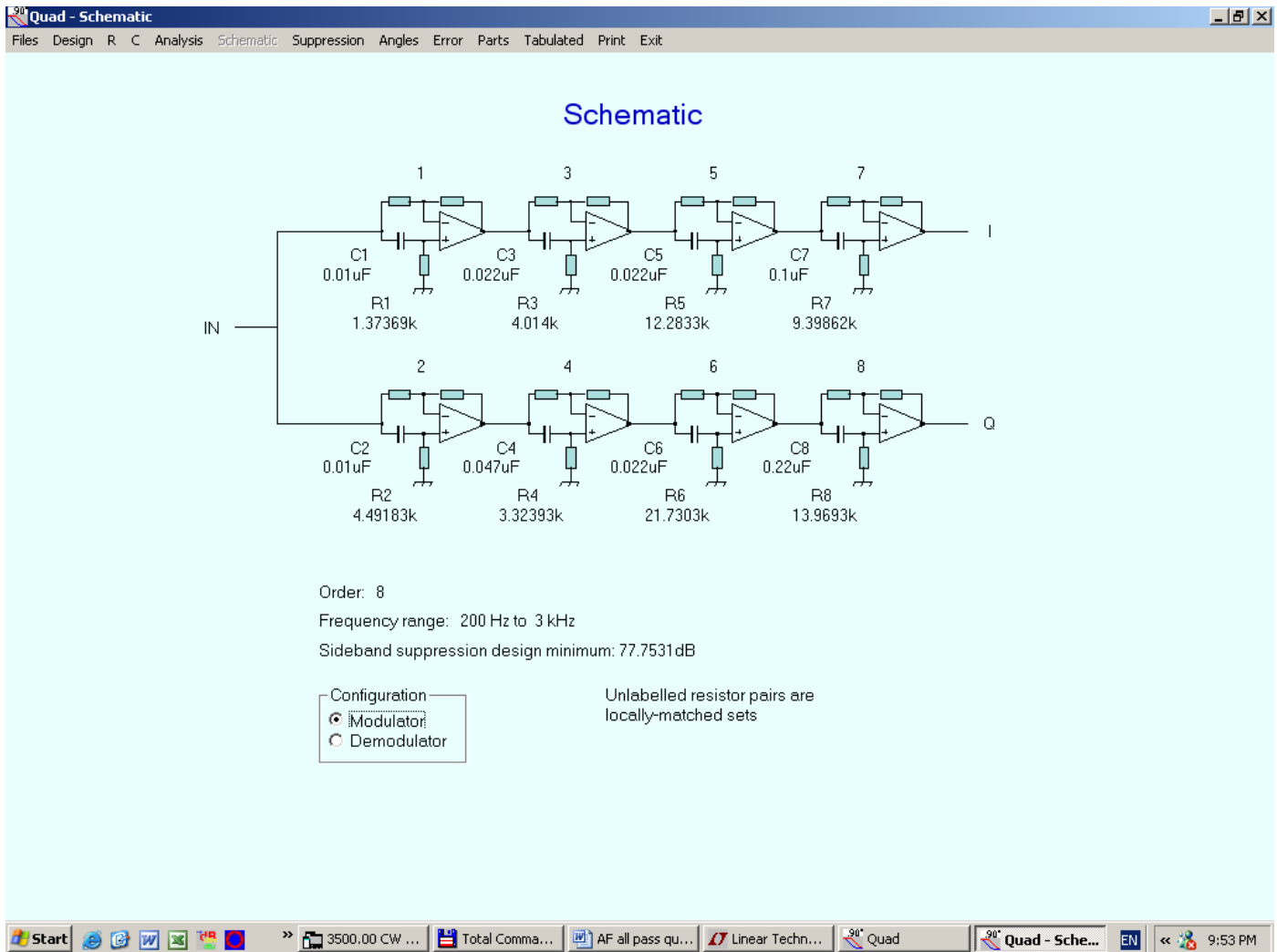
Phase angles



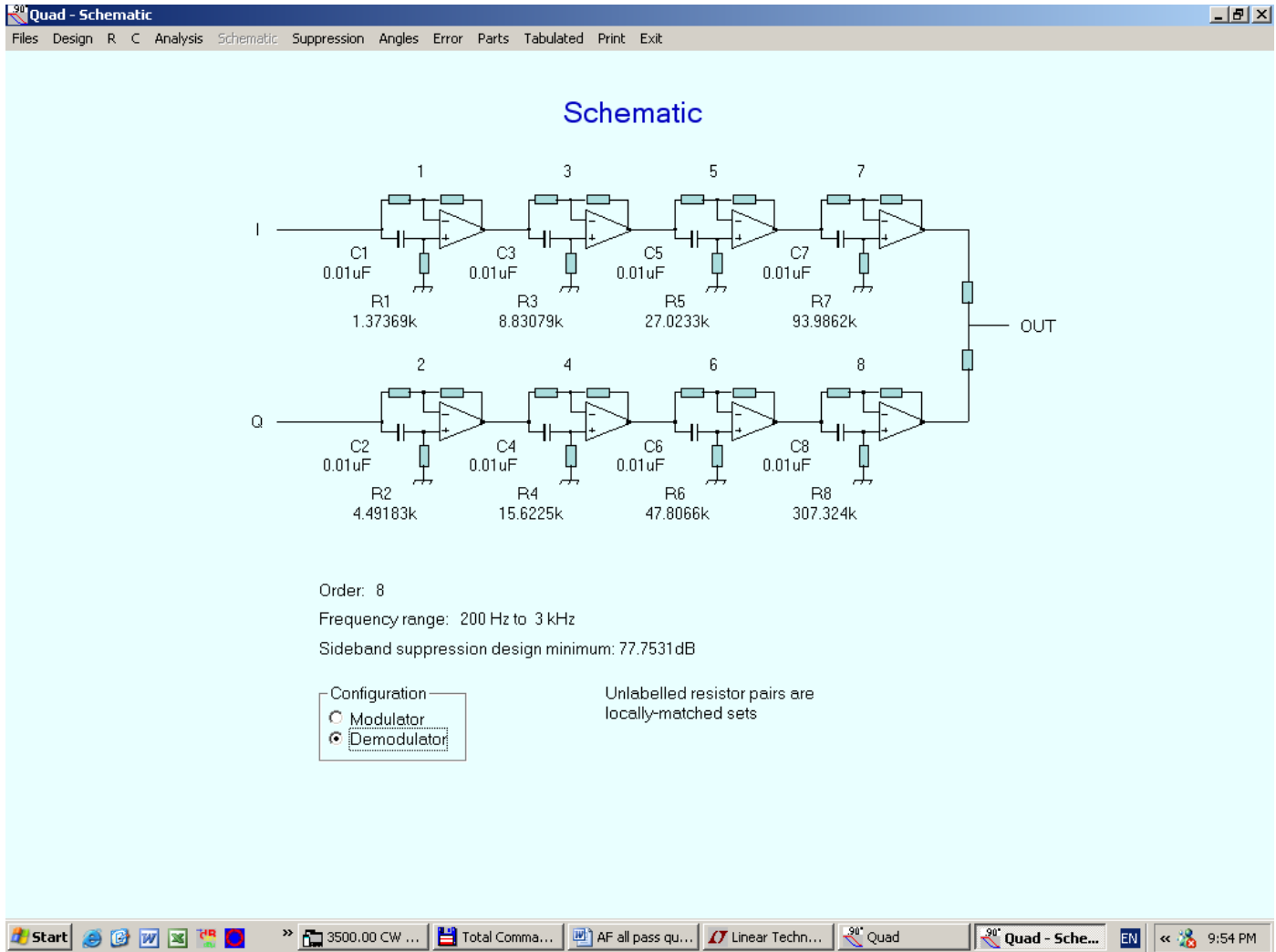
Design order: 8 Range: 200 Hz to 3 kHz Suppression minimum: 77.7531 dB
Use mouse to get data readout



Alternative values for the all pass SSB network when the C capacitors are non equally values.

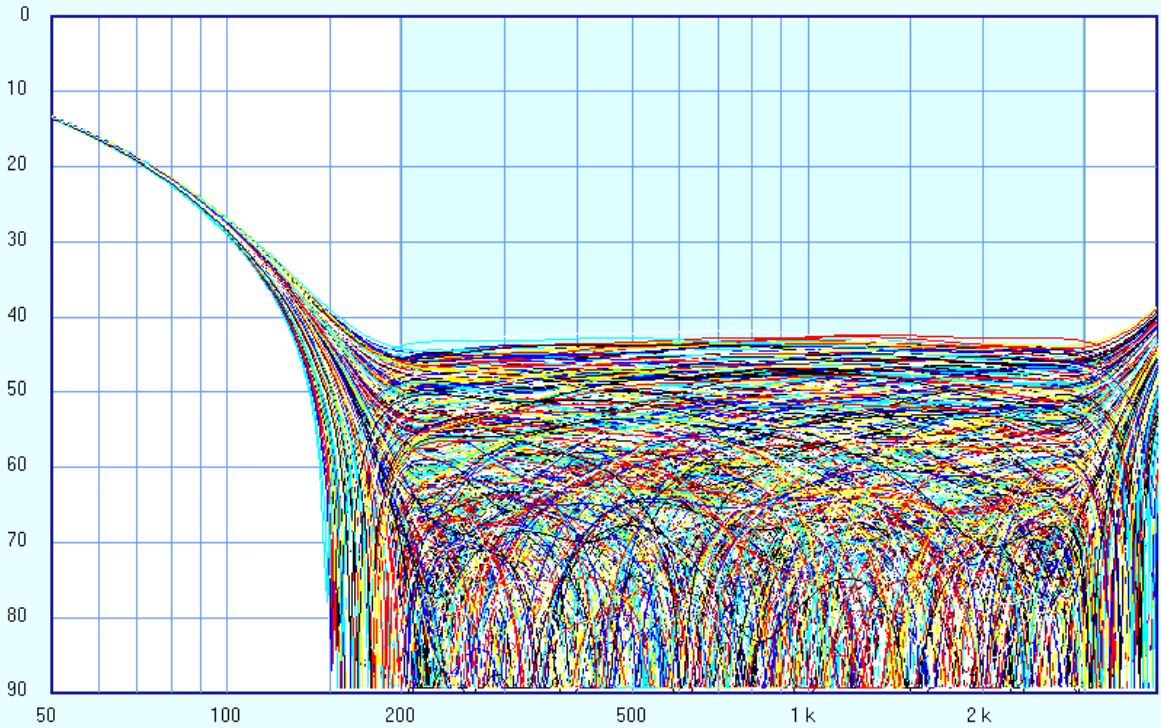


Schematics for the same network but in the demodulator circuit.



Component tolerances influence for the 1 %, 2 % and 5 % tolerance shows that final real results is unwanted sideband suppression which we can expecting from practical realization.

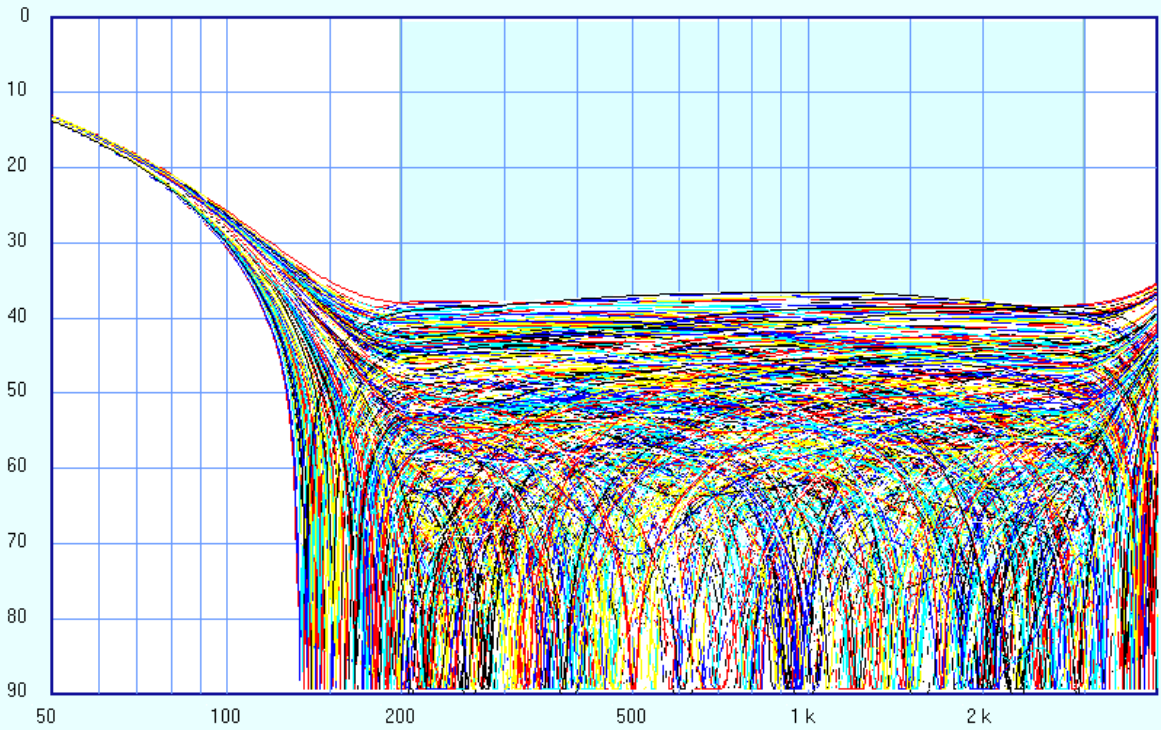
Sideband Suppression



Monte Carlo
Trial: 1023
Tolerance %:

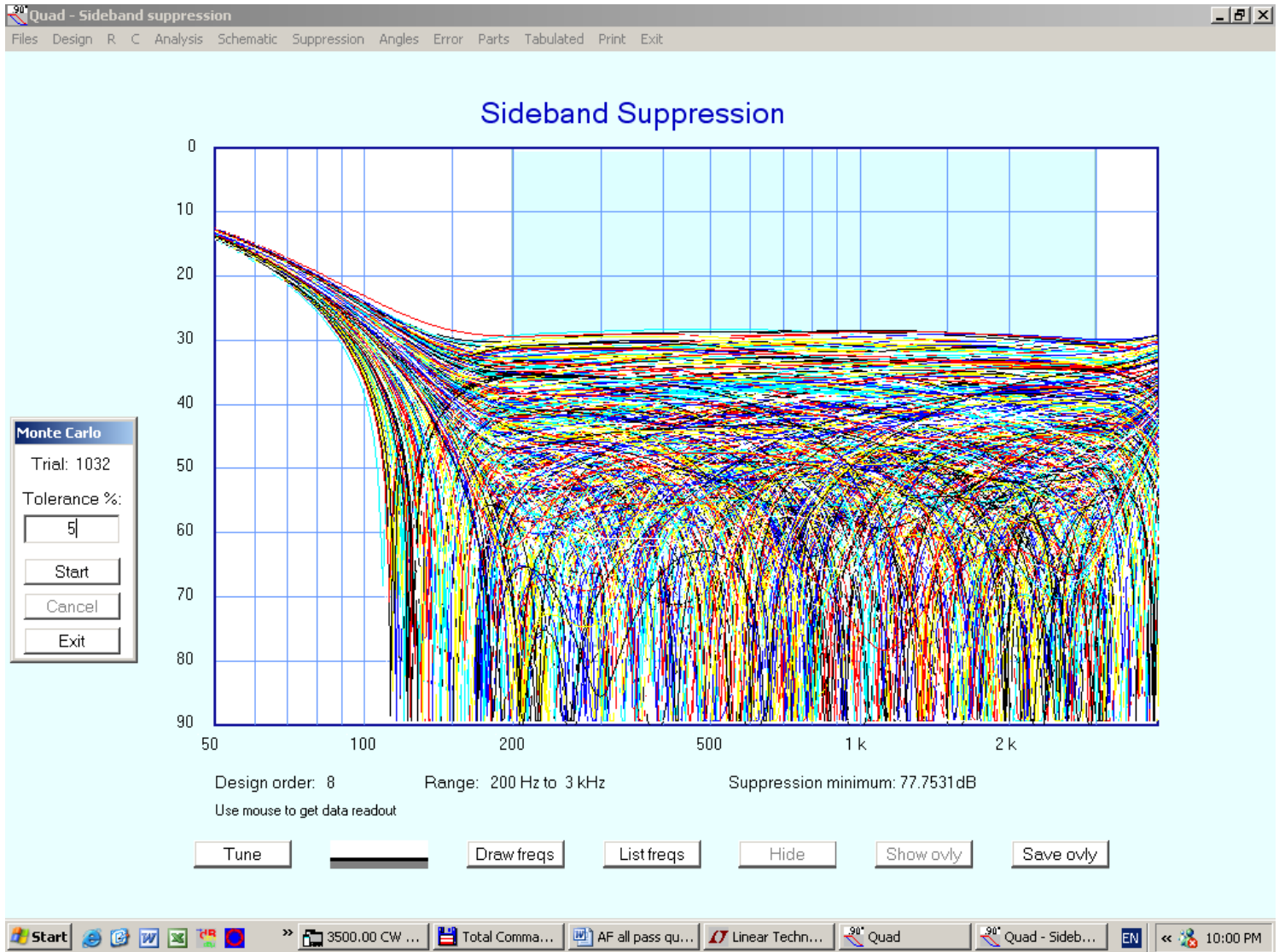
Design order: 8 Range: 200 Hz to 3 kHz Suppression minimum: 77.7531dB
Use mouse to get data readout

Sideband Suppression



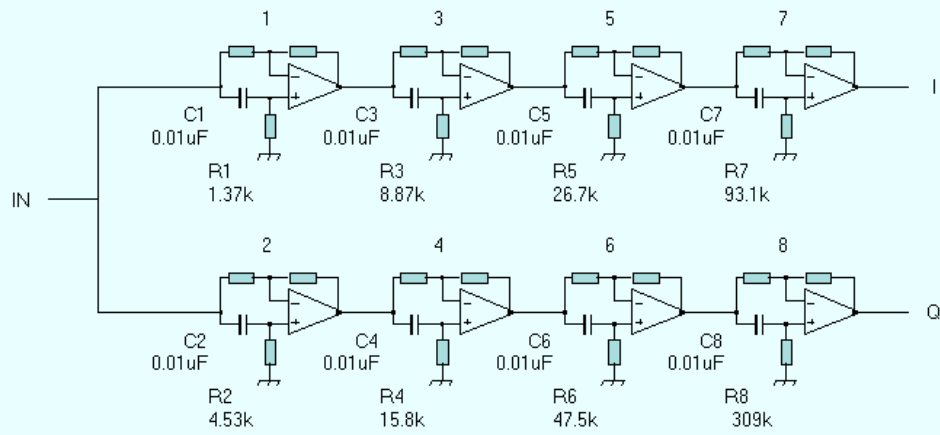
Monte Carlo
Trial: 1025
Tolerance %:

Design order: 8 Range: 200 Hz to 3 kHz Suppression minimum: 77.7531dB
Use mouse to get data readout



All pass SSB phase shifter realization with standard real 1% R and C components

Schematic

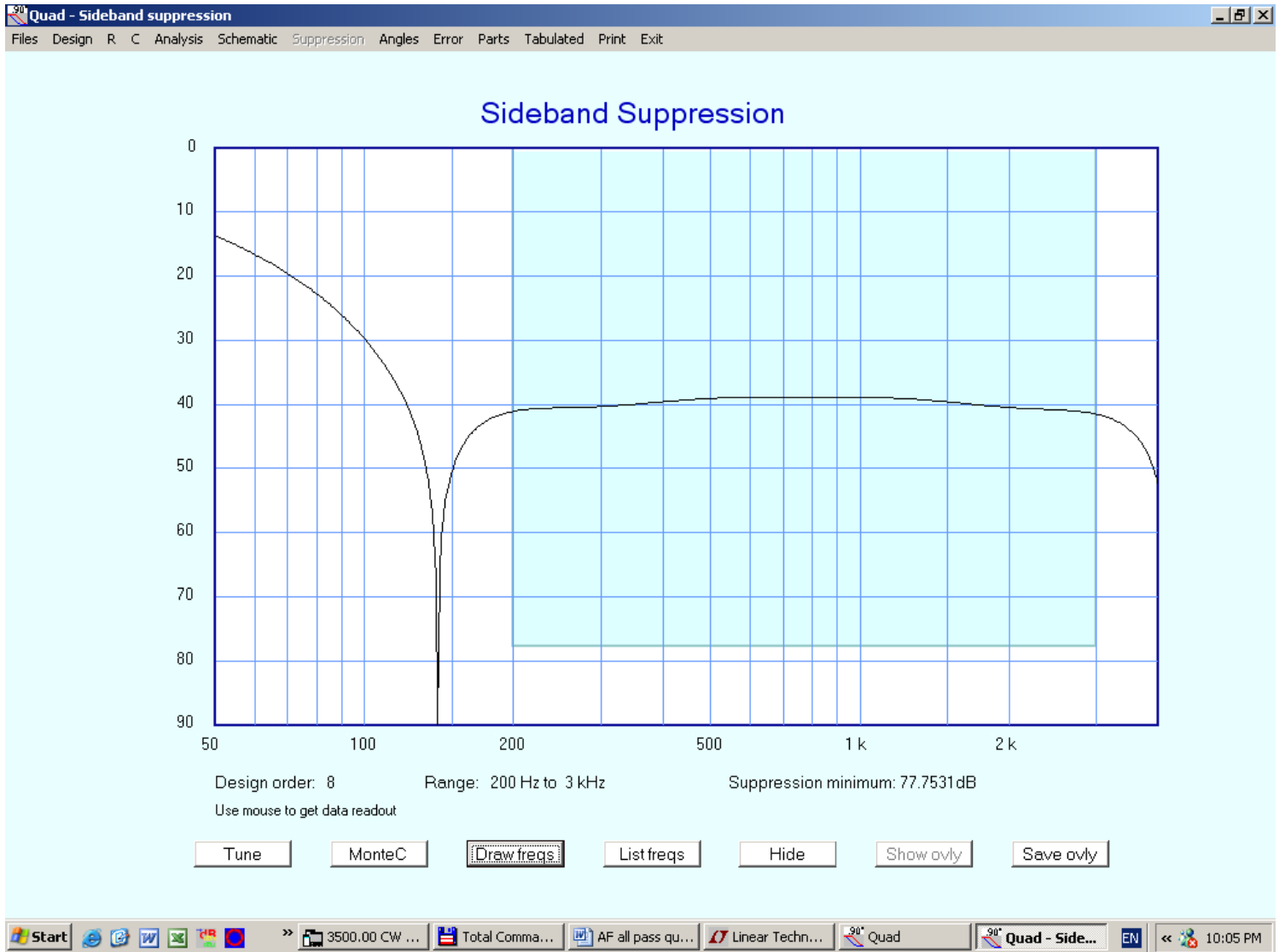


Order: 8
Frequency range: 200 Hz to 3 kHz
Sideband suppression design minimum: 77.7531dB

Configuration

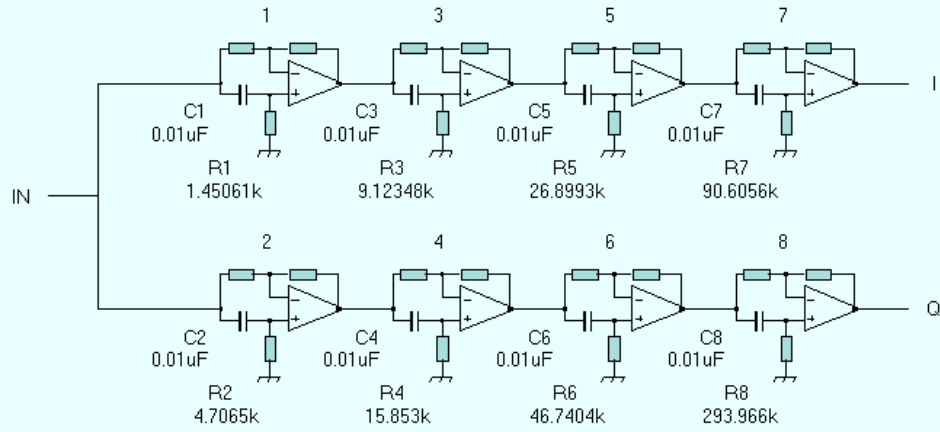
- Modulator
- Demodulator

Unlabelled resistor pairs are locally-matched sets



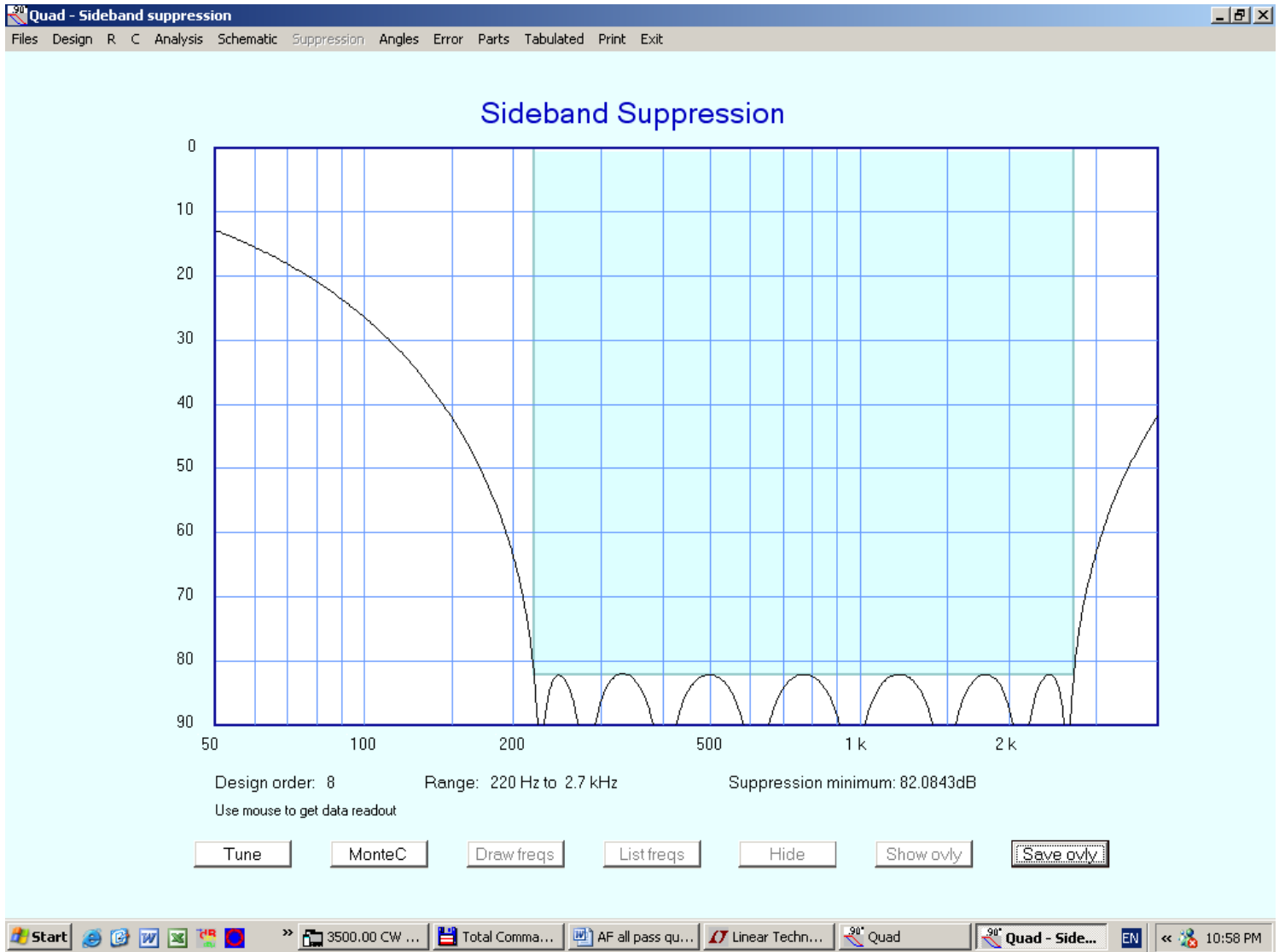
Alternative design with little changed AF corners and with optimization to the standard R and C values. First is done ideal and then real realization result.

Schematic



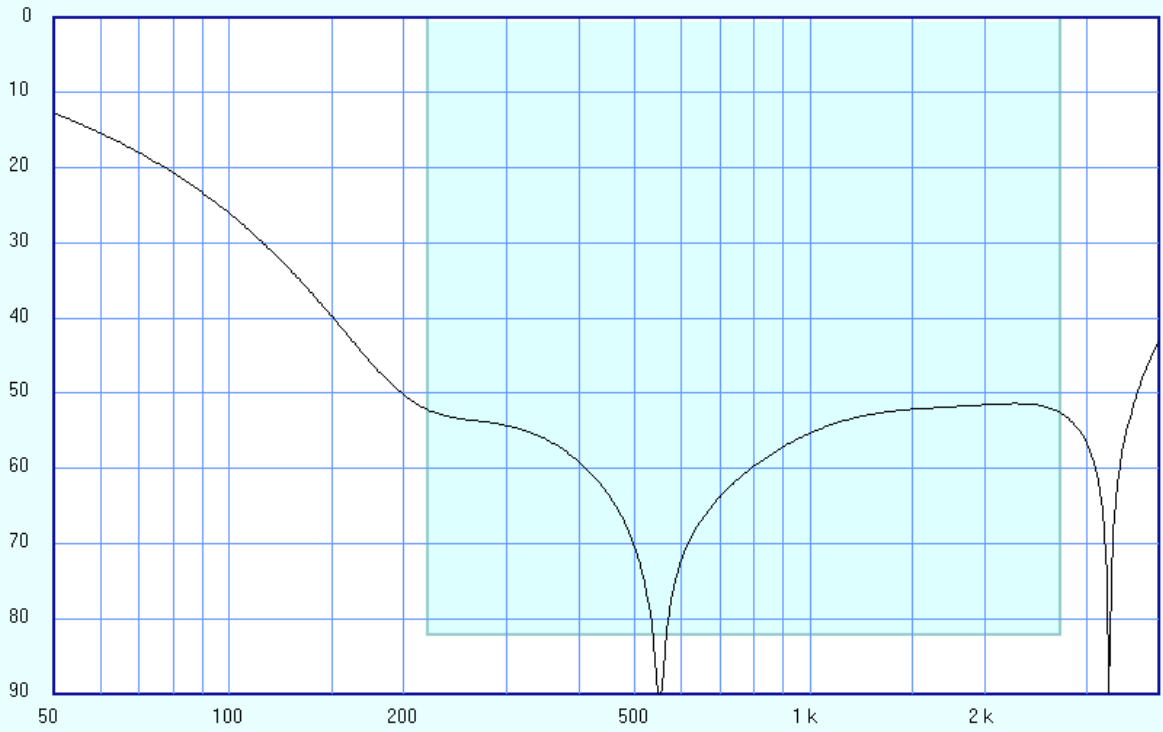
- Configuration
- Modulator
 - Demodulator

Unlabelled resistor pairs are locally-matched sets

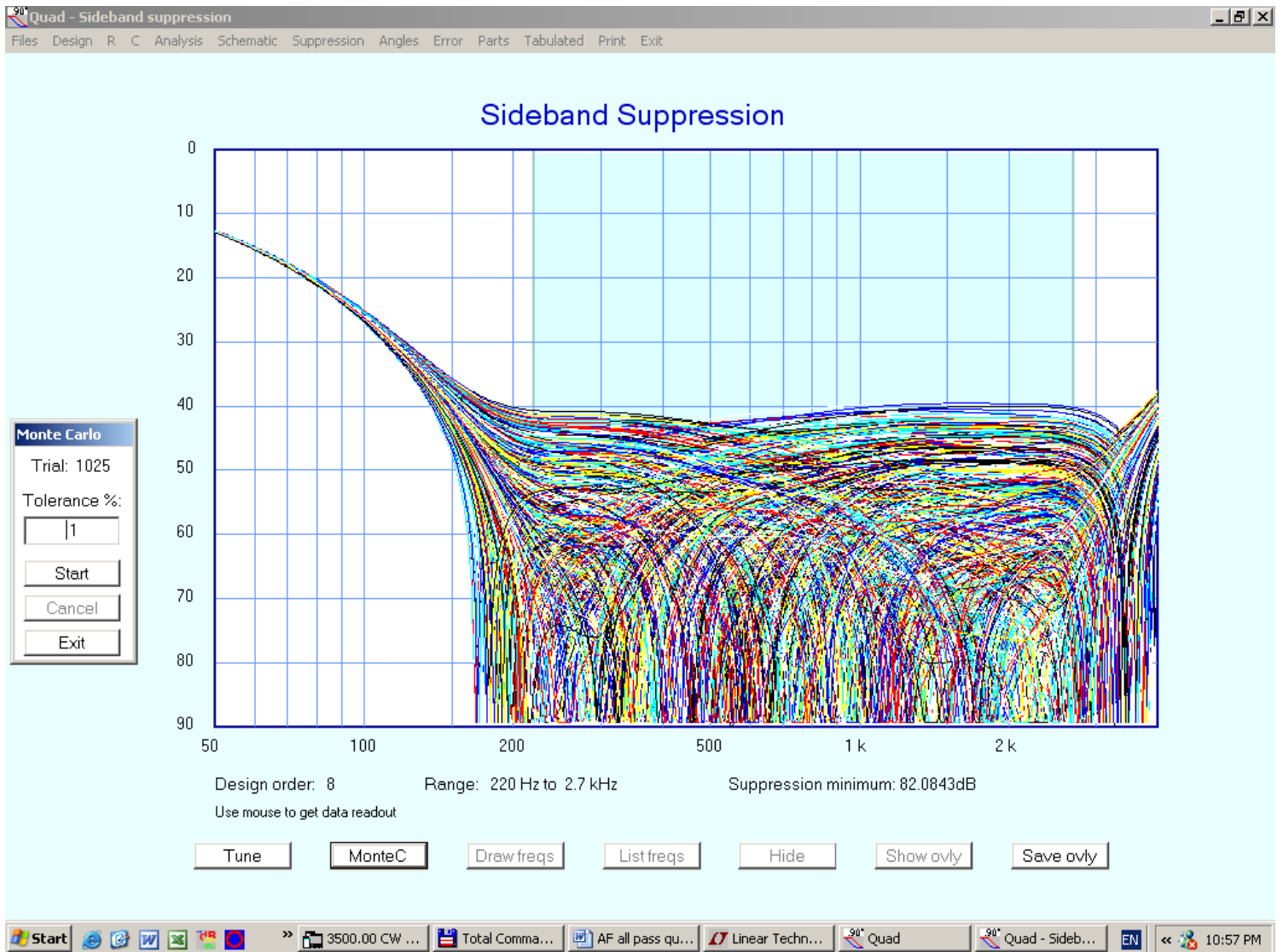


Sideband suppression with standard 1% components and their distribution around nominal values inside show they have influence to the final result.

Sideband Suppression

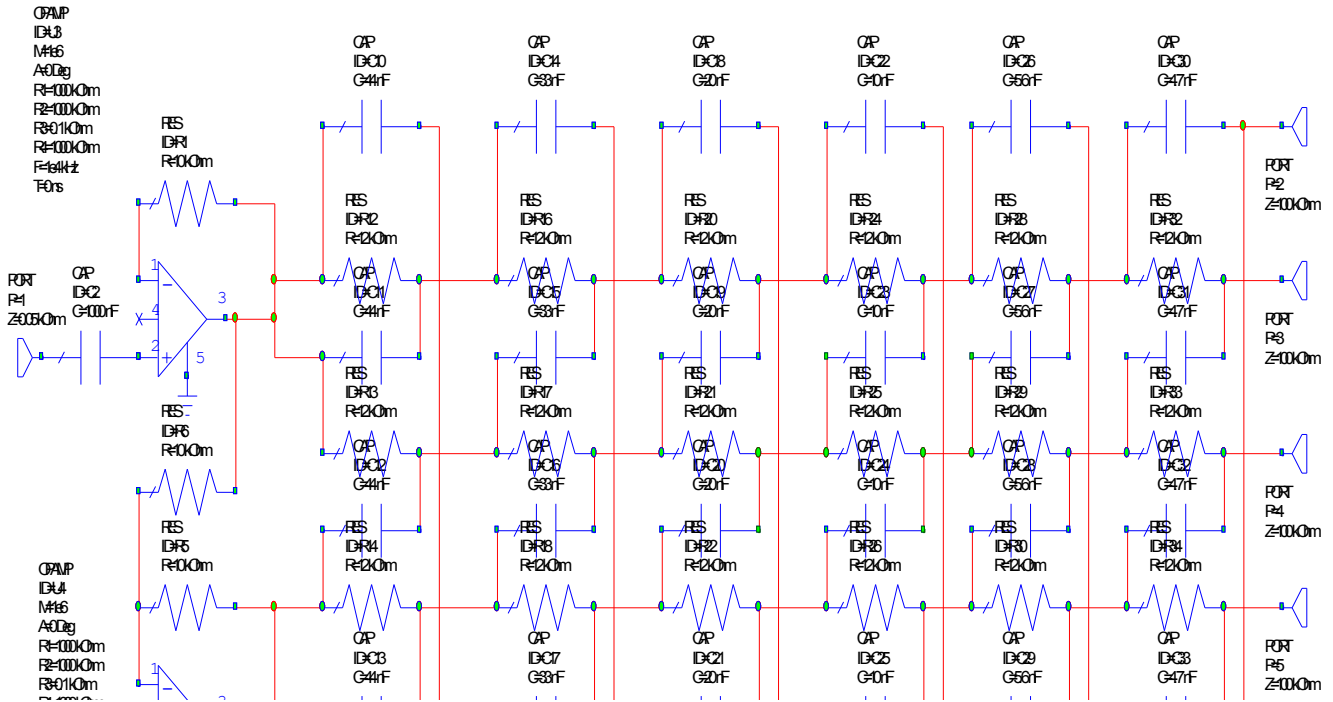


Design order: 8 Range: 220 Hz to 2.7 kHz Suppression minimum: 82.0843dB
Use mouse to get data readout

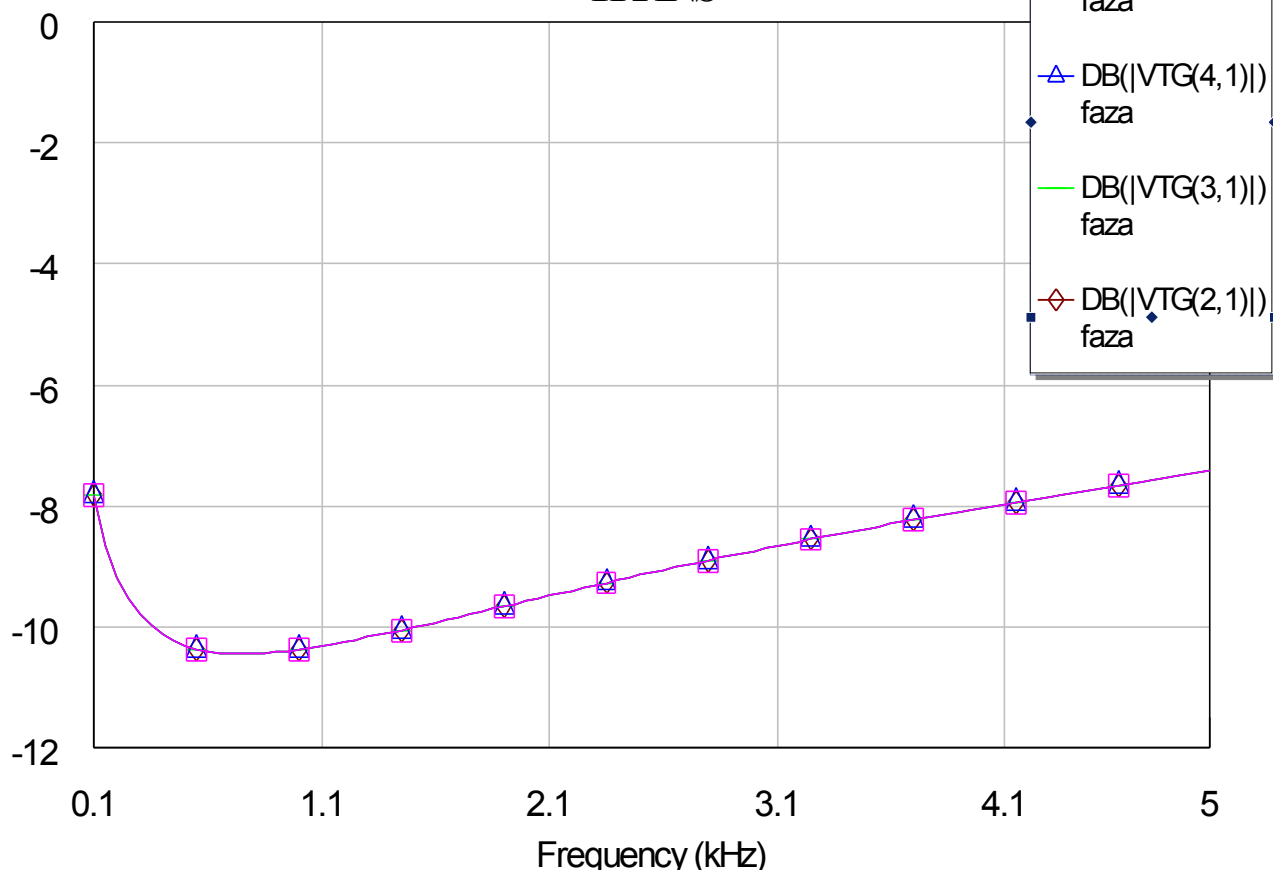


An all pass phase shift network realization for SSB work, schematic and PCB which I was used in test are down in the text. It is very important to lower gain all pass network outside wanted bandwidth practically we have to make attenuation to obtain stable network work at the frequencies over 0.5 MHz typically. This behavior was observed during simulation in freeware SPICE CAD from Linear Technology LTSpice www.linear.com and in the practical realization. All adjustment are done with DMM (digital multimeter) without built in OP AMP inside PCB all pass phase shifter. To achieve wanted tolerances all components are measured and then they had been selected and chosen to achieve nominal values with parallel combination 2 capacitors (typical accuracy is better than 1 %) . All resistors are serial combination of fixed resistor and trim pot. They were measured and adjusted with trim pots to wanted values. Next step in realization is inserting OP AMPs. OP AMPs were soldered and measuring at phase shifter done results better than worst case obtained with Monte Carlo simulation. A typical value was between 45-55 dB unwanted sideband suppression. Comparing this results with now very much favorite multiphase RC networks gave results in practical realization equal or better than with polyphase network one more thing polyphase network have relative big attenuation around 9-12 dB! .To be honest some additional work have to be done in realization to active all pass network and obtain good result but with help of ordinary DMM with C measurements possibility.

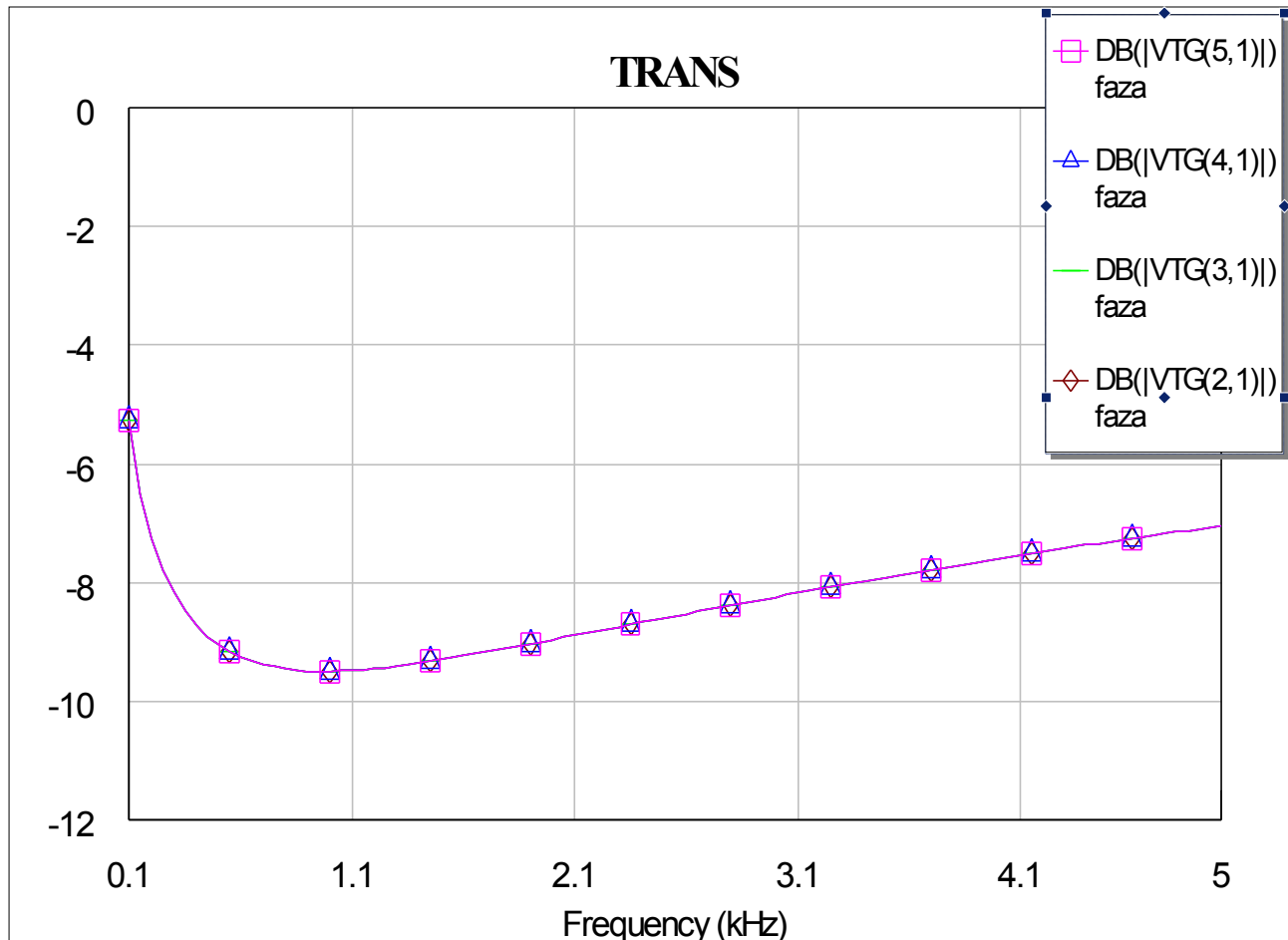
Down in text I made polyphase network simulation with 1% elements tolerances and all resistors are with next combination $24 \times 12K$, $C = (22nF + 22nF) \times 4$, $33nF \times 4$, $(10nF + 10nF) \times 4$, $10nF \times 4$, $5nF \times 4$ and $4nF \times 4$. 4 Outputs are terminated with 100K resistors which is necessary for summing. Pay attention for next observation that even if we terminate OP AMP with 10 MOhms loads we have still significant insertion loss, see diagrams below.



TRANS

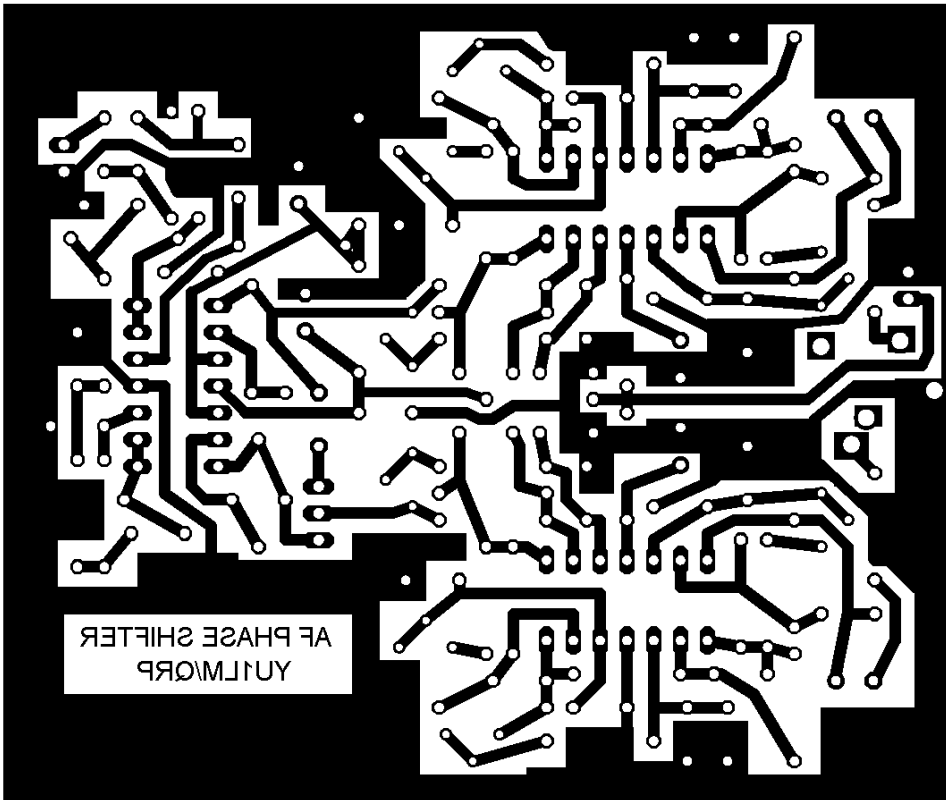


Polyphase network terminate with 100 k.loads

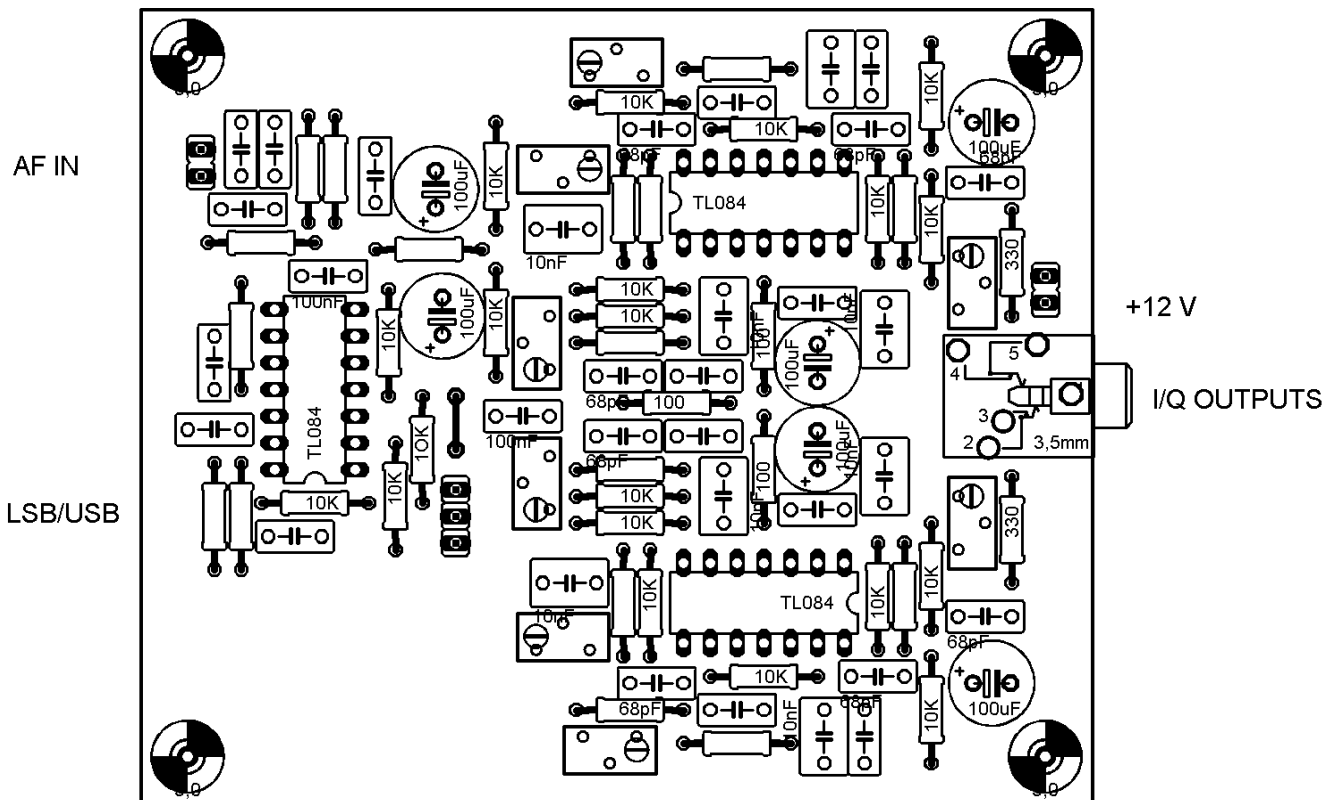


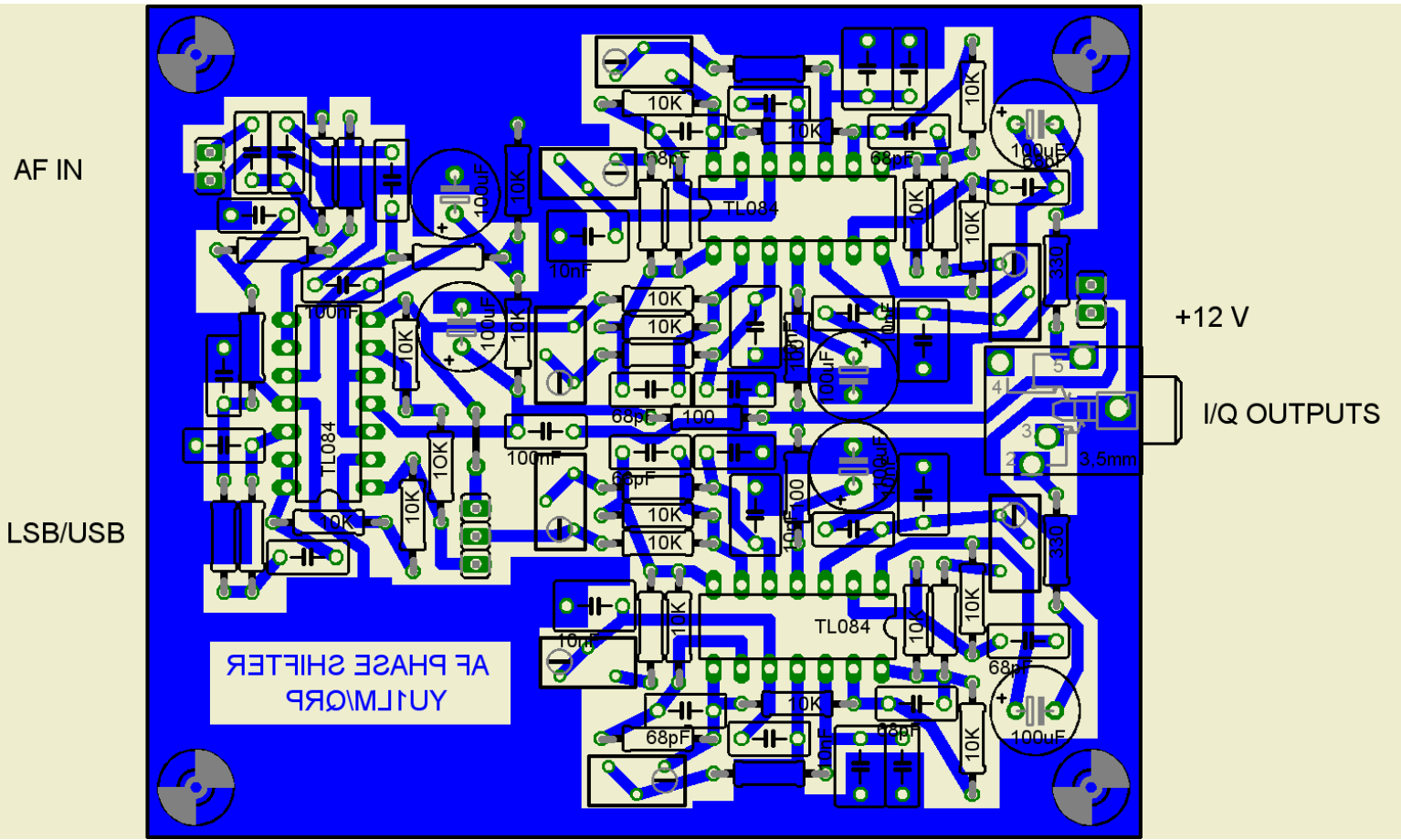
Polyphase network terminate with 10 Mohms unity gain buffer amplifier

The PCB for audio phase shift network is drawn at the pictures down. PCB is designed for max 8 order audio phase shift network. Values for unmarked resistors and capacitors are from schematics UP or from your new design in QUAD and they are frequency dependable values. Exact values are from the CAD or schematics which you choose. At the circuit input, it is good to limit used bandwidth, see values and simulations for entrance down.. There is solution down how at same PCB mount lower order phase shift networks. Network order can be even and odd. The values determine can be easily determined with software QUAD. It is very important that to strictly obey my proposal how to connect unused OP AMP. We don't like to obtain zero output in case of two equal signals are arriving at the + and - inputs of OP AMP. We don't like to test with this circuit CMRR from used OP AMP.



PCB size 90 x 75 mm





AF IN

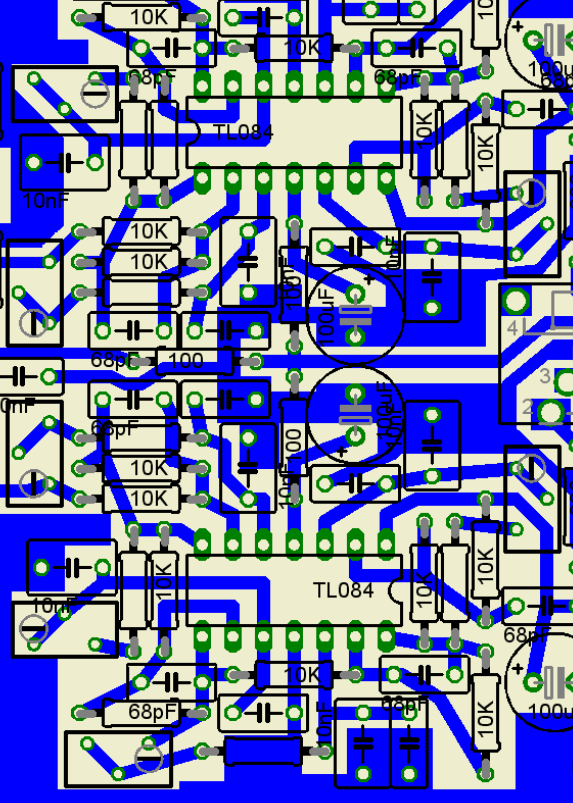
LSB/USB

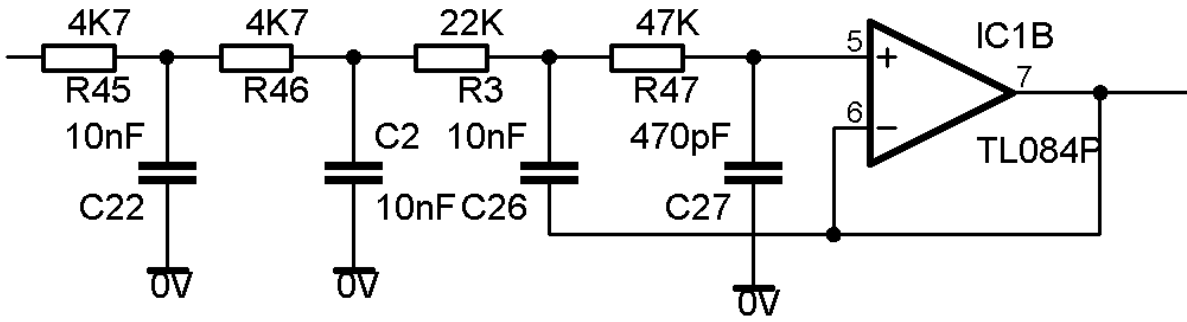
AF PHASE SHIFTER
YUTLW/RP

+12 V

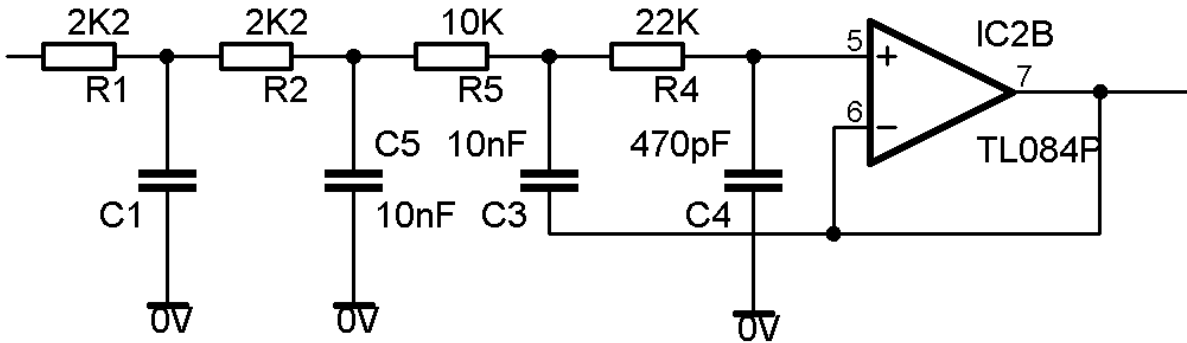
I/Q OUTPUTS

3.5mm

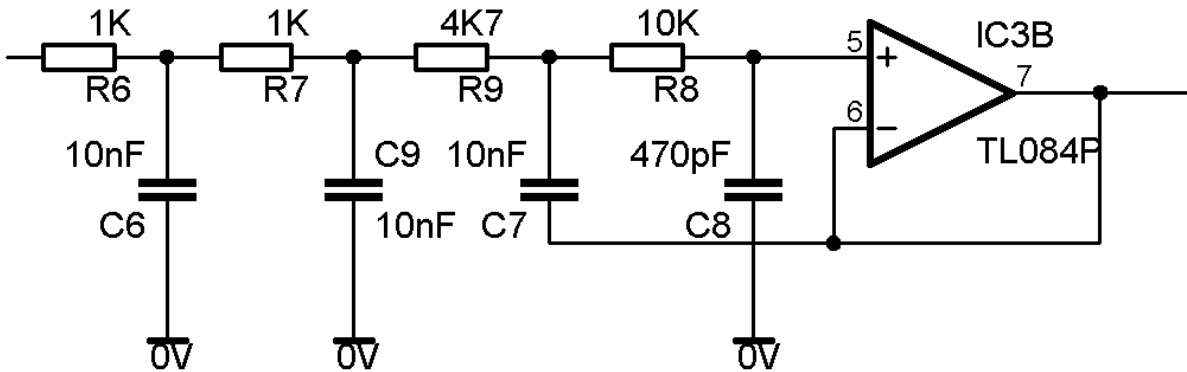




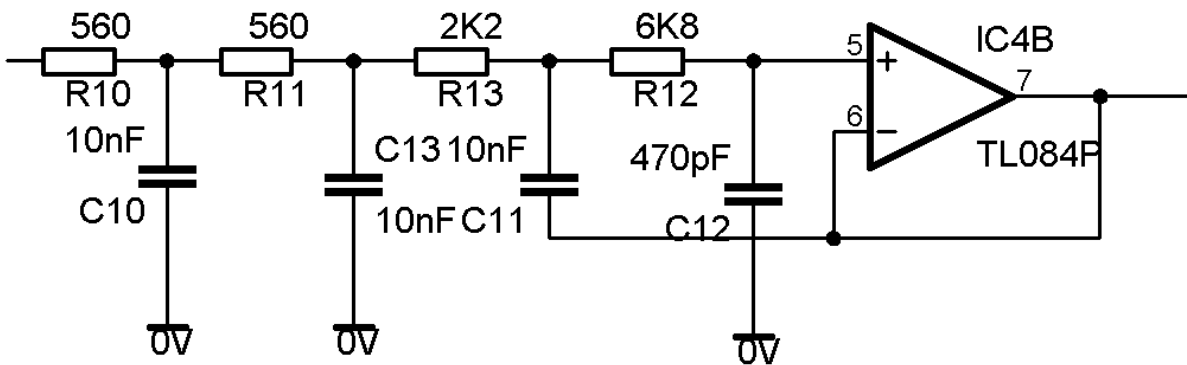
LOW PASS 2.2 kHz



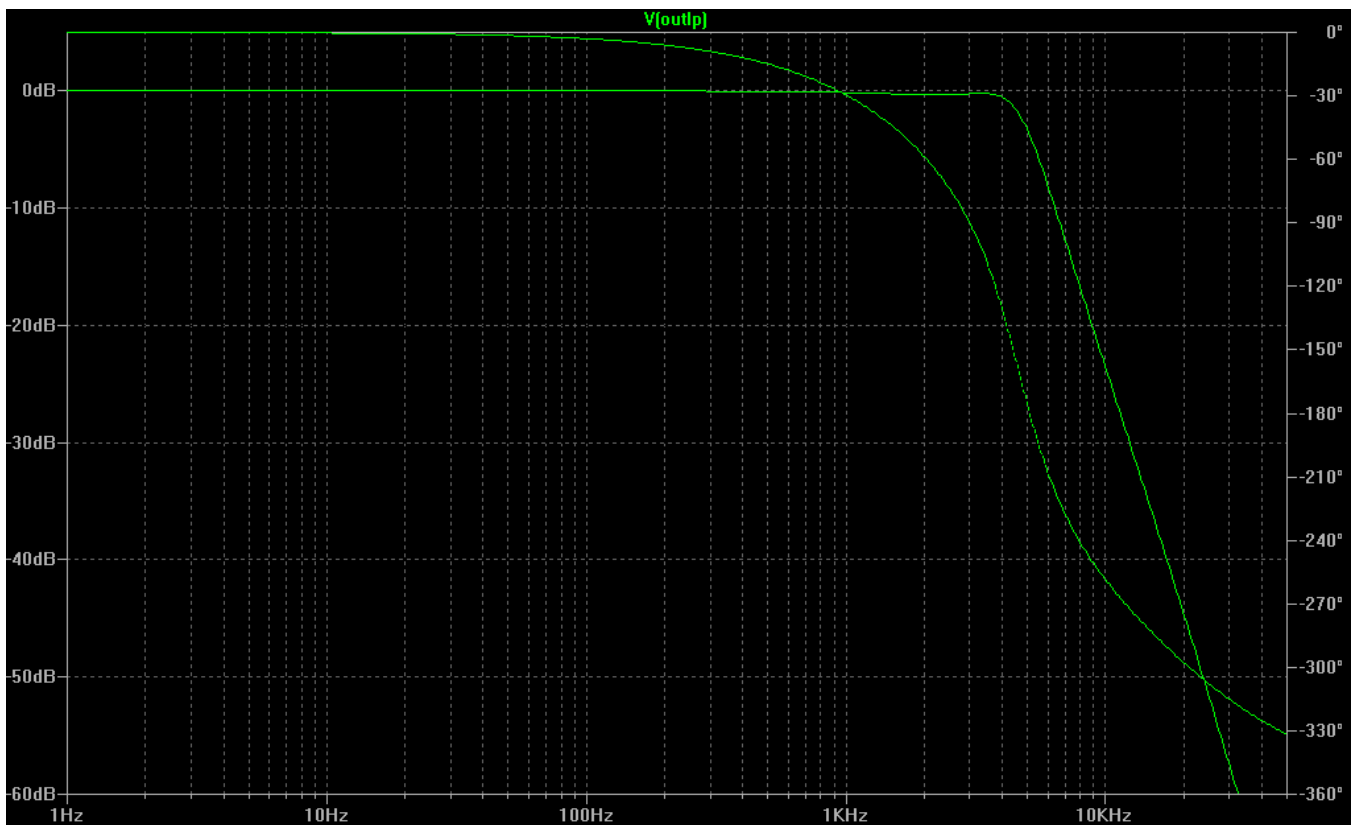
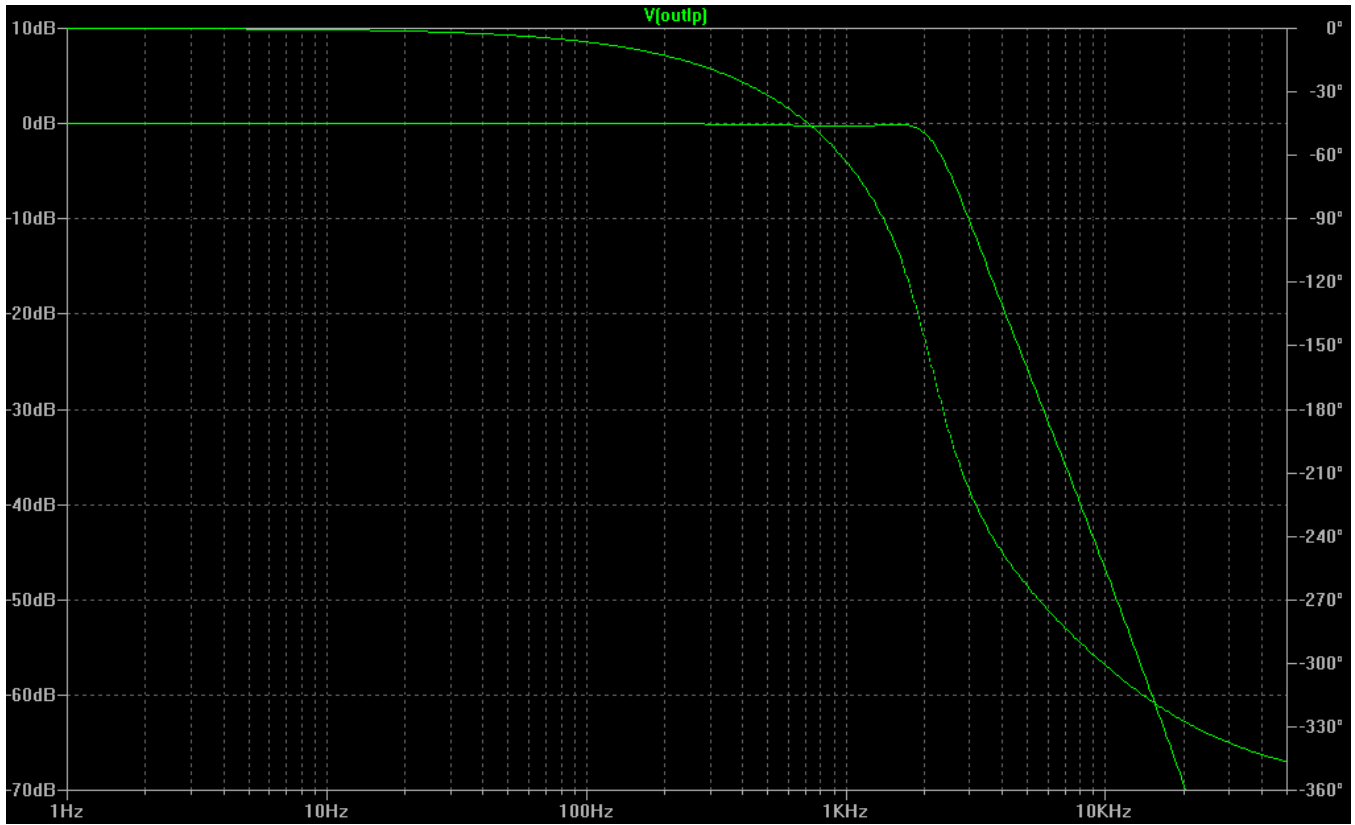
LOW PASS 3.3 kHz

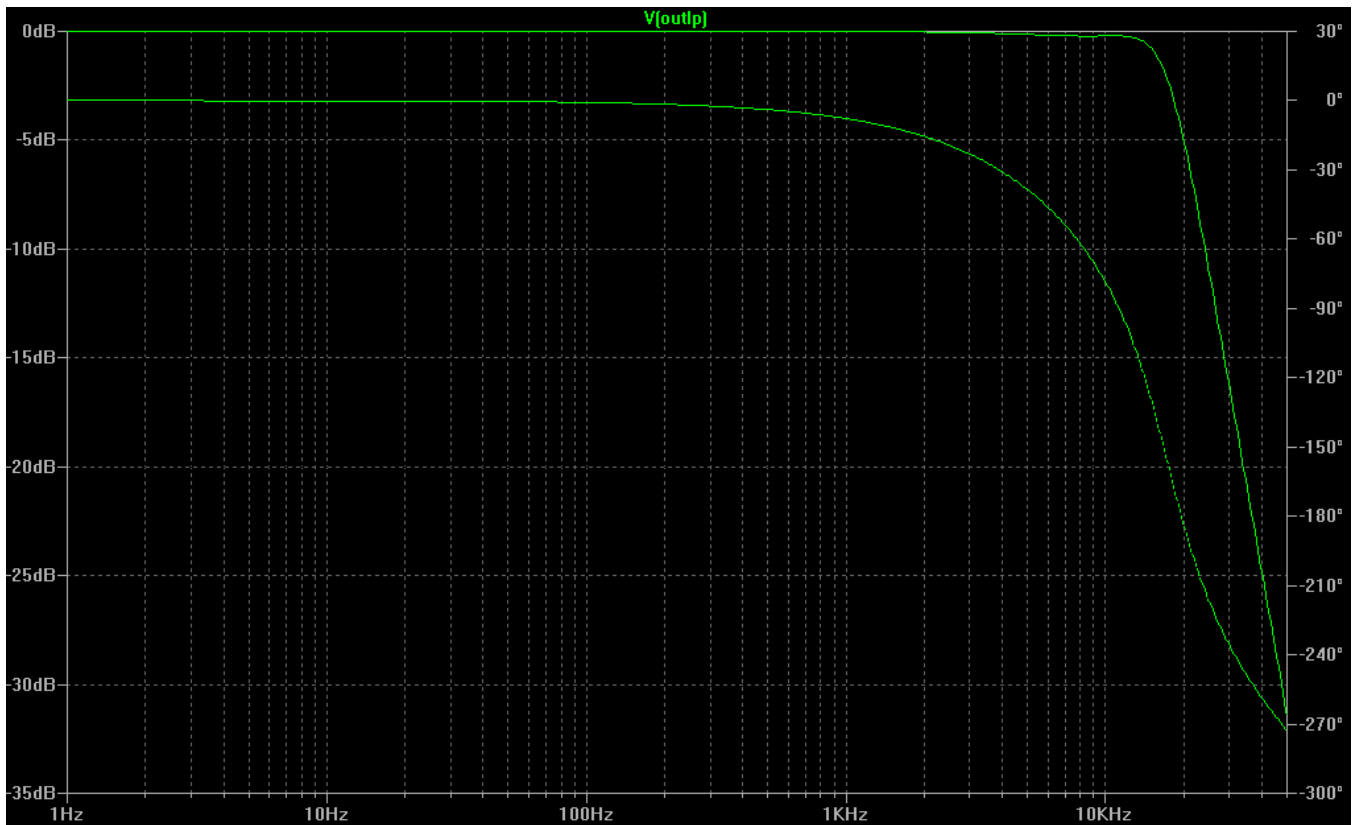
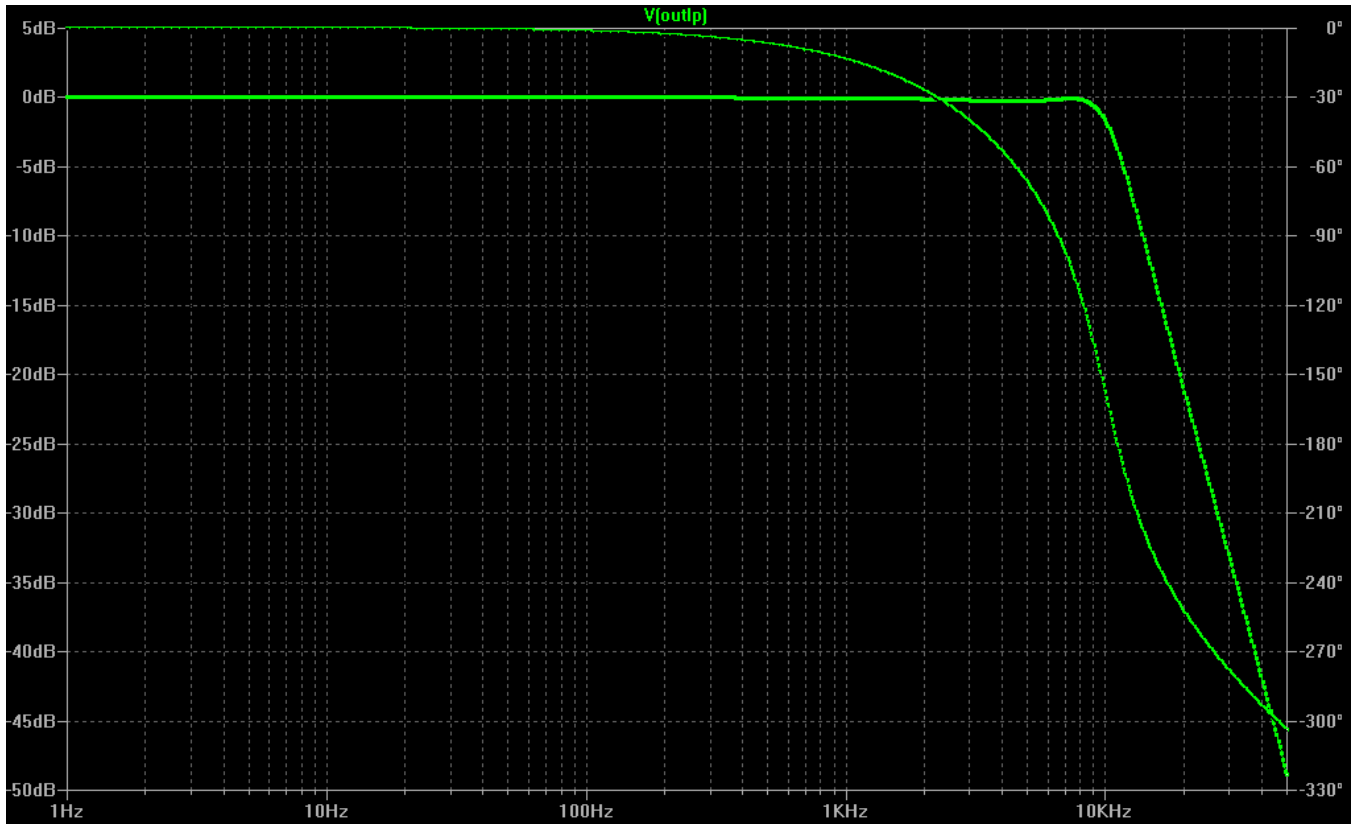


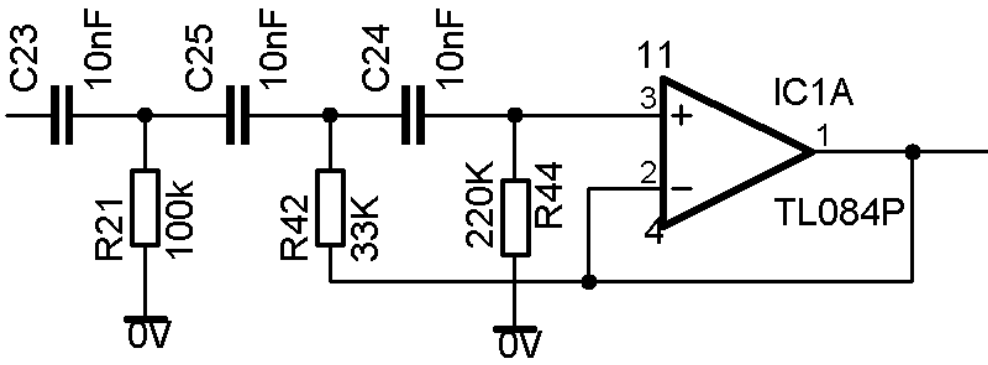
LOW PASS 10 kHz



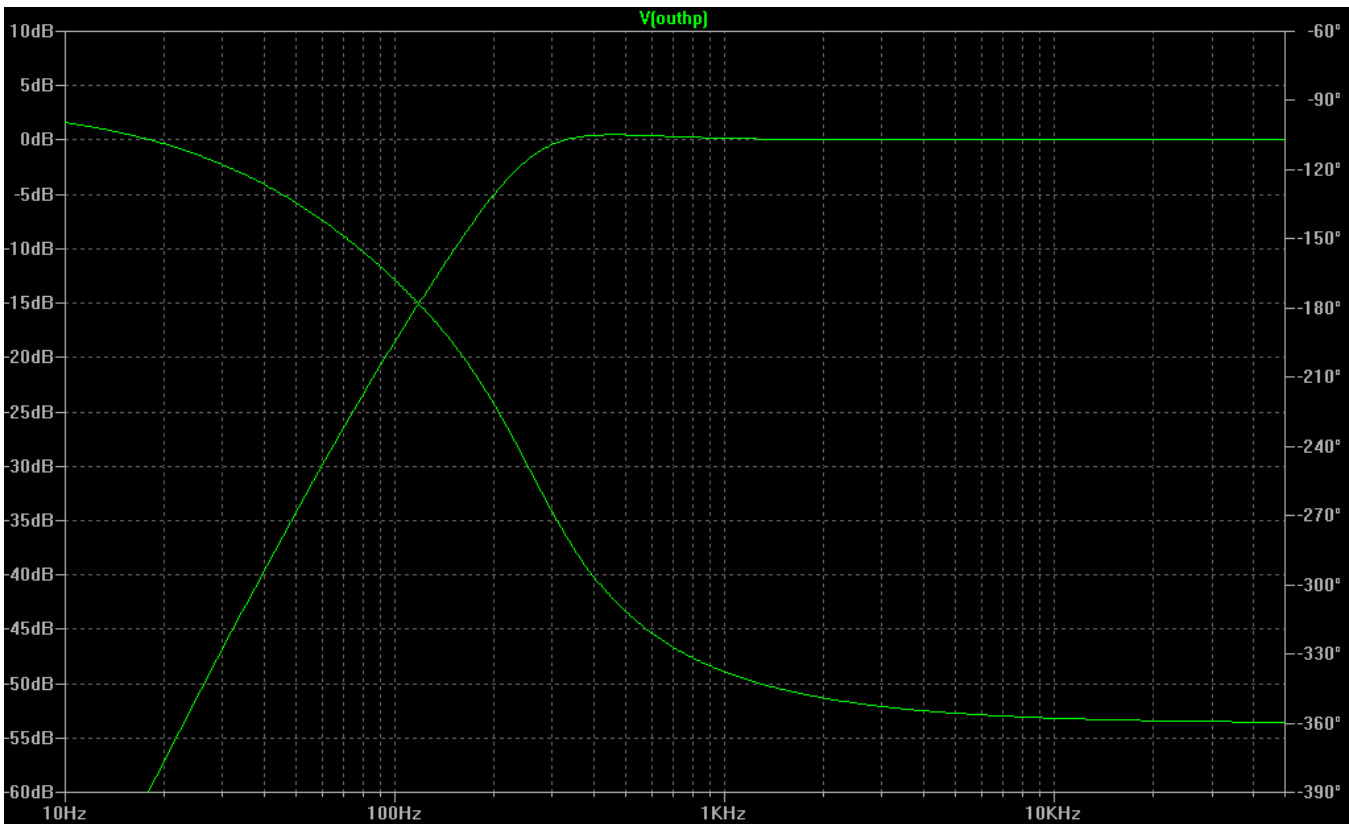
LOW PASS 18 kHz



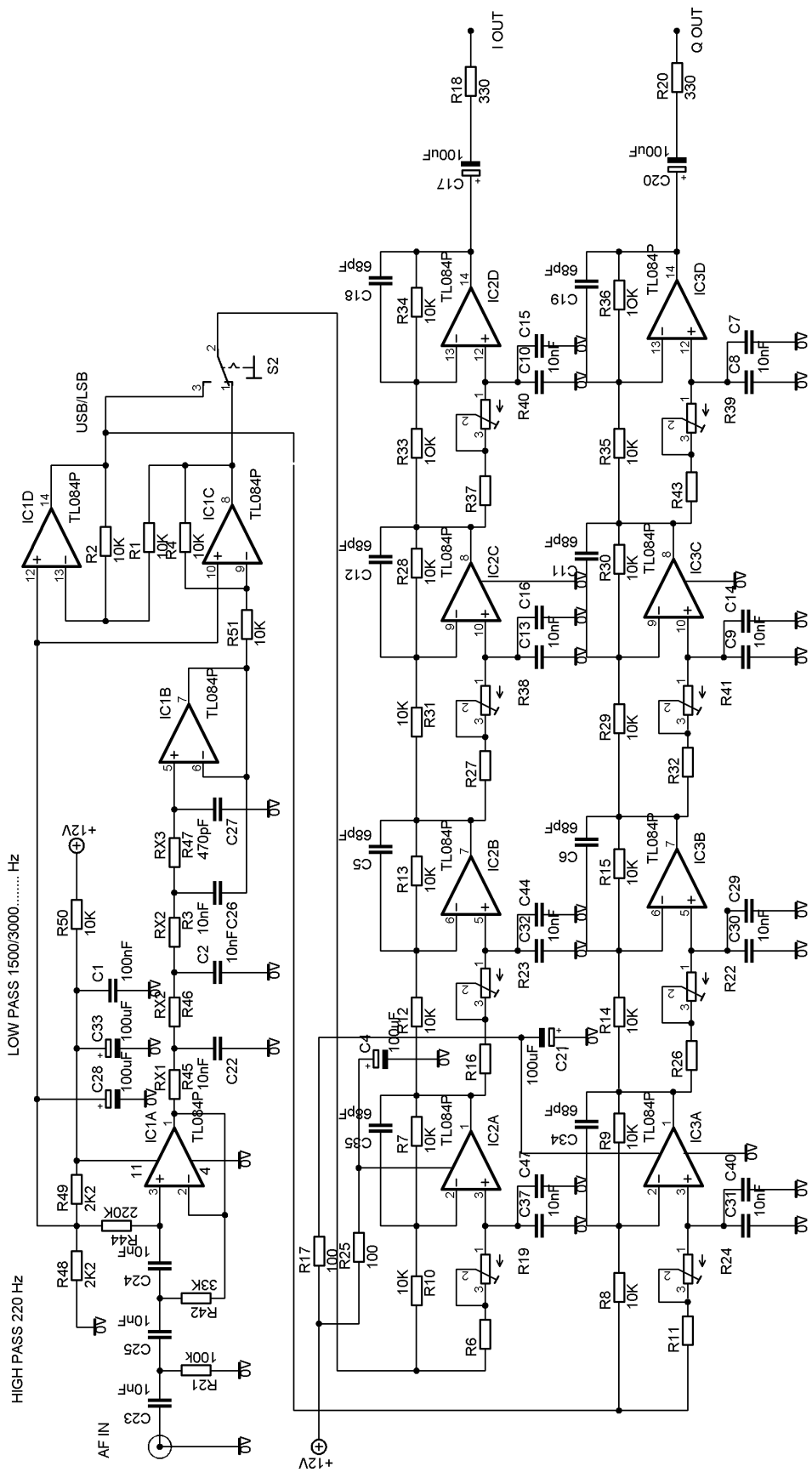




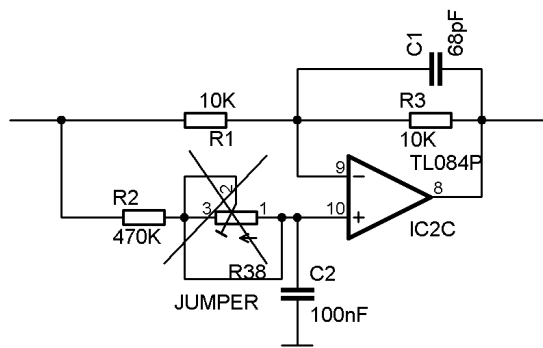
HIGH PASS 220 Hz



At last how schematic for the audio phase shift network 8 order is looking, see drawing down



AUDIO ALL PASS PHASE SHIFTER
YU1LM/QR



$$F = 1/2 \text{ Pi} \times R2 \times C2 = 6 \text{ Hz}$$

HOW TO CONNECT UNUSED SECTION FROM OP AMP I CASE AF PHASE SHIFT NETWORKS LOWER ORDER THEN 8

This is my attempt to give new “light” to the old way of obtaining audio quadrature 90 deg I/Q outputs. I wish you successfully realization and I apologize for possible mistakes which I made.

VY 73/72 Tasa YU1LM/QRP
Belgrade July 2006