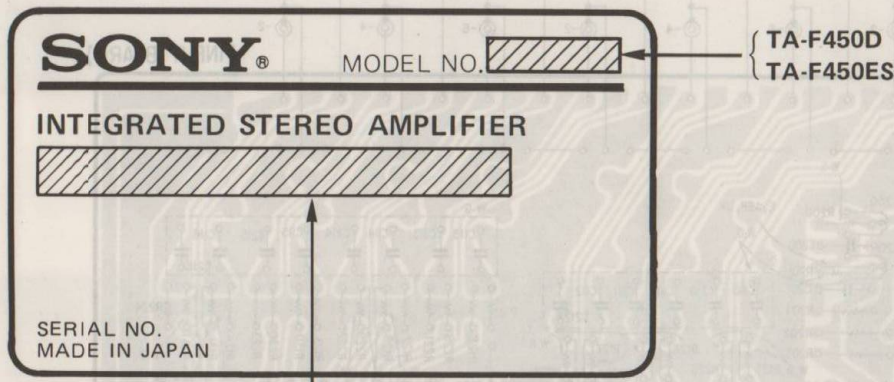


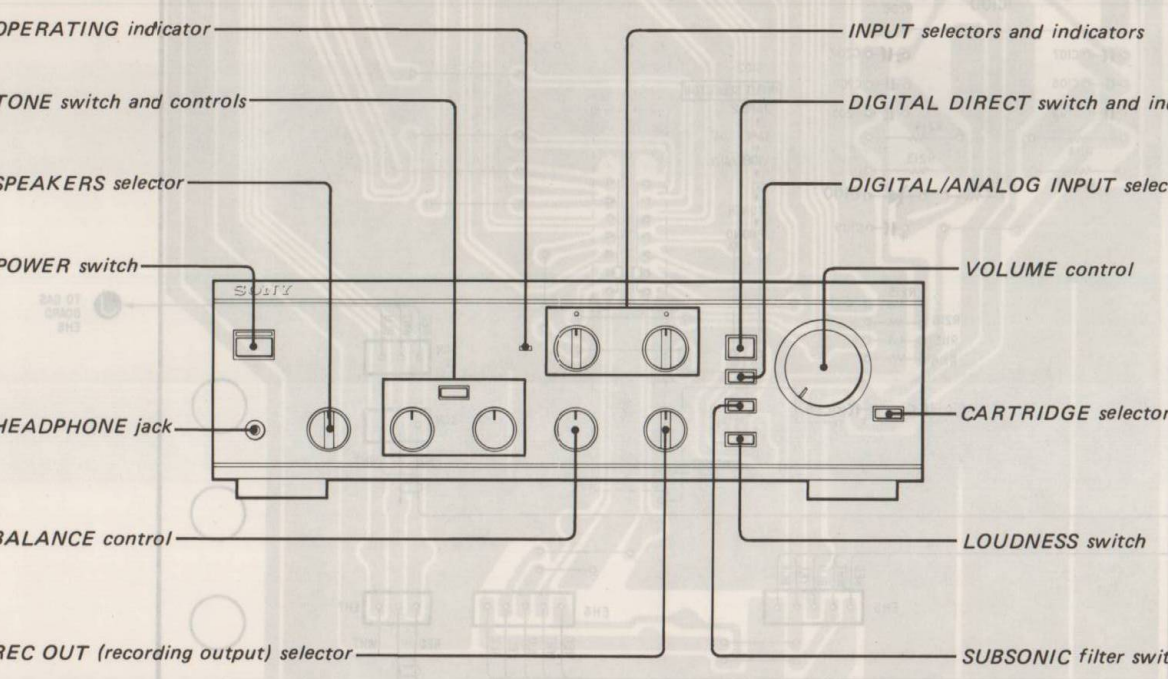
MODEL IDENTIFICATION
- Specification Label -



AEP, West Germany Model: AC: 220 V ~ 50/60 Hz 180 W
 UK Model: AC: 240 V ~ 50/60 Hz 440 W
 E Model: AC: 120/220/240 V ~ 50/60 Hz 205 W

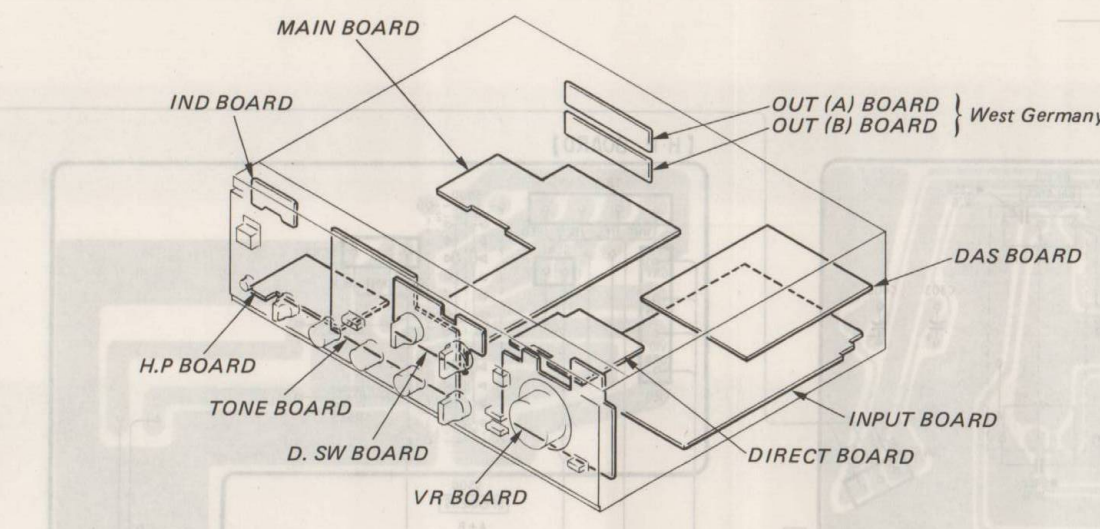
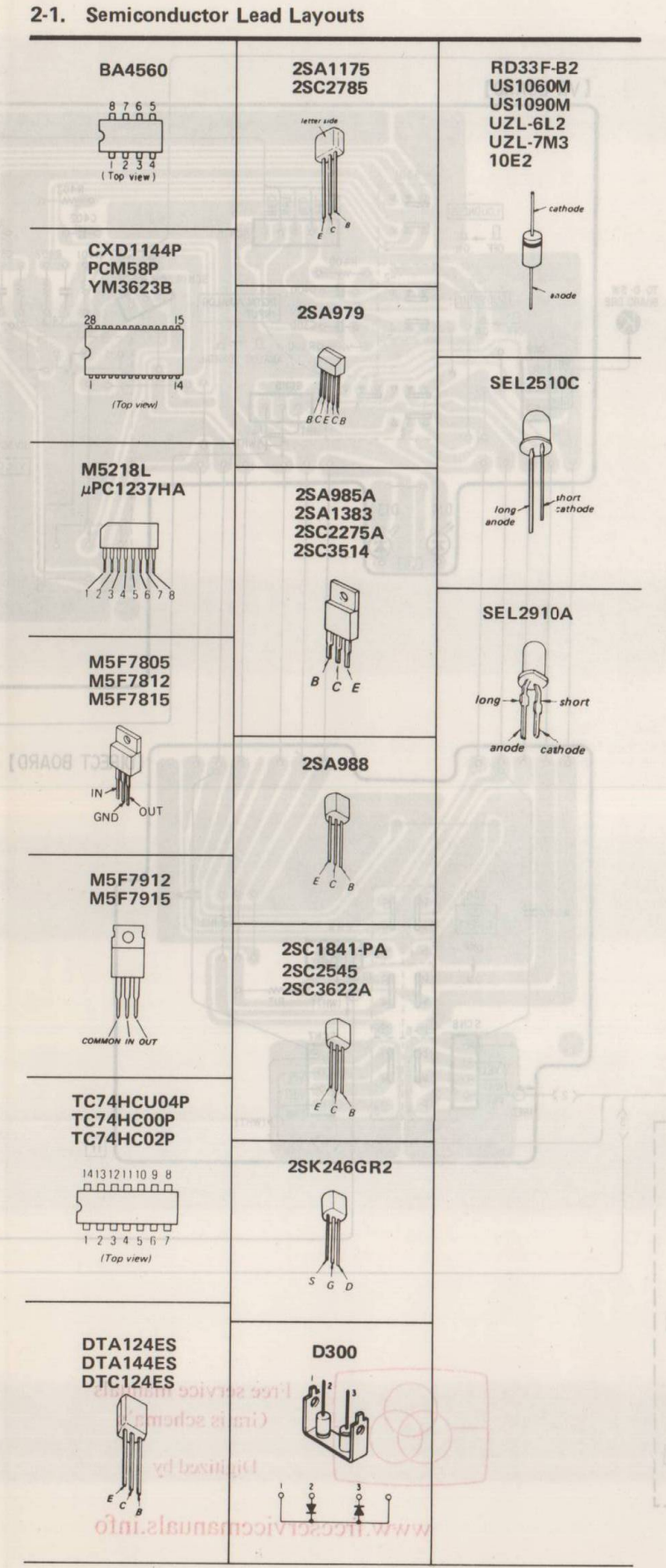
**SECTION 1
GENERAL**

LOCATION AND FUNCTION OF CONTROLS



**SECTION 2
DIAGRAMS**

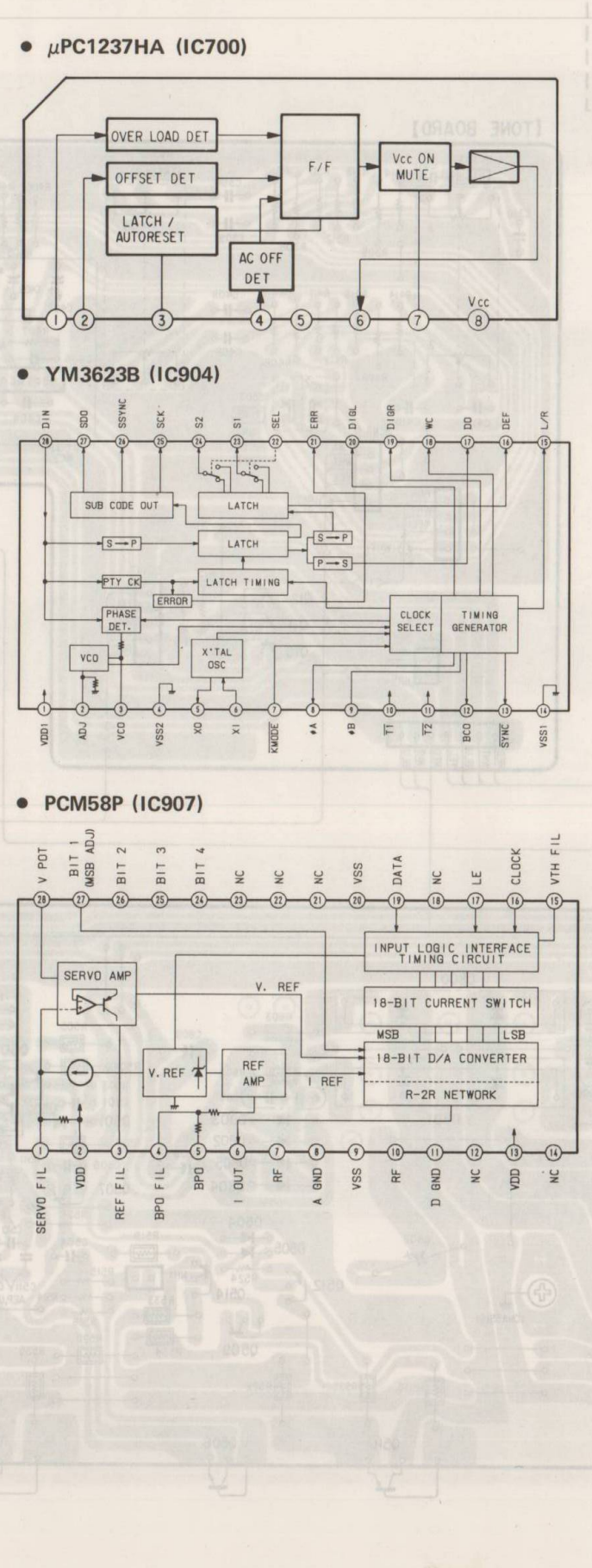
2-1. Semiconductor Lead Layouts



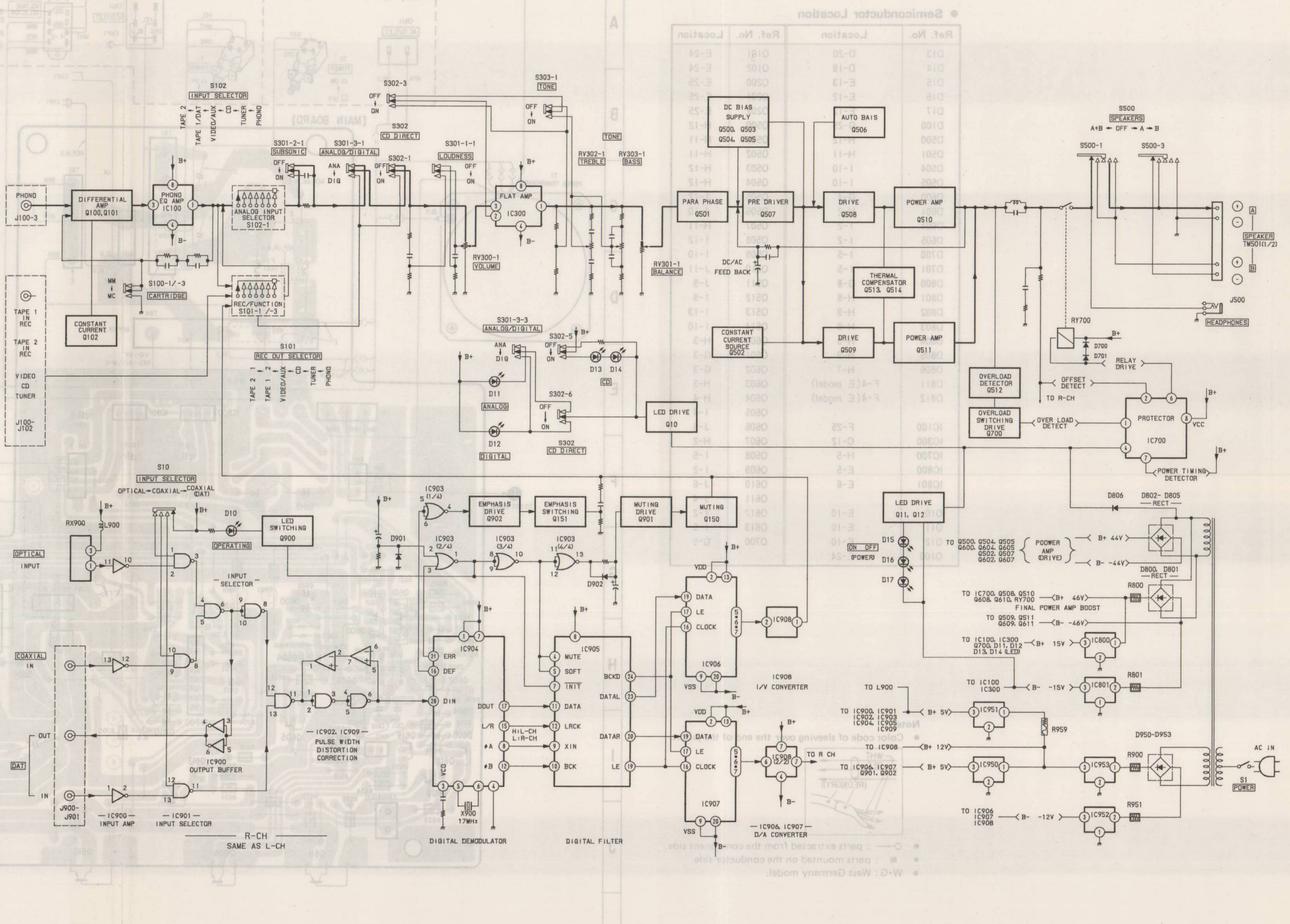
DESCRIPTION ON IC904 (YM3623B)

Pin No.	Name	I/O	FUNCTION
1	VDD1		System power supply pin. (+5V)
2	ADJ	I	Pin for adjustment of VCO frequency. No connected.
3	VCO	I/O	Pin for external capacitor of VCO.
4	VSS2		Grounding pin of VCO. Ground it together with pin (14). (Pins (4) and (14) are not connected inside.)
5	XO	O	Pin for X'tal vibrator. (16.9344 MHz ~ 20 MHz)
6	XI	I	Pin for X'tal vibrator or for an external clock signal input.
7	KMODE	I(PU)	'H': With the input at DIN (pin (24)) PLL is actuated, without it system operates with XI clock. 'L': System operates with XI clock not related with DIN input. (WAIT state)
8	φA	O	When XI clock is used, outputs XI frequency signal and when PLL operates, the signal frequency from this pin varies according to the transfer rate of DIN input data. If PLL is locked, the frequency will be Fs (input) x 384.
9	φB	O	Outputs 1/3-demultiplied signal of φA frequency. When PLL operates, signal frequency varies according to the transfer rate of DIN input data. If PLL is locked, the frequency will be Fs (input) x 128.
10	T1	I(PU)	Pin for test. No connected.
11	T2	I(PU)	Pin for test. No connected.
12	BCO	O	Bit-clock output pin for the signal from DO.
13	SYNC	O	Periodic signal output pin for the signal from DO.
14	VSS1	O	System ground. (0V)
15	L/R	O	L/R latch signal of DO output. 'H': L-channel data is output from DO pin. 'L': R-channel data is output from DO pin.
16	DEF	O	DE-EMPHASIS signal detected from user's bits. 'H': Input data is emphasized. 'L': Input data is not emphasized.
17	DO	O	Pin for 16-bit audio data output.
18	WC	O	Word-clock output pin for DO output.
19	DIGR	O	Pin for L-channel de-gitch signal output.
20	DIGL	O	Pin for R-channel de-gitch signal output.
21	ERR	O	'H': Parity error, or system is operated with XI clock. 'L': No error.
22	SEL	I(PU)	Mode select pin.
23	S1	O	Mode select pin.
24	S2	O	Mode select pin.
25	SCK	O	Pin for bit-clock for SUBCORD output.
26	SSYNC	O	Pin for synchronization signal for SUBCORD output.
27	SDO	O	Pin for SUBCORD data output.
28	DIN	I(PU)	Data input pin. (EIAJ format signal is applied.)

IC BLOCK DIAGRAM



2-3. BLOCK DIAGRAM

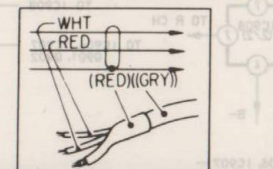
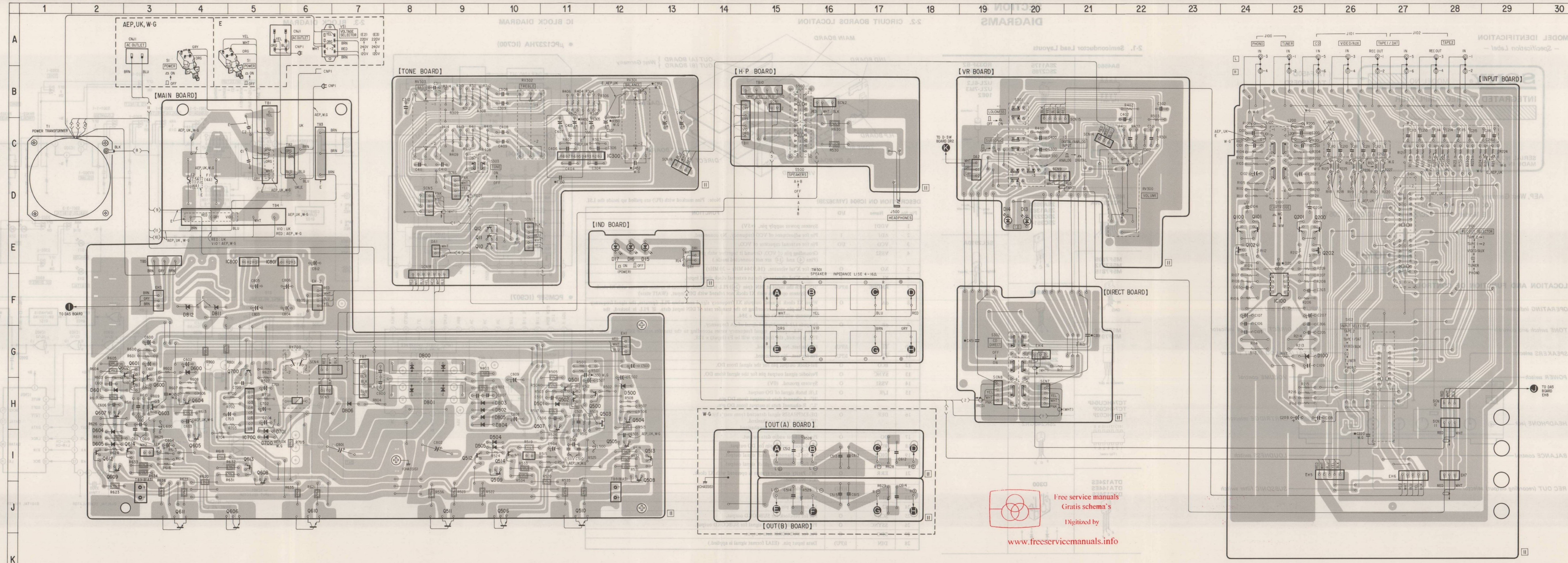


2-4. PRINTED WIRING BOARDS (MAIN BOARD)

● Semiconductor Location

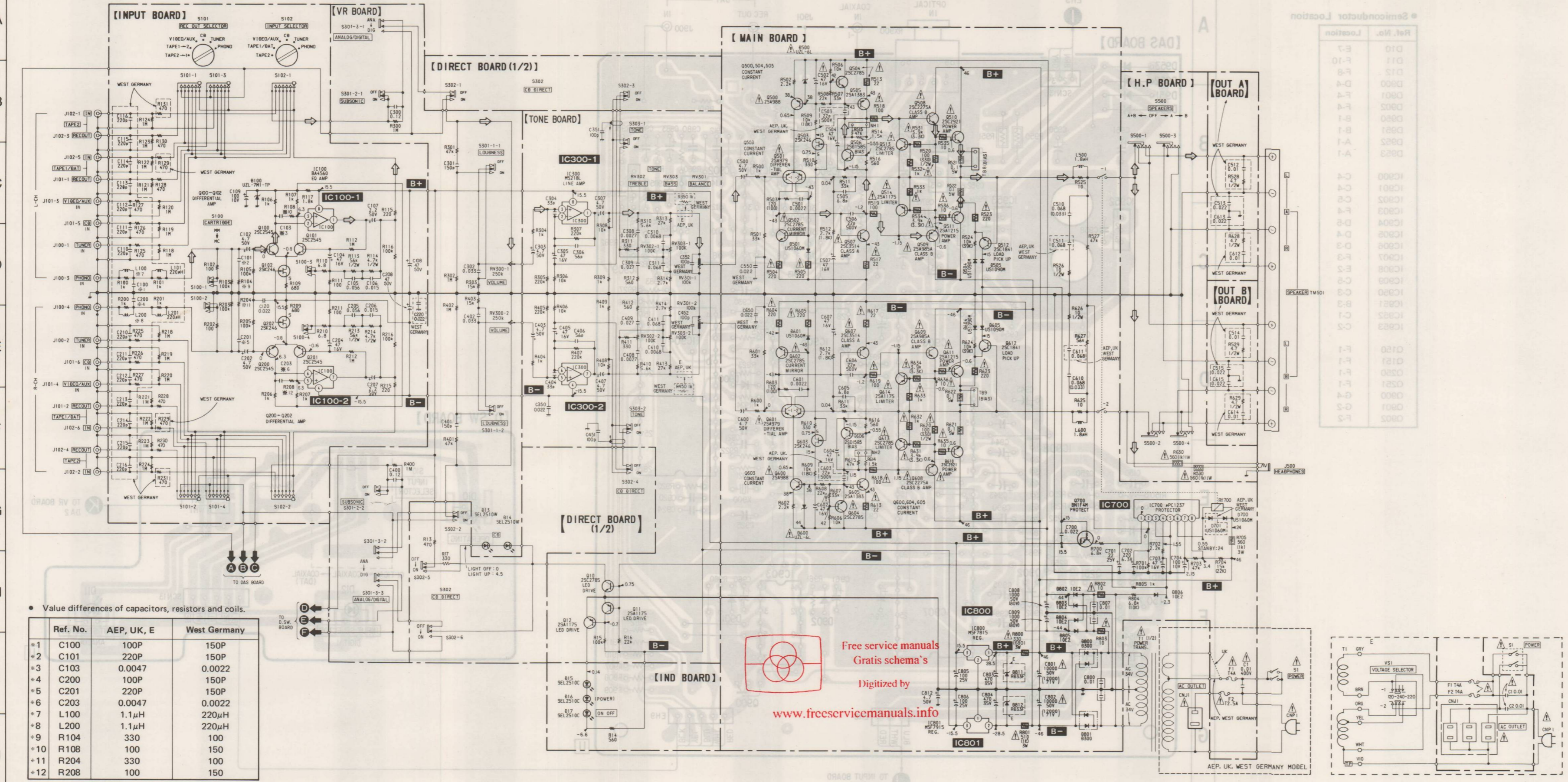
Ref. No.	Location	Ref. No.	Location
D13	D-20	Q101	E-24
D14	D-19	Q102	E-24
D15	E-13	Q200	E-25
D16	E-12	Q201	E-25
D17	E-12	Q202	E-25
D100	G-25	Q500	H-12
D500	H-12	Q501	H-11
D501	H-11	Q502	H-11
D504	I-10	Q503	H-12
D505	I-10	Q504	H-12
D600	G-4	Q505	I-12
D601	H-2	Q506	J-10
D604	I-2	Q507	H-11
D605	I-2	Q508	I-12
D700	I-5	Q509	I-10
D701	I-5	Q510	J-11
D800	G-8	Q511	J-9
D801	H-8	Q512	I-9
D802	H-9	Q513	I-13
D803	H-9	Q514	I-10
D804	H-9	Q600	H-3
D805	H-9	Q601	G-3
D806	H-7	Q602	G-3
D811	F-4 (E model)	Q603	H-3
D812	F-4 (E model)	Q604	H-4
		Q605	I-4
		Q606	J-5
		Q607	H-2
		Q608	I-5
		Q609	I-2
		Q610	J-6
		Q611	J-4
		Q612	I-2
		Q613	I-5
		Q700	G-5
IC100	F-25		
IC300	C-12		
IC700	H-5		
IC800	E-5		
IC801	E-6		
Q10	E-10		
Q11	E-10		
Q12	E-10		
Q100	E-24		

Note:
 ● Color code of sleeving over the end of the jacket.
 ○ : parts extracted from the component side.
 ■ : parts mounted on the conductor side.
 W-G : West Germany model.

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2-5. SCHEMATIC DIAGRAM (MAIN BOARD)



• Value differences of capacitors, resistors and coils.

Ref. No.	AEP, UK, E	West Germany	
*1	C100	100P	150P
*2	C101	220P	150P
*3	C103	0.0047	0.0022
*4	C200	100P	150P
*5	C201	220P	150P
*6	C203	0.0047	0.0022
*7	L100	1.1μH	220μH
*8	L200	1.1μH	220μH
*9	R104	330	100
*10	R108	100	150
*11	R204	330	100
*12	R208	100	150

Note: All capacitors are in μF unless otherwise noted, pF: μF 50WV or less are not indicated except for electrolytics and tantalums. All resistors are in Ω and 1/4W or less unless otherwise specified. Voltages are dc with respect to ground under no-signal condition. Voltage variations may be noted due to normal production tolerances. Waveforms are taken with an oscilloscope. Voltages are taken with a VOM (50kΩ/V). Signal path. Switches:

Ref. No.	Switch	Position
S1	POWER	OFF
S100	CARTRIDGE	MM
S101	REC OUT SELECTOR	PHONO
S102	INPUT SELECTOR	PHONO
S301-1	LOUDNESS	OFF
S301-2	SUBSONIC	OFF
S301-3	DIGITAL ANALOG INPUT	ANALOG
S302	CD DIRECT	OFF
S303	TOPE	OFF
S500	SPEAKERS	OFF
VS1 (E)	VOLTAGE SELECTOR	240V

Note: The bracketed numbers in the diagram are applied to the E model.

Note: The components identified by mark or dotted line with mark are critical for safety. Replace only with part number specified.

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