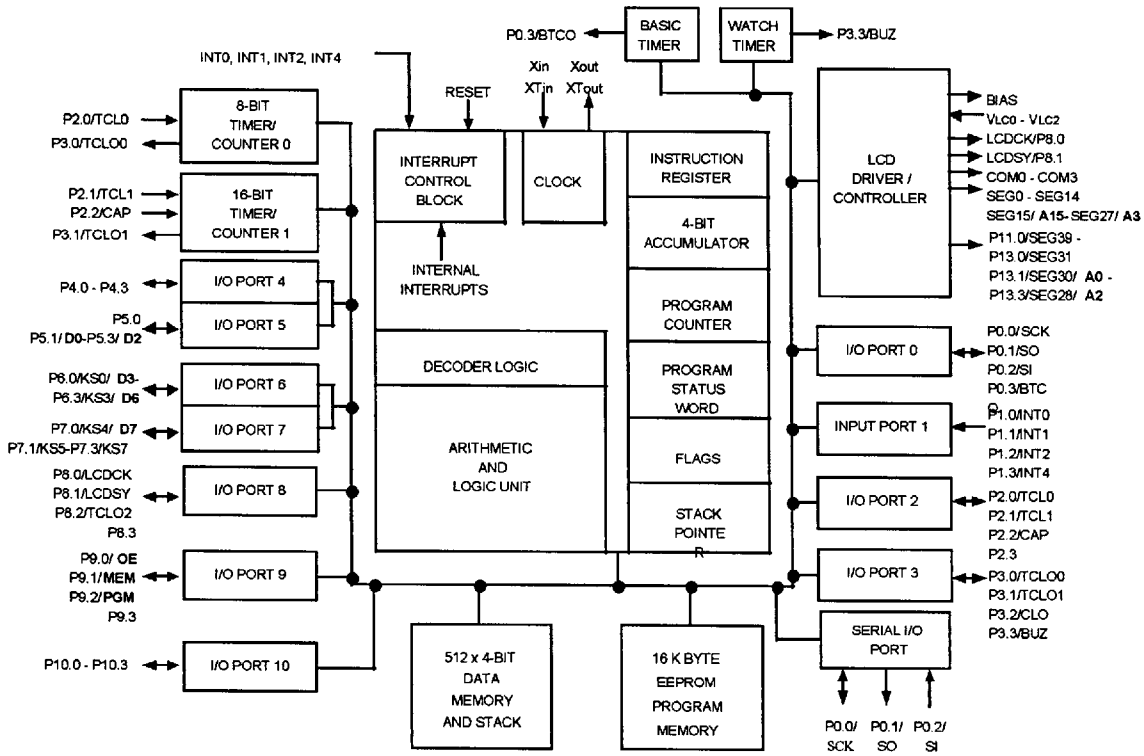
KS57P2016 MTP

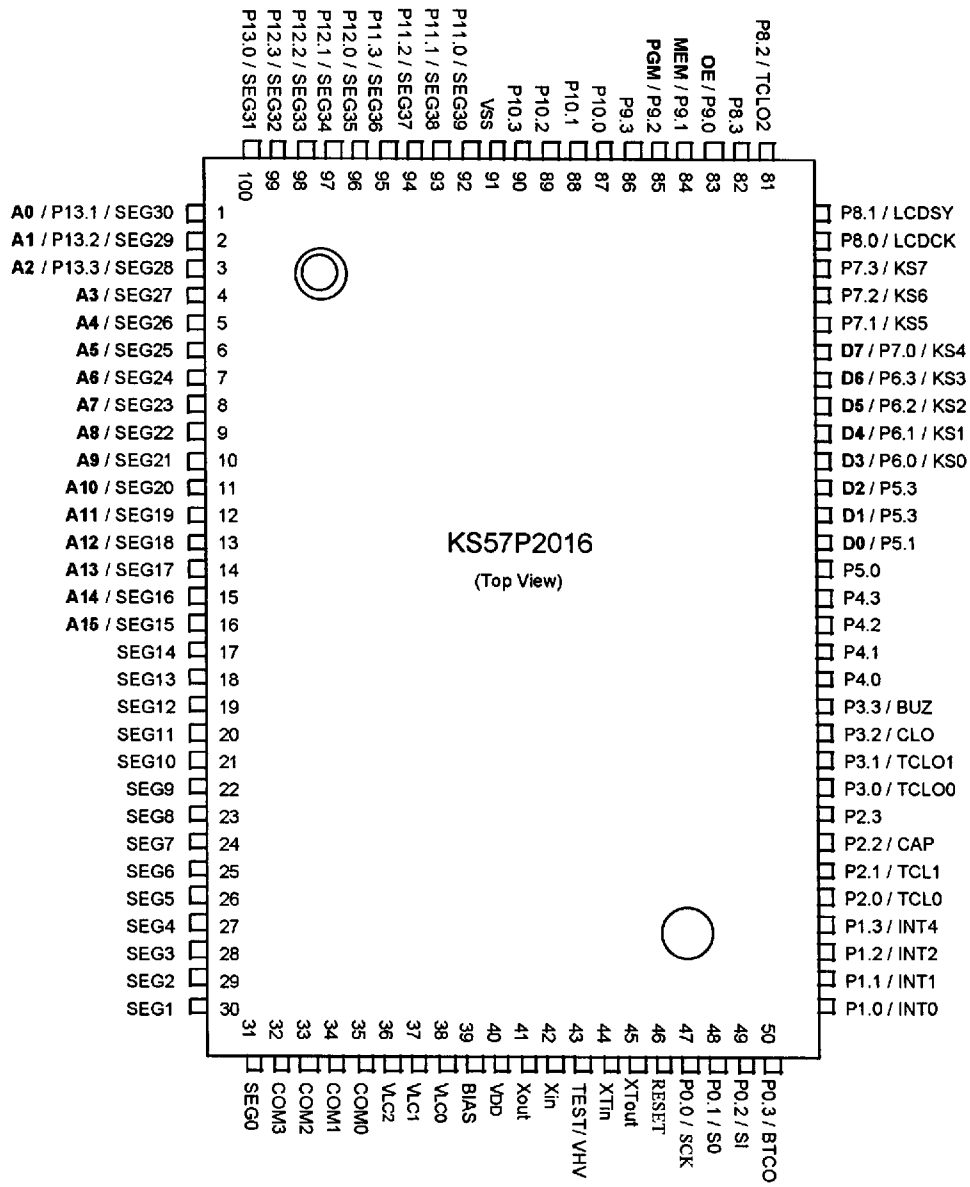
The KS57P2016 single-chip CMOS microcontroller is the MTP (Multiple Times Programmable) version of the KS57C2016 microcontroller. It has an on-chip E^2PROM instead of masked ROM. The KS57P2016 is fully compatible with the KS57C2016, both in function and in pin configuration.

Because of its simple programming requirements, the KS57P2016 is ideal for use as an evaluation chip for the KS57C2016. The MTP can be used for final EMI and latch-up, but the characteristics may vary slightly from the main chip.

BLOCK DIAGRAM



PIN ASSIGNMENTS



DESCRIPTIONS OF PINS USED TO READ/WRITE/ERASE THE E²PROM

Pin Name	Function
SEG30 / A0 – SEG15 / A15	Address lines for E²PROM read/write/erase
P7.0 / D7 P6.3 / D6 – P6.0 / D3 P5.3 / D2 – P5.1 / D0	8-bit data input/output pins for E²PROM read/write/erase
P9.2 / PGM, P9.1 / MEM, P9.0 / OE	Control lines for E²PROM read/write/erase
V_{DD}	Supply voltage pin (5 V is applied in most cases)
TEST	Voltage pin for E²PROM read/write/erase (normally V_{DD}+ 5 V)

COMPARISON OF KS57P2016 AND KS57C2016 FEATURES

Characteristic	KS57P2016	KS57C2016
Program Memory	16 K byte E²PROM	16 K byte mask ROM
Operating Voltage (V_{DD})	**4.5 V to 5.5 V**	2.7 V to 6.0 V
MTP Programming Mode	V_{DD} = 5 V ± 5 %, TEST = V_{DD} + 5 V	
Pin Configuration	100 QFP	100 QFP
E²PROM Programmability	Approximately 100 times	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When +5 V and V_{DD}+ 5 V are applied to the V_{DD} and TEST pins of the KS57P2016, respectively, the E²PROM programming mode is entered. The operating mode (read, write, or erase) is selected according to the input signals to the pins listed in Table below.

Operating Mode Selection Criteria

V_{DD}	TEST	Address	Data	PGM	MEM	OE	Mode
5 V	10 V	xxxxH	xxH	1	1	0	E²PROM read
		xxxxH	xxH	0	1	1	E²PROM write
		0002H	01H	0	0	1	E²PROM write protection
		0002H	02H	0	0	1	E²PROM read protection
		007FH	F0H	0	0	1	E²PROM erase

NOTES:
1. The character 'x' means an arbitrary number for address or data.
2. "0" means Low level; "1" means High level.

D.C. ELECTRICAL CHARACTERISTICS

(T_A = −40 °C to +85 °C, V_{DD} = 4.5V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	All input pins except as specified for V_{IH2}–V_{IH4}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 2, 6, 7, and RESET	0.8 V_{DD}		V_{DD}	
	V_{IH3}	Ports 4 and 5 with pull-up resistors assigned	0.7 V_{DD}		V_{DD}	
		Ports 4 and 5 are open-drain	0.7 V_{DD}		9	
	V_{IH4}	X_{IN}, X_{OUT}, and XT_{IN}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All input pins except V_{IL2} and V_{IL3}	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 2, 6, 7, and RESET			0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, and XT_{IN}			0.4	
Output High Voltage	V_{OH1}	V_{DD} = 4.5–5.5 V, I_{OH} = −1 mA Ports 0, 2, 3, 6–10, and BIAS	V_{DD} – 1.0	–	–	V
		I_{OH} = −100 µA	V_{DD} – 0.5			
	V_{OH2}	V_{DD} = 4.5 –5.5V, I_{OH} = −100 µA Ports 11–13 only	V_{DD} – 2.0			
		I_{OH} = −30 µA	V_{DD} – 1.0			
Output Low Voltage	V_{OL1}	V_{DD} = 4.5–5.5 V, I_{OL} = 15 mA Ports 4 and 5 only	–	0.4	2	V
		I_{OL} = 1.6 mA, ports 0, 2, 3, and 6–10		–	0.4	
		I_{OL} = 400 µA, ports 0, 2, 3, and 6–10			0.2	
	V_{OL2}	V_{DD} = 4.5–5.5 V, I_{OL} = 100 µA Port 11, 12, and 13 only			1	
		I_{OL} = 50 µA			1	
Input High Leakage Current	I_{LIH1}	V_I = V_{DD} All input pins except I_{LIH2} and I_{LIH3}	–	–	3	µA
	I_{LIH2}	V_I = V_{DD}; X_{IN}, X_{OUT}, XT_{IN}, and RESET			20	
	I_{LIH3}	V_I = 9 V, Ports 4 and 5 are open-drain			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V, All input pins except X_{IN}, X_{OUT}, and XT_{IN}	–	–	−3	µA
	I_{LIL2}	V_I = 0 V, X_{IN} X_{OUT}, XT_{IN}, and RESET			−20	
Output High Leakage Current	I_{LOH1}	V_O = V_{DD}; All output pins except ports 4 and 5	–	–	3	µA
	I_{LOH2}	Ports 4 and 5 are open-drain, V_O = 9 V			20	

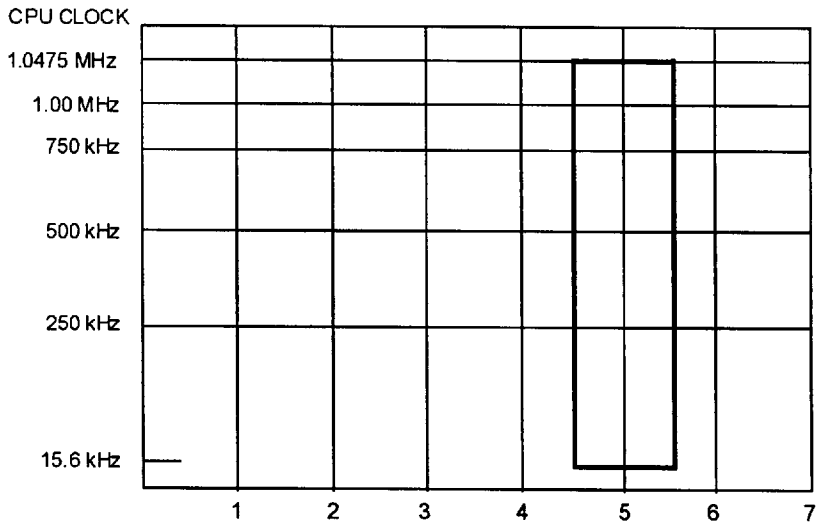
D.C. ELECTRICAL CHARACTERISTICS (Continued)

(T_A = −40 °C to +85 °C, V_{DD} = 4.5 V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Low Leakage Current	I_{LOL}	V_O = 0 V	–	–	−3	μA
Pull-up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5 V ± 10 % Port 0, 1 (except P1.3), 2, 3, and 6–10	15	40	80	KΩ
	R_{L2}	V_O = V_{DD} − 2 V; V_{DD} = 5 V ± 10 % Ports 4 and 5 only	15	40	70	
LCD Drive Voltage	V_{LCD}	–	2.5	–	V_{DD}	V
LCD Voltage Dividing Resistor	R_{LCD}	–	50	100	140	KΩ
COM Output Impedance	R_{COM}	V_{DD} = 5 V ± 10 %	–	3	6	KΩ
SEG Output Impedance	R_{SEG}	V_{DD} = 5 V ± 10 %	–	3	20	KΩ
Supply Current (1)	I_{DD1} (2)	V_{DD} = 5 V ± 10 % (3) 4.19-MHz crystal oscillator; C1 = C2 = 22 pF	–	2.5	8	mA
	I_{DD2} (2)	Idle mode; V_{DD} = 5 V ± 10 % 4.19-MHz crystal oscillator C1 = C2 = 22 pF		1.2	1.8	
	I_{DD3}	Stop mode; XT_{IN} = 0 V V_{DD} = 5 V ± 10 %		0.5	5	

NOTES:
1. Supply Current (I_{DD1} to I_{DD5}) does not include current drawn through internal pull-ups or LCD voltage dividing resistors.
2. Data includes power consumption for subsystem clock oscillation.
3. For high-speed controller operation, set the power control register (PCON) to 0011B; for low-speed, to 0000B.

STANDARD OPERATING VOLTAGE RANGE



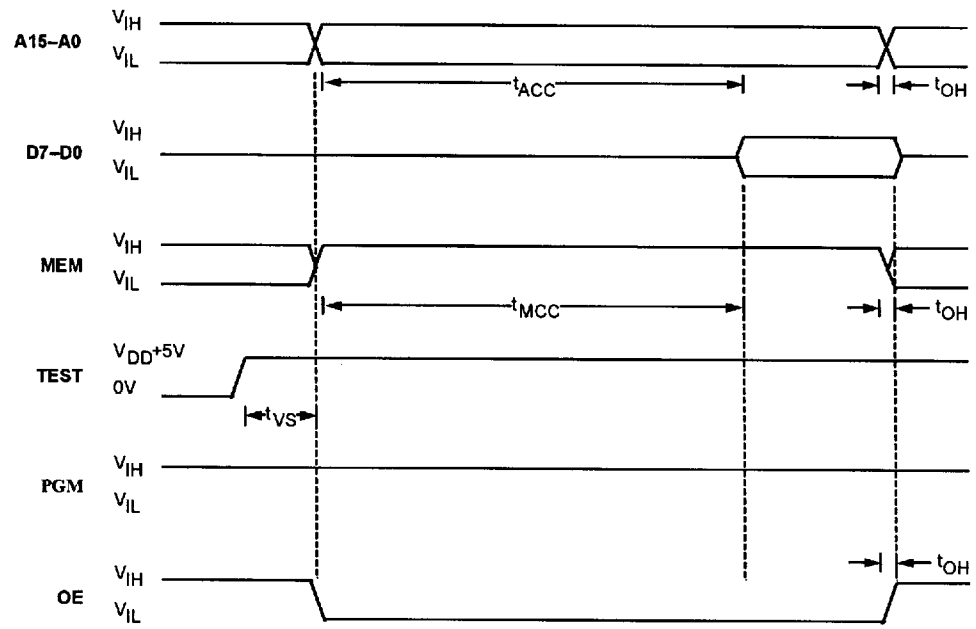
CPU CLOCK = 1/n x oscillator frequency (n = 4, 8, 64)

MTP PROGRAMMING CHARACTERISTICS

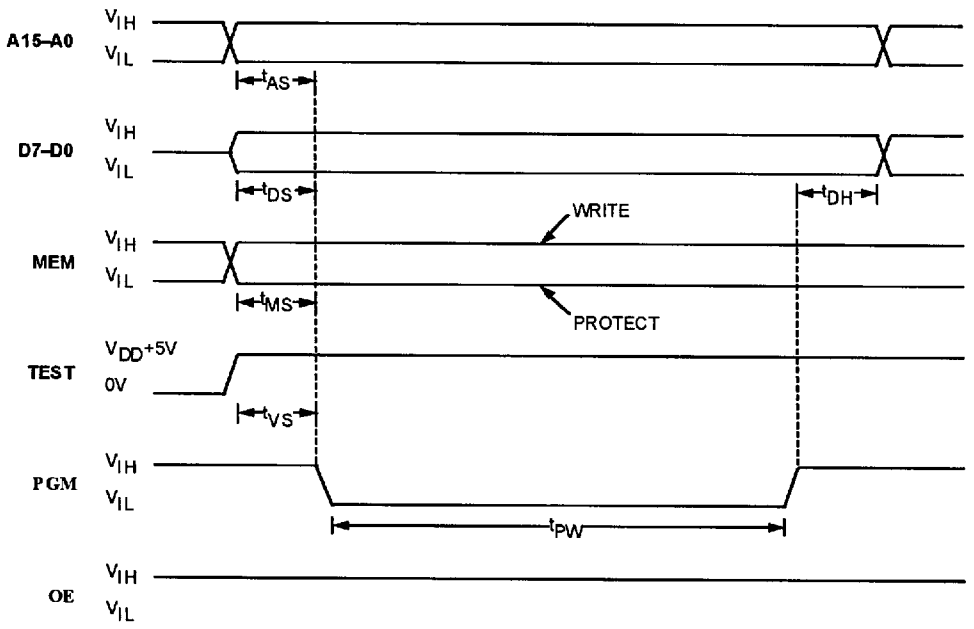
(T_A = – 40 °C to + 85 °C, V_{DD} = 5 V ± 5 %, TEST = V_{DD} + 5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TEST Setup Time	t_{VS}	—	—	2	—	μs
Address Setup Time	t_{AS}	—	—	2	—	μs
Data Setup Time	t_{DS}	—	—	2	—	μs
MEM Setup Time	t_{MS}	—	—	2	—	μs
Data Hold Time	t_{DH}	—	—	2	—	μs
PGM Pulse Width	t_{PW}	—	—	8	—	ms
Address to Data Delay	t_{ACC}	—	—	120	—	ns
MEM to Data Delay	t_{MCC}	—	—	120	—	ns
Address, MEM or OE Hold	t_{OH}	—	—	0	—	ns

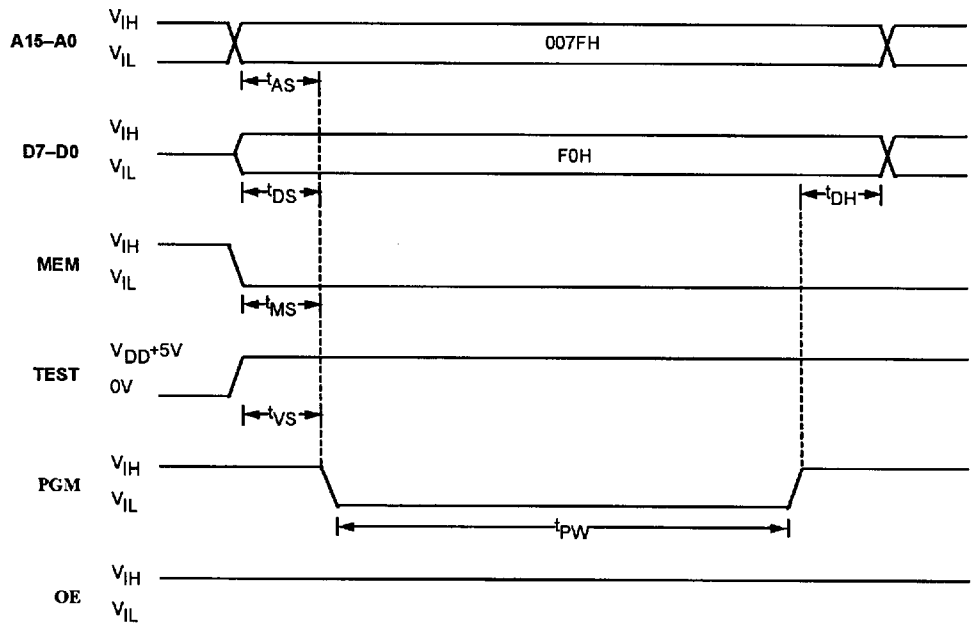
PROGRAM MEMORY READ TIMING



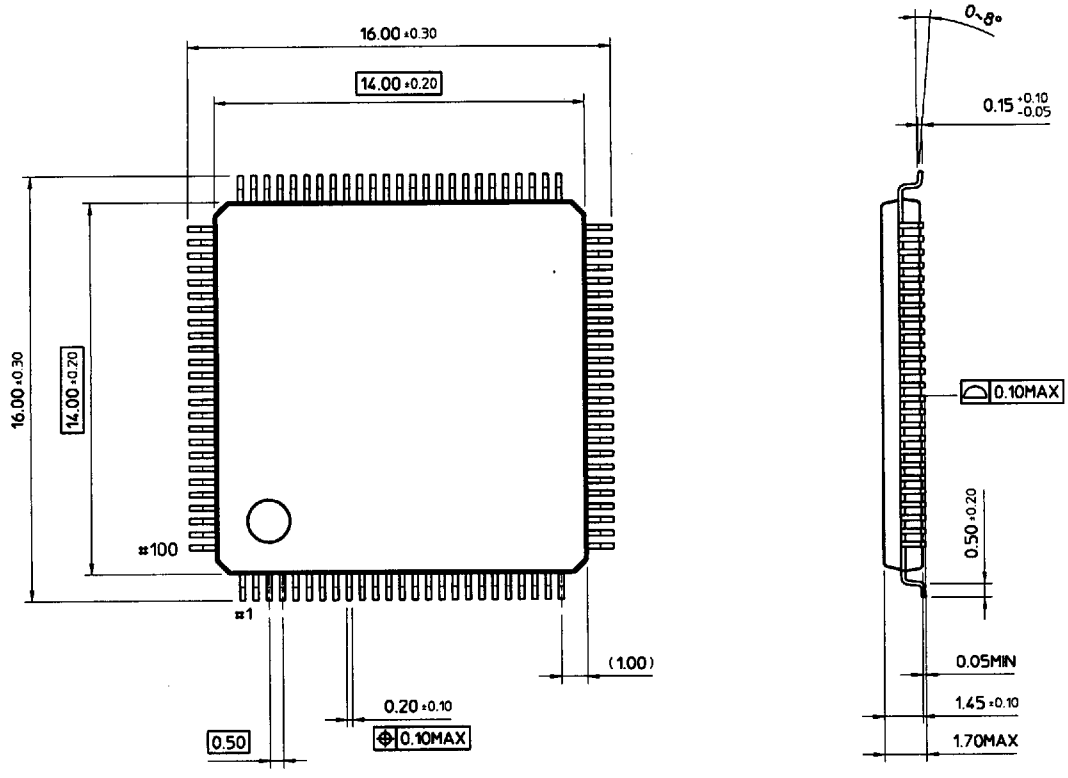
PROGRAM MEMORY WRITE TIMING



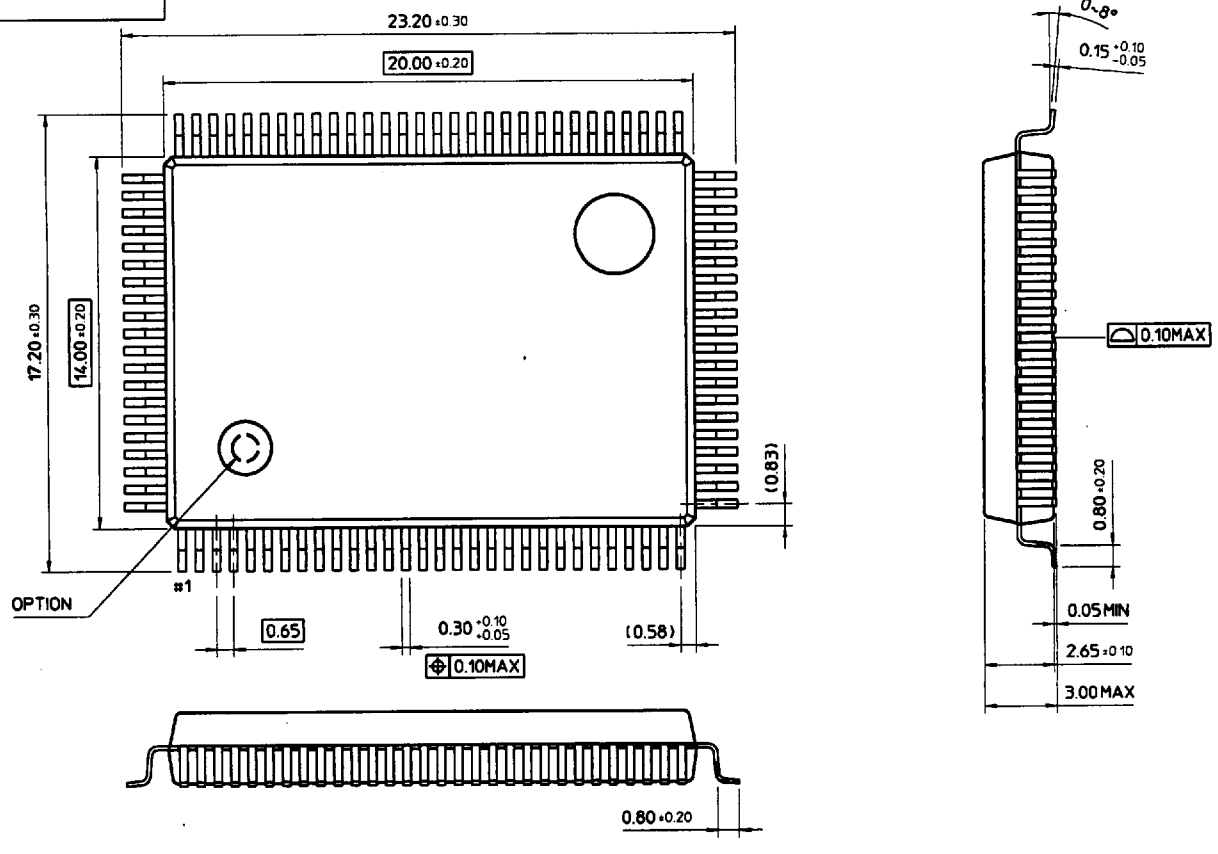
PROGRAM MEMORY ERASE TIMING



100-QFP-1414

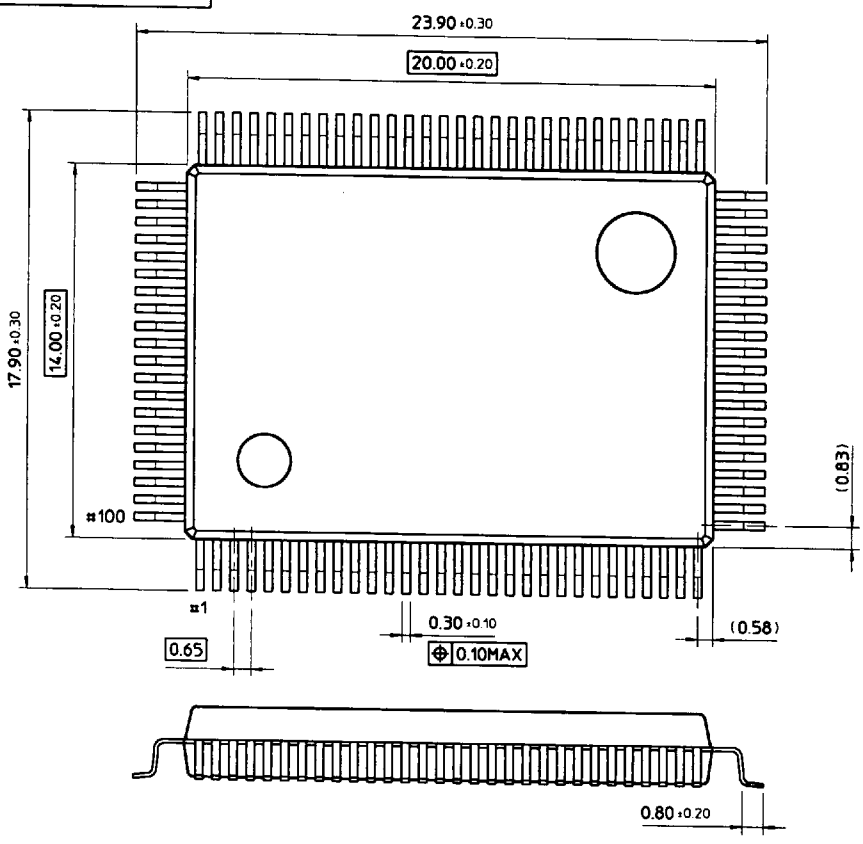


100-QFP-1420B



SAMSUNG ELECTRONICS

100-QFP-1420C



100-QFP-1420D