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An Improved Balanced, Floating Output Driver IC

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The design and implementation of an improved balanced, floating output driver IC for professional audio applications is described. It is shown that, when the most common existing designs are used to drive ground-referred loads, the grounded output is forced into current-limiting whenever the active output clips. This results in large current spikes flowing into the ground of the receiving device. Techniques used to eliminate this problem, as well as overall performance of the resulting design, are described.

0 INTRODUCTION

Output stages for professional audio products that mimic the performance of output transformers, but with lower cost, size, and weight, have been desired for many years. Such circuits are designed to accept a single-ended input voltage and to produce a differential output voltage with a low differential output impedance. They are further designed to possess a substantially higher common-mode output impedance (common-mode output impedance being defined as the impedance from either leg of the differential output to the ground or reference potential). This allows the differential output voltage to (within the limits of the power supply voltages) "float" with the common-mode voltage of the load, thus allowing the circuit to properly drive both balanced and ground-referred loads. The balanced, floating output driver topology introduced by Hay [1] in 1980 is one popular approach to this goal. This paper describes an alternative design which includes this benefit, without some of the drawbacks of the Hay design.

The first section of the paper gives a brief description of the Hay circuit, and shows the misbehavior that occurs when such circuits are clipped into single-ended loads. Subsequent sections describe the new design, how it addresses this problem, and presents the results of simulations showing various other aspects of the circuit's performance.

1 THE HAY CIRCUIT

1.1 Brief Description

The circuit described in [1] and shown in Figure 1 uses a combination of positive and negative feedback to emulate a floating voltage source [2]. It accepts a single-ended input voltage with respect to ground at terminal IN and produces a differential output voltage (equal to twice the input voltage) between nodes OUT+ and OUT-. This circuit accomplishes the desired goals with respect to differential and common-mode output impedances. Under normal operation, the

differential output impedance is determined by the sum of resistors R_{O1} and R_{O2}, which are typically between 10 and 100 ohms each. The combined positive and negative feedback effectively multiplies the values of R_{O1} and R_{O2}, increasing the common-mode output impedances. This tends to force the output currents through these resistors to be nearly equal and opposite, leaving only differential output current and little (or no) common-mode output current, as in an output transformer. The common-mode output impedances are quite sensitive to the matching of the ratios of the R/2R pairs. Mismatches of only a few percent in these resistor ratios can cause substantial mismatches in the common-mode output impedances (which affect system common-mode rejection, as will be discussed below), and can lead to instability as one or both of the common-mode output impedances may become infinite.

The problem of precise resistor-ratio matching has been addressed in monolithic implementations of the circuit by using wafer-stage laser trimming of thin-film resistors, which track very well over temperature. The circuit typically used [3], [4] is slightly modified from the original, as shown in Figure 2. A unity-gain inverter has been added to provide a balanced drive to the circuit. This equalizes the loading on R_{I1} and R_{I2}, providing improved signal balance when driving balanced loads. Resistors R_{I3} and R_{I4} provide minimum common-mode loads on the outputs, and improve the matching of the common-mode output impedances.

1.2 Clipping into Single-Ended Loads

When driving a single-ended load, as in Figure 3, under normal operation, the output currents remain nearly equal and opposite, as described above. However, if an input signal is applied to terminal IN that causes the output signal at the ungrounded output (in this case, OUT+), to exceed the maximum permitted by the power supply voltage, feedback through OA1 is no longer operational. As is expected, the differential output voltage waveform at the OUT+ output would be "clipped" at the opamp's maximum output voltage. Its output current will be the output voltage divided by the load resistance. What is not as obvious is that, while clipping is occurring, the output current of the grounded OUT- output will be quite high, typically limited only by any protective current limiting circuit in the opamp, or by the maximum opamp output voltage divided by the value of the 50-ohm output resistor. This is because the common-mode output-current control depends on combined feedback that includes both opamps. The disabling of OA1's input stage due to clipping disables the positive-feedback portion of the total loop, resulting in OA2 attempting to drive its series output resistor to twice the input voltage. The resulting current spikes must return from the receiving device to the driver circuit, and may flow through an indeterminate path, producing crosstalk into the audio signal. The results will likely be substantially more audible than brief periods of simple clipping due to their greater upper harmonic content. Also worth noting, is that, since these types of output stages have 6 dB less maximum output swing when driving a single-ended load than when driving a balanced load, clipping is more likely to occur under these circumstances.

As an illustration, the circuit in Figure 3 was simulated in PSpice using a Boyle-type macromodel of the 5532 opamp. The input stimulus was a 1 kHz sine wave with a peak voltage of 8V to drive the OUT+ output into clipping. The resulting voltage waveform at the OUT+ terminal is shown in Figure 4, and the current through R_{I2} is shown in Figure 5. Note that the peak currents out of the grounded output are limited to about 38 mA by the current limiting function built into the macromodel.

2 THE STRAHM CIRCUIT

An alternative approach to a floating, balanced output driver circuit was patented by Strahm in 1990 [5]. This topology separated the functions of differential and common-mode operation, controlling them with two different feedback loops. The differential loop is configured to force the differential output voltage to substantially equal the input voltage multiplied by some desired gain, and the common-mode feedback loop is configured to force the two output terminal currents to be equal and opposite. This at least opens up the possibility of preventing the misbehavior during clipping described above. Also, as described in the Strahm patent, precise resistor ratios are not necessary to maintain stability of the circuit.

A monolithic implementation of this concept was produced by Audio Teknology Incorporated during the early 1990's. It did not address the problem of clipping into single-ended loads because it was implemented in a way that did not preserve the functionality of the common-mode feedback loop when the differential feedback loop is broken due to voltage clipping.

3 THE NEW CIRCUIT

The new design is an improved (patent pending) implementation of the Strahm circuit that maintains control of the output common-mode current under clipping conditions while driving a ground-referred load. It also requires less active circuitry than the previous implementation.

3.1 Topology

A block diagram of the circuit is shown in Figure 6. Transconductance amplifier G_{m1} accepts a differential input voltage and delivers as its outputs a pair of differential output currents such that: $i_1 = -i_2 = g_{m1} \cdot v_{diff}$.
This transconductance amplifier, along with the identical inverting integrator stages and output buffers form a fully-differential operational amplifier. Resistors R_1 through R_4 set the differential closed-loop gain to 2. It should be noted that either terminal IN+ or IN- can be grounded, and the input signal connected in a single-ended fashion, with no loss of functionality.

Transconductance amplifier G_{m2} is a circuit that accepts a differential input voltage and delivers as its outputs a pair of matched output currents such that: $i_3 = i_4 = g_{m2} \cdot v_{cm}$.
These output currents sum with the output currents of transconductance amplifier. Note that the output currents from transconductance amplifier G_{m2} will cause both output voltages (V_{out+} and V_{out-}) to move in the same direction, while the output currents from transconductance amplifier G_{m1} will cause the two output voltages to move in opposite directions.

Resistors R_9 and R_{10} are used to sense the individual output currents. Resistors R_5 through R_8 are used to sense the common-mode output current. Thus, the voltage at the junction of R_5 and R_6 will be: $v_3 = \frac{v_1+v_2}{2}$, and the voltage at the junction of R_7 and R_8 will be: $v_4 = \frac{v_{out+}+v_{out-}}{2}$.
Noting that the currents through R_9 and R_{10} are: $i_{out+} = \frac{v_2-v_{out+}}{R_{10}}$ and $i_{out-} = \frac{v_1-v_{out-}}{R_9}$,
the input voltage to transconductance amplifier 8 will be: $v_{cm} = \frac{i_{out-} \cdot R_9 + i_{out+} \cdot R_{10}}{2} = \frac{(i_{out+}+i_{out-}) \cdot R_9}{2}$,

which is proportional to the common-mode output current: $\frac{(i_{out+}+i_{out-})}{2}$.
Negative feedback will tend to minimize the differential voltage at the transconductance amplifier's inputs. This will then tend to minimize the common-mode output current, leaving only differential (equal and opposite) currents. Resistors R_{11} and R_{12} serve to establish a minimum common-mode load for the circuit, which ensures that the negative feedback always exceeds the positive feedback.

Both transconductance amplifiers are designed to have a maximum possible output current that is achieved when the input voltage exceeds a predefined level. (This is a natural consequence of their implementations, as will be illustrated below). In order to ensure that the common mode feedback loop will remain active when the differential loop has been disabled due to clipping, the maximum output currents from transconductance amplifier G_{m2} must be made greater than the maximum output currents from transconductance amplifier G_{m1}. As an example, assume that terminal OUT- is shorted to ground, and that the input voltage v_{in} is sufficiently positive to drive v_2 to the maximum possible positive voltage allowed by the circuit power supplies. The negative feedback path via R_4 is now broken, as the voltage v_2 no longer responds to any change in the input voltage. Under such conditions, i_1 and i_2 will be at their maximum possible values (in opposite directions). Current i_1 will tend to drive voltage v_1 negative, and, if left unchecked, will cause a large current to flow through low-valued resistor R_9. However, if transconductance amplifier G_{m2} has sufficient output current capability to sink the maximum value of i_1, then the common-mode feedback loop will act to minimize the common-mode output current. Under these conditions, i_4 will be substantially equal to $-i_1$, and i_{out-} will be substantially equal to $-i_{out+}$.

3.2 Implementation

A simplified device-level schematic of the design is shown in Figure 7. The differential input- and feedback- resistors R_1 through R_4 perform the same functions as their like-numbered counterparts in Figure 6. The function of differential-input, differential-output transconductance amplifier G_{m1} from Figure 6 is fulfilled by the familiar differential pair consisting of transistors Q_1 and Q_2, their associated emitter degeneration resistors and current sources I_1 through I_3. The transconductance from the bases of Q_1 and Q_2 to either of the collectors is $g_{m1} = \frac{1}{\frac{4kT}{qI_1}+2R_{E1}}$.
Since I_2 and I_3 are each half of I_1, the maximum current available at either collector is $I_1/2$.

The function of differential-input, dual-output transconductance amplifier G_{m2} from Figure 6 is fulfilled by transistors Q_3 through Q_5, their associated emitter degeneration resistors, transistors Q_6 through Q_8, and current source I_8. Transistor Q_3 has an emitter area twice that of Q_4 and Q_5. Also, Q_3's emitter degeneration resistor is half the value of the emitter-degeneration resistors associated with Q_4 and Q_5. Thus, with no differential voltage applied between the base of transistor Q_3 and the common bases of transistors of Q_4 and Q_5, Q_3 will operate at a collector current equal to $I_8/2$, and transistors Q_4 and Q_5 will each operate at a collector current equal to $I_8/4$. Similarly, transistor Q_6 has an emitter area twice that of transistors Q_7 and Q_8. Thus, ignoring base currents, the collector current of Q_6 will be mirrored to the collectors of Q_7 and Q_8 with a gain of .5, such that each will operate at a collector current equal to one half of Q_6's collector current. The transconductance from the bases of Q_3 and Q_4/Q_5 to either of the identical

current outputs will be: $g_{m2} = \frac{1}{\frac{4kT}{qI_8}+2R_{E2}}$.

The maximum output current available from in either direction from the collectors of Q_4 and Q_5 is equal to $I_8/2$. As described above, current source I_8 is larger in value than current source I_1 in order to ensure that the common-mode feedback loop will remain active after the differential feedback loop is disabled by clipping.

Resistors R_5 through R_{12} perform the same functions as their counterparts in Figure 6. Added here is C_3, which serves to convert the common-mode loop from one which servos the common-mode output current to zero to one which servos the output common-mode voltage to zero at high frequencies. This isolates the loop from resonant loads whose response peaks would tend to degrade stability.

The inverting integrator stages from Figure 6 are implemented by emitter-followers Q_9 and Q_{10} and their associated current sources, current-source-loaded common-emitter stages Q_{11} and Q_{12}, and Miller capacitors C_1 and C_2. The buffer stages from Figure 6 are implemented with the triple-Darlington complementary emitter followers formed by Q_{17} through Q_{32}.

The circuit is designed for fabrication in a 40 V dielectrically-isolated complementary bipolar process. Additional elements not shown in Figure 7 include output-current limiting, ESD protection structures on all pins, and buffering and bias-current cancellation at the common-mode feedback inputs. All critical resistors are implemented in SiChrome thin film, for low temperature and voltage coefficients.

3.3 Application Circuits

Figure 8 is a simple representation of the new IC that is useful for behavioral analysis. The fully-differential amplifier OA1 is a block defined as having a pair of differential inputs (D_{IN+} and D_{IN-} in the figure) that affect the differential outputs such that:

$V_{out+} - V_{out-} = A_D(V_{din+} - V_{din-})$, where A_D is the differential open-loop gain.

It also has a pair of differential inputs (C_{IN+} and C_{IN-} in the figure) which affect common-mode operation such that:

$V_{out+} + V_{out-} = 2A_C(V_{cin+} - V_{cin-})$, where A_C is the common-mode open loop gain.

Any input offset voltage present due to device mismatches at the C_{IN+} and C_{IN-} inputs will be appear across resistors R_9 and R_{10}, resulting in common-mode output currents flowing through these resistors. These currents will then be converted to a common-mode output offset voltage across R_{11} and R_{12} and any external load resistance. This can result in hundreds of millivolts of output common-mode offset voltage due to only a few millivolts of input offset voltage.

The circuit in Figure 9 provides a convenient, low-cost way to prevent this, and is one of the pinout configurations for the new IC. Here the combination of the external 100 nF capacitor and 1 MΩ resistor form a 1.6 Hz highpass filter. Thus, at frequencies well below the audio band, the common-mode feedback loop works to servo the common-mode output voltage to zero, while, in the audio band, it continues to work to servo the common-mode output current to zero. The resulting common-mode output offset voltage is equal to the input offset voltage at the C_{IN+} and C_{IN-} inputs.

This input-offset could be dominated by the effects of input bias currents across the 1 MΩ resistor, R_{ext}. For this reason, as mentioned above, emitter-follower buffers, and bias current cancellation circuitry were added to these inputs.

Similar common-mode offset effects occur in devices based on the Hay circuit. IC implementations typically include provisions for ac-coupling R_6 and R_9 in Figure 2 to their respective outputs [3], [4] to minimize the common-mode output offset. Figure 10 shows an alternate pinout configuration and application circuit for the new IC that allows it to serve as a pin-for-pin compatible replacement for such devices. This works similarly to the circuit in Figure 9, except that R_7 and R_8 are each individually ac-coupled to their respective output terminals.

Both versions perform similarly. The version depicted in Figure 10 will be most appropriate for existing designs, while new designs incorporating the version in Figure 9 will benefit from the lower cost of the external components and less required PC board real estate.

4 PERFORMANCE

This section discusses the results of PSpice-based simulations of the new circuit. These simulations were run using the complete IC schematic with models from the intended production process. The application circuit was that of Figure 9. Power supply voltages were set to +/-15 V. Unless otherwise noted, the circuit was loaded with 20 kΩ in parallel with 100 pF to ground at each output.

Figures 11 and 12 show the results of a transient simulation driving the circuit with a 8 V-peak, 1 kHz sine wave, with the OUT- terminal grounded. Figure 11 is the expected clipped voltage waveform at the active OUT+ terminal, and Figure 12 is the current from the grounded OUT- terminal, which remains under control. The slight tilt to the clipped portion of the current waveform is due to the ac coupling of the common-mode feedback loop.

The common-mode rejection performance of a balanced driver-receiver system can be modeled as a Wheatstone bridge [6], as shown in Figure 13. R_{CMO1} and R_{CMO2} are the common-mode output impedances of the driver, and R_{DO} is the driver differential output impedance. R_{CMI1} and R_{CMI2} are the common-mode input impedances of the receiver. There may also be a receiver differential input impedance shunting R_{DO}, but as R_{DO} is usually the lower value by far, it dominates the performance. Though R_{DO} is not shown in [6], it is a necessary addition to model driver circuits, like the Hay circuit and the new design, that have differential output impedances that are much less than the sum of the common-mode output impedances. The low differential output impedance has the benefit of desensitizing the common-mode rejection performance to mismatches in the common-mode output impedances.

The differential output impedance in the new design is essentially the sum of R_9 and R_{10}. The common-mode output impedances are determined by (referring to Figure 9) loading resistors R_{11} and R_{12} and the feedback-multiplied values of R_9 and R_{10}. However, they are sensitive to the ratios of R_1 to R_3 and R_2 to R_4. Mismatches here result in differential conversion of the common-mode input voltage, translating to a mismatch in the common-mode output impedances.

Overall system common-mode rejection performance is also quite sensitive to the receiver common-mode input impedances [6]. Making these as high as possible desensitizes the bridge to mismatches in the common-mode output impedances. It should also be noted that, to obtain

maximum common-mode rejection ratio (CMRR), the driver IC must be driven from a low source impedance. Any source resistance appears in series with R_1 in Figure 9, and degrades the ratio match between R_1/R_3 and R_2/R_4. This is also true of the devices based on the Hay circuit.

Figure 14 shows the application schematic used to assess system common-mode performance. Monte-Carlo analysis was run using typical distributions from the intended production process. Two sets of 100 runs each were run for common-mode input impedances of 18 kΩ (typical of existing four-resistor differential-amplifier line receiver ICs) and 1 MΩ. The results are illustrated Table 1. Similar results are expected from existing Hay-based ICs, based on their data-sheet specifications. Note that these results are for an *ideal* receiver with perfectly matched common-mode input impedances. The worst-case results for the 18 kΩ case exceed the specifications of some 4-resistor differential-amplifier line receiver ICs, because the overall CMRR performance is being dominated by mismatches in the common-mode output impedances of the driver. This clearly points out the benefits of using a receiver of the type described in [6], with bootstrapped common-mode input impedance.

Table 2 shows typical results of simulations for other performance parameters. Total harmonic distortion performance holds up well even when loaded with a 600 Ω single-ended load. This is due, in part, to the use of the triple-darlington output buffer stage.

Output noise is lower than existing ICs based on the Hay circuit, primarily due to lower thermal noise from fewer, lower-valued resistors. The 5 kΩ input impedance of the new design is lower than the 10 kΩ that is typical with existing devices, but this was deemed acceptable as these circuits are typically driven directly from opamp outputs.

The output slew rate performance is very similar with balanced and single-ended loads. Particular attention was paid to ensuring that the slewing behavior was symmetrical under both conditions.

The output current limit is typically 70 mA at an ambient temperature 25° C, and decreases with increasing temperature. It remains well above the 44 mA peak current requirement established in [7] throughout the IC's -40° C to +85° C operating range. This value was based on driving 1000 feet of cable, terminated in 600Ω, to +26 dBu levels with music signals.

The device is designed to operate from minimum supply voltages of +/- 4V over its operating temperature range, and will hold up at even lower supply voltages at higher temperatures, where junction voltages are smaller. This aids in ensuring ample time to sense the loss of power supply voltage in an audio product, and mute, before the output driver ceases proper operation.

5 CONCLUSIONS

A new balanced, floating output driver IC design for professional audio applications was described. It was shown that the new design does not misbehave when clipped into a single-ended load, as do existing designs.

The new design also allows a method of minimizing common-mode output offset voltage with lower-cost external components, and less PC board real estate, than existing designs.

Simulations showing expected performance in a number of areas was presented. Based on these results, the overall performance of the new design appears to meet or exceed the performance of existing designs.

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[2] Bill Whitlock, *Subtleties Count in Wide-Dynamic-Range Analog Interfaces.* EDN, June 4, 1998, p. 148. (Cahners, Newton, Massachusetts)

[3] *SSM 2142 Balanced Line Driver,* Data Sheet, Revision B. Analog Devices, Norwood, Massachusetts.

[4] *DRV134, DRV135 Audio Balanced Line Drivers,* Data Sheet, 1998. Burr-Brown, Tucson, Arizona.

[5] Chris N. Strahm, *Balanced Output Circuit*, US Patent #4,979,218.

[6] Bill Whitlock, *A New Balanced Audio Input Circuit for Maximum Common-Mode Rejection in Real-World.* Presented at the 101st Convention of the Audio Engineering Society, Preprint #4372, 1996, pp. 2 -3.

[7] Dennis Bohn, *Practical Line Driving Requirements*, RaneNote 126, 1991. Rane Corporation, Mukilteo, Washington.

Figure 1 - Tom Hay's Circuit

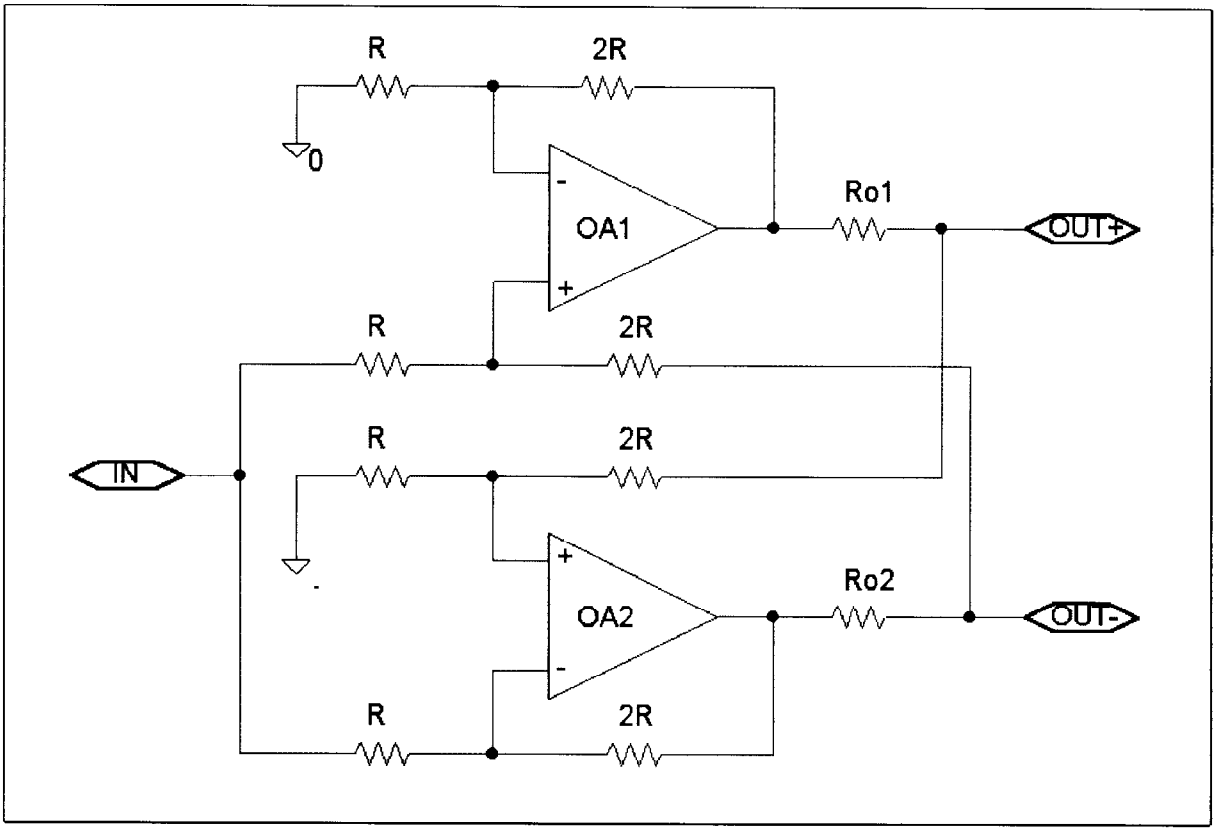

Figure 2 - Typical IC Implementation of Hay Circuit

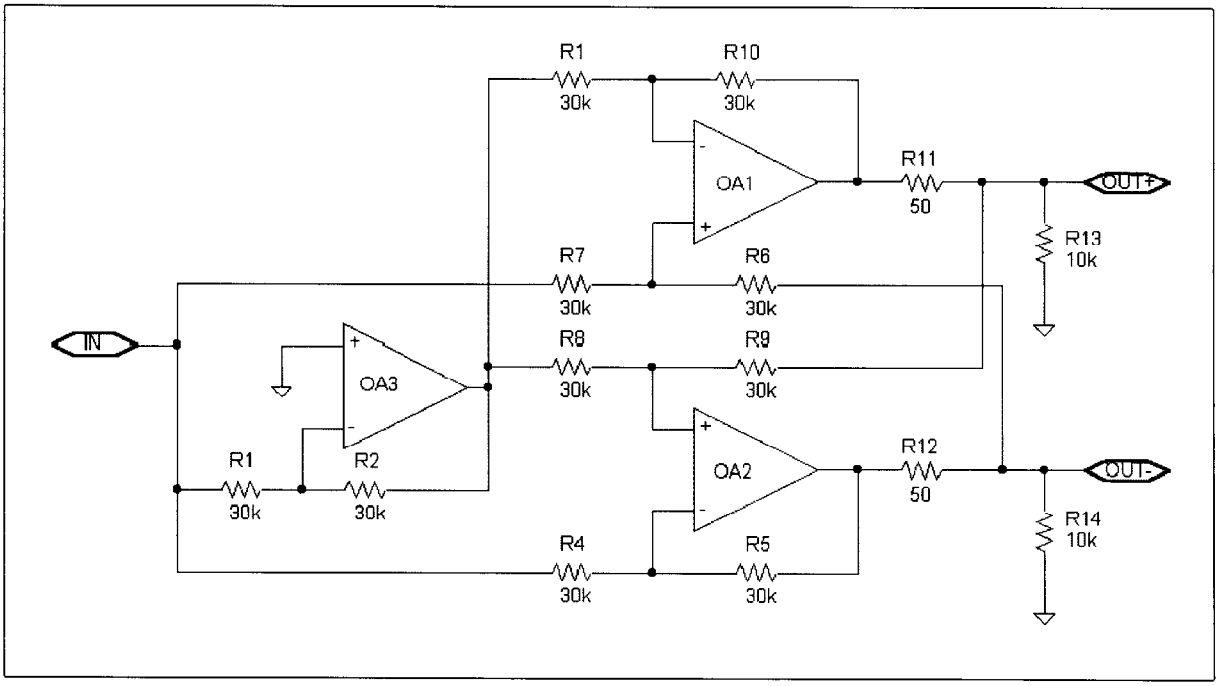

Figure 3 - Simulation Schematic of Hay Circuit

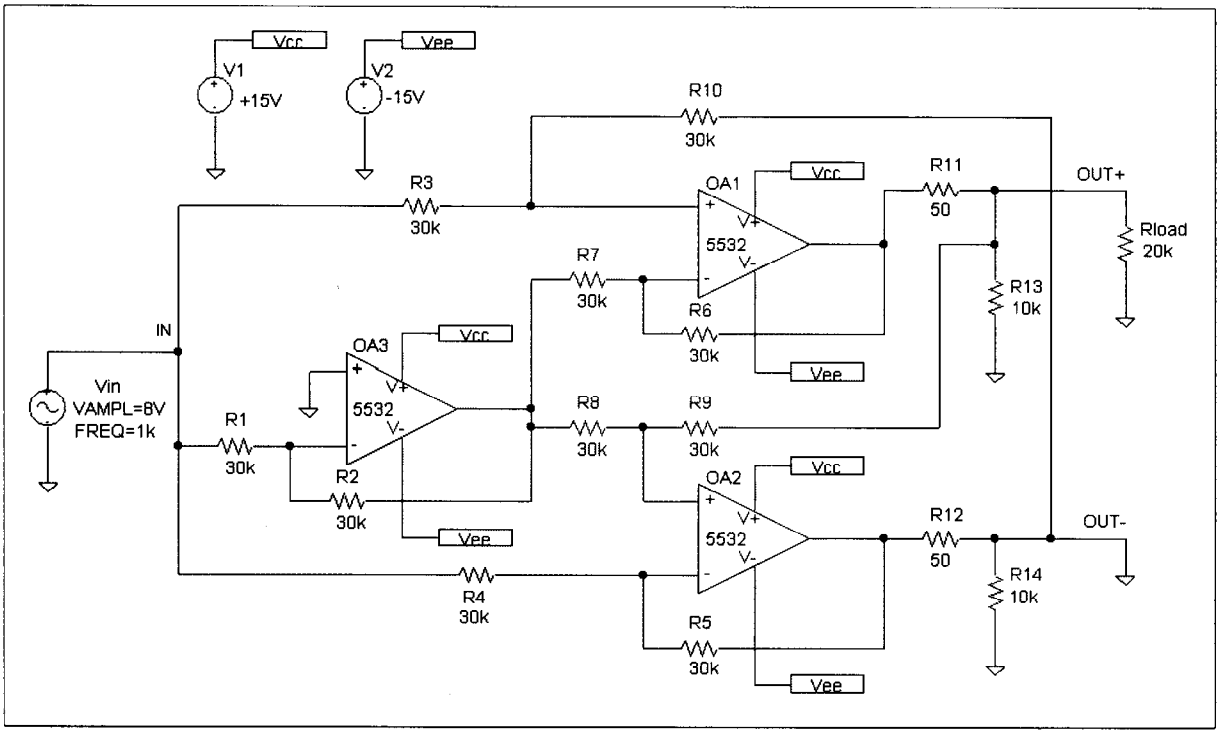

Figure 4 - Voltage Waveform at OUT+

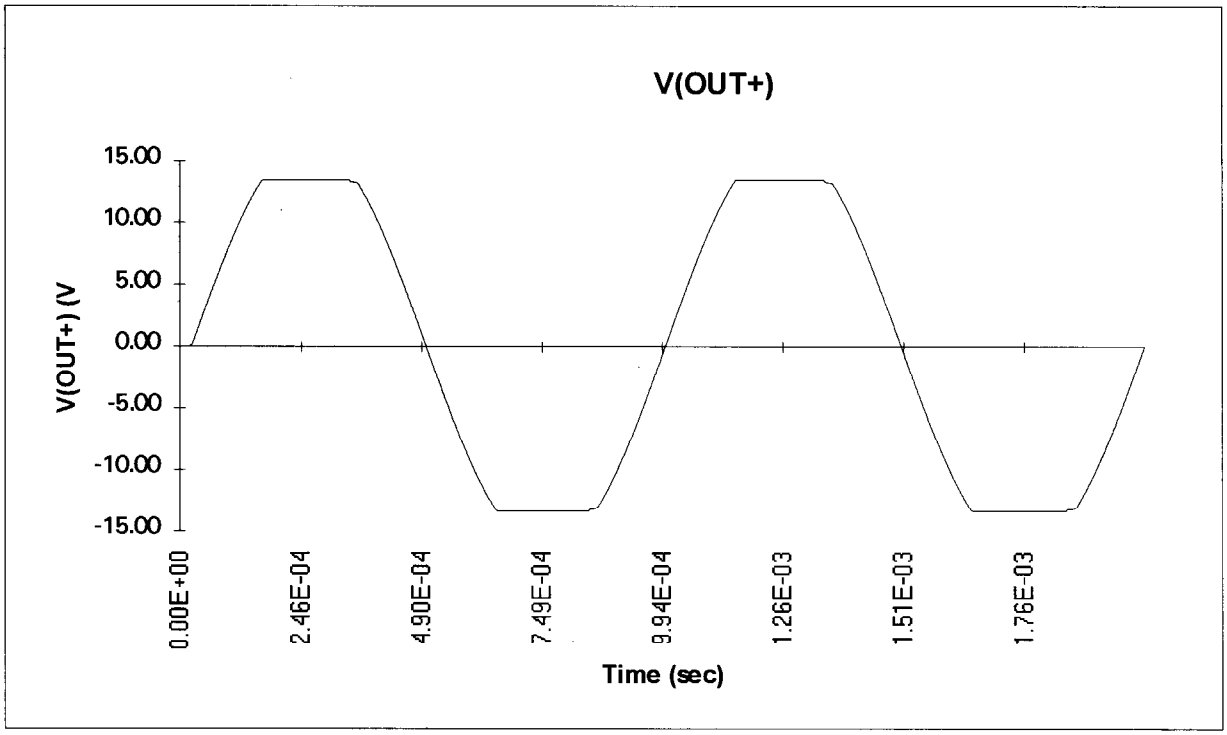

Figure 5 - Current Waveform Through R12

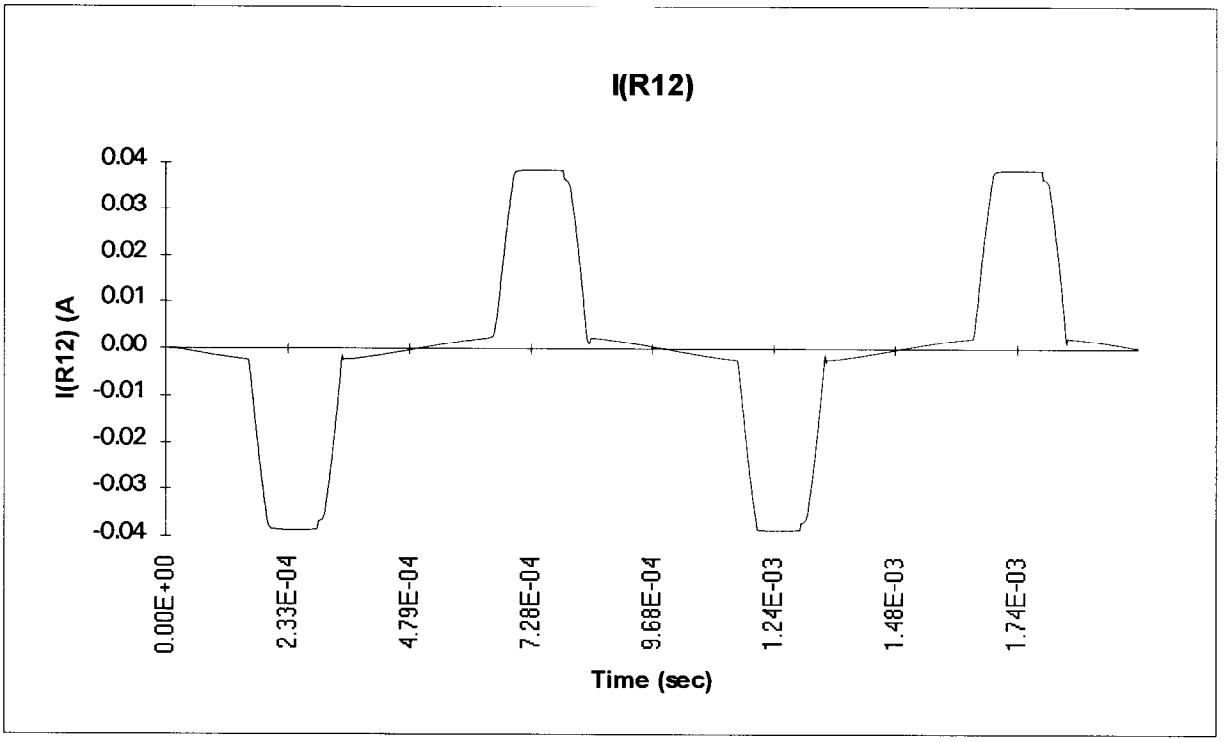

Figure 6 - Block Diagram of New Circuit

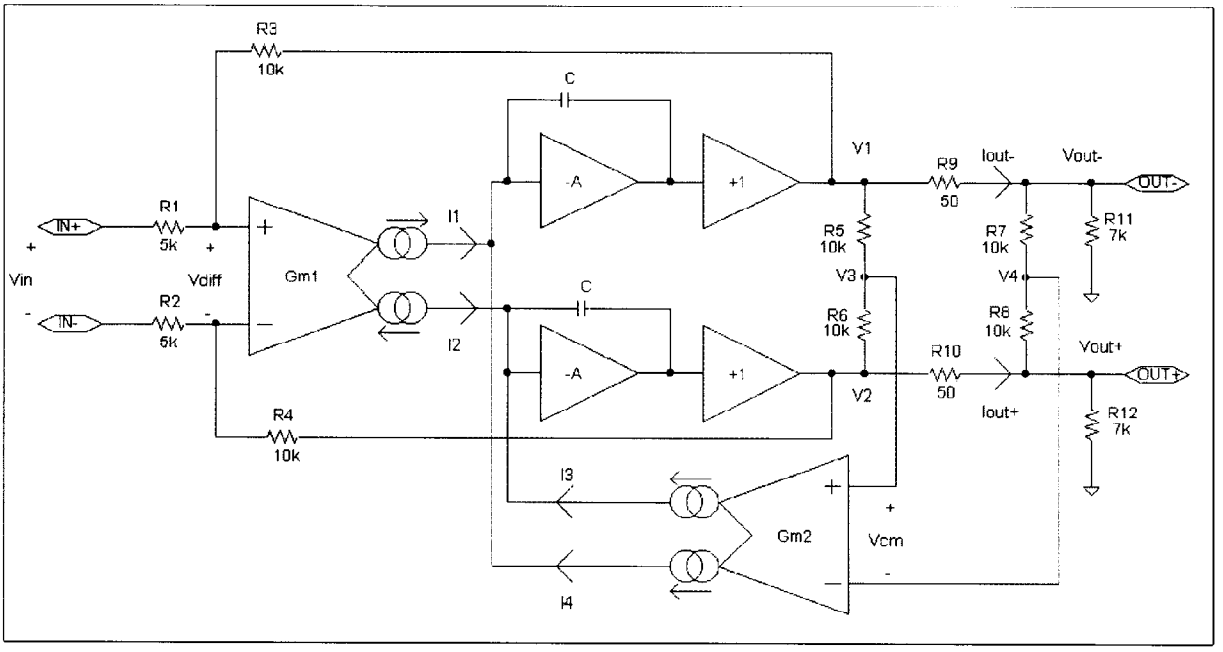

Figure 7 - Simplified Schematic of the New Design

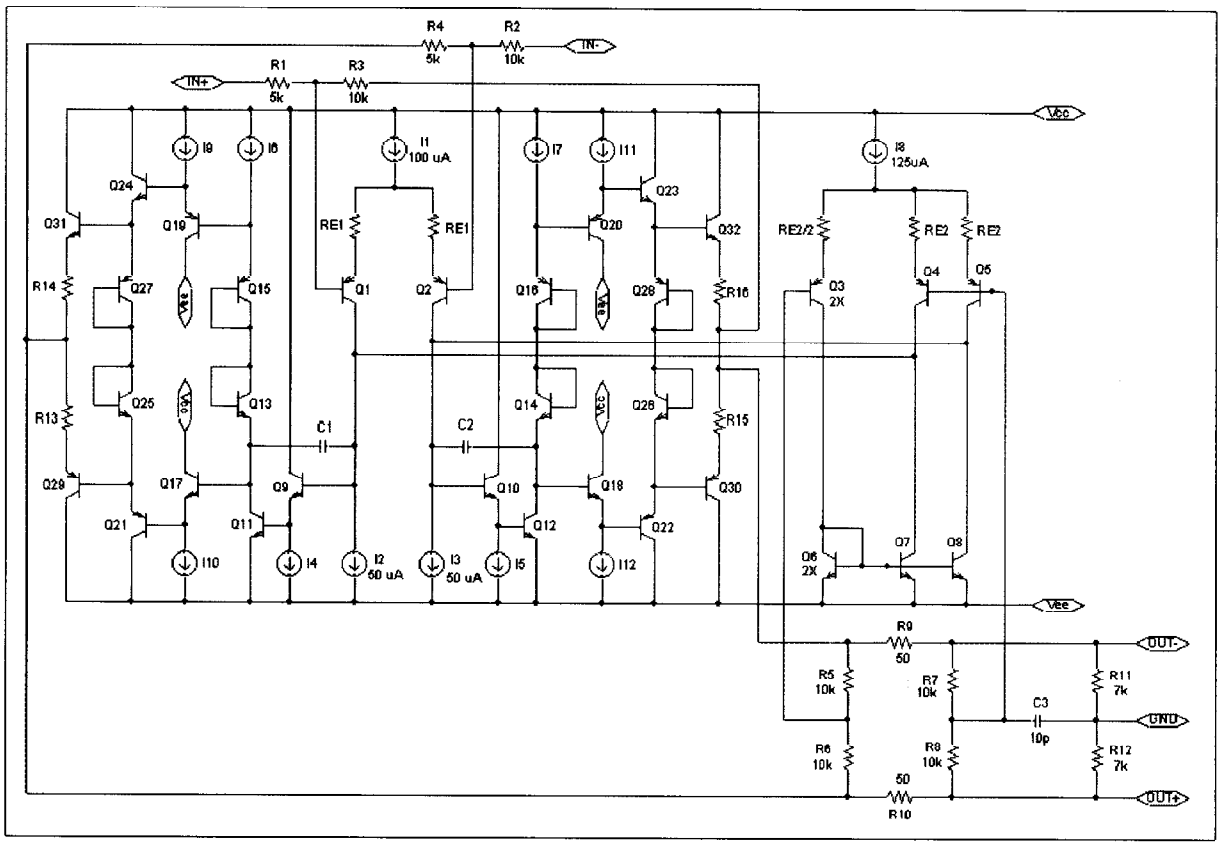

Figure 8 - Behavioral Schematic of New IC

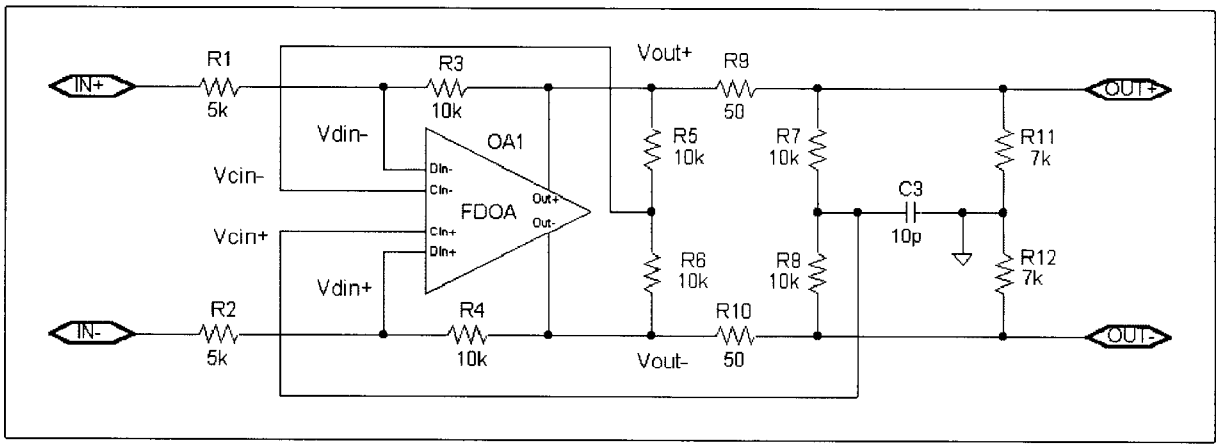

Figure 9 - Application Circuit with One-Capacitor CM Offset Reduction

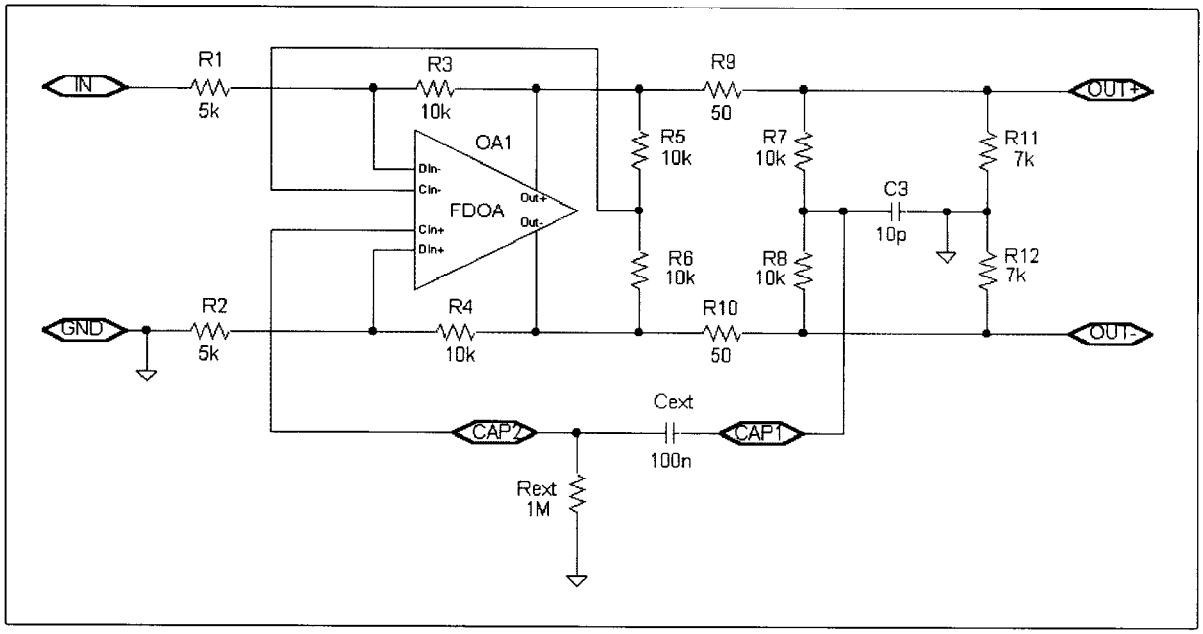

Figure 10 - Application Circuit w/ 2-Capacitor CM Offset Reduction

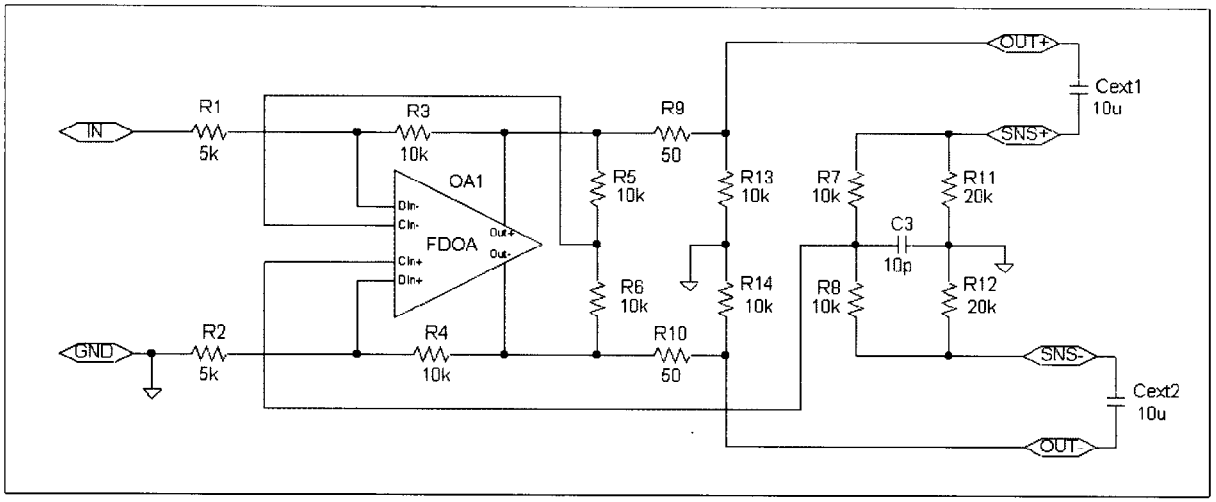

Figure 11 - Voltage Waveform at OUT+ for New Design (see text)

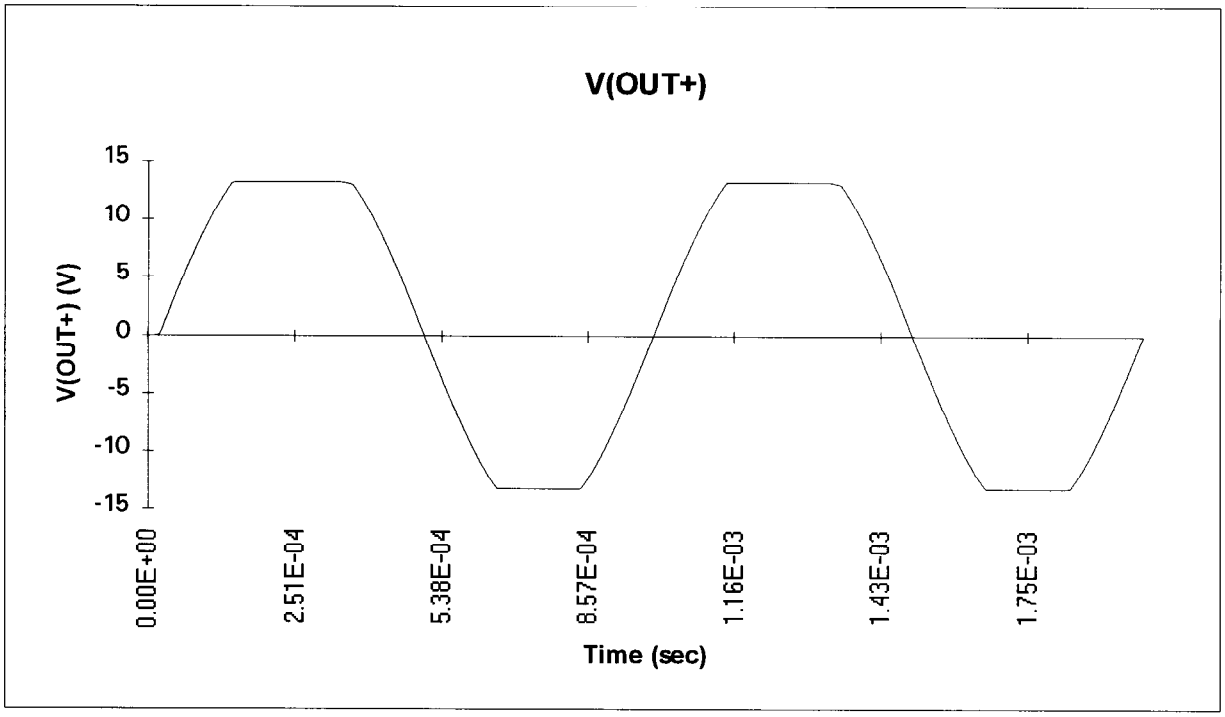

Figure 12 - Current through R10 for New Design (see text)

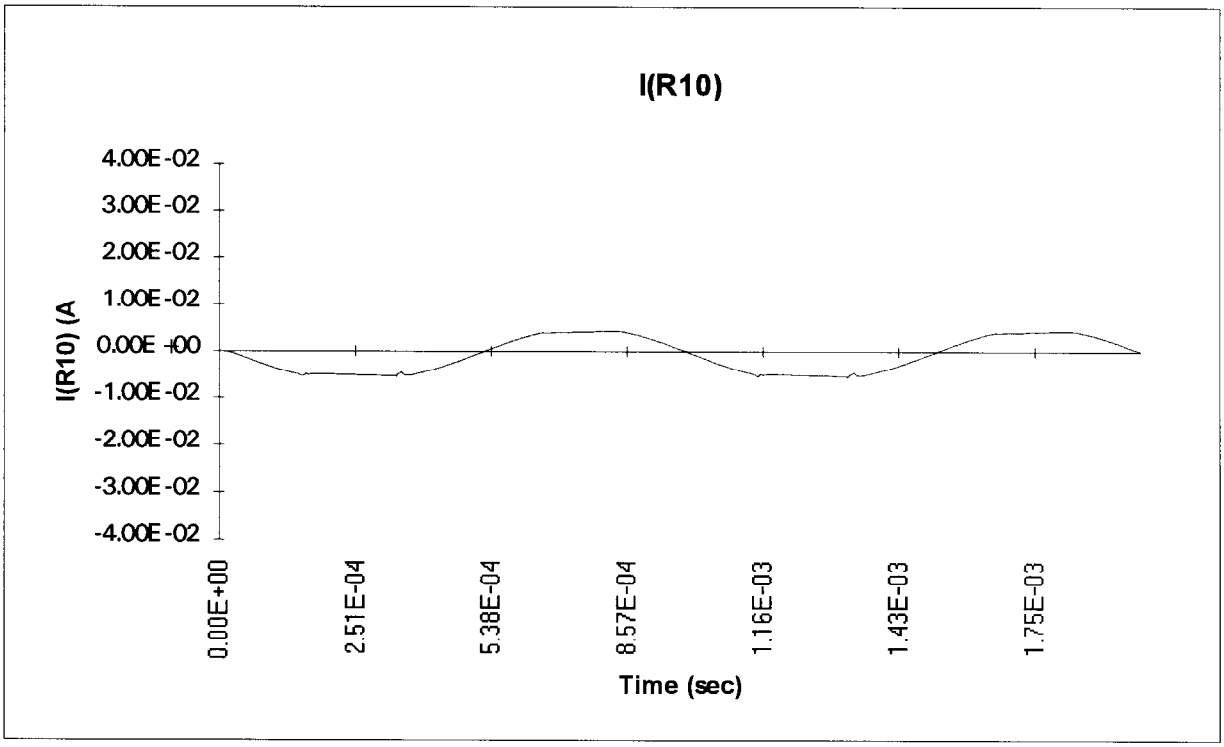

Figure 13 - Wheatstone Bridge Model of Balanced Driver/Receiver

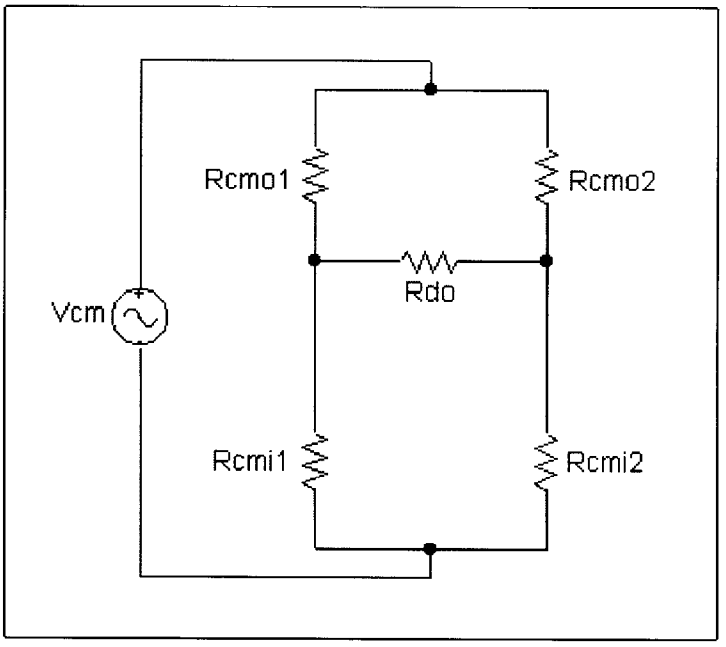

Figure 14 - Simulation Circuit for CMRR Performance

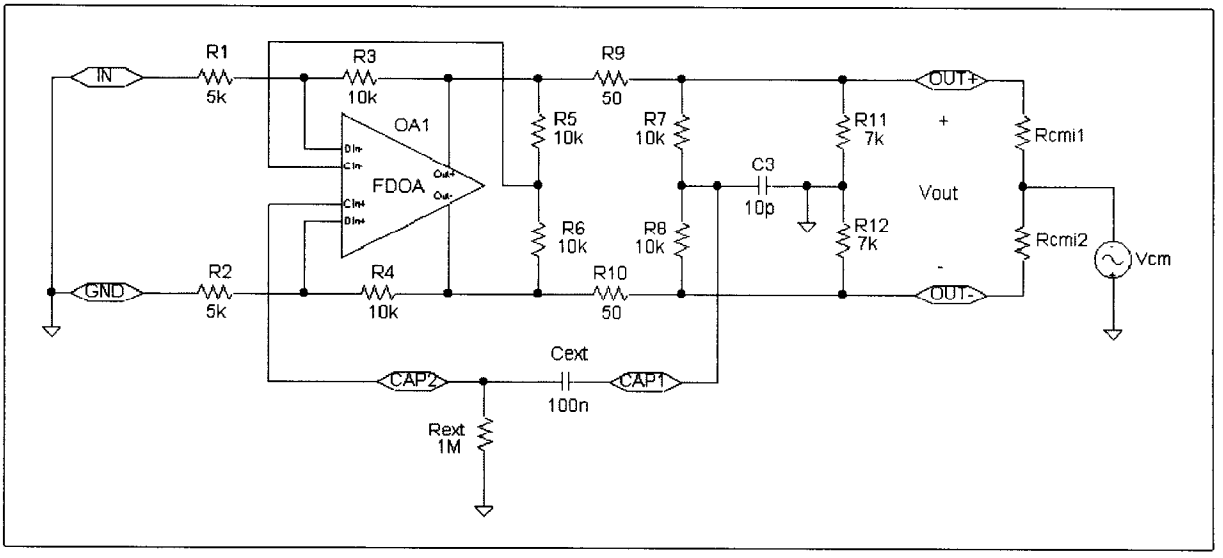

Table 1 - Results of Monte-Carlo Analysis of CMRR Performance

R_{cmi1}, R_{cmi2}	Median CMRR @ 60 Hz	Worst Case CMRR @ 60 Hz
18 kΩ	82 dB	71 dB
1 MΩ	110 dB	98 dB

Table 2 - Summary of Typical Performance Based on Simulations

Parameter	Conditions	Typical
THD	20 Hz - 20 kHz, 10 Vrms out, 600 Ω Load, Balanced	.001%
THD	20 Hz - 20 kHz, 10 Vrms out, 600 Ω Load, Single-Ended	.0018%
Output Noise	20 Hz - 20 kHz NBW, 600 Ω Load, Balanced	-104 dBV
Output Noise	20 Hz - 20 kHz NBW, 600 Ω Load, Single-Ended	-102 dBV
Slew Rate	600 Ω Load, Balanced.	16 V/us
Slew Rate	600 Ω Load, Single-Ended	15 V/us
Vout max	+/-18 V Supplies, 600 Ω Load, Balanced	+27 dBu
PSRR	+/-4 V to +/-18 V	105 dB
Supply Current	No Input Signal	4 mA
Output Current	Short Circuit	70 mA
Supply Range		+/-4 - +/-18 V