International
IOR Rectifier

APPLICATION NOTE

Application Note AN-1158

IRS2053M Functional Description

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1 IRS2053M General Description

The IRS2053M is a three channel Class D audio amplifier driver with integrated PWM modulators and over current protection. Combined with six external MOSFETs and external passive components, the IRS2053M forms three complete Class D amplifiers. The versatile structure of the analog input section with an error amplifier and a PWM comparator has flexibility of implementing different types of PWM modulator schemes.

Loss-less current sensing utilizes $R_{DS(on)}$ of the MOSFETs. The protection control logic monitors the status of the power supplies and load current through each MOSFET.

For the convenience of half bridge configuration, the analog PWM modulator and protection logic are constructed on a floating well.

The IRS2053M implements start-up click noise reduction to suppress unwanted audible noise during PWM start-up and shutdown.

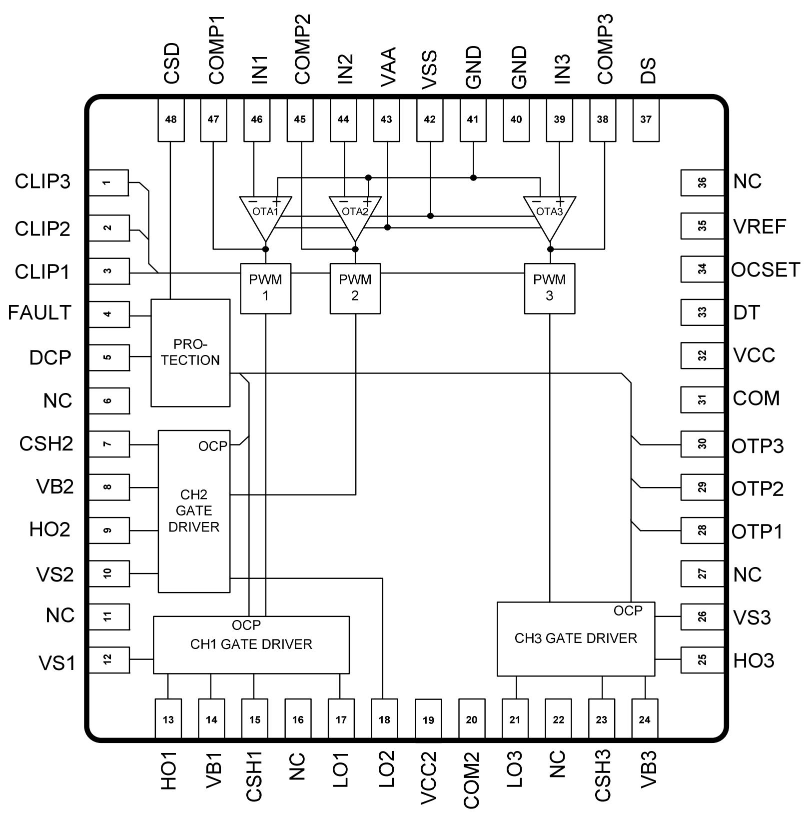

Figure 1 Functional Block Diagram of IRS2053M

1.1 Typical Implementation

The following explanations are based on a typical application circuit with self-oscillating PWM topology shown in Figure 2. For further information on the design, refer to the IRAUDAMP11 reference design.

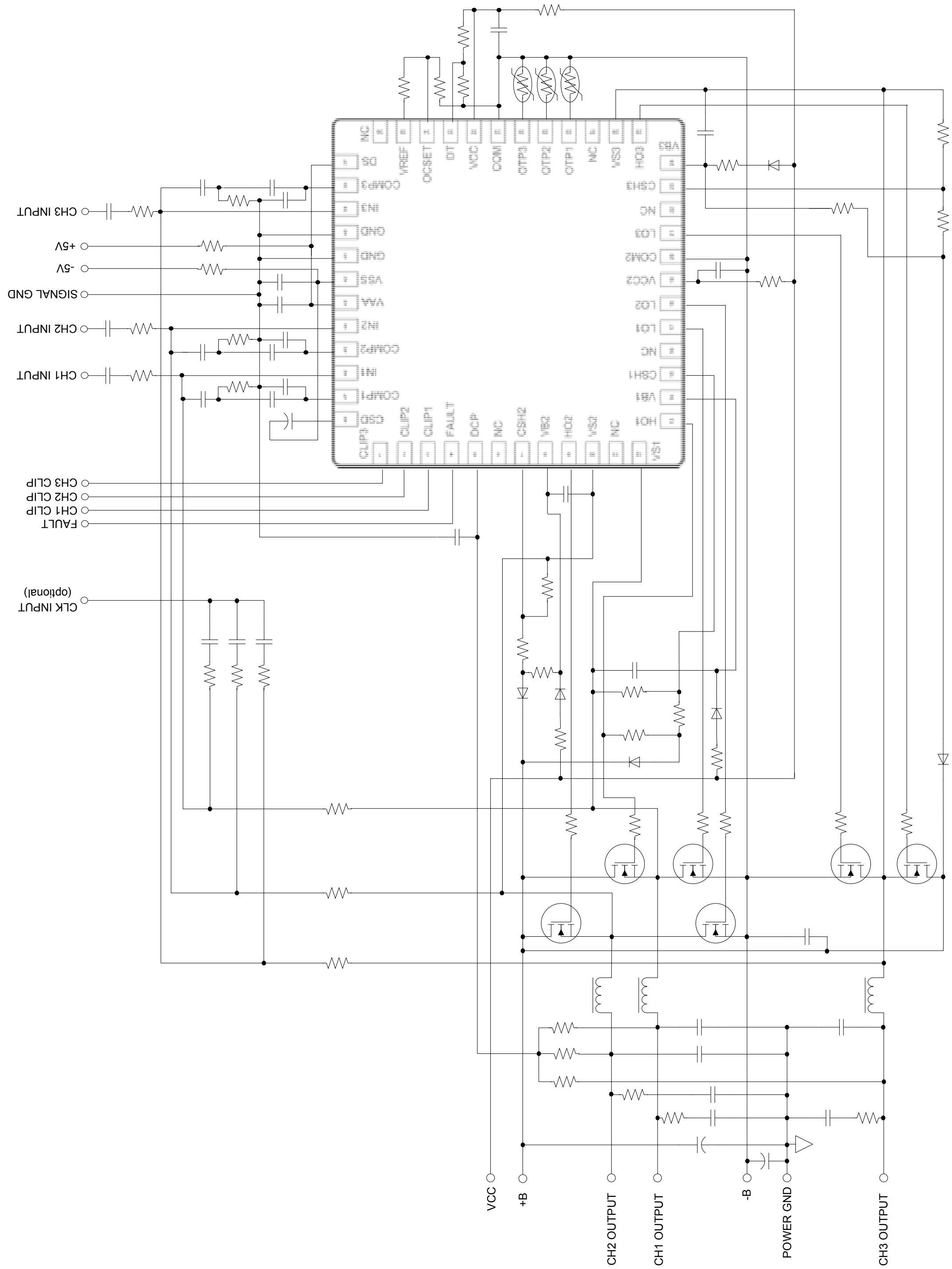

Figure 2 IRS2053M Typical Application Circuit

2 Input Section

The audio input stage of the IRS2053M is configured as an inverting error amplifier.

In Figure 3, the voltage gain of the amplifier G_V is determined by input resistor R_{IN} and feedback resistor R_{FB}.

$$G_V = \frac{R_{FB}}{R_{IN}}$$

Since the feedback resistor R_{FB} is part of an integrator time constant, which determines switching frequency, changing overall voltage gain by R_{IN} is simpler and, therefore, recommended in most cases.

Note that the input impedance of the amplifier is equal to the input resistor R_{IN}.

A DC blocking capacitor C3 should be connected in series with R_{IN} to minimize DC offset in the output. Minimizing DC offset is essential for audible noise-less Turn-ON and -OFF. A ceramic capacitor is not recommended due to the potential cause of distortion.

The connection of the non-inverting input IN+ is a reference for the error amplifier, and thus is crucial for audio performance. Connect IN+ to the signal reference ground in the system, which has the same potential as the negative terminal of the speaker output.

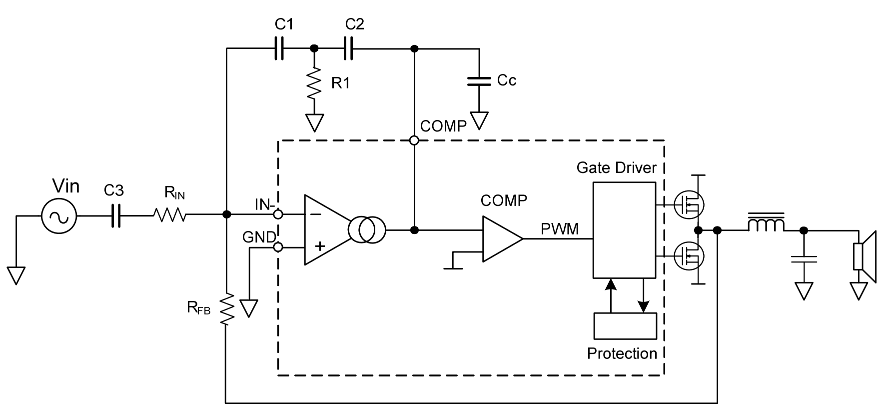

Figure 3 IRS2053M Typical Control Loop Design

2.1 OTA (Operating Trans-conductance Amplifier)

The front-end error amplifier of the IRS2053M features an operational trans-conductance amplifier (OTA), which is carefully designed to obtain optimal audio performance. The OTA outputs a current to the COMP pin, unlike a voltage output in an operational amplifier (OPA). The non-inverting input is internally tied to the GND pin.

The inverting input has clamping diodes to GND to improve recovery from clipping as well as ensuring stable start up. The OTA output COMP is internally connected to the PWM comparator whose threshold is (VAA-VSS)/2.

For stable operation of the OTA, a compensation capacitor Cc minimum of 1nF is required. The OTA shuts down when V_{CSD}<Vth2.

2.2 PWM Modulator

The IRS2053M allows the user to choose from numerous ways of PWM modulator implementations. In this section, all the explanations are based on a typical application circuit of a self-oscillating PWM.

2.2.1 Self-Oscillating PWM Modulator Design

The typical application features a self-oscillating PWM scheme. For better audio performance, front end 2nd order integration is chosen.

2.2.2 Self-Oscillating Frequency

Self-oscillating frequency is determined mainly by the following items in Figure 3.

- Integration capacitors, C1 and C2
- Integration resistor, R1
- Propagation delay in the gate driver
- Feedback resistor, R_{FB}
- Duty cycle

The bus voltage and input resistance R_{IN} have little influence on the self-oscillating frequency. Note that as is the nature of a self-oscillating PWM, the switching frequency decreases as PWM modulation deviates from idling.

2.2.3 Determining Self-Oscillating Frequency

Choosing the switching frequency entails making many design trade offs.

At lower switching frequencies, the efficiency at the MOSFET stage improves, but inductor ripple current increases. Also output PWM switching carrier leakage increases.

At higher switching frequencies the efficiency degrades due to switching losses, but wider bandwidth can be achieved. The inductor ripple decreases yet iron losses increase. The junction temperature of the gate driver IC might be a stopper for going to a higher frequency.

For these reasons, 400kHz is chosen for a typical design example, which can be seen in the IRAUDAMP8 reference design.

2.2.4 Choosing External Components Value

For suggested component values of components for a given target self-oscillating frequency, refer to Table 1.

The OTA output has limited voltage and current compliances. This set of component values ensures that the OTA operates within its linear region so optimal THD+N performance can be achieved.

In case the target frequency is somewhere in between the frequencies listed in Table 1, adjust the frequency by tweaking R1, if necessary.

Target Self-Oscillation Frequency (kHz)	C1=C2 (nF)	R1 (ohms)
500	2.2	200
450	2.2	165
400	2.2	141
350	2.2	124
300	2.2	115
250	2.2	102
200	4.7	41.2
150	10	20.0
100	10	14.0
70	22	4.42

Condition:IRS2053M with IRF6665, DS=VAA, Vbus=+/-35V, DT=25ns, R_{FB}=47k.

Table 1 External Component Values vs. Self Oscillation Frequency

2.3 Clock Synchronization

In the PWM control loop design example, the self-oscillating frequency can be set and synchronized to an external clock. Through a set of resistors and a capacitor, the external clock injects periodic pulsating charges into the integrator, forcing oscillation to lock up to the external clock frequency. A typical setup with 5Vp-p 50% duty clock signal uses R_{CK}=22k and C_{CK}=100pF in Figure 4. To maximize audio performance, the self-running frequency without clock injection should be 20 to 30% higher than the external clock frequency.

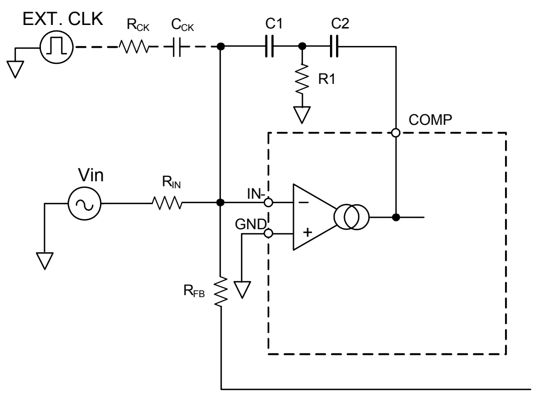

Figure 4 External Clock Sync

Figure 5 shows how a self-oscillating frequency locks up to an external clock frequency. A design of a400kHz self-oscillating frequency synchronizes to an external clock whose frequency is within the red boarder lines.

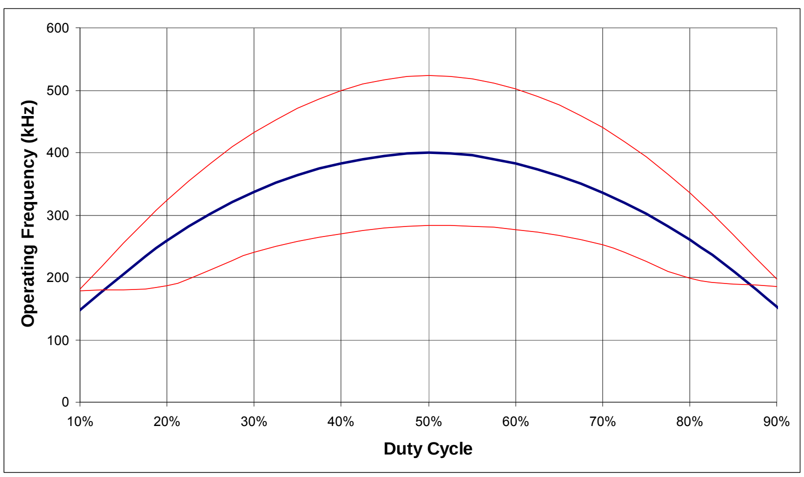

Figure 5 Typical Lock Range to External Clock

2.4 DS (Delay Select) pin

The DS pin offers options to bypass an internal delay block to achieve shorter latency, as shown in Table 2.

DS Pin	Propagation Delay (TYP)
VAA	325 ns
VSS	100 ns

Table 2 Propagation Delay and DS pin Bias

2.5 Click Noise Elimination

The IRS2053M has a unique feature that minimizes Turn-ON and -OFF audible click noise. When CSD is in between Vth1 and Vth2 during start up, an internal closed loop around the OTA enables an oscillation that generates voltages at COMP and IN-, bringing them to steady state values. It runs at around 1MHz, independent from the switching oscillation.

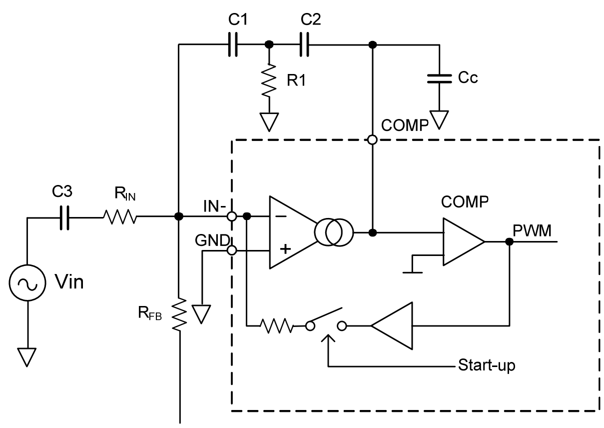

Figure 5 Click Noise Elimination

As a result, all capacitive components connected to COMP and IN- pins, such as C1, C2, C3 and Cc in Figure 5, are pre-charged to their steady state values during the start up sequence. This allows instant settling of PWM operation.

To utilize the click noise reduction function, the following conditions must be met.

1. CSD pin has slow enough ramp up from Vth1 to Vth2 such that the voltages in the capacitors can settle to their target values.
2. High-side bootstrap power supply needs to be charged up prior to starting oscillation.
3. Audio input has to be zero.
4. For internal local loop to override external feedback during the startup period, DC offset at speaker output prior to shutdown release has to satisfy the following condition.

$$DCoffset < 30\mu A \cdot R_{FB}$$

2.6 CSD Voltage and OTA Operational Mode

The CSD pin determines the operational mode of the IRS2053M as shown in Figure 6. The OTA has three operational modes; cut off, local oscillation and normal operation while the gate driver section has two modes; normal and shutdown with CSD voltage.

When V_{CSD} < Vth2, the IC is in shutdown mode and the OTA is cut off. When Vth2< V_{CSD} < Vth1, the HO and LO outputs are still in shutdown mode. The OTA is activated and starts local oscillation, which pre-biases all the capacitive components in the error amplifier. When V_{CSD}>Vth1, shutdown is released and PWM operation starts.

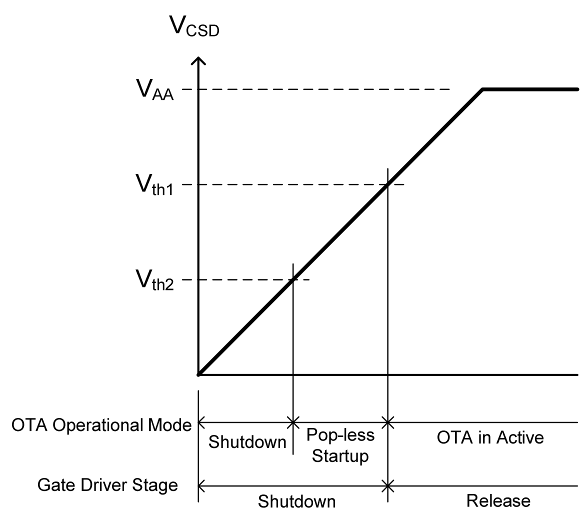

Figure 6 V_{CSD} and OTA Mode

2.7 Self-oscillation Start-up Condition

The IRS2053M requires the following conditions be met to start PWM oscillation in the typical application circuit.

- All the control power supplies, VAA, VSS, VCC and VBS are above the under voltage lockout thresholds.
- CSD pin voltage is over Vth1 threshold.
- $|i_{IN}| < |i_{FB}|$

Where $i_{IN} = \dfrac{V_{IN}}{R_{IN}}$, $i_{FB} = \dfrac{V_{+B}}{R_{FB}}$.

Note that this condition also limits the maximum audio input voltage feeding into R1. If this condition is exceeded, the amplifier stops its oscillation during the operation period. This allows a 100% modulation index; however, care should be taken so that the high-side floating supply does not decay due to a lack of low-side pulse ON state.

3 MOSFET Selection

There are a couple of limitations on the size of the MOSFET to be used with the IRS2053M.

1. Power dissipation

Power dissipation from the gate driver stage in the IRS2053M is proportional to switching frequency and the gate charge of the MOSFET. The higher the switching frequency, the lower the gate charge of the MOSFET that can be used.

Refer to Junction Temperature Estimation later in this application note for details.

2. Switching Speed

Internal over current protection has a certain time window to measure the output current. If switching transition takes too long, the internal OCP circuitry starts monitoring voltage across the MOSFET which induces false triggering of OCP. Less than 20nC of gate charge per output is recommended.

The IRS2053M accommodates a range of IR Digital Audio MOSFETs, providing a scalable design for various output power levels. For further information on MOSFET section, refer to AN-1070, Class D Amplifier Performance Relationship to MOSFET Parameters.

4 Over Current Protection (OCP)

The IRS2053M features over current protection to protect the power MOSFETs during abnormal load conditions. The control logic is shown in Figure 8. The IRS2053M starts a sequence of events when it detects an over current condition during either high-side or low-side turn on of a pulse.

As soon as either the high-side or low-side current sensing block detects over current:

1. The OC Latch (OCL) flips logic states and shutdowns the outputs LO and HO.
2. The CSD pin starts discharging the external capacitor Ct.
3. When V_{CSD}, the voltage across Ct, falls below the lower threshold Vth2, an output signal from COMP2 resets OCL.
4. The CSD pin starts charging the external capacitor Ct.
5. When V_{CSD} goes above the upper threshold Vth1, the logic on COMP1 flips and the IC resumes operation.

As long as the over current condition exists, the IC will repeat the over current protection sequence at a repetition rate dependent upon capacitance at the CSD pin.

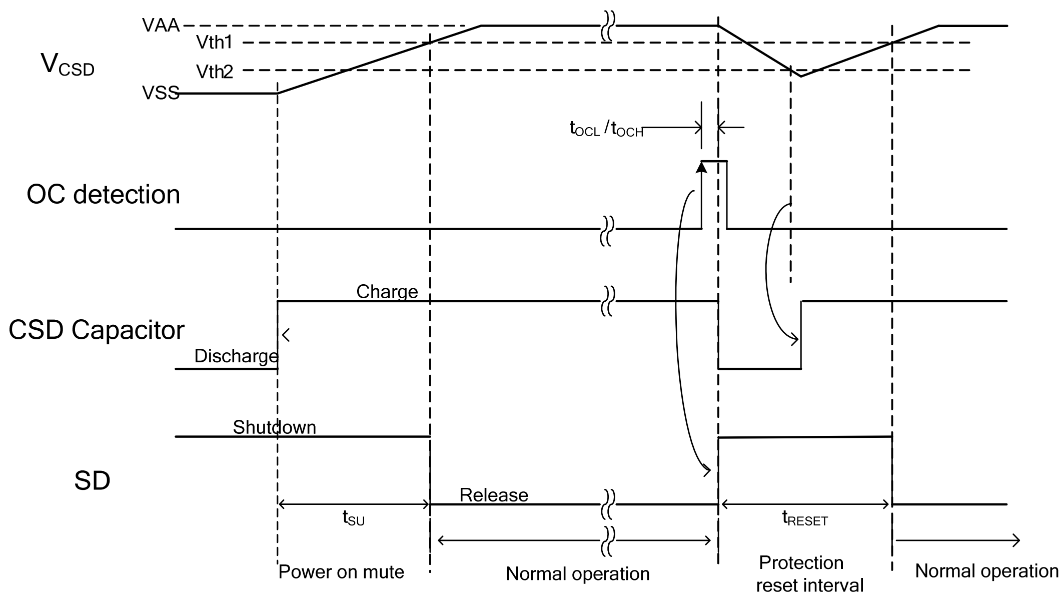

Figure 7 Over Current Protection Timing Chart

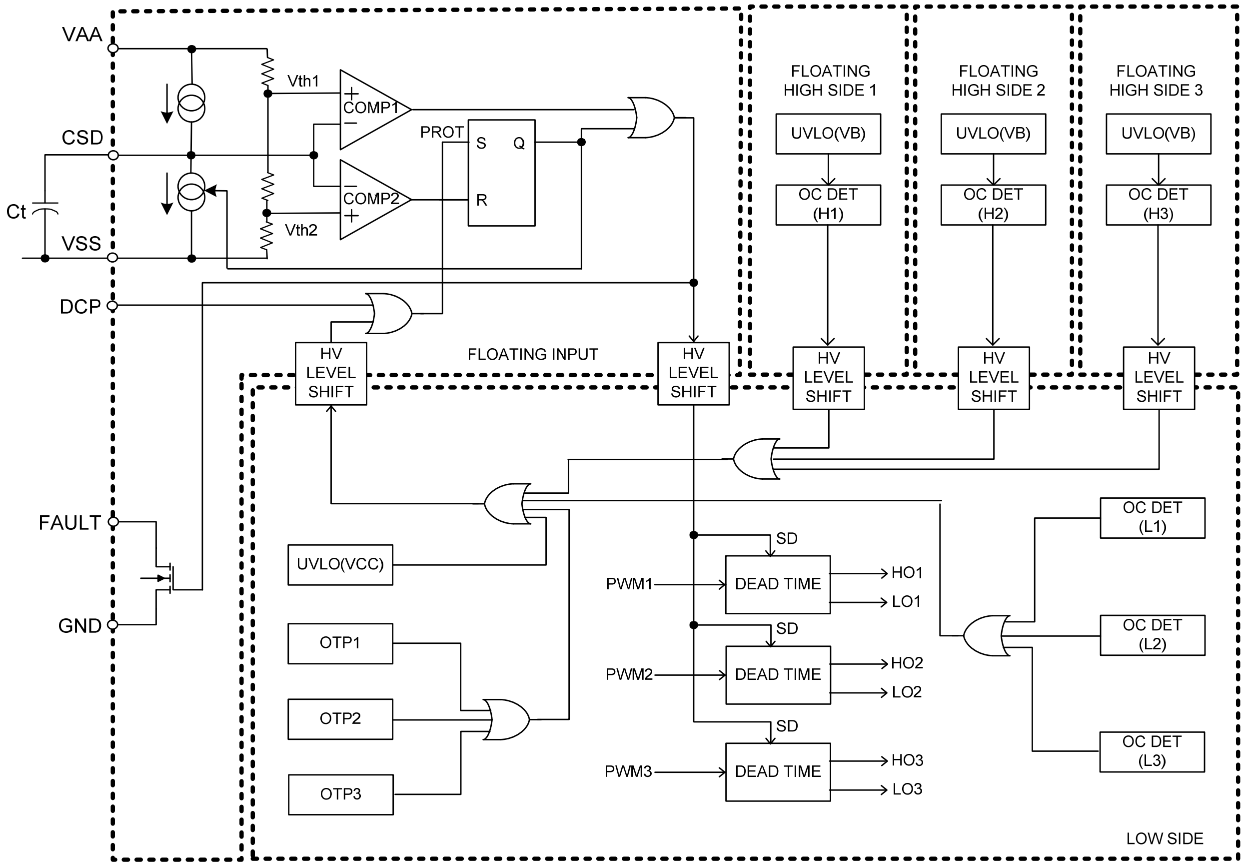

Figure 8 Shutdown Functional Block Diagram

4.1 Protection Control

The internal protection control block dictates the operational mode, normal or shutdown, using the input of the CSD pin. In shutdown mode, the IC forces LO and HO to output 0V with respect to COM and VS respectively to turn off the power MOSFETs.

The CSD pin provides five functions.

1. Power up delay timer
2. Self-reset timer
3. Shutdown input
4. Latched protection configuration
5. Shutdown status output (host I/F)

The CSD pin cannot be paralleled with another IRS2053M.

The operating statuses of the protections are shown in Table 3.

Event	CSD	FAULT
UVCC, rising edge	recycle	L until CSD>Vth1
UVCC, falling edge	n/a	n/a
UVAA, rising edge	n/a	L at VAA<UVAA
UVAA, falling edge	n/a	L at VAA<UVAA
UVBS, rising edge	n/a	n/a
UVBS, falling edge	n/a	n/a
Over Current Protection	keep recycling until OCP goes away	held L until OCP goes away
DC Protection	held L until DCP goes away	held L until DCP goes away
Clip Detection	n/a	n/a
OTP1-3 Inputs	keep recycling until OTP goes away	held L until OTP goes away

*CSD recycle: CSD pin voltage discharges down to Vth2 and charges back to VAA, if CSD pin is configured as self reset protection.

Table 3 Events and Actions of CSD and FAULT

4.1.1 Self Reset Protection

By putting a capacitor between CSD and V_{SS}, the IRS2053M resets itself after entering shutdown mode.

After the OCP event, the CSD pin discharges Ct voltage V_{CSD} down to the lower threshold V_{th2} to reset the internal shutdown latch. Then, the IRS2053M begins to charge Ct in an attempt to resume operation. Once the voltage of the CSD pin rises above the upper threshold, V_{th1}, the IC resumes normal operation.

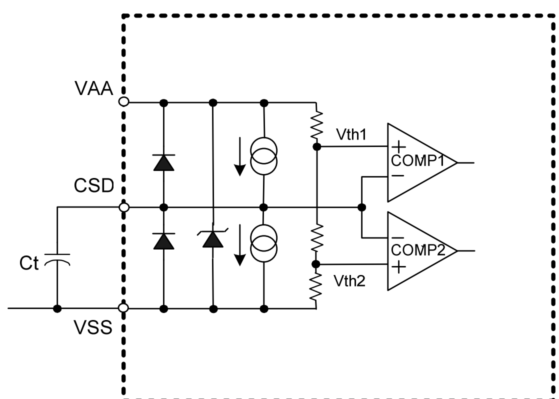

Figure 9 Self Reset Protection Configuration

4.1.2 Designing Ct

The timing capacitor, Ct, is used to program t_{RESET} and t_{SU}.

- t_{RESET} is the amount of time that elapses from when the IC enters the shutdown mode to the time when the IC resumes operation. t_{RESET} should be long enough to avoid over heating the MOSFETs from the repetitive sequence of shutting down and resuming operation during over current conditions. In most of applications, the minimum recommended time for t_{RESET} is 0.1 second.
- t_{SU} is the amount of time between powering up the IC in shutdown mode to the moment the IC releases shutdown to begin normal operation.

The Ct determines t_{RESET} and t_{SU} as following equations:

$$t_{RESET} = \frac{Ct \cdot V_{AA}}{1.1 \cdot I_{CSD}} \quad [s]$$

$$t_{SU} = \frac{Ct \cdot V_{AA}}{0.7 \cdot I_{CSD}} \quad [s]$$

where I_{CSD} = the charge/discharge current at the CSD pin
V_{AA} = the floating input supply voltage with respect to V_{SS}.

4.1.3 Shutdown Input

The IRS2053M can be shut down by an external shutdown signal SD. Figure 10 shows how to add an external discharging path to shutdown the PWM.

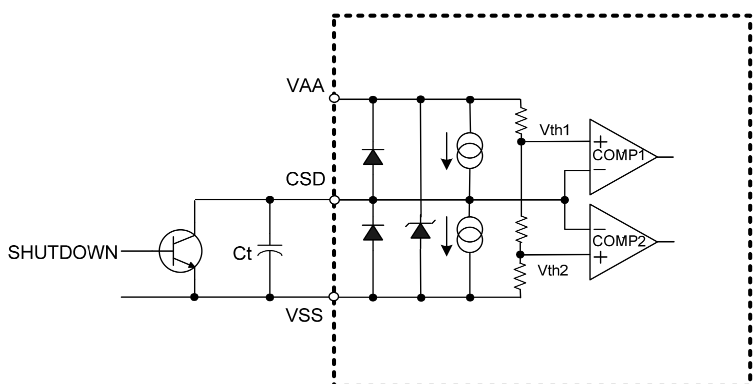

Figure 10 Shutdown Input

4.1.4 Latched Protection

Connecting CSD to V_{AA} through a 10k Ω or less resistance configures the over current protection latch. The latch locks the IC in shutdown mode after over current is detected. An external reset switch can be used to bring CSD below the lower threshold Vth2 for a minimum of 200ns to properly reset the latch. After the power up sequence, a reset signal to the CSD pin is required to release the IC from the latched shutdown mode.

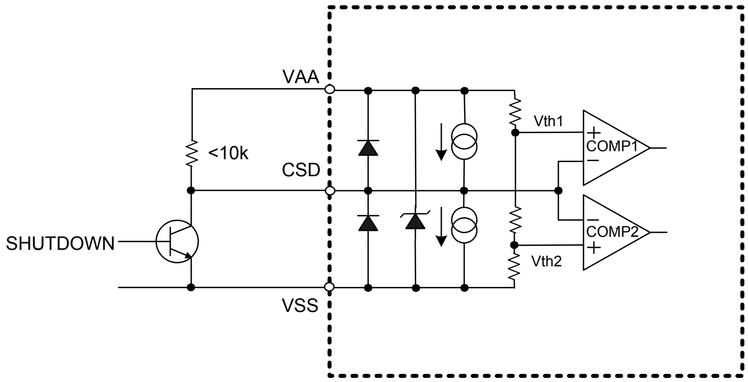

Figure 11 Latched Protection with Reset Input

4.1.5 Interfacing with System Controller

The IRS2053M can communicate with an external system controller through a simple interfacing circuit shown in Figure 12. A generic PNP transistor U1 detects the sink current at the CSD pin during an OCP event and outputs a shutdown signal to an external system controller. Another generic NPN transistor U2 can then reset the internal protection logic by pulling the CSD voltage below the lower threshold Vth2 for a minimum of 200ns. Note that the CSD pin is configured to operate in latched OCP. After the power up sequence, a reset signal to the CSD pin is required to release the IC from the shutdown mode.

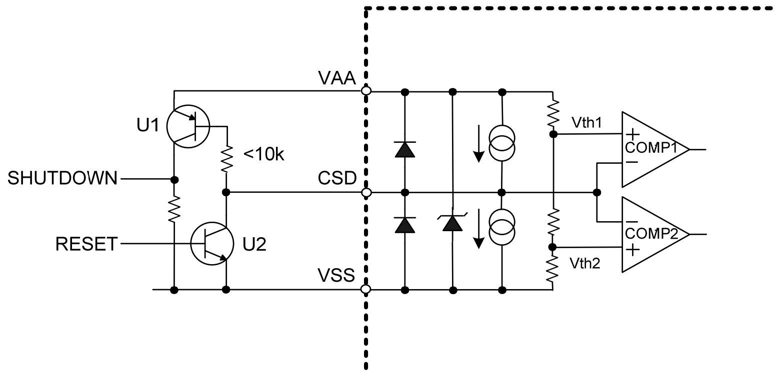

Figure 12 Interfacing with Host Controller

4.2 Programming OCP Trip Level

In a Class D audio amplifier, the direction of the load current alternates with the audio input signal. An over-current condition can therefore occur during either a positive current cycle or a negative current cycle. The IRS2053M uses the $R_{DS(on)}$ of the output MOSFETs as current sensing resistors. Due to the structural constraints of high voltage ICs, current sensing is implemented differently for the high side and low side. If the measured current exceeds a predetermined threshold, the OCP block outputs a signal to the protection block, forcing HO and LO low and protecting the MOSFETs.

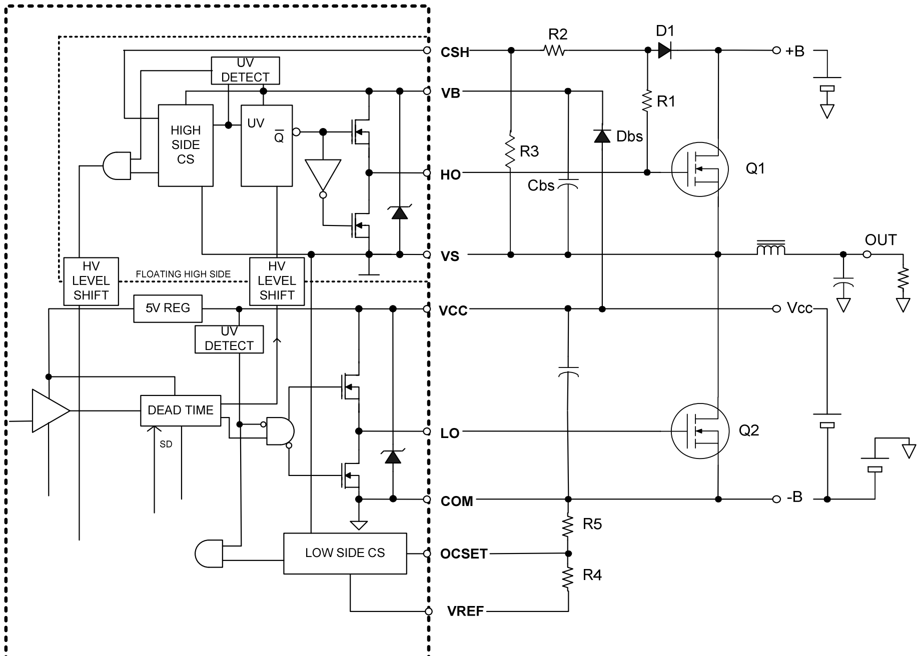

Figure 13 Bi-directional Over Current Protection

4.2.1 Low Side Over Current Sensing

For negative load currents, low-side over current sensing monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level.

Low-side current sensing is based on the measurement of V_{DS} across the low side MOSFET during the low-side on state. In order to avoid triggering OCP from overshoot, a blanking interval inserted after LO turn on disables over current detection for 450ns.

The OCSET pin is to program the threshold for low-side over current sensing. When the measured V_{DS} measured of the low side MOSFET exceeds the voltage at the OCSET pin with respect to COM, the IRS2053M begins the OCP sequence described earlier.

Note that the programmable OCSET range is 0.5V to 5.0V. To disable the low side OCP, connect OCSET to VCC directly.

To program the trip level for over current, the voltage at OCSET can be calculated using the equation below.

$V_{OCSET} = V_{DS(LOW\ SIDE)} = I_{TRIP+} \times R_{DS(on)}$

In order to minimize the effect of the input bias current at the OCSET pin, select resistor values for R4 and R5 such that the current through the voltage divider is 0.5mA or more.

* Note: Using V_{REF} to generate an input to OCSET through a resistive divider provides improved immunity from fluctuations in V_{CC}.

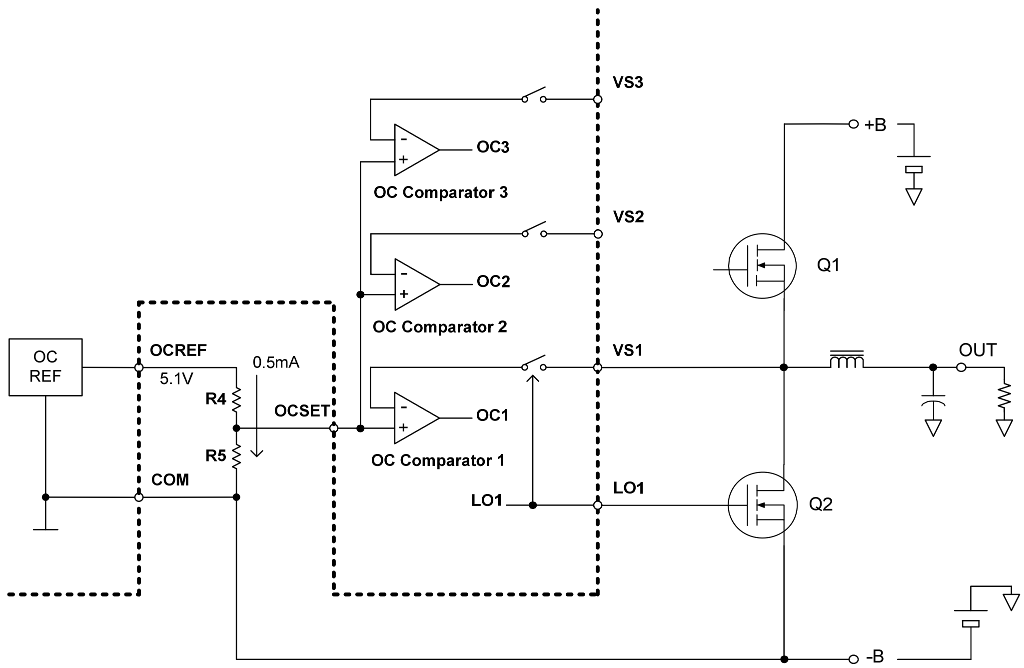

Figure 14 Low Side Over Current Sensing

4.2.2 Low Side Over Current Setting

Assume that the low side MOSFET has $R_{DS(on)}$ of 100mΩ. V_{OCSET} to set the current trip level at 30A is given by:

$V_{OCSET} = I_{TRIP+} \times R_{DS(on)} = 30A \times 100m\Omega = 3.0V$

Choose R4+R5=10 kΩ to properly load the VREF pin.

$$R_5 = \frac{V_{OCSET}}{V_{REF}} \cdot 10k\Omega$$
$$= \frac{3.0V}{5.1V} \cdot 10k\Omega$$
$$= 5.8k\Omega$$

where $V_{REF} = 5.1V$

Based on the E-12 series resistor values, choose R5 = 5.6kΩ and R4 = 3.9kΩ to complete the design.

In general, $R_{DS(on)}$ has a positive temperature coefficient that needs to be considered when setting the threshold level. Also, variations in $R_{DS(on)}$ will affect the selection of external or internal component values.

4.2.3 High Side Over-Current Sensing

For positive load currents, high-side over current sensing also monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level. High-side current sensing is based on the measurement of V_{DS} across the high-side MOSFET during high-side turn on through pins CSH and Vs. In order to avoid triggering OCP from overshoot, a blanking interval inserted after HO turn on disables over current detection for 450ns.

In contrast to low-side current sensing, the threshold at which the CSH pin engages OC protection is internally fixed at 1.2V. An external resistive divider R2 and R3 can be used to program a higher threshold.

An external reverse blocking diode, D1, is required to block high voltages from feeding into the CSH pin while the high side is off. Due to a forward voltage drop of 0.6V across D1, the minimum threshold required for high-side over current protection is 0.6V.

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot \left(V_{DS(HIGHSIDE)} + V_{F(D1)}\right)$$

where $V_{DS(HIGH\ SIDE)}$ = the drain to source voltage of the high side MOSFET during high side turn on
$V_{F(D1)}$ = the forward drop voltage of D1

Since $V_{DS(HIGH\ SIDE)}$ is determined by the product of drain current I_D and $R_{DS(on)}$ of the high side MOSFET. V_{CSH} can be rewritten as:

$$V_{CSH} = \frac{R3}{R2 + R3} \cdot \left(R_{DS(ON)} \cdot I_D + V_{F(D1)}\right)$$

The reverse blocking diode D1 is forward biased by a 10kΩ resistor R1.

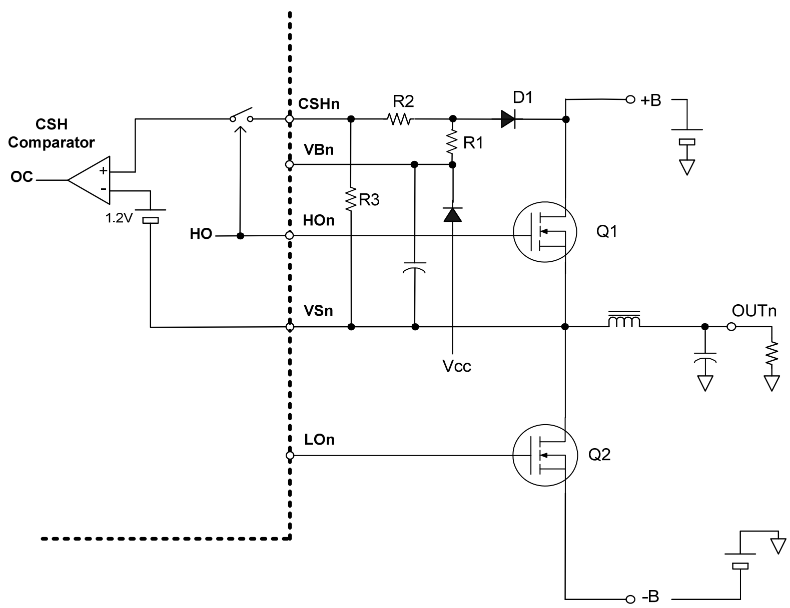

Figure 15 Programming High Side Over Current Threshold

4.2.4 High Side Over Current Setting

Figure 15 demonstrates the typical circuitry used for high side current sensing. In the following example, the over current protection level is set to trip at 30A using a MOSFET with an $R_{DS(on)}$ of 100mΩ. The component values of R2 and R3 can be calculated using the following formula:

Let R2 + R3=10 kΩ.

$$R_3 = 10k\Omega \cdot \frac{Vth_{OCH}}{V_{DS} + V_F}$$

where Vth_{OCL} = 1.2V
V_F = the forward voltage of reverse blocking diode D1 = 0.6V.
$V_{DS@ID=30A}$ = the voltage drop across the high side MOSFET when the MOSFET current is 30A.

Therefore, $V_{DS@ID=30A} = I_D \times R_{DS(on)}$ = 30A x 100mΩ = 3V

Based on the formulas above, R2 = 6.8kΩ and R3 = 3.3kΩ.

4.2.5 Choosing the Right Reverse Blocking Diode

The selection of the appropriate reverse blocking diode D1 depends on its voltage rating and speed. To effectively block bus voltages, the reverse voltage must be higher than the voltage difference between +B and –B and the reverse recovery time must be as fast as the bootstrap charging diode. A diode such as the NXP BAV21W, a 200V, 50ns high speed switching diode, is more than sufficient.

5 Over Temperature Protection

The three over temperature protection inputs OTP1, OTP2 and OTP3 monitor external PTC type temperature sensors. The PTC sensor can be arranged to monitor MOSFET temperatures on each channel. Each OTP pin supplies 0.6mA from an internal current source to bias an external PTC resistor. Over temperature protection is activated when the voltage at any OTP input pin goes higher than 2.8V.

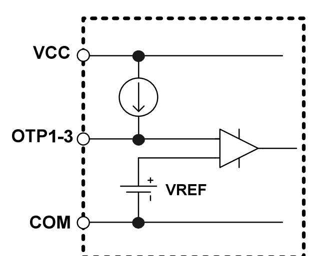

Figure 16 Over Temperature Protection Input Structure

6 DC Offset Protection

The DCP input detects excessive DC offset voltage at the speaker outputs and shuts down PWM operations. The DCP input is referenced to GND. If the input voltage exceeds the positive or negative detecting threshold, the DC offset protection shuts down PWM operations and reports a fault via the FAULT pin.

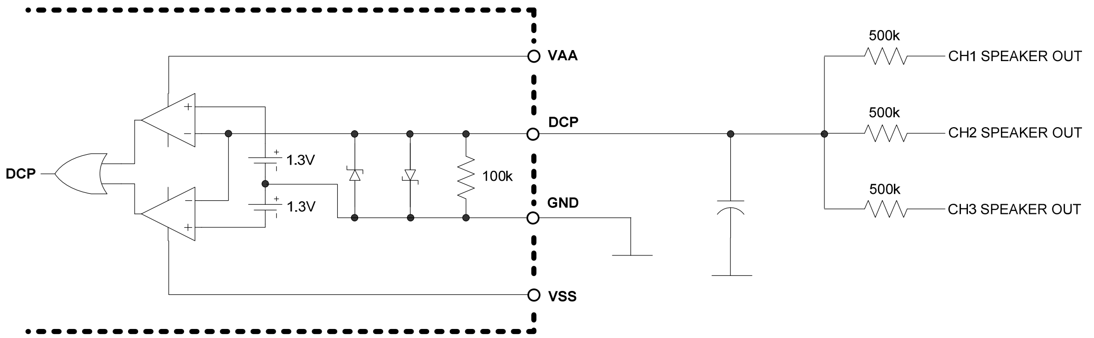

Figure 17 DC Offset Protection Input Structure

7 Fault Output

The FAULT output is an open drain output referenced to GND. Its purpose is to report whether the IRS2053M is in shutdown mode or in normal operating mode. If the FAULT pin is open, the IRS2053M is in normal operating mode.

8 CLIP Output

When the output of the amplifier looses track of an expected target value, the amplifier enters clipping condition. The purpose of the CLIP output is to flag this condition. The voltage at the COMP pin is monitored with a window comparator. The drain of an open drain MOSFET at the CLIP pin is pulled to GND for 1uS plus the clip detection time when a clipping condition is detected. The detection threshold at the COMP pin is set at 10% and 90% of VAA-VSS. Each channel has independent CLIP outputs. The CLIP outputs are disabled when the IRS2053M is in shutdown mode.

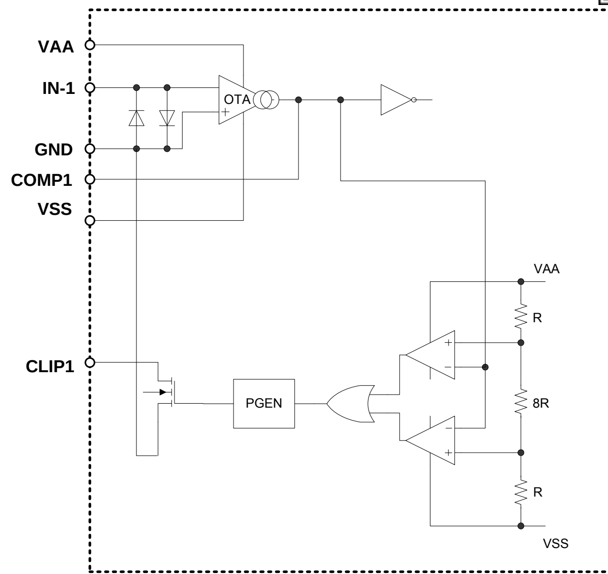

Figure 18 Clipping Detection

9 Deadtime Design

Dead time is the blanking period inserted between either high-side Turn-OFF and low-side Turn-ON, or low-side Turn-OFF and high-side Turn-ON. Its purpose is to prevent shoot through, or a rush of current through both MOSFETs. In the IRS2053M, an internal dead time generation block allows the user to select the optimum dead time from a range of preset values. Selecting a preset dead time through the DT pin voltage can easily be done through an external voltage divider. This way of setting dead time prevents outside noise from modulating the switching timing, which is critical to the audio performance.

9.1 How to Determine Optimal Deadtime

The effective deadtime in an actual application differs from the deadtime specified in this datasheet due to the switching fall time, tf. The deadtime value in this datasheet is defined as the time period between the beginning of turn-off on one side of the switching stage and the beginning of turn-on on the other side as shown in Figure 19. The fall time of the MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective deadtime of a Class D audio amplifier.

(Effective deadtime) = (Deadtime in datasheet) – tf

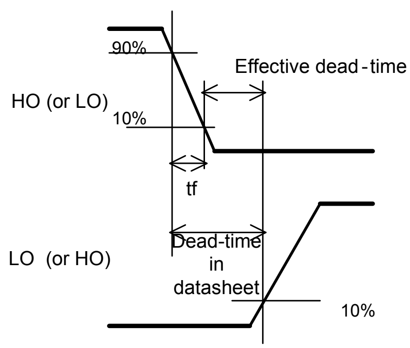

Figure 19 Effective Dead Time

A longer deadtime period is required for a MOSFET with a larger gate charge value because of the longer tf. Although a shorter effective, deadtime setting is beneficial to achieving better linearity in Class D amplifiers, the likelihood of shoot-through current increases with narrower deadtime settings. Negative values of effective deadtime may cause excessive heat dissipation in the MOSFETs, leading to potentially serious damage.

To calculate the optimal deadtime in a given application, the fall time tf for both HO and LO in the actual circuit need to be taken into account. In addition, variations in temperature and device parameters could also affect the effective deadtime in the actual circuit. Therefore, a minimum effective deadtime of 10ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

9.2 Programming Deadtime

The IRS2053M selects the deadtime from a range of preset deadtime values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined deadtime by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using V_{CC}. The relationship between the operation mode and the voltage at DT pin is illustrated in the Figure 20 below.

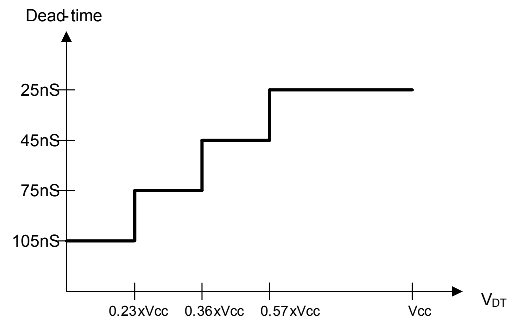

Figure 20 Deadtime vs. V_{DT}

Table 4 suggests pairs of resistor values used in the voltage divider for selecting deadtime. Resistors with up to 5% tolerance are acceptable when using these values.

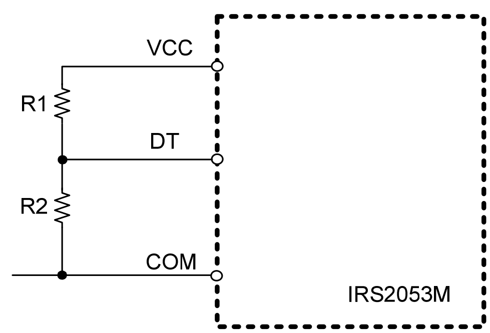

Figure 21 External Voltage Divider for DT Pin

Deadtime Mode	R1	R2	DT Voltage
DT1	<10k	Open	Vcc
DT2	5.6kΩ	4.7kΩ	0.46 x Vcc
DT3	8.2kΩ	3.3kΩ	0.29 x Vcc
DT4	Open	<10k	COM

Table 4 Recommended Resistor Values for Dead Time Selection

10 Power Supply Considerations

10.1 Supplying V_{AA} and V_{SS}

For best audio performance, it is preferred to produce V_{AA} and V_{SS} with external regulators, such as the three terminal regulators. Standard 7805 and 7905 regulators are suitable.

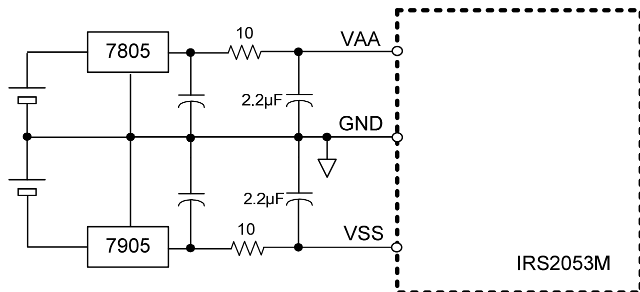

Figure 22 Supplying V_{AA} and V_{SS} with External Regulators

When switched mode regulators provide V_{AA} and V_{SS}, it is required to place a two-stage noise filter in the supply lines as shown in Figure 23 to prevent noise from influencing the switching ripple voltage on +/-5V.

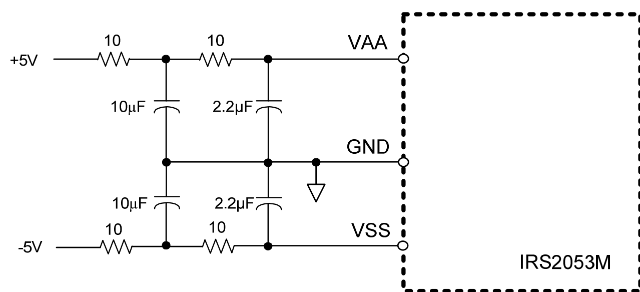

Figure 23 Supplying V_{AA} and V_{SS} from Switched Mode Power Supply

10.2 Recommended Power Supply Configuration for Gate Driver Stage

Figure 24 shows the recommended power supply configuration for gate driver power supplies. Gate driver stage has five power supply inputs.

1. VB1-VS1: CH1 high side gate drive supply
2. VB2-VS2: CH2 high side gate drive supply
3. VB3-VS3: CH3 high side gate drive supply
4. VCC-COM: low side logic supply
5. VCC2-COM2: CH1-3 low side gate drive supply

R_{VBS1} - R_{VBS3} prevent C_{VBS1} – C_{VBS3} from over-charging due to under shoots in VS1 – VS3. R_{VBS1} - R_{VBS3} reduce switching noise triggered by Qrr of bootstrap diode D_{BS1} – D_{BS3} .

All power supplies except VCC-COM generate switching noise. R_{VCC2} isolates the switching noise from low side gate drive current and bootstrap charge pump current feeding into VCC. These optional filtering resistors are effective to achieve best audio performance in higher power applications (>100W).

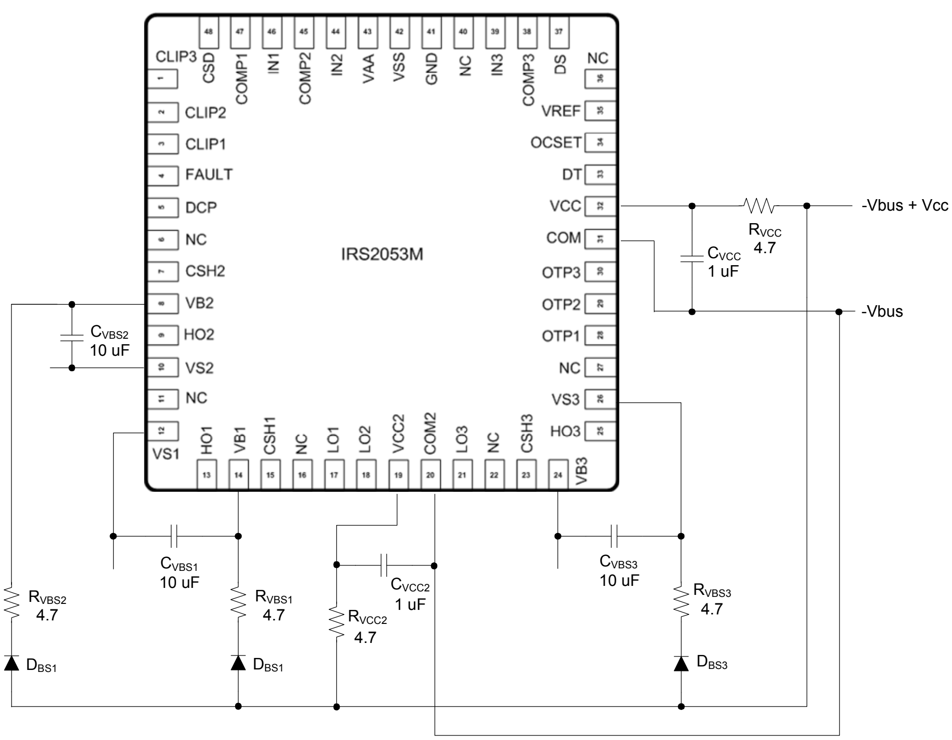

Figure 24 Recommended Power Supply Configurations for Gate Driver Stage

10.2.1 V_{CC} and V_{CC2}

The Non-floating section of IRS2053M has two supply voltages, VCC and VCC2. The VCC is paired with COM to supply logic and small signal circuitries. The VCC2 and COM2 feed power to LO1-3 low side gate drive stages.

It is recommended to supply both VCC and VCC2 from a single supply source. VCC must be equal or higher than VCC2, but no more than 5V.

10.2.2 COM and COM2

COM and COM2 must be tied to each other in as short a distance as possible.

10.2.3 Bottom Pad Connection

The Exposed bottom pad in the MLPQ48 package where the IC die sits has the same voltage potential as COM and COM2. However, it is not directly connected inside. The pad may be tied to COM and COM2 with short distance trace(s), or may be floated. Do not use the bottom pad as the low side power supply return path.

10.3 Designing High-side Bootstrap Power Supply

The high-side driver requires a floating supply VBn referring to respective switching node VSn where the source of the MOSFET is connected. A charge pump method (floating bootstrap power supply) eliminates the need of a floating power supply and thus is used in the typical application circuit.

10.3.1 Floating Bootstrap Power Supply

The floating bootstrap power supply charges bootstrap capacitor C_{BS} from the low-side power supply VCC during the low-side MOSFET ON period. When the high-side MOSFET is ON, the charging diode turns off to float the VBS supply. C_{BS} retains its voltage as a floating power supply referenced to VS. Before C_{BS} discharges and VBS crosses the under voltage lock out threshold UVBS, the next charging cycle should start by turning on the low-side MOSFET.

Figure 25 depicts the low-side MOSFET ON state. I_1 turns off the high-side MOSFET first, then I_2 turns on the low side the MOSFET. As soon as switching node VS reaches negative supply –B, the bootstrap diode D_{BS} turns on and starts charging C_{BS} with current I_3 from VCC. Note that VBS = VCC – (forward drop voltage of D_{BS}).

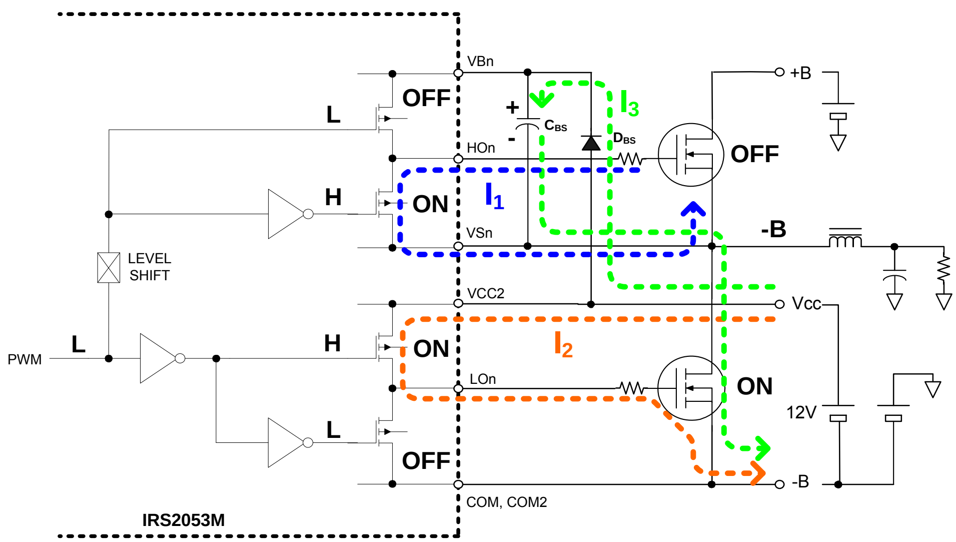

Figure 25 Charging VBS: Low-side ON Period

After the low-side conduction period, I4 in Figure 26 turns off the low-side MOSFET. Then I_5 turns on the high-side MOSFET, lifting VS up to +B. As long as the high side is ON, the bootstrap diode D_{BS} isolates the floating power supply VBS.

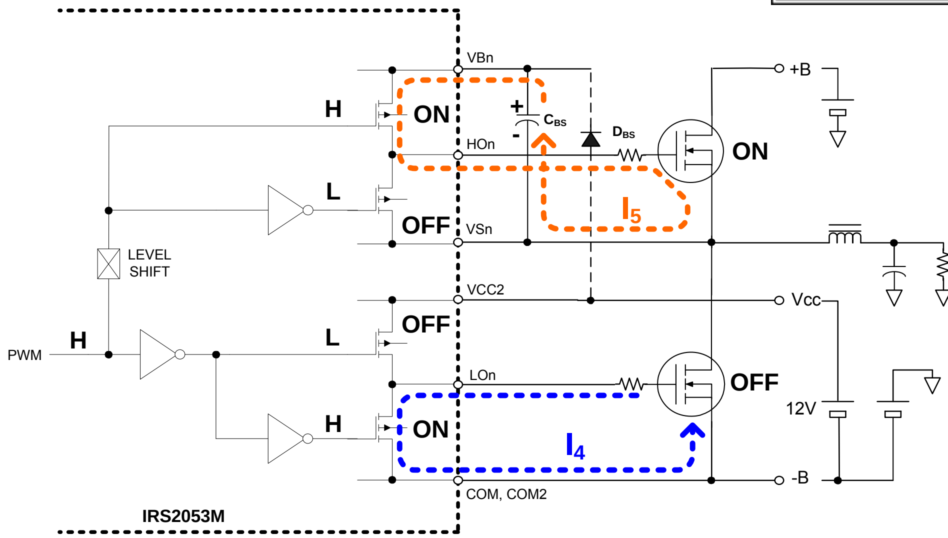

Figure 26 High-side ON Period

10.3.2 Choosing Bootstrap Capacitance

Since a MOSFET is a voltage driven device, I_5 is only to fill up the gate charge of the high-side MOSFET during the rising edge that is a one time event for entire high-side MOSFET on-time. After that, no more current flows from C_{BS}. In spite of that, the high-side gate driver stage in the IRS2053M has quiescent current consumption I_{QBS} to drain the charge of C_{BS} during the high-side MOSFET ON-time. High-side sensing bias current I_{R1} via detecting diode D1 is another current to take into considerations. (Figure 28) Normally, leakage current in the gate of a MOSFET is negligibly small compared to the I_{QBS} and I_{R1}.

The minimum bootstrap capacitance is determined as follows.

$$C_{BS} >> \frac{(I_{QBS} + I_{R1}) \cdot t_{ON}}{VCC - 1.5 - UVBS}$$

Where C_{BS}: floating bootstrap capacitance [F]
I_{QBS}: high-side quiescent current [A]
I_{R1}: high-side current sensing bias current [A]
t_{ON}: longest high-side MOSFET conduction time [s]
VCC: low-side power supply voltage [V]
UVBS: high-side under voltage lockout threshold [V]
1.5: voltage drop in the bootstrap charging diode D_{BS}

The bootstrap capacitor sees the VCC supply voltage. A ceramic capacitor (X7R, X5R or X5S type) or aluminium electrolytic capacitor with 25V or higher voltage rating is recommended.

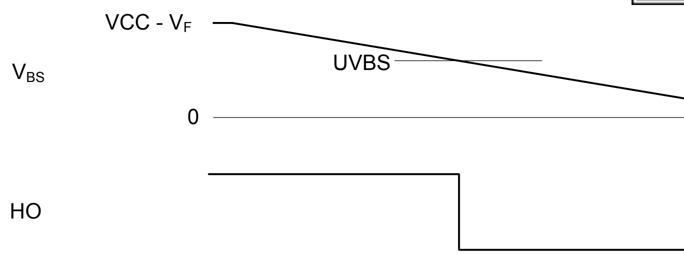

Figure 27 V_{BS} Discharging

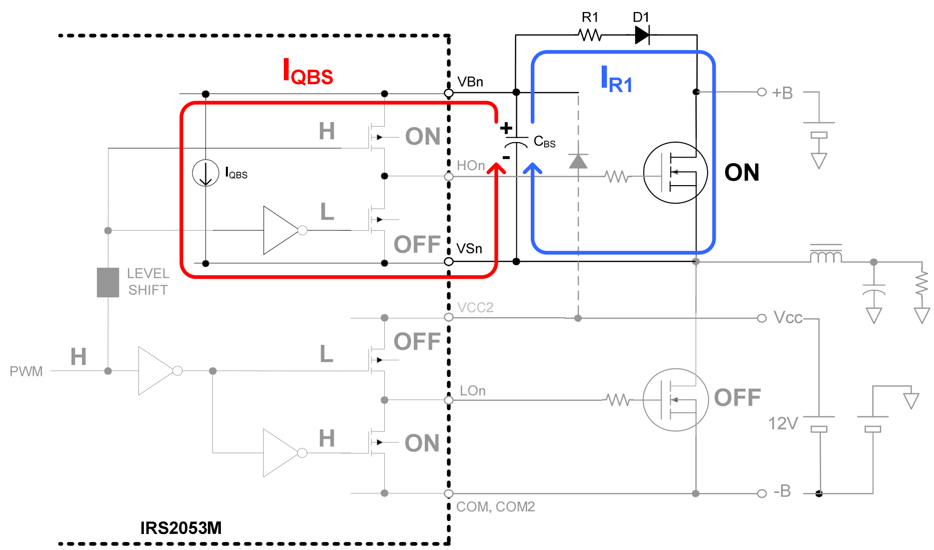

Figure 28 C_{BS} Discharging During High-side ON Period

10.3.3 Choosing Bootstrap Diode

The bootstrap diode blocks bus voltage (+B)-(-B) + (voltage overshoot), therefore a diode with voltage rating of 1.5 x bus voltage is a minimum requirement. In order to charge the bootstrap capacitor in a very short low-side ON period in a high PWM modulation ratio, a fast recovery type is necessary. One with a short reverse recovery time of trr<50ns is recommended.

10.3.4 Damping Resistor

Inserting a damping resistor in series with bootstrap diode D_{BS} is an effective way to eliminate the following potential problems in bootstrap power supply design.

- EMI noise due to reverse recovery charge of the bootstrap diode; note that this diode is a switching device for the charge pump
- Overcharge to bootstrap supply capacitor C_{BS}

Figure 29 explains how the floating supply voltage VBS is over charged by a negative spike on VS voltage that is induced by stray inductances in –B feeding line. Generally, a 1 to 5 ohms resistor helps to prevent these issues.

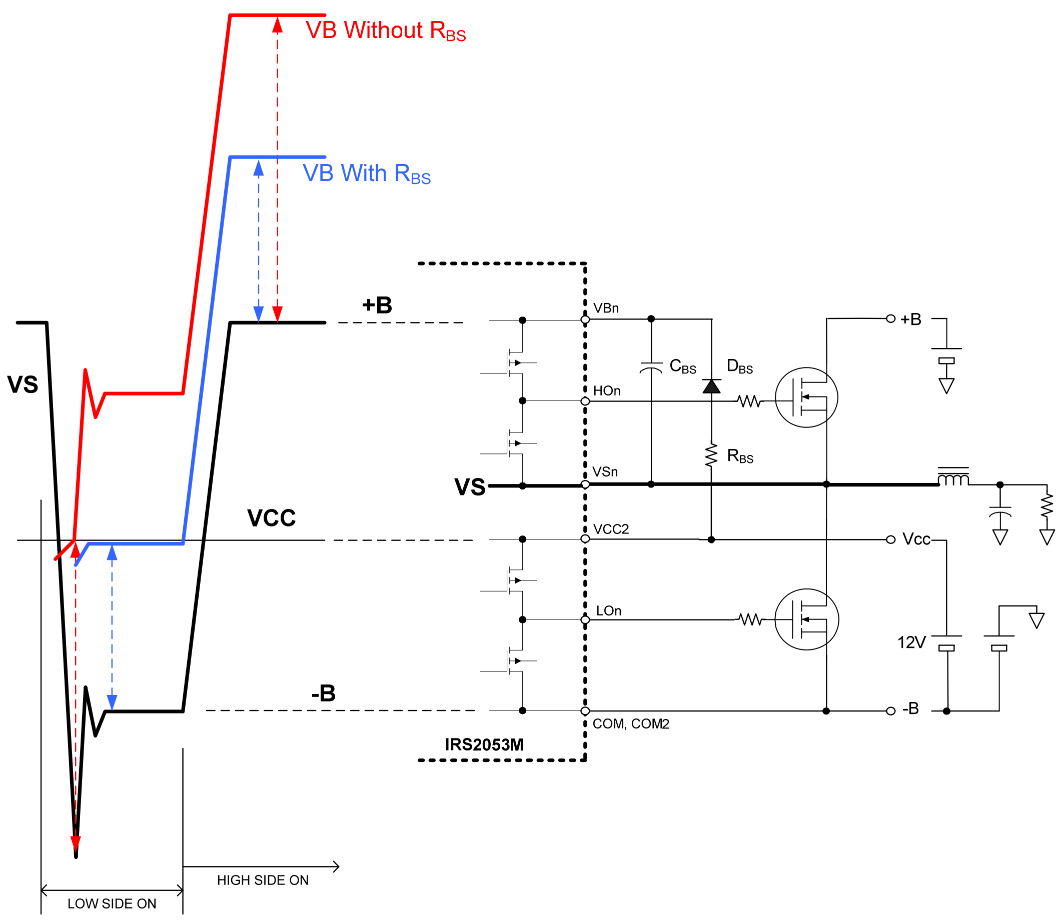

Figure 29 V_{BS} Charging With and Without R_{BS}

10.3.5 Charging V_{BS} Prior to Start

For proper start-up, it is necessary for the high side bootstrap capacitor be charged prior to PWM start-up through a resistor R_{CHARGE} from the positive supply bus to the V_B pin. By utilizing an internal 15.3V Zener diode between V_B and V_S, this scheme eliminates the need to charge the boot strap capacitor through low side turn on during start up.

The value of this charging resistor is subject to several constraints:

- The minimum resistance of R_{CHARGE} is limited by the maximum PWM modulation index of the system. When HO is high, R_{CHARGE} drains the bootstrap power supply so it reduces holding up time, hence maximum continuous HO on time.
- The maximum resistance of R_{CHARGE} is limited by the current charge capability of the resistor during startup:

  $I_{CHARGE} > I_{QBS}$

  where I_{CHARGE} = the current through R_{CHARGE}
  I_{QBS} = the high side supply quiescent current.

I_{CHARGE} generates a DC offset at the speaker output prior to PWM start up. Check that the DC offset does not exceed a condition for click noise elimination. See Click Noise Elimination section for more detail.

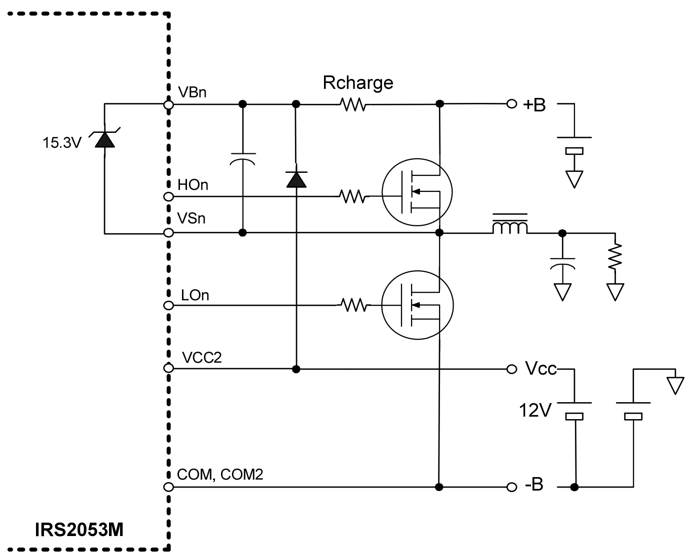

Figure 30 Boot Strap Supply Pre-charging

10.4 Start-up Sequence (UVLO)

The protection control block in the IRS2053M monitors the status of V_{AA} and V_{CC} to ensure that both voltage supplies are above their respective UVLO (under- voltage lockout) thresholds before beginning normal operation. If either V_{AA} or V_{CC} is below the under voltage threshold, LO and HO are disabled in shutdown mode until both V_{AA} and V_{CC} rise above their voltage thresholds.

10.4.1 Power-down Sequence

As soon as V_{AA} or V_{CC} falls below its UVLO threshold, protection logic in the IRS2053M turns off LO and HO, shutting off the power MOSFETs.

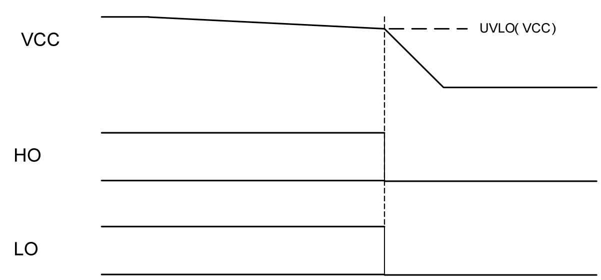

Figure 31 IRS2053M UVLO Timing Chart

10.5 Power Supply Decoupling

Because the IRS2053M contains analog circuitry, careful attention must be given to decoupling the power supplies for proper operation of the IC. Ceramic capacitors minimum of 0.1µF or aluminium capacitors minimum of 1uF should be placed close to the power supply pins of the IC on the board. Due to large capacitance variations, Y5V dielectric or similar type ceramic capacitors are not recommended.

Please refer to the application note AN-978 for general design considerations of a high voltage gate driver IC.

11 Junction Temperature Estimation

The power dissipation in the IRS2053M is dominated by the following items:

- P_{MID}: Power dissipation of the input floating logic and protection circuitry
- P_{LSM}: Power dissipation of the Input Level Shifter
- P_{LOW}: Power dissipation in low side
- P_{LSH}: Power dissipation of the High-side Level Shifter
- P_{HIGH}: Power dissipation in high side

The following equations are for reference only. Because of the non-linear characteristics in gate drive stage, these assumptions may not be accurate.

11.1 P_{MID}: Power Dissipation of the Input Floating Logic and Protection Circuitry

The power dissipation of the input floating section is given by:

$$P_{MID} = (V_{AA} - V_{SS}) \cdot I_{QAA1}$$

Where

I_{QAA1} = floating input section quiescent supply current in normal operation mode

11.2 P_{LSM}: Power Dissipation of the Input Level Shifter

$P_{LSM} = 1.5 \times 10^{-9} \times f_{SW} \times V_{SS\ BIAS} \times 3$

Where

f_{SW} = the PWM switching frequency
$V_{SS\ BIAS}$ = the bias voltage of V_{SS} with respect to COM

11.3 P_{LOW}: Power Dissipation of Low Side

The power dissipation of the low side comes from the losses of the logic circuitry and the losses of driving LO.

$$P_{LOW} = P_{LDD} + 3 \cdot P_{LO}$$

$$= (I_{QCC} \cdot V_{CC}) + 3 \cdot \left(Vcc \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\text{int})}} \right)$$

Where

P_{LDD} = power dissipation of the internal logic circuitry

P_{LO} = power dissipation from of gate drive stage for LO

R_O = output impedance of LO, typically 20 Ω for the IRS2053M

$R_{g(int)}$ = internal gate resistance of the low side MOSFET, typically 2Ω

R_g = external gate resistance of the low side MOSFET

Qg = total gate charge of the low side MOSFET

11.4 P_{LSH}: Power Dissipation of the High-side Level Shifter

P_{LSH} = 0.4nC x fsw x V_{BUS} x 3

Where

f_{SW} = PWM switching frequency
V_{BUS} = difference between the positive bus voltage and negative bus voltage

11.5 P_{HIGH}: Power Dissipation of High Side

The power dissipation of the high side comes from the losses of the logic circuitry and the losses of driving HO.

$$P_{HIGH} = 3 \cdot (P_{LDD} + P_{HO})$$

$$= 3 \cdot \left(I_{QBS} \cdot V_{BS}\right) + 3 \cdot \left(V_{BS} \cdot Q_g \cdot f_{SW} \cdot \frac{R_O}{R_O + R_g + R_{g(\mathrm{int})}}\right)$$

Where

P_{LDD} = power dissipation of the internal logic circuitry

P_{HO} = power dissipation of the gate drive stage for HO

R_O = equivalent output impedance of HO, typically 20 Ω for the IRS2053M

$R_{g(int)}$ = the internal gate resistance of the high side MOSFET, typically 2Ω

R_g = external gate resistance of the high side MOSFET

Qg = total gate charge of the high side MOSFET

11.6 P_D: Total Power Dissipation

Total power dissipation, P_D, is given by

$$P_D = P_{MID} + P_{LSM} + P_{LOW} + P_{HSM} + P_{HIGH} \cdot$$

11.7 T_J: Junction Temperature

Given junction to ambient thermal resistance Rth_{JA}, the junction temperature T_J can be calculated from the formula provided below and must not exceed 150°C.

$$T_J = [Rth_{JA} \cdot P_d + T_A] < 150°C$$

12 Board Layout Considerations

The floating input section of the IRS2053M consists of a low noise OTA error amplifier and a PWM comparator along with CMOS logic circuitry. The high frequency bypass capacitor $C_{VAA\text{-}VSS}$ should be placed closest to the IRS2053M to supply the logic circuitry. C_{VAA} and C_{VSS} are for stable operation of the OTA and should be placed close to the IC.

Gate driver supply capacitors C_{VCC}, C_{VCC2}, C_{VBS1}, C_{VBS2} and C_{VBS3} provide gate-charging current and should also be placed close to the IRS2053M.

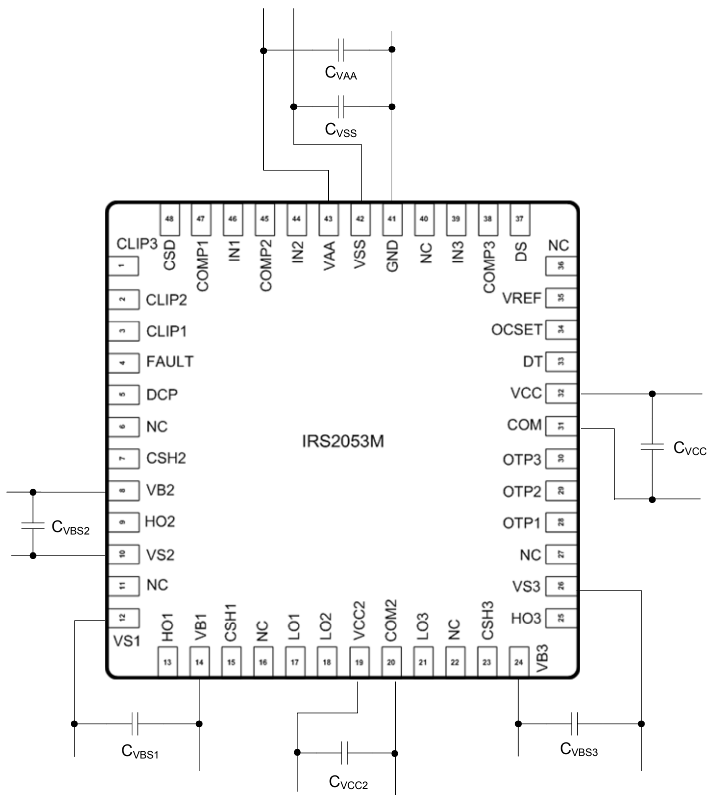

Figure 32 Placement Sensitive Bypass Capacitors

12.1 Ground Plane

In addition to the key component locations mentioned above, it is important to properly pour ground planes to obtain good audio performance. Since each functional block within the IRS2053M refers to different potentials, it is recommended to apply three reference potentials.

12.1.1 Analog Ground

The Input analog section around the OTA is referenced to the signal ground, or GND, which should be a quiet reference node for the audio input signal. The peripheral circuits in the floating input section such as CSD and COM pins refer to this ground. These nodes should all be separate from the switching stages of the system. In order to prevent potential capacitive coupling to the switching nodes, use a ground plane only in this part of the circuit. Do not share the ground plane with gate driver or power stages.

12.1.2 Gate Driver Reference

The gate driver stage of the IRS2053M is located between pins 7 and 30 and is referenced to the negative bus voltage, COM and COM2. This is the substrate of the IC and acts as ground. Although the negative bus is a noisy node in the system, both of the gate drivers refer to this node. Therefore, it is important to shield the gate drive stages with the negative bus voltage so that all the noise currents due to stray capacitances flow back to the power supply without degrading signal ground.

12.1.3 Power Ground

Power ground is the ground connection that closes the loops of the bus capacitors and inductor ripple current circuits. Separate the power ground and input signal grounds from each other as much as possible to avoid common stray impedances.

Figure 33 illustrates how to paint out reference planes. The power GND plane should include a negative bus cap. Power reference plane should include Vcc. Also, use distinctly different symbols for the different grounds.

For further board layout information, refer to AN-1135, PCB Layout with IR Class D Audio Gate Drivers

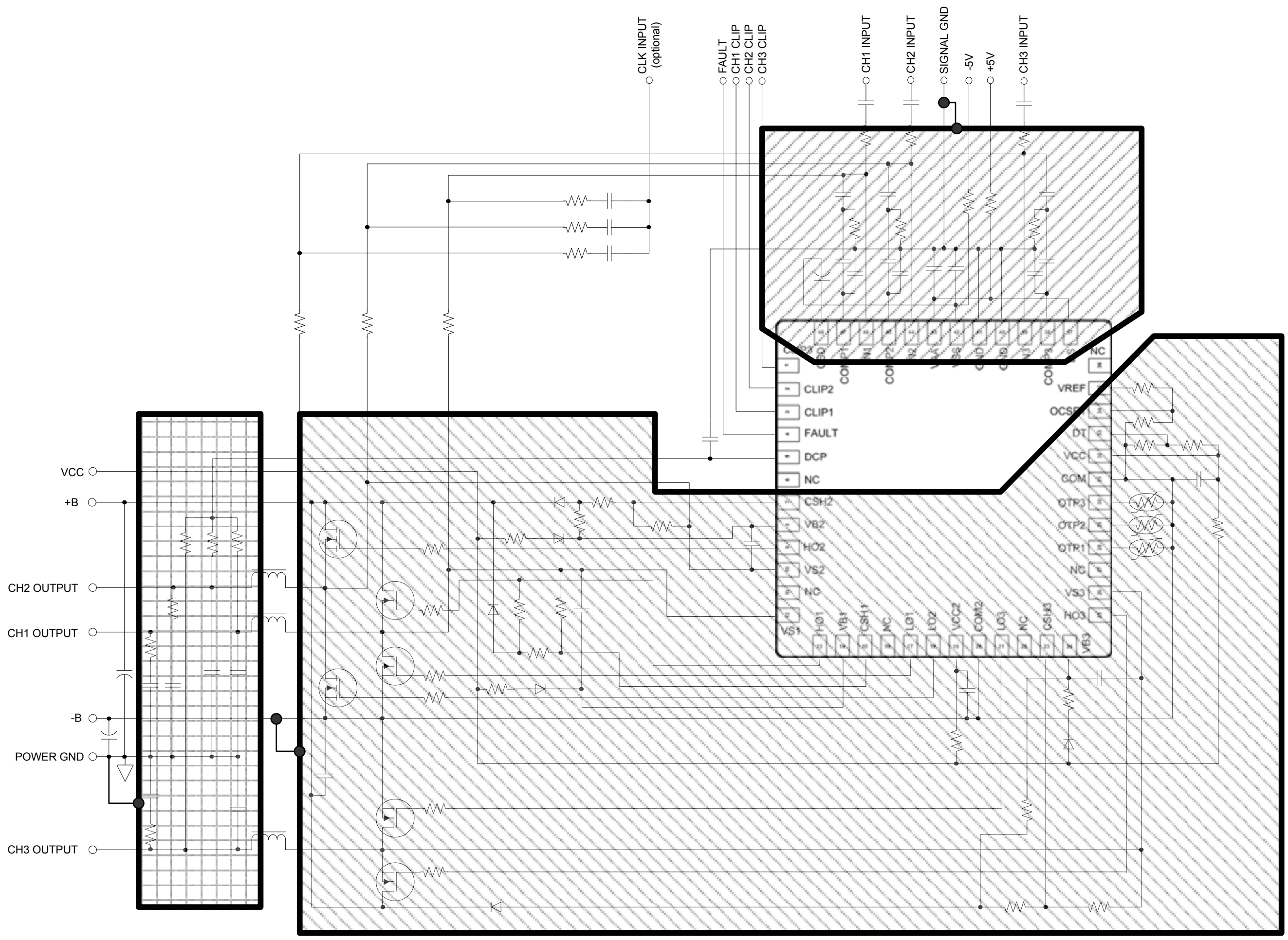

Figure 33 Applying Ground Planes

Revision History

Date	Change
1/22/2010	Initial issuance
2/27/2010	Proofread
6/9/2010	Added Events and Fault table