Electrothermal Subcircuits for LTspice

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Standard SPICE models for the BJT, MOSFET, Diode, JFET, and IGBT are isothermal models which means they operate at a fixed temperature during each run.

For audio power amplifier simulations we need to use electrothermal subcircuits to simulate thermal-runaway, current hogging and transient thermal distortion such as thermal lag distortion in Class-AB amplifiers.

This paper covers 5 electrothermal subcircuits for BJTs, MOSFETs, JFETs, Diodes and IGBTs in LTspice. They are clip-on subcircuits which means they are placed over the top of existing isothermal BJT's, etc, to make them behave like electrothermal devices.

Five Clip-on subcircuits or 'widgets' for LTspice

The 5 subcircuits and assemblies are:

	BJT	**MOSFET**	**Diode**	**JFET**	**IGBT**
Assembly	QthB.asy	MthB.asy	DthB.asy	JthB.asy	IGBTthB.asy
Subcircuit	QthB.asc	MthB.asc	DthB.asc	JthB.asc	IGBTthB.asc
Original .asy	npn.asy, pnp.asy	nmos.asy, pmos.asy	D.asy	njf.asy, pjf.asy	IGBT_B.asy*

* IGBT_B.asy is my custom isothermal subcircuit – see **Section 5** IGBT and **Appendix 5**.

When you drop these subcircuit assemblies onto your original devices it cuts the wires leading to the devices and wires it into the subcircuit. This can be seen by removing U1 as shown in **Figure 1**. The original isothermal MOSFET is on the left. The clip-on (with dotted lines) is added giving the third assembly. Then to illustrate what has happened we remove the clip-on subcircuit to see on the RHS that the wires have been cut by the subcircuit.

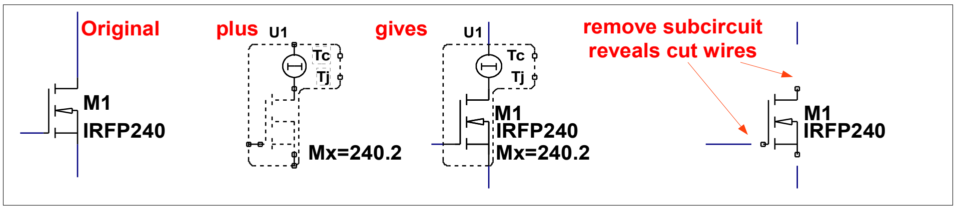


Figure 1. LTspice clip-on subcircuit for a MOSFET. RHS reveals cut wires by placing U1 on M1.

BTW: If after adding the electrothermal subcircuit you would like to remove them, then you rejoin the wires and you are back to the original (isothermal) circuit.

5 Generic electrothermal subcircuits for LTspice

A generic subcircuit is one that can be used for any part number just like the SPICE in-build models do for the BJT, MOSFET, etc. Of my 5 generic subcircuits, the BJT is the easiest to use, so it is covered first.

1. Using the BJT electrothermal subcircuit – QthB

The internals of the QthB subcircuit is shown in **Appendix 1** since this section is a basic tutorial.

This section covers the basics of how to use it.

'Q' is the designator for BJT's in SPICE. The 'B' in QthB means it is a **Block subcircuit,** which is the LTspice term for a subcircuit created as a schematic and assigned to an assembly of the same name. The Block form is human readable and probing of voltages and current are possible and you can see how it works [footnote [1]].

The QthB subcircuit uses **linear interpolation** of currents between two isothermal BJTs:

1) the original "cold" transistor, and
2) a BJT in the subcircuit which runs "hot" at temperature Tj2.

Collector currents and base currents are interpolated using **6 multipliers** using the Poly(2) source [footnote [2]].

1 To save subcircuit currents you need to have turned on the save node V's and I's in Control Panel>Save Defaults.
2 'Bi' Behavioural sources can be used instead of Poly(2) sources. Poly(2) sources as multipliers (usually) result in less

The QthB subcircuit (same as for all my other subcircuits) use a **thermal model** made from a RC ladder to simulate the thermal resistance from the junction to case. The RC thermal model is based on the IRFP9640 [ref: IRF9640 thermal model Vishay Application Note 90298] which has a TO-220 case and it's thermal properties are **scalable** to suit other cases such as TO-246 for the NJL3281 and IRFP240, or even scale for TO-92's and SMD's. It uses 4 R's and 5 C's [footnote [3]].

The thermal washer and the heatsink are added outside the subcircuit on the main circuit with 3 R's and 1 C for each package. When several devices share one main heatsink the heatsink properties are **subdivided** per device – e.g. if two TO-264 devices share a 0.5C/W heatsink, then each device is assigned 1 °C/W thermal resistance and the 'C' value (for thermal inertial) is scaled by half using the equation for capacitance `Cs=Ts/Rsa` , where Ts is the user parameter chosen for the heatsinks *Time constant* (usually **Ts is shrunk in time** so the simulation can reach 99% of final temperature in 10 seconds real time which may be 1-5 minutes of PC time (depending on your circuit) .

Figure 1.2 shows the demo jig comparing the original MJL3281 (LHS) to the electrothermal subcircuit (RHS). **Figure 1.3** shows the plots for currents and the models Tj changing as the input sweep progresses over 1 second, eventually reaching 400°C.

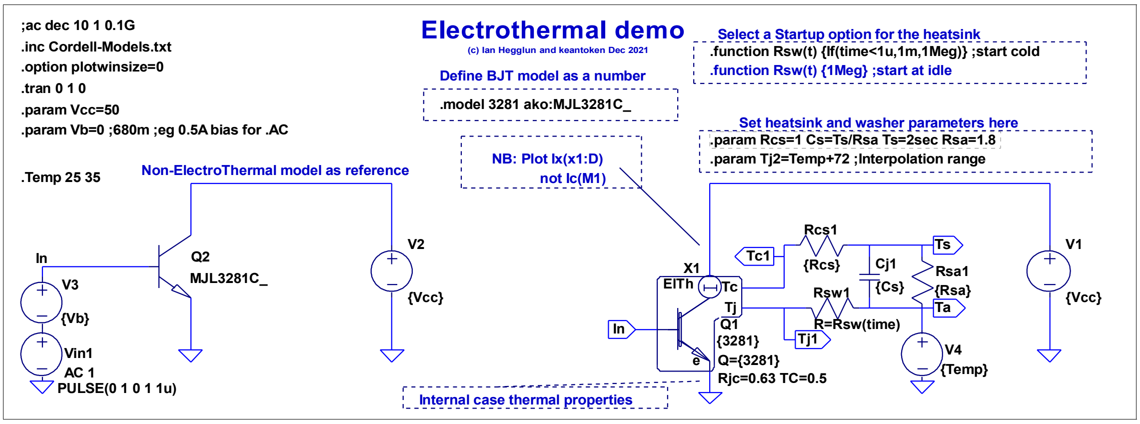


Figure 1.2. Demo jig comparing the original BJT (LHS) to the electrothermal subcircuit (RHS)

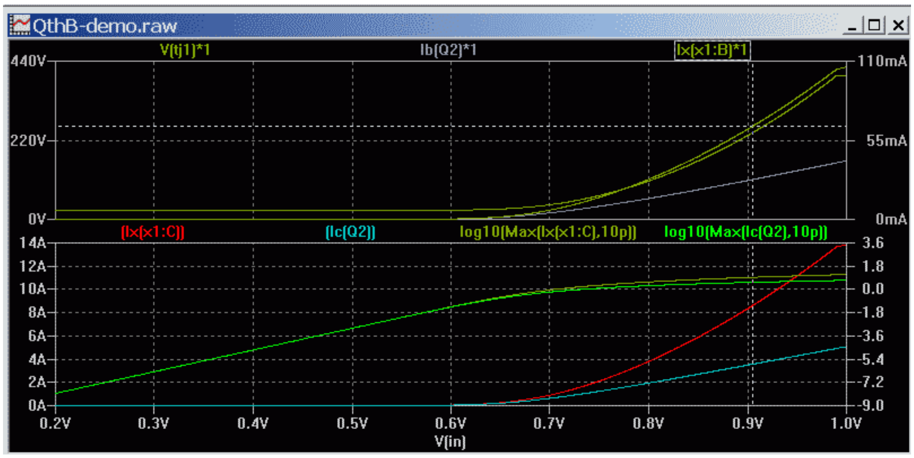


Figure 1.3. Demo jig plots for the original BJT Ic(Q2) to the electrothermal subcircuit Ix(x1:C)

Notice the electrothermal subcircuit current Ix(x1:C) (red) has significantly higher current than the isothermal model. Notice the electrothermal model reaches 13A while the isothermal reaches 4A. This difference is due to the junction heating up during the input sweep. It is effectively "thermal runaway". This electrothermal plot is what happens in real transistors with relatively slow input sweeps.

For datasheet plots the sweep time is made very fast (10us to 100us). This is necessary so the junction temperature does not change by a significant amount. All original SPICE models are based on isothermal plots.

In real amplifiers the junction temperature can change significantly during one cycle when the lowest audio

convergence issues than Bi and Bv sources. The Help file suggests Bv sources be avoided for convergence reasons.

3 With a scalable model you don't change each R and C individually, they are all scaled by 2 parameters Rjc and Tc.

frequency is used (20Hz). But does this temperature change affect THD much in real amplifiers? And if so, is it audible? [footnote [4]]. Electrothermal simulations can now answer this question. Any bets? [footnote [5]].

Even if thermal distortion doesn't affect sound quality amps there is still the need for electrothermal simulations to check bias time-lag in Class-AB bias sensors (a.k.a. Thermal lag Distortion or TLD), and to check SOA, and to check for current hogging with parallel power transistors.

Back to the jig in **Figure 1.2**, you can see how the external thermal RC components are 'wired' to the subcircuit and how they are defined as parameters [footnote [6]]. The label **`{3281}`** replaces the label for Q1 (originally '**`MJL3281C_`**').

The label **`Q={3281}`** applies to the BJT inside the subcircuit. The label **`Rjc=0.63 TC=0.5`** applies to the subcircuit thermal model for a TO-264 case. These thermal parameters are entered using into the "**`PARAMS`**" dialogue area using RtClk on the subcircuit circle. The tick box allows it to be displayed or hidden from view on the main circuit.

The parameter card **`.param Tj2=Temp+72`** sets the interpolation range. The value of "72" is the largest that LT-XVII appears to run with, possibly due to a numerical range bug? [footnote [7]] But LT-IV appears to accept values up to 200°C.

The resistor 'Rsw1' has value R=Rsw(time) which has a low resistance of 1mΩ [footnote [8]] for the first 1us for the start of a transient run (10 seconds). This **disables the thermal model** while LTspice finds the operating point. It forces Tj = Temp, effectively isothermal for the first 1us. After 1us the value of R changes to 1MΩ which enables the electrothermal model.

The switch resistor is a custom function **`.function Rsw(t) {If(time<1u,1m,1Meg)}`** for starting from cold (Temp default is 27°C) [footnote [9]]. You can deselect this function and enable the alternative **`.function Rsw(t) {1Meg}`** to start *warmed up at idle* (that's with no input signal) [footnote [10]].

The BJT is area scalable by factor **`m`** and when it not specified it defaults to unity. Area scaling factors are useful for sensitivity analysis with variable device parameters and when devices are paralleled to check for current sharing of slightly different device gains.

That's the basics for using the BJT electrothermal subcircuit. I suggest you run the demo files for the BJT. You can see how to do an AC plot. You can see how to do the PNP – notice you need to add the parameter **`PNP=1`** giving

```
Q={1302} PNP=1
```

with a space between them.

2. MOSFET electrothermal subcircuit

The MthB subcircuit can be viewed in **Appendix** 2 since this section is a basic tutorial.

4 Low order 2nd and 3rd harmonic distortion in the low frequency range (<100Hz) is only audible above a few percent!

5 I bet thermal distortion isn't audible in most of our amplifiers that use lots of negative feedback. And I bet thermal distortion may audible in some amplifiers that use *very little* negative feedback. BTW 'Absolutely no negative feedback amplifiers' do not exist in reality due to small amounts of feedback even when we don't deliberately apply any negative feedback, like parasitic emitter resistance of the bond wires and metallisation. There is also thermal feedback from self-heating and thermal couplings. Perhaps it is necessary to call designs that do not deliberately apply any negative feedback 'no added negative feedback amplifiers' ? Any other suggestions?

6 For an introduction see Bob Cordell's Power Amplifier book 2nd Ed. p384-389 for Thermal models using resistors and capacitors (RC) equivalent models to represent heatsink thermal resistance and heat capacity respectively.

7 From what I have heard and found, is LT-XVII uses exactly the same code as LT-XVII for the engine, only the GUI and plotting code was changed. If in LT-XVII the Tj does exceed Temp+72 (or '99' total at 27°C) the interpolation becomes extrapolation and the effect of Tj changing is less accurate than interpolation. If you want to see if the errors are OK then install LT-IV in a separate directory and set Tj2 to the largest Tj.

8 I found 1µΩ was too low – it made finding the operating point very slow or even couldn't find it – 1mΩ works well.

9 It has an abrupt change at 1µs but this does not seem to matter so a smooth function is apparently not need. For a smooth function the DnLim(x,y,z) can be used (or is it UpLim)?

10 If starting at idle can't find the operating point you can use the first function from cold and run for 10 seconds with no input signal (using delay 10s in the signal voltage source) and then another 10 seconds with the input signal. Using .trans of 20 seconds.

MOSFET thermal parameters are passed into the **generic subcircuit** using the "`PARAMS`" (using RtClk on the subcircuit circle) **Figure 2.1** [footnote [11]]. For the IRFP240 MOSFET the parameters are: **`VtoTc=-6m Rjc=0.8 TC=0.5`**

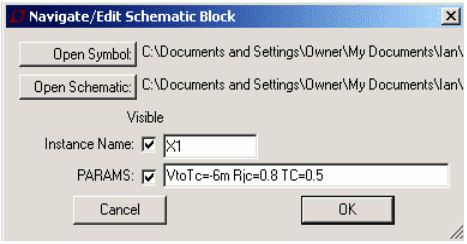


Figure 2.1. Entering parameters for the MthB subcircuit

Figure 2.2 shows the demo jig that compares the original IRFP240 (LHS) to the electrothermal subcircuit (RHS). **Figure 2.3** shows the plots for currents and the models junction temperature changing as the input sweep progresses over 0.5 second (3V to 6V input sweep), eventually reaching 120°C.

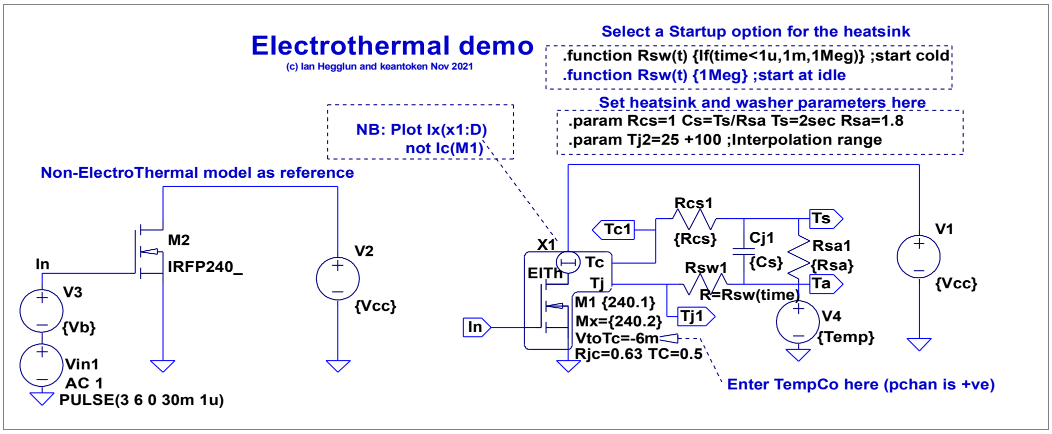


Figure 2.2. Demo jig comparing the original MOSFET (LHS) to the electrothermal subcircuit (RHS)

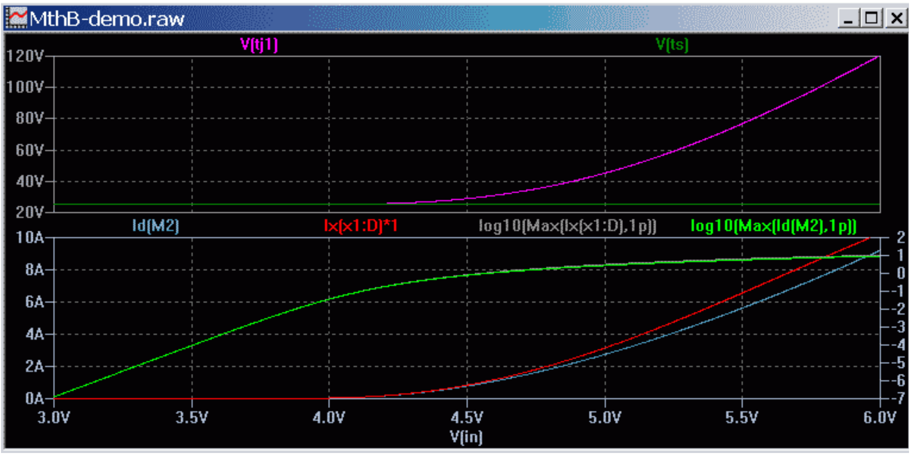


Figure 2.3. Demo jig plots for the original MOSFET Id(M2) to the electrothermal subcircuit Ix(x1:D)

Notice the subcircuit has the model number passing as **`Mx={240.2}`**, where 'Mx' is used instead of 'M' because '**`m`**' is already used for MOSFET area scaling and SPICE is not case sensitive. The 'x' in Mx is used because X is the designator for subcircuits.

The designator for the original MOSFET (M1) in Figure 2.2 has been changed to **`{240.1}`** where curly **braces are necessary** to tell SPICE to look up the model associated with that number [footnote [12]].

The designator for the subcircuit MOSFET (X1) in Figure 2.2 is **`{240.2}`** and the curly braces are not necessary in this instance (but are used here so you don't need to remember which one needs braces).

The decimal points in these designators are different because they are for cold (**`x.1`**) and hot (**`x.2`**) operating

11 Alternatively, entering parameters in the "SpiceLine" (using Ctrl+RtClk).
12 Changing M1 name to a number is my preferred option as it is more compact and can be placed beside 'M1' {xxx}.

temperatures, namely 'Temp' for the cold original MOSFET and Tj2 for the hot MOSFET. The definitions for these MOSFETs are:

```
.model 240.1 ako:IRFP240_ Vto={4.0-(0*6m-1m)*(Temp-25)}
.model 240.2 ako:IRFP240_ Vto={4.0-(0*6m-1m)*(Tj2-25)}
```

These definitions work on both LT-IV and LT-XVII. They are the definitions I use in my simulations.

However, the LT-XVII MOSFET models are **simpler** like the BJT subcircuit above. LTXVII MOSFET models need **only one definition** and no decimal points, we can simply use:

```
.model 240 ako:IRFP240h VtoTc=0
```

For the LT-XVII vdmos the original MOSFET (M1) and the subcircuit (X1) can both use the **same definition** [footnote [13]].

Notice how **:ako** model statements [footnote [14]] above allow models to be used from an existing library. This is a definite improvement on my earlier approach where I created special modified library models (which is cumbersome and they all need updating when the main model is updated). KISS.

For p-channel's, you don't need to enter a switch parameter (unlike BJT's … **PNP=1** switch). Instead, you change the VtoTc coefficient as a <u>positive</u> parameter for the p-channel MthB subcircuit (see Figure 2.2). The n-channel VtoTc is usually negative.

The MOSFET is area scalable by factor **m** and when it not specified it defaults to unity. Area scaling factors are useful for sensitivity analysis with variable device parameters and when devices are paralleled to check for current sharing of slightly different device gains. The thermal model is also scaled by **m** by dividing Rjc by **m** and the Time constants are unchanged so all the thermal model 'C' values increase with **m**.

That's the MOSFET electrothermal model. It is the most tricky one because I am use the legacy LT-IV VDMOS. But if you only ever use LT-XVII the MOSFET subcircuit is just as easy as the BJT one.

3. Diode generic electrothermal subcircuit

The DthB subcircuit can be viewed in **Appendix 3**.

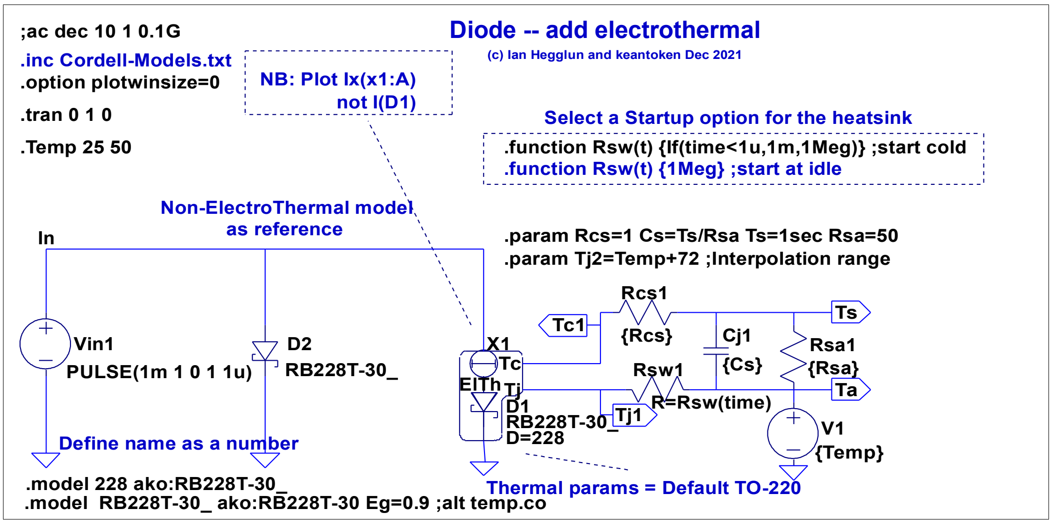


Figure 3.2. Demo jig comparing the original diode D2 (LHS) to the electrothermal subcircuit X1

13 VDMOS models that I have made available to the public have usually been in both formats for LT-IV and LT-XVII. The LT-IV version usually has an underscore added (IRFP240_) and the LT-XVII version has an 'h' added there already exists one in the LTspice standard MOS library (or the Bordodynov MOS library).

14 The **ako:** statement for **<u>a</u>** **<u>k</u>**ind **<u>o</u>**f". It allows a variation on the original model for any parameter even gender.

Figure 3.3. Demo jig plots for the original MOSFET Id(M2) to the electrothermal subcircuit Ix(x1:D)

In **Figure 3.2** the RB228T-30 is a standard Schottky diode in LTspice XVII. You can alter the temperature coefficient using the Eg parameter as shown with an **ako:** definition (the underscore is added to disambiguate the name). The original LTspice model has Eg=0.81. My alternate version has an Eg of 0.9. The default Eg for silicon is 1.11V, 0.69 for the Schottky barrier diode and 0.67 for Germanium. You can play with the demo jigs to see what difference Eg makes [footnote [15]].

The DthB subcircuit also works with Zener diodes. See **Appendix 3** for a demo with two 5.1V zeners.

The Diode is area scalable by factor **m** and when it not specified it defaults to unity. Area scaling factors are useful for sensitivity analysis with variable device parameters and when devices are paralleled to check for current sharing of slightly different devices. The thermal model is also scaled by **m** by dividing Rjc by **m** and the Time constants are unchanged so all the thermal model 'C' values increase with **m** .

The DthB subcircuit is the easiest of the 5 to use. It is also the simplest of them all internally to see how it works (see **Appendix 3**).

4. JFET electrothermal subcircuit

The JthB subcircuit can be viewed in **Appendix 4**.

The internals of the JthB subcircuit is a mix of the MthB subcircuit and the QthB subcircuit. It needs gate current interpolation for the gate diode. But it does not need subthreshold interpolation like the MOSFET because the LTspice JFET does not have subthreshold conduction.

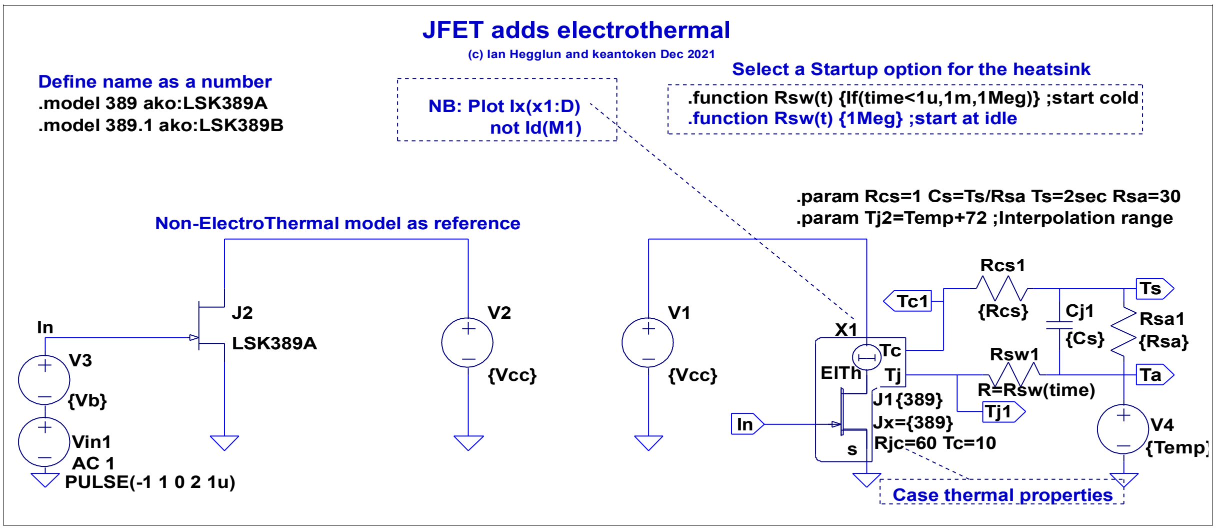


Figure 4.2. Demo jig comparing the original JFET J2 (LHS) to the electrothermal subcircuit X1

15 Parameter Eg is used with parameter XTI to model how parameter Is (saturation current) varies with temperature right down to absolute zero. Saturation current thermal properties dominate over the exponential term exp^(Vd/Vt).

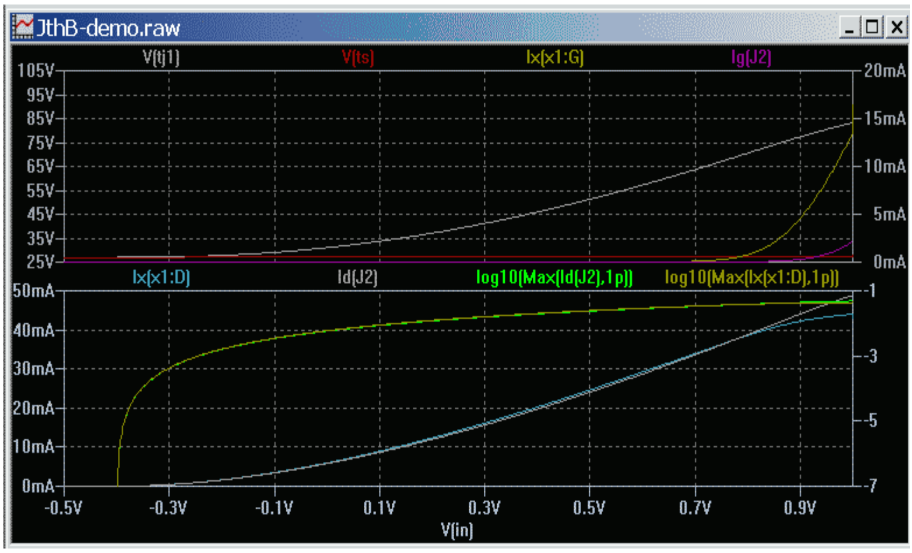


Figure 4.3. Demo jig plots for the original JFET Id(J2) to the electrothermal subcircuit Ix(x1:D)

If you have absorbed the 3 sections above then there's not much new to add here. One thing of interest is how the gate diode current is significantly affected by the junction temperature; compare Ix(x1:G) to Ig(J2) from 0.7V input and up. Otherwise for the JFET shown there is little change in Ix(x1:D) with junction temperature increase to 75°C compared to Id(J2) which is isothermal.

The junction to case parameters used for this TO-92 device is `Rjc=60 Tc=10` [footnote [16]].

The diode is area scalable by factor **m** and when it not specified it defaults to unity. The thermal model is also scaled by **m** by dividing Rjc by **m** and the Time constants are unchanged so all the thermal model 'C' values increase with **m** .

5. IGBT generic electrothermal subcircuit

The IGBTthB subcircuit can be viewed in **Appendix 5**.

The internals of the IGBTthB subcircuit is a combination of the MthB subcircuit and a custom isothermal IGBTB subcircuit.

The custom isothermal IGBT_B subcircuit is covered in **Appendix 5**.

The IGBTthB subcircuit differs from the MthB subcircuit by adding a PNP transistor to amplify the drain current of a n-channel MOSFET giving an n-IGBT. It seems intuitive that the pins are labelled D,G,S of a MOSFET because the BJT part is effectively acting as a current amplifier of the MOSFET.

The symbol I prefer is that of a BJT base, collector and emitter with an isolated gate like a MOSFET. For my *generic* subcircuits I have omitted the emitter arrow so that my subcircuits can be **either polarity** with one symbol. An 's' is added to the source leg so the source is distinguishable when rotated.

Figure 5.2 shows the demo jig for comparing the original IGBT Z2 (LHS) to the electrothermal subcircuit X1. The middle circuit M2 and Q2 form an IGBT as used for the IGBT_B subcircuit. This combination is also used in the X1 subcircuit for interpolation.

Notice the electrothermal subcircuit current Ix(x1:C) (red) has significantly *lower* current than the isothermal model; the electrothermal model reaches 15A at 10V input, while the isothermal reaches 33A. This difference is due to junction heating during the input sweep. It is effectively thermal compression. Datasheet plots must use fast input sweeps (10us to 100us) for effectively isothermal plots. All original SPICE models are based on isothermal plots [footnote [17]].

16 TO-92 and most SMD's have a longer time constant than TO-220 and TO-264 power devices. TO-92's in free air typically take 100 seconds to reach say 99% of final (about 5 simple time constants). But for the sake of faster simulations, like a factor of 1000, you can set the TO-92 and SMD device Tc to 100ms (or less).

17 Interestingly, you could use an electrothermal model to fit parameters when a relatively slow input seep is used.

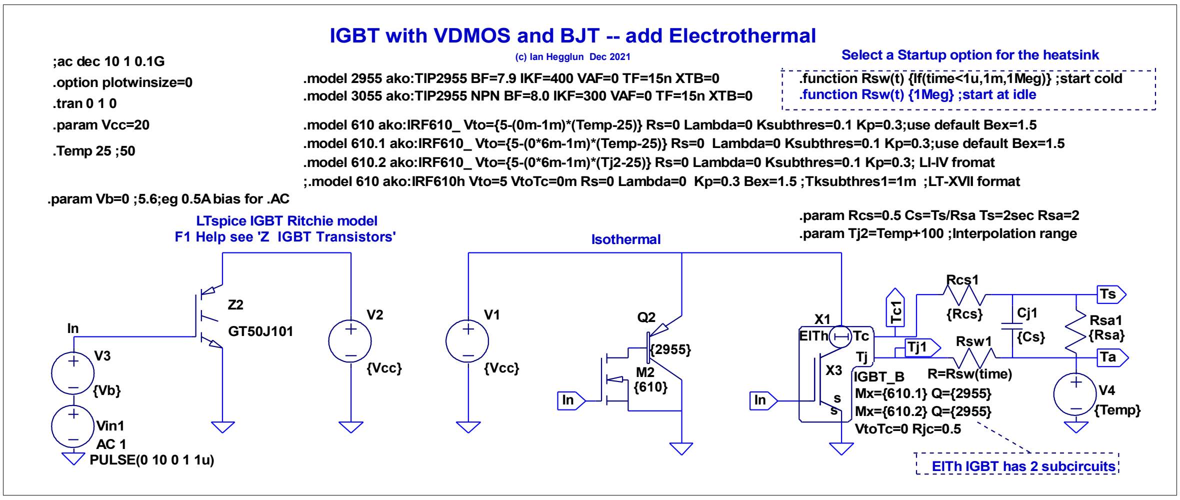


Figure 5.2. Demo jig comparing the original IGBT Z2 (LHS) to the electrothermal subcircuit X1 Middle: M2 and Q2 form an IGBT as used for the <u>isothermal</u> IGBT_B subcircuit and X1 subcircuit.

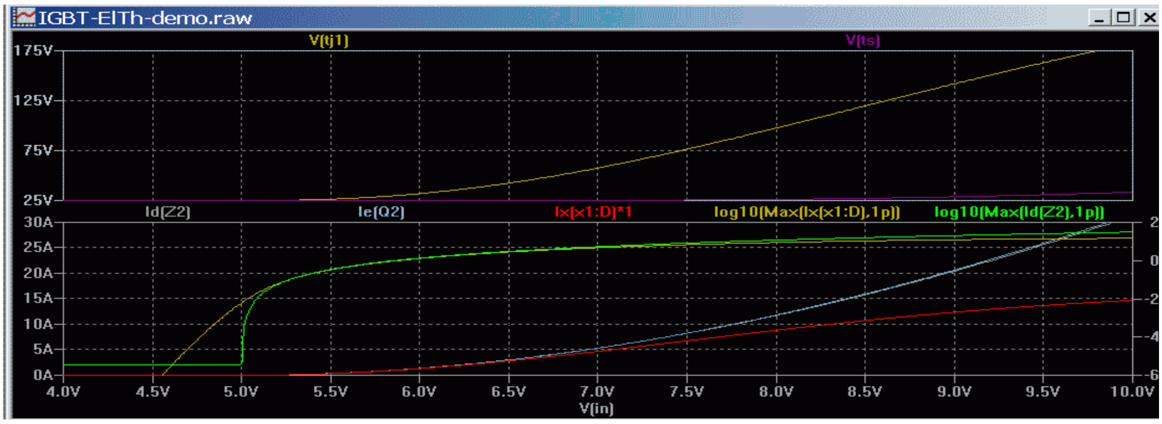


Figure 5.3. Demo jig plots for the original IGBT Id(M2) to the electrothermal subcircuit Ix(x1:D) Ic(Q2) is the <u>isothermal</u> custom IGBT with discretes M2 and Q2.

Interestingly, the IGBT offers an extra degree of freedom to allow the temperature coefficient to be either positive (like BJT's) or negative (like MOSFET's) at the high current end in linear mode. The determining factor for the temperature coefficient to be either positive or negative is mainly the BJT's Beta temperature coefficient.

For example, the IGBT_B demo using the GT50J101 Ritchie model [footnote [18]] shows a slight negative temperature coefficient and a very small threshold voltage temperature coefficient, assuming the model is accurate! These are desirable properties for Class-AB amplifiers using conventional voltage spreaders. The IGBT_B demo has XTI=0 [footnote [19]] to match the Ritchie model, but changing XTI to 1.85 then the temperature coefficient of the IGBT goes to **<u>almost zero over the entire current range</u>**.

If an IGBT can be manufactured like this, would give us analog amplifier designers an exceptional power device whose gain is almost unaffected by temperature changes [footnote [20]].

Like the MOSFET subcircuit the use of the legacy LT-IV vdmos model makes it more complicated than LT-XVII vdmos models. But then the LT-IV can be used on either platform without any changes.

The MOSFET is area scalable by factor **m** while the BJT is independently scalable by **mq**. When **mq** is not specified it defaults to **m** and when neither are specified they default to unity. Area scaling factors are useful for parameter fitting of new devices, and for sensitivity analysis in circuits, and when devices are paralleled to check for current sharing of device with slightly different gains. The thermal model is scaled by **mq** by dividing Rjc by **mq** and the Time constants are unchanged so the thermal model 'C' values increase with **mq**.

18 The IGBT Ritchie model is inbuilt in LTspice. See the help file, it's under 'Z' for IGBT.
19 BJT parameter XTI is an exponent for the Beta temperature coefficient. Is is an addition to the original GP model.
20 You can make your own IGBTs, eg an IRF610 plus a MJL1302. But please, don't add a base-emitter resistor.

That completes the basics and use of the 5 electrothermal subcircuits for LTspice.

Summary

Features of the 5 electrothermal subcircuits for LTspice include:

- Use of a 'clip-on' subcircuit – easy to add-on, and easy to return to the original
- Easy to modify key model parameters of standard models using `ako:` statements
- Easy setting of thermal model parameters using datasheet Rjc and Tc info
- Generic subcircuits – the same subcircuit covers all BJT's, another for all MOSFET's, etc
- Same subcircuit runs LT-IV models or LT-XVII new temp-co parameters
- Same subcircuit for PNP and NPN's, same for nMOSFET and pMOSFET, etc
- Easy to start from either cold or to start from warmed up idle
- Easy to accelerate simulations to reach steady state in a few minutes for most power amps.

Acknowledgement

Anthony of diyAudio a.k.a. keantoken originally contacted me around 2015 with a basic subcircuit for interpolating between two BJT's and MOSFET's. I worked on ways to improve interpolation accuracy in the subthreshold exponential region. I have also put a lot of work into making theses subcircuits easy as possible to use and to make them run reliably and as fast as possible. Thanks Anthony for the original idea.

Resources: all free for use under Creative Commons 4 Attribution

LTspice models and white papers https://paklaunchsite.jimdo.com/spice-models/
VDMOS models for LTspice library http://bordodynov.ltwiki.org/

Examples using the above Electrothermal models:

https://paklaunchsite.jimdo.com/spice-models/

- StdTopology-Ctrlx-ElTh.zip
- diyAudio_TBP-Zero-MOS-diode-Autobias.zip
- Unanticipated-amp-Schottky-Autobias-jFET-cas-IRFP240-G-37v.zip
- Unanticipated-amp-MOS-diode-Autobias-jFET-cas-IRFP240-G-37v.zip
- Wideband-Diamond-Splitter-Autobias-Spreader-various.zip eg diyAudio.com here and diyAudio.com here
- …

…Appendix

Appendix Contents: [Note: First timers – the DthB is the simplest so start there]

Appendix 1

1.1 Internal circuit of the QthB subcircuit

See QthB circuit below:

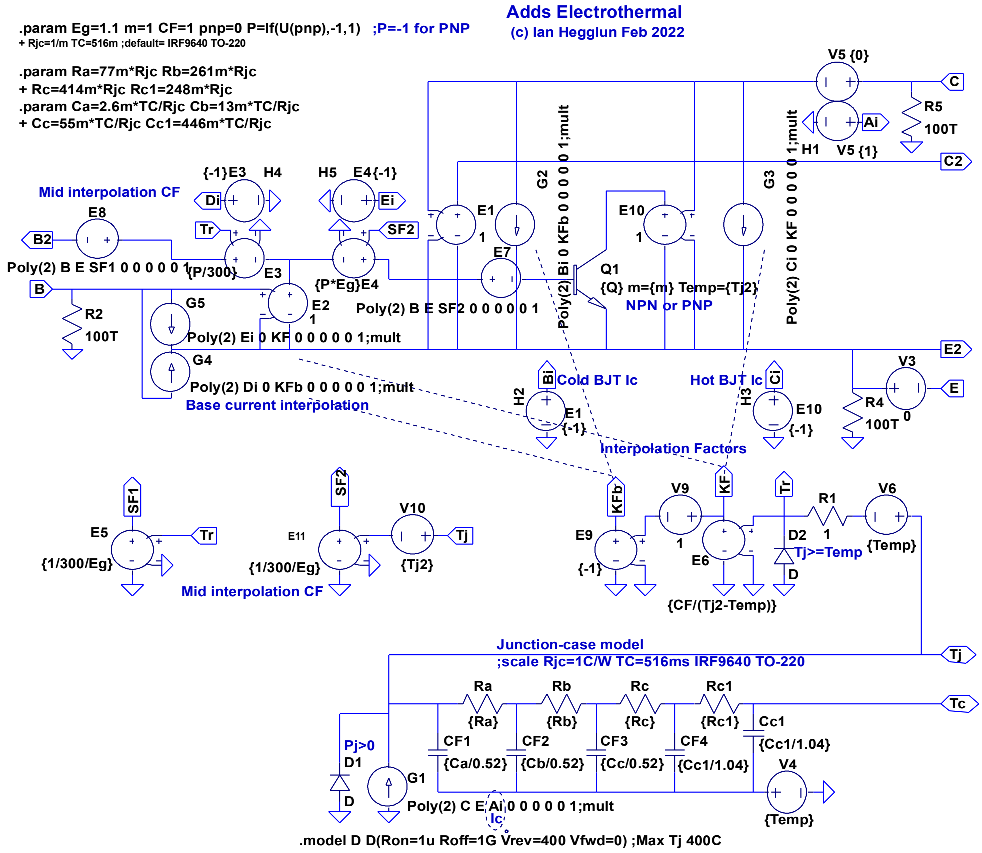


Figure A1.1. Internal circuit of the QthB subcircuit

1.2. How the QthB subcircuit works

The QthB subcircuit uses **linear interpolation** of currents between two isothermal BJTs:

1) the original "cold" transistor, and

2) a BJT inside the subcircuit which runs "hot" at temperature Tj2.

Collector currents and base currents are interpolated using **6 multipliers** using the Poly(2) source [footnote [21]].

In **Figure A1.1** multipliers G2 and G3 interpolate the collector currents of the external BJT and internal BJT (Q1) respectively. Multiplier G2 is scaled by voltage 'KFb' and multiplier G3 is scaled by voltage 'Kfb'. KF is a normalised factor that varies linear-wise from 0 to 1 for Tj from Temp to Tj2. KFb is a normalised factor that varies linear-wise from 1 to 0 for Tj from Temp to Tj2.

Voltage for Tj is generated by the **thermal model** made from a RC ladder to simulate the thermal resistance from the junction to case.

The RC thermal model is based on the IRFP9640 [ref: IRF9640 thermal model Vishay Application Note

21 "Bi' Behavioural sources can be used instead of Poly(2) sources. Poly(2) sources as multipliers (mostly) result in less convergence issues than B sources.

90298] which has a TO-220 case.

The RC thermal model thermal properties are **scalable** to suit other cases such as TO-246 for the NJL3281 and IRFP240, or TO-92's and SMD's. The RC thermal model uses 4 R's and 5 C's in a ladder [footnote 22]. With a scalable model you don't change each R and C individually, they are all scaled by 2 parameters Rjc and Tc.

For interpolating base current 4 multipliers are used:
G4 and G5 interpolate the base currents as voltages 'Di' and Ei, and
E7 and E8 are Poly(2) voltage sources that are scaled by 'SF1' and 'SF2' respectively with Vbe as the other multiplier variable. E7 and E8 provide offset voltage for interpolating the low Vbe exponential region which can't be done accurately using just collector current interpolation with G2 and G3.

In addition to E7 and E8 multipliers an offset voltage from E3 is applied to the external BJT base and an offset voltage from E4 is applied to the internal BJT (Q1) base. These provide additional offset voltage for interpolating the low Vbe exponential region.

The correction multipliers and offset voltages have been arranged to follow the equations for NPNs

$$\partial Vbe1=\frac{(Eg-Vbe)}{Eg}\times\frac{(Tj-Temp)}{Tabs+Temp} \quad \text{and} \quad \partial Vbe2=\frac{(Eg-Vbe)}{Eg}\times\frac{(Tj-Tj2)}{Tabs+Temp}$$

where Eg for silicon is 1.11V, 0.69 for the Schottky barrier diode and 0.67 for Germanium. This equation is derived from the Gummel-Poon BJT model which includes XTI but has been removed here (since it's effect on interpolation was found to be small enough to leave out in my 2021 version [footnote 23]). In the subcircuit Eg defaults to 1.1 but you can pass this parameter into the subcircuit if you want to change it by adding **`Eg=<myvalue>`** to each BJT on the main circuit.

To cater for PNPs the polarity of E3 and E4 need to be reversed. This is done using parameter 'P' which takes the value of -1 when the flag **`PNP=1`** is added to each BJT on the main circuit. For an NPN a flag is not needed since the default value for 'P' is forced to +1 inside the subcircuit.

1.2.1. Checking interpolation

To check the accuracy of interpolation a special demo circuit is provided where Tj is forced to 0%, 50% and 100% [footnote 24]. This is also done for the isothermal model. The electrothermal model should give the same currents for all 3 cases over a wide range of input voltage. In this jig the electrothermal effect over time is disabled and Tj is held constant for each of these 3 Tj steps. **Figure 1.2.1** shows the demo jig plots.

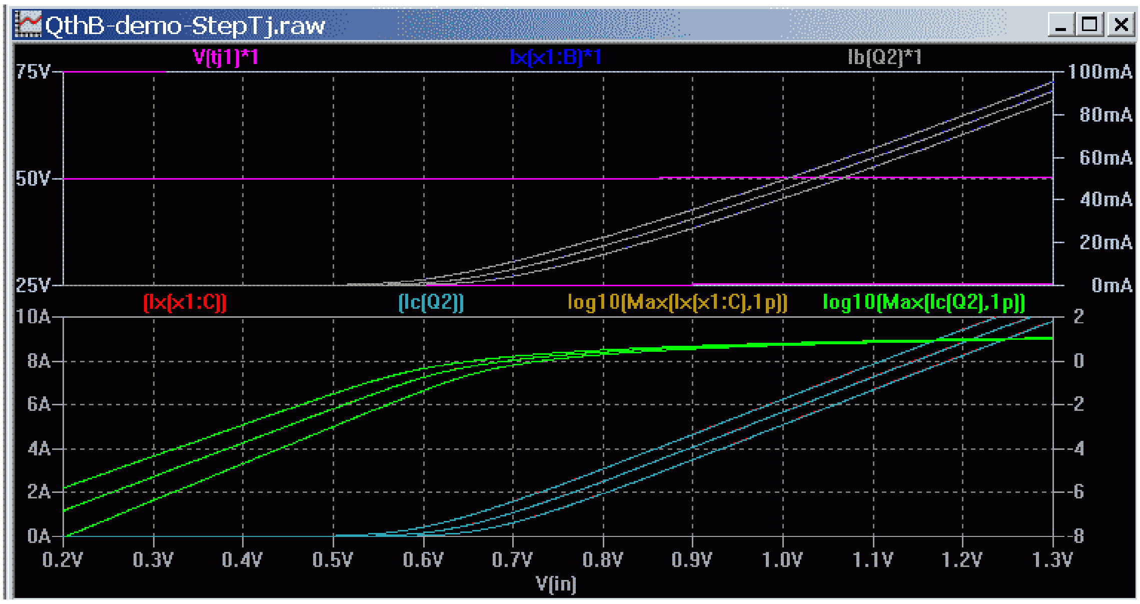


Figure 1.2.1. Tj stepping demo jig for 0%, 50%,100% interpolation

The log plot for the subcircuit is on top of the reference isothermal plot, showing good accuracy in the

22 The ladder type is more intuitive than the Cauer type but the Cauer is easier to fit to datasheets than the ladder type.
23 See the earlier 2016 versions with equations with XTI if you wish to check how significant XTI is for interpolation.
24 File QthB-demo-StepTj.asc

exponential region as well as at high currents. BTW extrapolation with higher temperatures is fairly good at say 200% but not demonstrated here – you try the jig to check. This means it is not important to set the interpolation temperature range above the suggested `Tj2=Temp+72` in this latest public release [footnote [25]].

1.3. An example using the QthB subcircuit

Figure A1.3 is an interesting amplifier design that appeared on diyAudio as a clone of the TBP-zero [footnote [26]]. A standard LTspice simulation cannot tell you much about the thermal stability without emitter resistors. Electrothermal models allows us to try different heatsink mounting arrangements. Since the TBP article is in Japanese and I could not see how the transistors were mounted.

I found from simulations that thermal runaway can be prevented without emitter resistors. One ohm base resistors are used for current sharing with 3 pair in parallel [footnote [27]]. **Figure A1.3** shows my simulation configuration for 9 thermal subcircuits: 2 for the 6 power transistors, 4 for the drivers, 2 for the pre-drivers and one for the spreader/Vbe-multiplier.

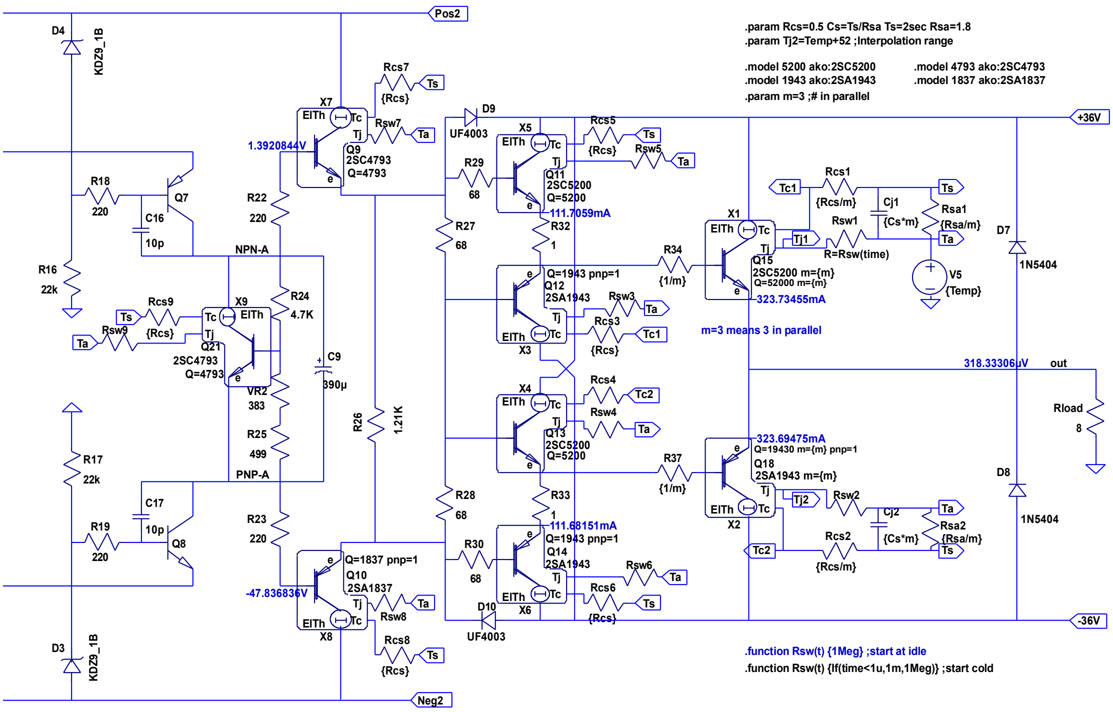


Figure A1.3. Electrothermal circuit example using 9 QthB subcircuits

Thermal bias stability is possible with no emitter resistors when the driver transistor Q12 and Q13 are mounted on a **thermal spreader plate** of the main power transistors. This makes the driver transistors operate at a junction temperature as close as possible to the main power transistors junction temperature. This means most of the change in Vbe of the main power transistors with junction temperature change is cancelled by driver transistors Q12 and Q13. The spreader transistor Q21 is mounted on the heatsink to cancel the remaining temperature changes.

In this simulation the 3 pairs of power transistors are combined into one pair using the SPICE parameter **`m=3`** for area scaling [footnote [28]]. The subcircuit's thermal model also gets scaled by `3` (by dividing Rjc by `3`, the Time constants are unchanged so all the thermal model 'C' values increase by the factor of `3`). The heatsink and other thermal values are also scaled by a factor of `3`. Combining three parallel devices into one will run faster. Sometimes the circuit won't start unless less electrothermal subcircuits are used.

How to do current-hogging sims. If you add 3 pair of power transistors each with electrothermal models

25 Tj2=Temp+70 is chose for the the issue found with LT-XVII to prevent it failing to run. LT-IV seems OK above this.

26 The TBP-zero amp (Technical Brain Power amp) was a bridge (balanced) amp where the 'zero' refers to no emitter resistors in the power transistors. http://www.technicalbrain.co.jp/products_tbp_zero_ex_e.html

27 For good current sharing I'm assuming the 3 NPNs are from the same tube, same date marking, likewise the 3 PNPs.

28 Both the original transistor and the subcircuit transistors name need an m=3 added (see X1 above). Alternatively, the subcircuit transistors can have the m=3 added to parameters (they also appear in the “SpiceLine” area).

then you will have a total of 13 QthB subcircuits. I have not tried this but I expect it to be too slow to start, if it starts at all. To try this, remove 4 subcircuits for Q9, Q10, Q11, and Q14 and you now have 9 subcircuits rather than 14 (it might start with 9).

To check current hogging first try adding an offset voltage of 5mV or 10mV to one of the 3 NPNs in parallel. This forces one to start at a higher (or lower) current than the others (depending on the polarity of the offset voltage). Then check the Tj of this offset transistor to see if it's current share increases or decreases as they all move towards their final currents and temperatures. If the current share diverges you get current hogging.

If there is hogging then try increasing the base resistors to stop hogging [footnote [29]]. Be aware this current hogging simulation assumes the BJT temperature coefficient for beta (BF) is modelled accurately enough by XTB to match your datasheet or measurements. So caution is advised when you first power up a real circuit with no emitter resistors when a simulation showed no current hogging by adding base resistors. An example of checking for current sharing with an electrothermal simulation can be seen in a diyAudio post here.

Appendix 2

2.1 Internal circuit of the MthB subcircuit

See MthB circuit below:

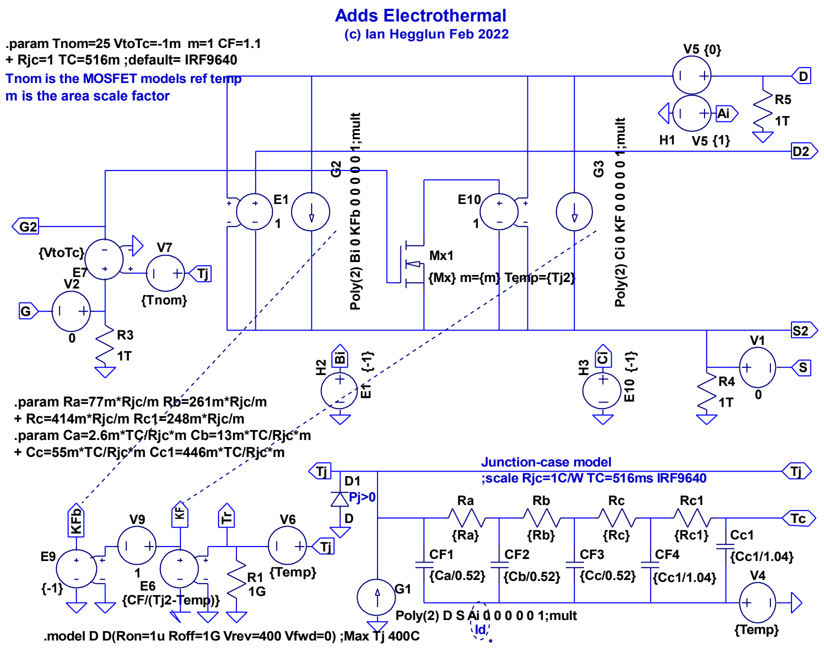


Figure A2.1. Internal circuit of the MthB subcircuit

2.2. How the MthB subcircuit works

The MthB subcircuit **Figure A2.1** is similar to the QthB subcircuit but the MOSFET version does not need gate current interpolation. The MthB subcircuit uses two Poly(2) source multipliers (G2,G3) for **linear interpolation** of drain currents between two isothermal MOSFETs:

1) the original "cold" MOSFET, and
2) a MOSFET inside the subcircuit which runs "hot" at temperature Tj2.

The RC thermal model is the same as the QthB subcircuit. Refer to the above section for details.

Multiplier G2 is scaled by voltage 'KFb' and multiplier G3 is scaled by voltage 'Kfb'. KF is a normalised factor that varies linear-wise from 0 to 1 for Tj from Temp to Tj2. KFb is a normalised factor that varies linear-wise from 1 to 0 for Tj from Temp to Tj2.

To cater for the legacy VDMOS used in LT-IV it is necessary to create two `ako:` statements: one for the

29 Adding base resistors is preferred to adding emitter resistors because they can be small wattage. But base resistors may not reduce current hogging if your power transistor's Beta temperature coefficient (XTB) is significant (>0.5). The PNP may have a higher XTB than the NPN so the PNP may require some emitter resistance rather than base R?

original MOSFET outside the subcircuit and one for the MOSFET inside the subcircuit. Both MOSFETs have their VtoTc temperature coefficient set to zero so the subcircuit can interpolate the voltage for the exponential subthreshold region for better accuracy. For the MOSFET inside the subcircuit its curly brace equations use Tj2 while the MOSFET outside the subcircuit its curly brace equations use Temp.

These two different model temperature parameters are necessary because you cannot pass temperature into the old VDMOS model in LT-IV like you can for a BJT in LT-IV because the old VDMOS model in LT-IV does not support the temp.co parameter VtoTc (now the LT-XVII VDMOS supports the parameter VtoTc).

To cater for P-channel VDMOS you need to reverse the polarity of the temp.co that you pass into the subcircuit. You do not need to use a flag for the subcircuit for the VDMOS p-channel since that is already taken care of in the model statement of the p-channel.

1.2.1. Checking interpolation

To check the accuracy of interpolation a special demo circuit is provided where Tj is forced to 0%, 50% and 100% [footnote [30]]. This is also done for the isothermal model. The electrothermal model should give the same currents for all 3 cases over a wide range of input voltage. In this jig the electrothermal effect over time is disabled and Tj is held constant for each of these 3 Tj steps. **Figure 2.2.1** shows the demo jig plots.

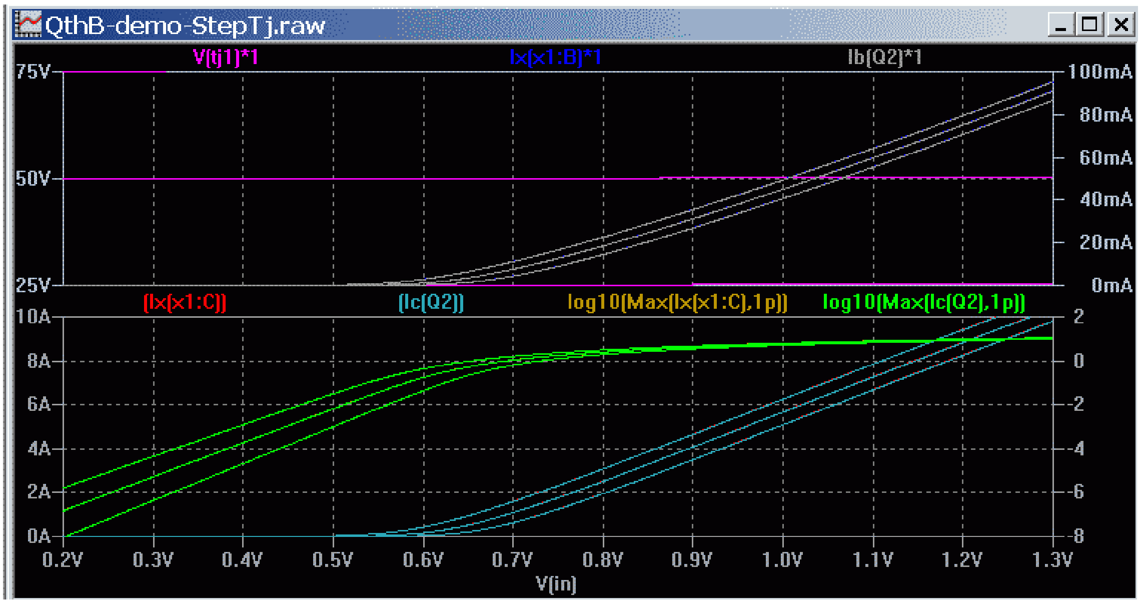


Figure 2.2.1. Tj stepping demo jig for 0%, 50%,100% interpolation

The log plot for the subcircuit is on top of the reference isothermal plot, showing good accuracy in the exponential region as well as at high currents. BTW extrapolation with higher temperatures is fairly good at say 200% but not demonstrated here – you try the jig to check. This means it is not important to set the interpolation temperature range above the suggested `Tj2=Temp+72` in this latest public release [footnote [31]].

2.3 An example using the MthB subcircuit

The example chosen is the basic 3 stage power amp topology or 'standard topology' so called by some members of the diyAudio forum. I took member 'ctrx' v12 circuit here. I have modified the compensation to obtain clean clip recovery [footnote [32]]. The modified circuit s shown in **Figure A2.3.1**.

30 File MthB-demo-StepTj.asc
31 Tj2=Temp+70 is chose for the the issue found with LT-XVII to prevent it failing to run. LT-IV seems OK above this.
32 I added a Schottky diode for anti-saturation of the current source for the VAS and added some Miller comenstation.

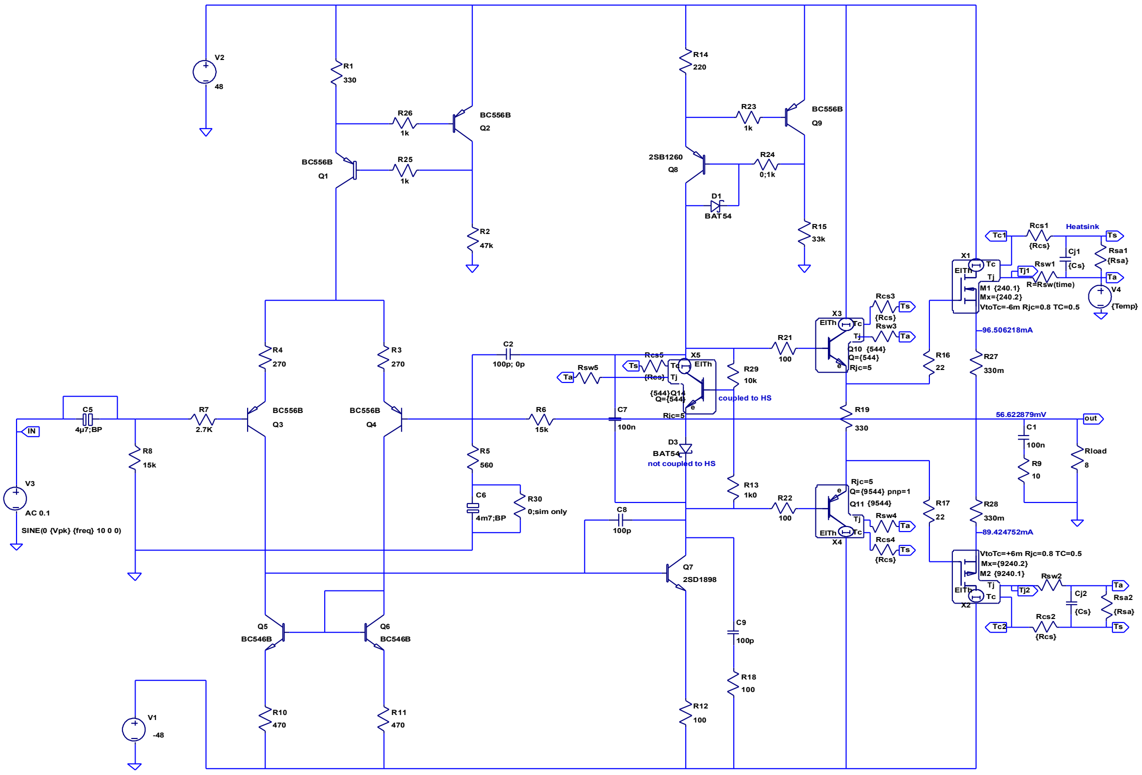


Figure A2.3.1. Modified 'ctrlx' v12 circuit with electrothermal added.

Figure A2.3.2 shows the idle current change during warm up with no input signal. The actual time for the warm-up phase is shrunk here to speed up simulation time – warmup can typically take 20 minutes real time.

Figure A2.3.2. Starting from cold with no input signal.

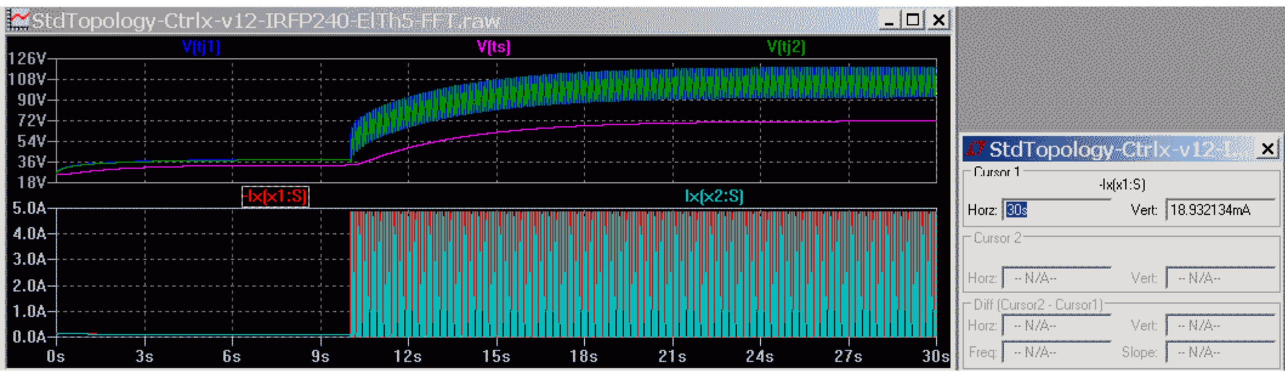


Figure A2.3.3. Input signal after warmed up then wait for steady state. The idle current falls to 19mA!

Figure A2.3.3 shows steady state with 40Vpk output. The sink temperature rises to 72°C and the idle current falls to 19mA! This means the spreader temperature coefficient is far too large for these MOSFETs.

Figure A2.3.4 has a Schottky diode added to the emitter of the Vbe multiplier/spreader to lower the temperature coefficient of the Vbe multiplier. Idle current now remains about the same when running hot.

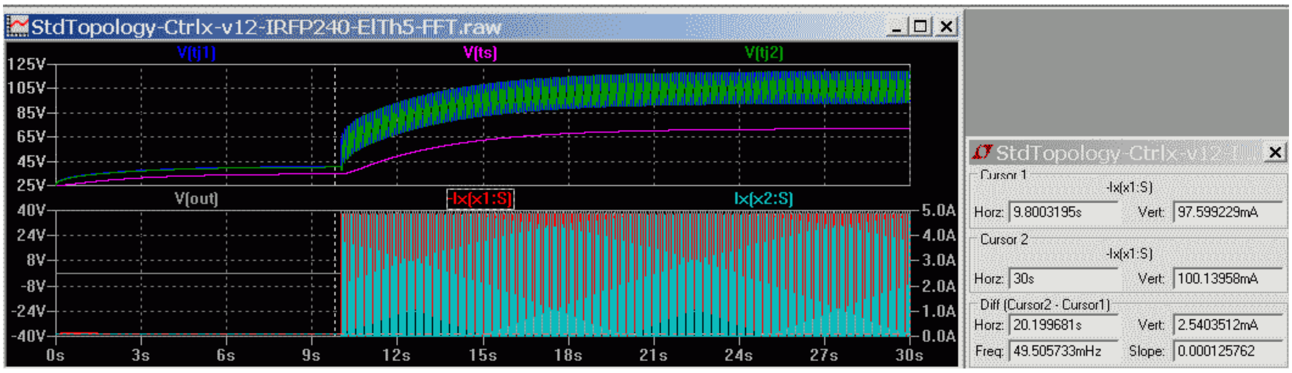


Figure A2.3.4. Vbe multiplier with BAT54. Idle current is 98mA and 100mA at high power.

Repeating the electrothermal simulation with MJL3281/1302 BJTs, see **Figure A2.3.5.** The idle/crossover bias starts at 96mA and reaches 111mA when warmed up the rises to 130mA. which is acceptable.

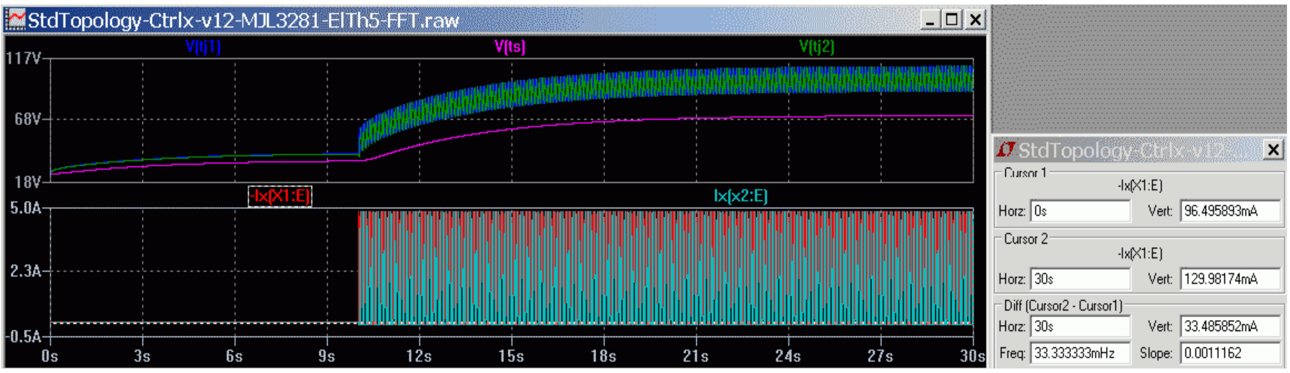


Figure A2.3.5. Electrothermal simulation with MJL3281/1302 BJTs. The idle current rises to 130mA.

Appendix 3

3.1Internal circuit of the DthB subcircuit

See DthB circuit below:

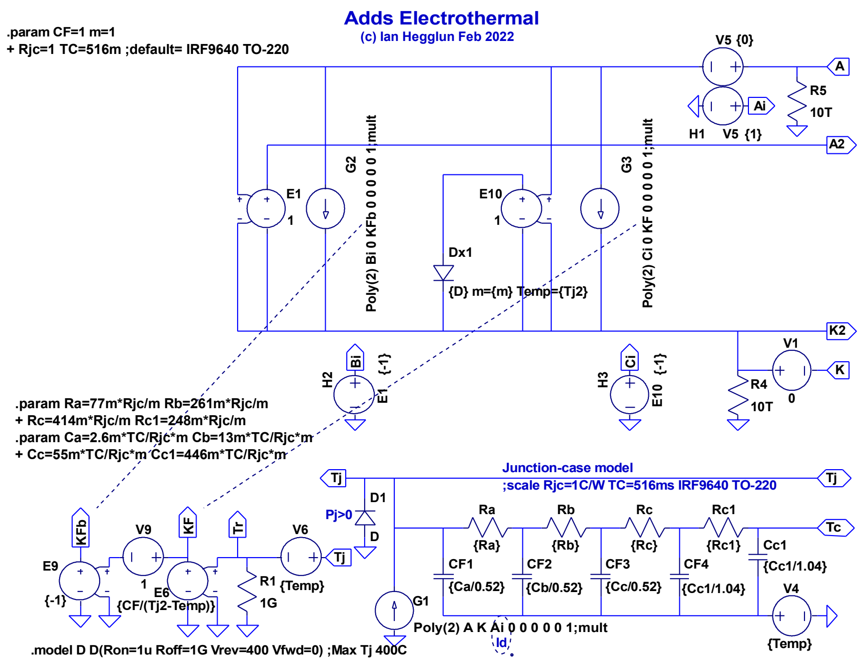


Figure A3.1. Internal circuit of the DthB subcircuit

3.2. How the DthB subcircuit works

[Under construction]. This is the simplest of the 5 electrothermal subcircuits. It is the best one to start at to understand how interpolation is done using the Poly(2) multiplier.

The cold diode is external to the subcircuit and current is monitored by E1 and converted to voltage Bi using H2. Current through the hot diode Dx1 is monitored giving voltage Ci. Current through the cold diode is scaled by Bi and thermal factor 'Kfb'. Current through the hot diode is scaled by Ci and thermal factor 'Kf'.

The RC thermal model is the same as the MthB and QthB subcircuit. Refer to Appendix 1 QthB thermal model explanation above. The thermal model is also scaled by **`m`** by dividing Rjc by **`m`** and the Time constants are unchanged so all the thermal model 'C' values increase with **`m`**.

3.3 An example using the DthB subcircuit

[Under construction] eg The electrothermal Schottky diode as part of an Autobias loop diyAudio.com here

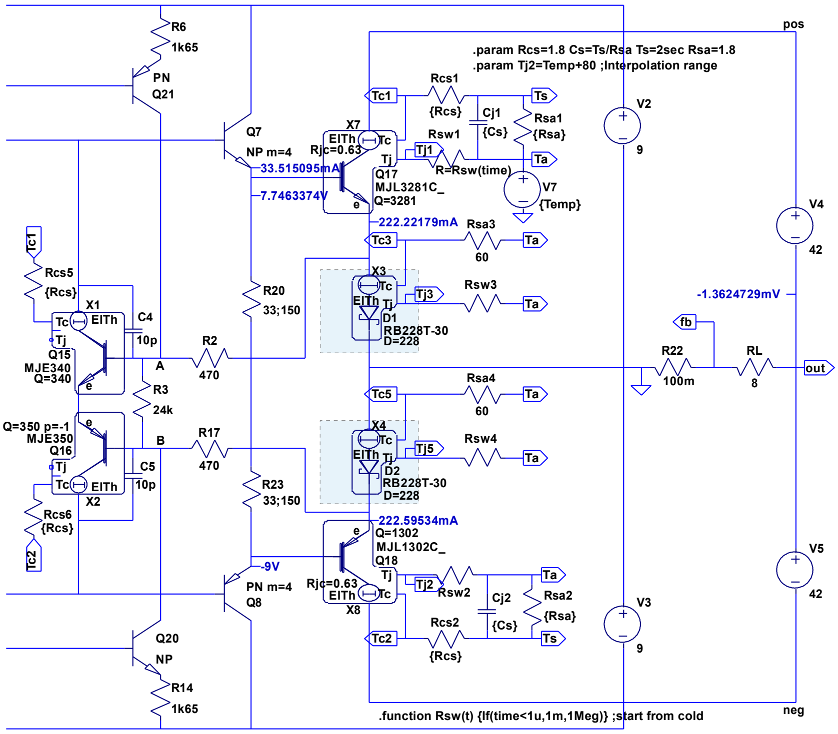


Figure A3.3. Example using the DthB subcircuit in a wideband Autobias loop

In **Figure A3.3** the value of Rsa3 and Rsa4 are 60°/W thermal resistance which corresponds to two TO-220's vertical on a PCB without any additional heatsink. The thermal time constant (Tc) for the Schottky diodes is set at 0.1 seconds (but not shown on schematic); the actual time constant is more like 100 seconds but it is deliberately shrunk to allow the simulation to reach say 99% of final temperatures in around 20 seconds.

3.4 Using DthB as a Zener diode

Figure A3.4 shows the demo jig for the DthB subcircuit for a Zener diode. Note the polarity of Vin is reversed so the Zener diode has a negative voltage applied to it. The Zener diode is effectively upside down to the normal orientation for a Zener diode. In practice the DthB subcircuit would be rotated and mirrored so the Zener has its cathode toward the top of the page.

Figure A3.5 shows the jig plot for a BZX84C5V1 Zener diode with Tj stepped 25, 50 and 75°C.

Figure A3.6 shows the datasheet plots for various BZX84 series zener voltage with temperature.

Figure A3.7 shows the jig plot for a 1N751 Zener diode with Tj stepped 25, 50 and 75°C.

Figure A3.8 shows the plots for BZX84C5V1 and 1N751 Zener diode with Iz stepped 2m, 5m and 10mA. The Vz is the BZX84C5V1 and Vz1 is the 1N751. Temp-co's are +0.56m/°C for the BZX84C5V1 at 2mA, and -0.81m/°C at 2mA for the 1N751. The datasheets shows 5.1V zeners have a zero temperature coefficient with a part-to part variation of ±0.3m/°C from 0°C to 100°C.

Now to the next demo, the electrothermal version that is enabled by setting Rsw1 to **`R=Rsw(time)`** . We can now view the effect on the Zener current as it heats up as the voltage sweeps more negative. (The **`DthB-`**

`Zener-demo.asc` in the download zip file and is set for this sweep).

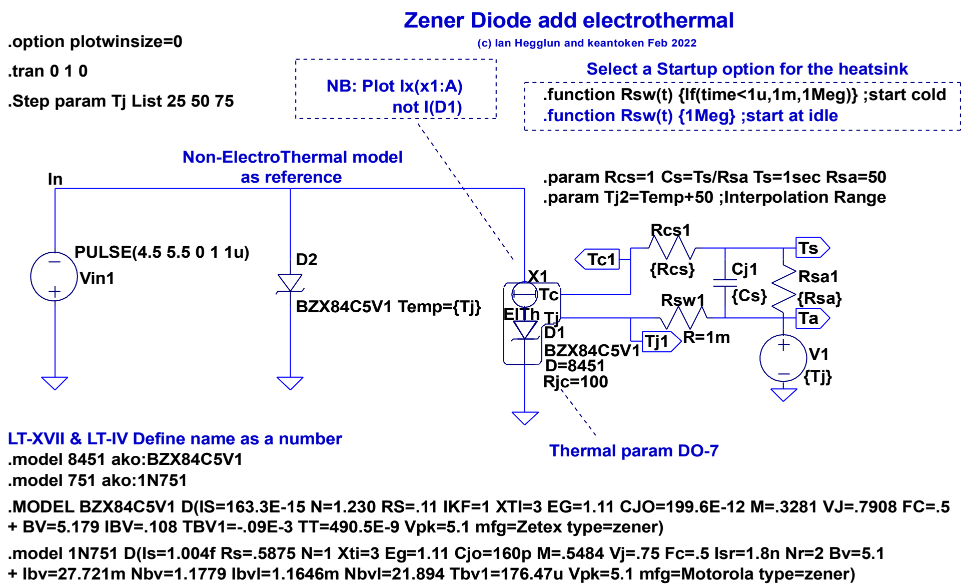


Figure A3.4. Jig using the DthB subcircuit as a Zener diode. Note Vin polarity is reversed

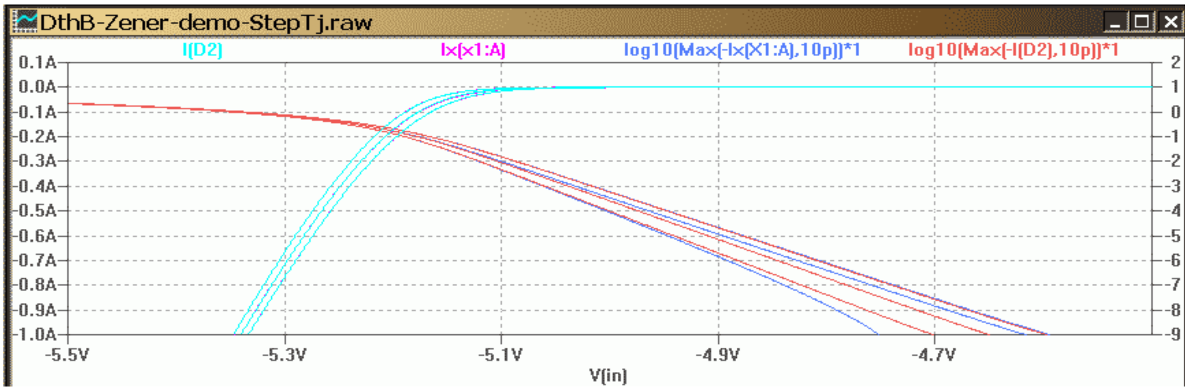


Figure A3.5. Jig plot for a BZX84C5V1 Zener diode with Tj stepped 25, 50 and 75°C.

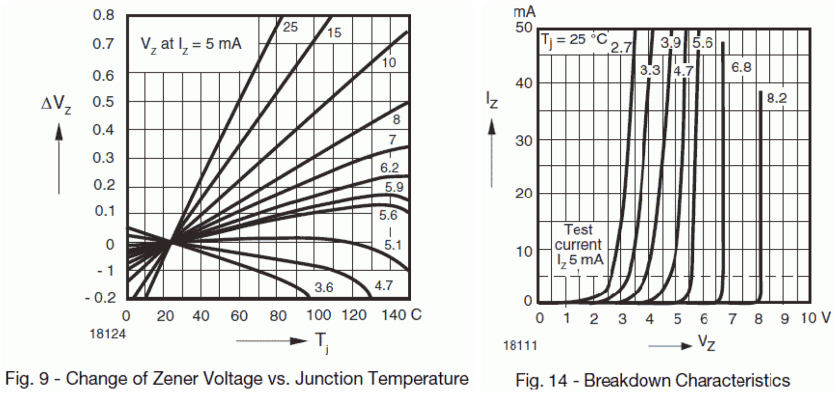


Figure A3.6. Datasheet plots for the BZX84 series Zener diode

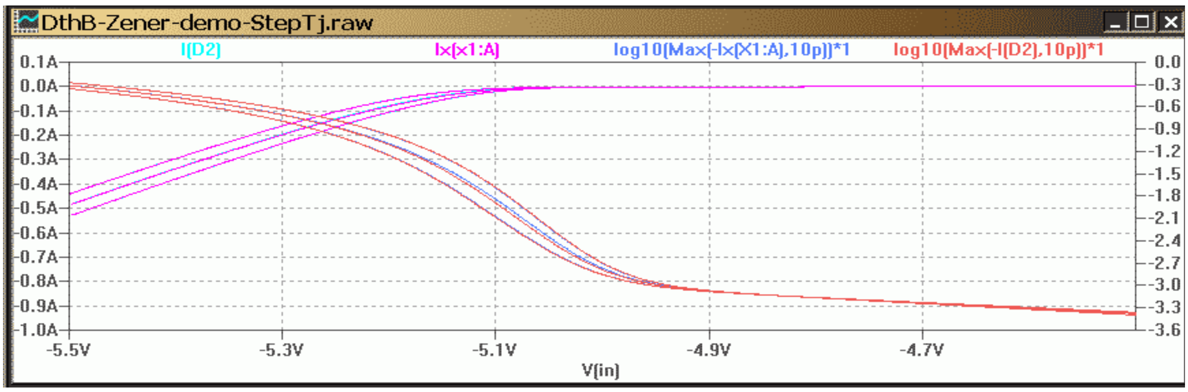


Figure A3.7. Jig plot for a 1N751 Zener diode with Tj stepped 25, 50 and 75°C.

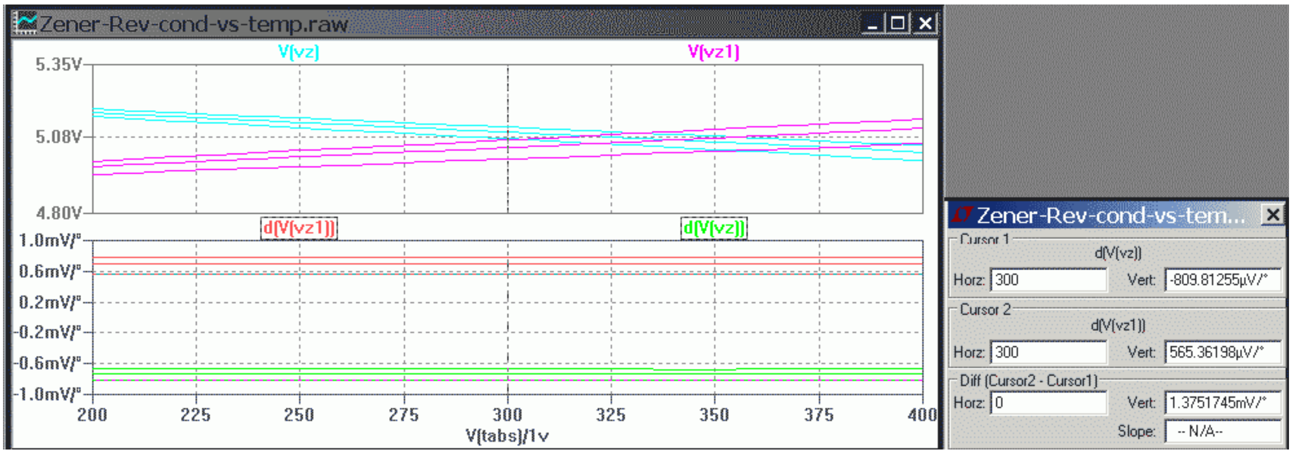


Figure A3.8. Plot for BZX84C5V1 and 1N751 Zener diode with Iz stepped 2m, 5m and 10mA.
Vz is the BZX84C5V1 & Vz1 is the 1N751. Temp-co's are +0.56m/°C & -0.81m/°C resp. @ 2mA, 27°C

Appendix 4

4.1Internal circuit of the JthB subcircuit

See JthB circuit below:

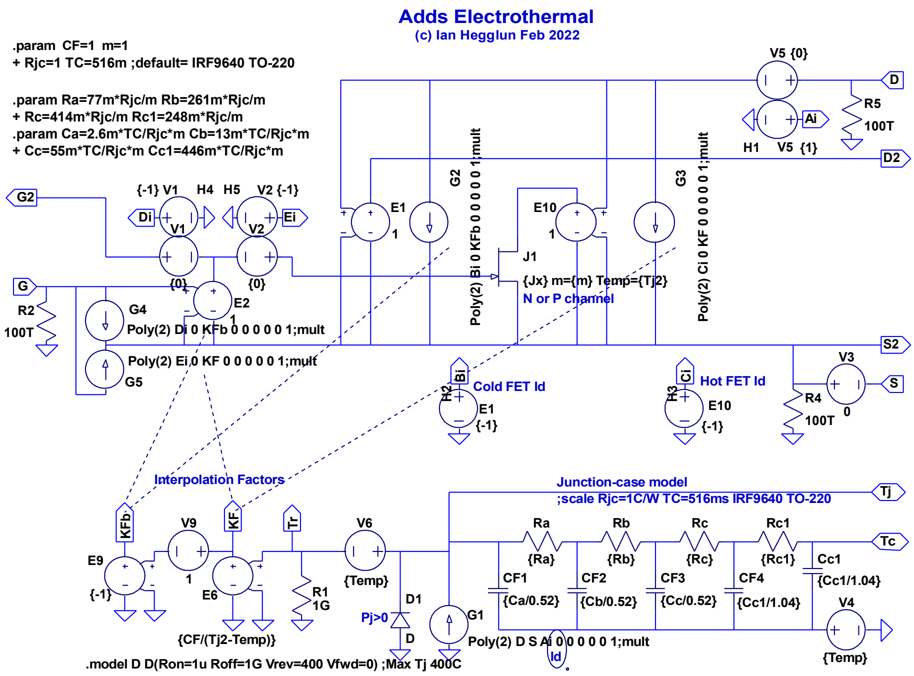


Figure A4.1. Internal circuit of the JthB subcircuit

4.2. How the JthB subcircuit works

[Under construction] The JFET gate current is interpolated as per the BJT (see QthB). But the JFET does not need the exponential region as per the BJT because the LTspice JFET does not model the subthreshold region.

The RC thermal model is the same as the QthB subcircuit. Refer to Appendix 1 QthB thermal model explanation above.

4.3 An example using the JthB subcircuit

[Under construction] See the demo circuits '`JthB-demo.asc`' and '`JthB-demo-P.asc`'. **Figure A4.3.1** shows the LSK389A n-channel JFET as modelled by Bob Cordell. The electrothermal model is very similar to the isothermal model except when the gate conducts significant current.

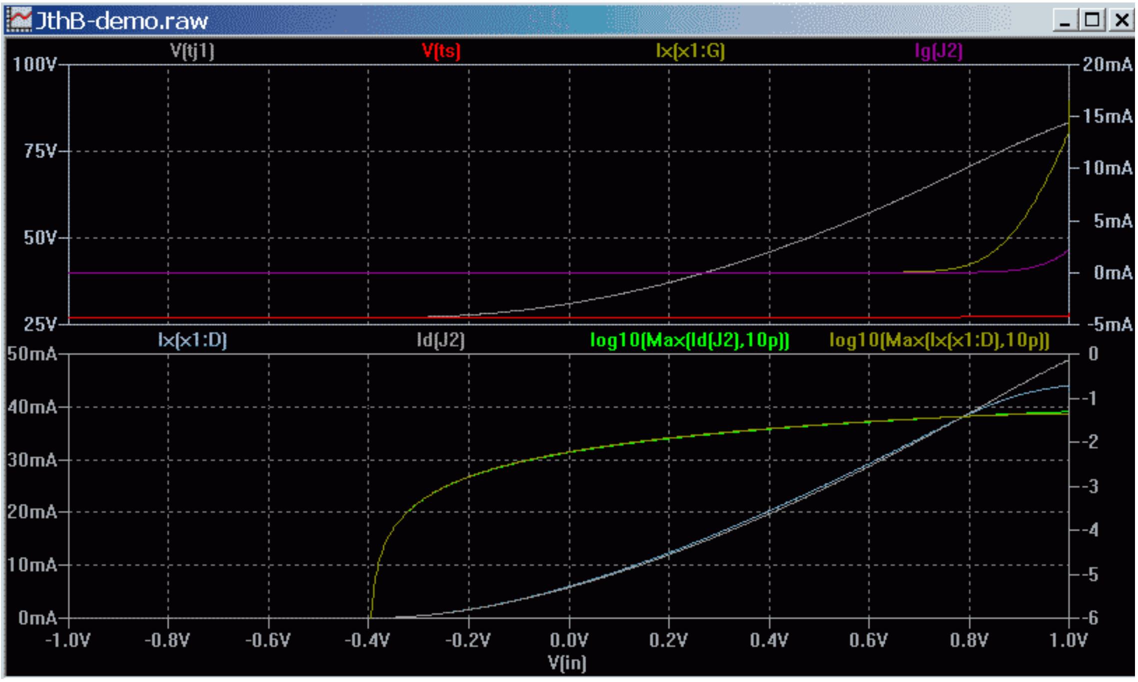


Figure A4.3.1. The LSK389A n-channel JFET (J2) and the electrothermal Ix(x1:D)

The reason the gate current is significantly different to the isothermal is the gate diode forward voltage drops significantly with a junction temperature of around 75°C at the end of the input voltage 2 second sweep. Interestingly, this JFET shows remarkably little change in character with rising temperature, unlike the BJT which is a highly temperature sensitive device compared to this JFET.

Appendix 5

5.1 Internal circuit of the IGBTthB subcircuit

See IGBTthB circuit below:

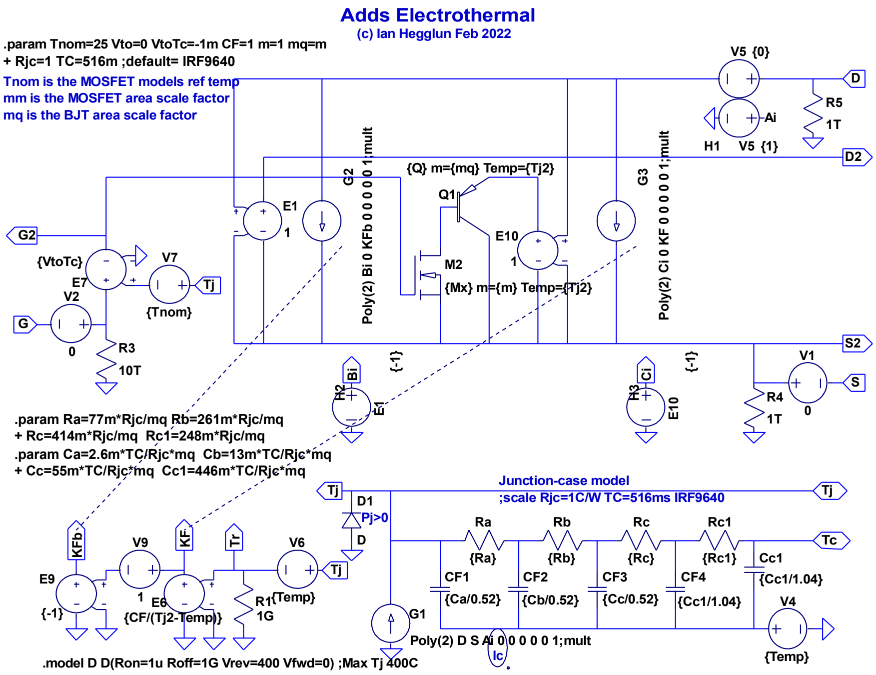


Figure A5.1. Internal circuit of the IGBTthB subcircuit

5.2. How the IGBTthB subcircuit works

The internals of the IGBTthB subcircuit is a combination of the MthB subcircuit and a custom isothermal IGBTB subcircuit. The custom isothermal IGBT_B subcircuit is covered below.

The IGBTthB subcircuit differs from the MthB subcircuit by adding a PNP transistor to amplify the drain current of a n-channel MOSFET giving an n-IGBT. It seems intuitive that the pins are labelled D,G,S of a MOSFET because the BJT part is effectively acting as a current amplifier of the MOSFET.

The symbol I prefer is shown below: an isolated gate like a MOSFET but with collector and emitter like a BJT. For the sake of my *generic* subcircuits I have omitted the emitter arrow so that my subcircuits can be **either polarity** with one symbol. The letter 's' is added to the source leg.

In **Figure A5.1** the internal IGBT is formed from a VDMOS (M2) and a BJT (Q1) both operate at `Temp=Tj2`. The MOSFET is area scalable by factor `m` while the BJT is independently scalable by `mq`. When `mq` is not specified it defaults to `m` and when neither are specified they default to unity. Area scaling factors are useful for parameter fitting to datasheet plots, or for sensitivity analysis in a circuit, and when devices are paralleled to check for current sharing of slightly different devices.

5.3 An example using the IGBTthB subcircuit

Figure A5.3 shows the IGBTthB subcircuit with all the parameters displayed. X1 is the name of the electrothermal subcircuit. X1a is the name of the isothermal subcircuit – the original IGBT that X1 clips onto. "IGBT_B" is a part name of X1a and the parameters "**Mx={610.1} Q={2955}**" specify the two models used by the isothermal subcircuit X1a. Then"**Mx={610.2} Q={2955}**" specify the two models used by the electrothermal subcircuit X1 [footnote [33]]. And "**VtoTc=0 Rjc=0.5**" specify further model for the isothermal subcircuit X1a.

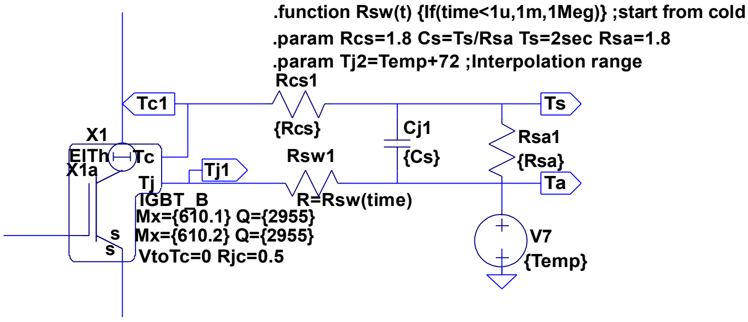
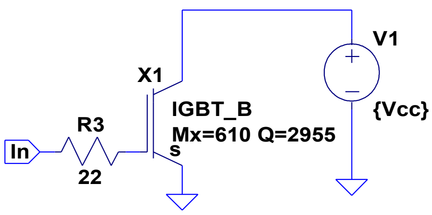


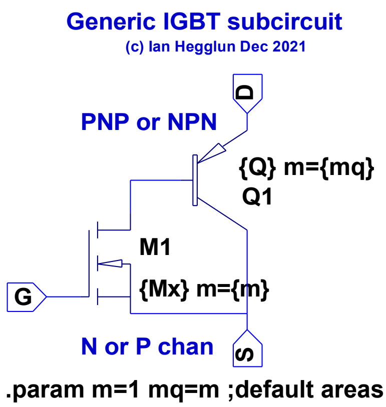
Figure A5.3. Electrothermal circuit example using the IGBTthB subcircuit X1.

5.4. The custom IGBT_B isothermal subcircuit

The custom IGBT_B subcircuit is used for the isothermal IGBTthB subcircuit [footnote [34]].

The custom IGBT_B subcircuit is defined by two models as numbers; one for the MOSFET and the other for the BJT (see **Figure A5.3** Right). In this example Mx=610 is for an IRF610 and Q=2955 is for a 2N2955.





33 When m and mq area scaling are used use the following "`Mx={610.1} m={m} Q={2955} mq={mq}`" and "`Mx={610.2} m={m} Q={2955} mq={mq}`". Alternatively, you can add `m={m}` and `mq={mq}` to "parameters" (seen in the SpiceLine area). Note: Parameter Rjc passing (via SpiceLine) if different to the default 1C/W, use the Rjc for the unscaled device (m=1) – the internal thermal then model uses the mq scale factor for the BJT only.

34 That means the IGBTthB subcircuit has effectively two subcircuits that need defining with 2 models as numbers.

Figure A5.3. Left: Using the custom IGBT_B isothermal subcircuit in the demo jig
Right: Internal circuit of the custom IGBT_B isothermal subcircuit

Figure A5.4 shows the IGBT Demo jig. It compares the LTspice Ritchie IGBT model Z2 (LHS) to the electrothermal subcircuit X1 RHS. In the middle is the circuit used in X1. The model definitions use the **`.ako`** statement to modify the IRF610 MOSFET parameters as well as the 2N2955 BJT that are used as rough guide for some parameters [footnote [35]].

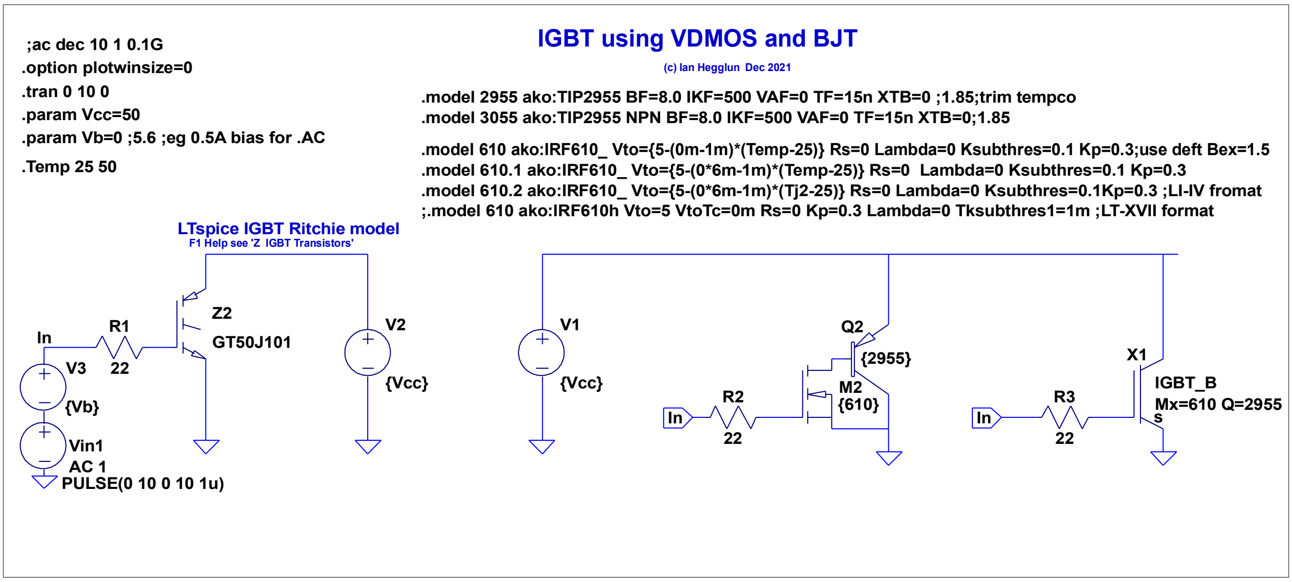


Figure A5.4. Demo jig comparing the original IGBT Z2 (LHS) to the electrothermal subcircuit X1
Middle: M2 and Q2 form an IGBT as used for X1

Figure A5.6 shows the current curve of the isothermal IGBT matches the GT50J101 curve. At low current the subcircuit has subthreshold conduction unlike the Ritchie model. That is a good reason to use the VDMOS in a subcircuit rather than the Ritchie model supplied in LTspice. Also by using my own subcircuit I can choose my preferred symbol and terminal naming. Further, my custom subcircuit is in Block form to see inside and probe internal currents and it is open-source so anybody can change it to suit their needs.

The temperature coefficient of the subcircuit can be made to match by changing the BJT parameter XTB (exponent for Beta). This temp.co works with the MOSFETs temp.co's. The MOSFET's temp.co's depend on the process used which for the IRF610 first generation process is in the range of -3 to -6 mV/°C for the n-channel and opposite polarities for the p-channel,

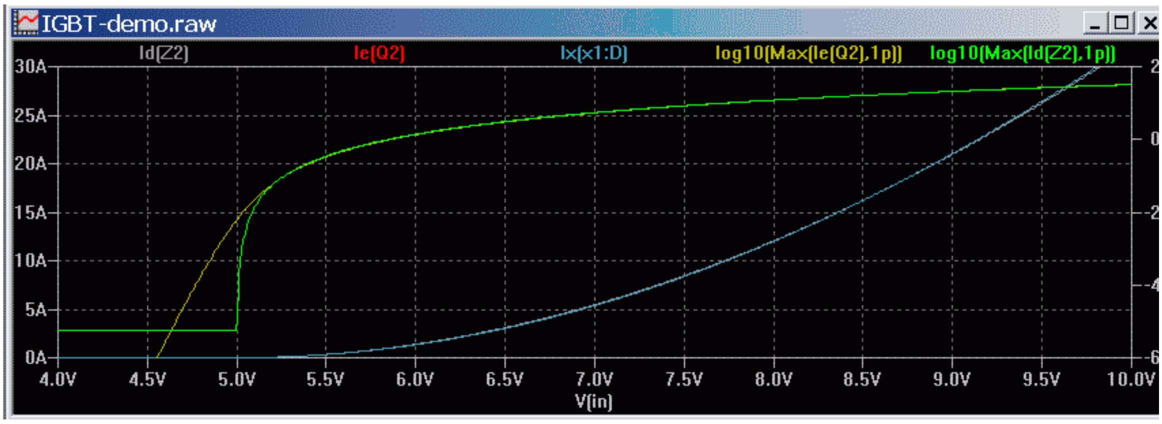


Figure A5.6. Demo jig plots for the original IGBT Id(M2) to the electrothermal subcircuit Ix(x1:D)

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Appendix 6

[Q & A maybe. Any questions?]

Please contact me via my PAK site contact page https://paklaunchsite.jimdo.com/contact

35 The Ritchie model MOSFET's Kp seems about 5 times larger than what I found best. BTW Cgs is F/cm^2 not F!

==================The-End====================