TDA8947J

4-channel audio amplifier (SE: 1 W to 25 W; BTL: 4 W to 50 W)

Rev. 01 — 06 February 2004 **Preliminary data**

1. General description

The TDA8947J contains four identical audio power amplifiers. The TDA8947J can be used as: four Single-Ended (SE) channels with a fixed gain of 26 dB, two times Bridge-Tied Load (BTL) channels with a fixed gain of 32 dB or two times SE channels (26 dB gain) plus one BTL channel (32 dB gain) operating as a 2.1 system.

The TDA8947J comes in a 17-pin Dil-Bent-Sil (DBS) power package. The TDA8947J is pin compatible with the TDA8944AJ and TDA8946AJ.

The TDA8947J contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions with no unnecessary audio holes. Almost any supply voltage and load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heatsink and ambient temperature) allow it.

2. Features

- SE: 1 W to 25 W, BTL: 4 W to 50 W operation possibility (2.1 system)
- Soft clipping
- Standby and mute mode
- No on/off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Pin compatible with TDA8944AJ and TDA8946AJ.

3. Applications

- Television
- PC speakers
- Boom box
- Mini and micro audio receivers.

PHILIPS

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	operating	9	18	26	V
		no (clipping) signal [1]	-	-	28	V
I_q	quiescent supply current	V_{CC} = 18 V; $R_L = \infty$	-	100	145	mA
I_{stb}	standby supply current		-	-	10	µA
$P_{o(SE)}$	SE output power	THD = 10 %; R_L = 4 Ω				
		V_{CC} = 18 V	7	8.5	-	W
		V_{CC} = 22 V	-	14	-	W
$P_{o(BTL)}$	BTL output power	THD = 10 %; R_L = 8 Ω				
		V_{CC} = 18 V	16	18	-	W
		V_{CC} = 22 V	-	29	-	W
THD	total harmonic distortion	SE; P_o = 1 W	-	0.1	0.5	%
		BTL; P_o = 1 W	-	0.05	0.5	%
$G_{v(max)}$	maximum voltage gain	SE	25	26	27	dB
		BTL	31	32	33	dB
SVRR	supply voltage ripple rejection	SE; f = 1 kHz	-	60	-	dB
		BTL; f = 1 kHz	-	65	-	dB

[1] The amplifier can deliver output power with non clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8947J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6. Block diagram

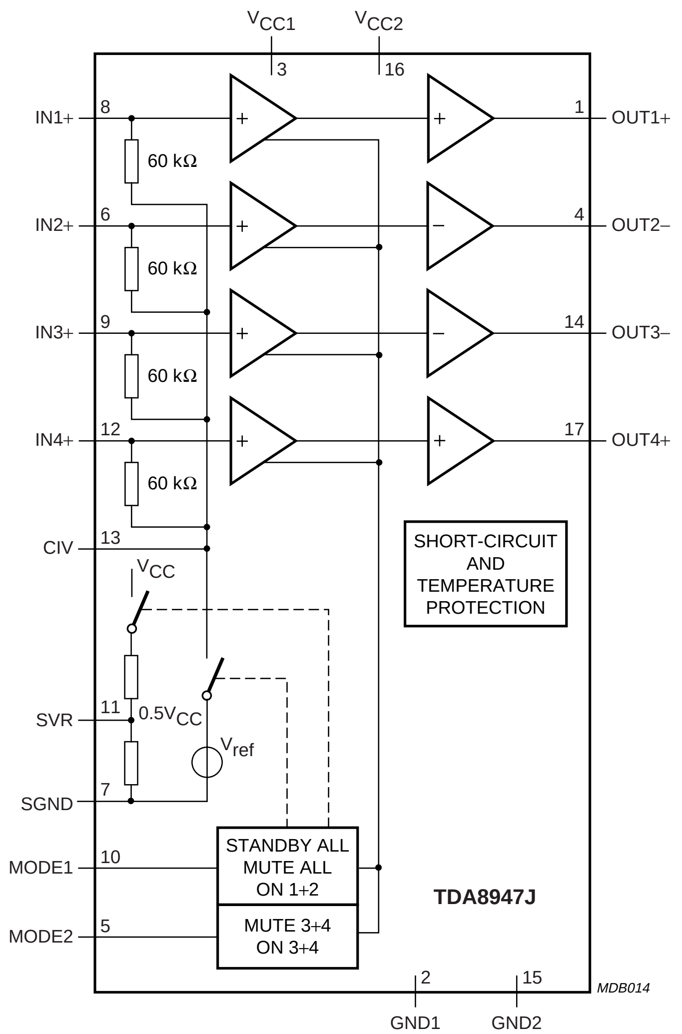


Fig 1. Block diagram.

7. Pinning information

7.1 Pinning

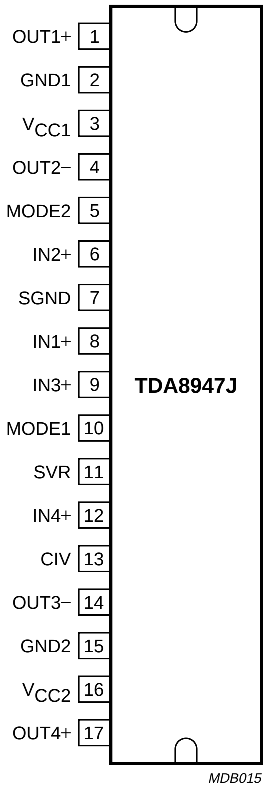


Fig 2. Pin configuration.

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
OUT1+	1	non inverted loudspeaker output of channel 1
GND1	2	ground of channels 1 and 2
V_{CC1}	3	supply voltage channels 1 and 2
OUT2–	4	inverted loudspeaker output of channel 2
MODE2	5	mode selection 2 input: mute and on for channels 3 and 4
IN2+	6	input channel 2
SGND	7	signal ground
IN1+	8	input channel 1
IN3+	9	input channel 3
MODE1	10	mode selection 1 input: standby, mute and on for all channels
SVR	11	half supply voltage decoupling (ripple rejection)
IN4+	12	input channel 4

Table 3: Pin description...*continued*

Symbol	Pin	Description
CIV	13	common input voltage decoupling
OUT3–	14	inverted loudspeaker output of channel 3
GND2	15	ground of channels 3 and 4
V_{CC2}	16	supply voltage channels 3 and 4
OUT4+	17	non inverted loudspeaker output of channel 4
TAB	-	back side tab or heats spreader has to be connected to ground

8. Functional description

8.1 Input configuration

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)} \quad (1)$$

For SE application R_i = 60 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(60 \times 10^3 \times 220 \times 10^{-9})} = 12\ \text{Hz} \quad (2)$$

For BTL application R_i = 30 kΩ and C_i = 470 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(30 \times 10^3 \times 470 \times 10^{-9})} = 11\ \text{Hz} \quad (3)$$

As shown in Equation 2 and Equation 3, large capacitor values for the inputs are not necessary, so the switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behavior.

8.2 Power amplifier

The power amplifier is a BTL and/or SE amplifier with an all-NPN output stage, capable of delivering a peak output current of 4 A.

Using the TDA8947J as a BTL amplifier offers the following advantages:

- Low peak value of the supply current
- Ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking capacitor
- Good low frequency performance.

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10 %; see Figure 8.

The maximum output power is limited by the supply voltage (V_{CC} = 26 V) and the maximum output current (I_o = 4 A repetitive peak current).

For supply voltages V_{CC} > 22 V, a minimum load is required; see Figure 5:

- SE: R_L = 3 Ω
- BTL: R_L = 6 Ω.

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom, compared to the average power output, for transferring the loudest parts without distortion.

The Average Listening Level (ALL) music power, without any distortion, yields:

- SE at $P_{o(SE)}$ = 5 W, V_{CC} = 18 V, R_L = 4 Ω and THD = 0.2 %:

$$P_{o(ALL)SE} = \frac{5 \cdot 10^3}{15.85} = 315 \text{ mW} \quad (4)$$

- BTL at $P_{o(BTL)}$ = 10 W, V_{CC} = 18 V, R_L = 8 Ω and THD = 0.1 %:

$$P_{o(ALL)BTL} = \frac{10 \cdot 10^3}{15.85} = 630 \text{ mW} \quad (5)$$

The power dissipation can be derived from Figure 9 (SE and BTL) for a headroom of 0 dB and 12 dB, respectively.

Table 4: Power rating as function of headroom

Headroom	Power output		Power dissipation (all channels driven)
	SE	BTL	
0 dB	P_o = 5 W	P_o = 10 W	P_D = 17 W
12 dB	$P_{o(ALL)}$ = 315 mW	$P_{o(ALL)}$ = 630 mW	P_D = 9 W

For heatsink calculation at the average listening level, a power dissipation of 9 W can be used.

8.3 Mode selection

The TDA8947J has three functional modes which can be selected by applying the proper DC voltage to pin MODE1.

Standby — The current consumption is very low and the outputs are floating. The device is in the standby mode when V_{MODE1} < 0.8 V, or when the MODE1 pin is grounded. In the standby mode, the function of pin MODE2 has been disabled.

Mute — The amplifier is DC-biased, but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in the mute mode when 4.5 V < V_{MODE1} < (V_{CC} – 3.5 V).

On — The amplifier is operating normally. The on mode is activated at V_{MODE1} > (V_{CC} – 2.0 V). The output of channels 3 and 4 can be set to mute or on mode.

The output channels 3 and 4 can be switched on/off by applying a proper DC voltage to pin MODE2, under the condition that the output channels 1 and 2 are in the on mode (see Figure 3).

Table 5: Mode selection

Voltage on pin		Channel 1 and 2	Channel 3 and 4 (sub woofer)
MODE1	MODE2		
0 to 0.8 V	0 to V_{CC}	standby	standby
4.5 to (V_{CC} – 3.5 V)	0 to V_{CC}	mute	mute
(V_{CC} – 2.0 V) to V_{CC}	0 to (V_{CC} – 3.5 V)	on	mute
	(V_{CC} – 2 V) to V_{CC}	on	on

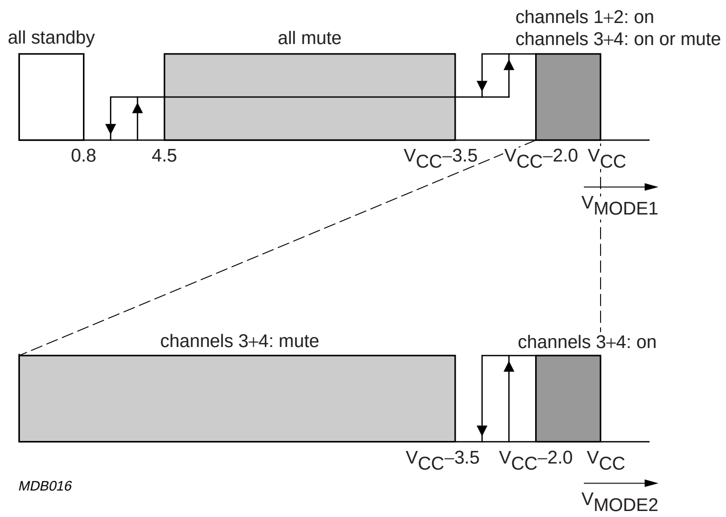


Fig 3. Mode selection.

8.4 Supply voltage ripple rejection

The Supply Voltage Ripple Rejection (SVRR) is measured with an electrolytic capacitor of 150 µF on pin SVR using a bandwidth of 20 Hz to 22 kHz. Figure 11 illustrates the SVRR as function of the frequency. A larger capacitor value on pin SVR improves the ripple rejection behavior at the lower frequencies.

8.5 Built-in protection circuits

The TDA8947J contains two types of detection sensors: one measures local temperatures of the power stages and one measures the global chip temperature. At a local temperature of approximately 185 °C or a global temperature of approximately 150 °C, this detection circuit switches off the power stages for 2 ms. High impedance of the outputs is the result. After this time period the power stages switch on automatically and the detection will take place again; still a too high temperature switches off the power stages immediately. This protects the TDA8947J against shorts to ground, to the supply voltage and across the load, and against too high chip temperatures.

The protection will only be activated when necessary, so even during a short-circuit condition, a certain amount of (pulsed) current will still be flowing through the short, just as much as the power stage can handle without exceeding the critical temperature level.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage	operating		–0.3	+26	V
		no (clipping) signal	[1]	–0.3	+28	V
V_I	input voltage			–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current			-	4	A
T_{stg}	storage temperature	non-operating		–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	total power dissipation			-	69	W
$V_{CC(sc)}$	supply voltage to guarantee short-circuit protection			-	24	V

[1] The amplifier can deliver output power with non clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.

10. Thermal characteristics

Table 7: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	all channels driven	1.3	K/W

11. Static characteristics

Table 8: Static characteristics

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; V_i = 0 V; measured in test circuit Figure 12; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage	operating	[1]	9	18	26	V
		no (clipping) signal	[2]	-	-	28	V
I_q	quiescent supply current	$R_L = \infty$	[3]	-	100	145	mA
I_{stb}	standby supply current			-	-	10	µA
Output pins							
V_O	DC output voltage		[4]	-	9	-	V
ΔV_{OUT}	differential output voltage offset	BTL mode	[5]	-	-	170	mV
Mode selection pins							
V_{MODE1}	selection voltage on pin MODE1	on		$V_{CC} - 2.0$	-	V_{CC}	V
		mute		4.5	-	$V_{CC} - 3.5$	V
		standby		0	-	0.8	V
V_{MODE2}	selection voltage on pin MODE2	on: channels 3 and 4	[6]	$V_{CC} - 2.0$	-	V_{CC}	V
		mute: channels 3 and 4		0	-	$V_{CC} - 3.5$	V
I_{MODE1}	selection current on pin MODE1	$0 < V_{MODE1} < (V_{CC} - 3.5\ V)$		-	-	20	µA
I_{MODE2}	selection current on pin MODE2	$0 < V_{MODE2} < (V_{CC} - 3.5\ V)$		-	-	20	µA

[1] A minimum load is required at supply voltages of V_{CC} > 22 V: R_L = 3 Ω for SE and R_L = 6 Ω for BTL.

[2] The amplifier can deliver output power with non clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.

[3] With a load connected at the outputs the quiescent current will increase.

[4] The DC output voltage, with respect to ground, is approximately $0.5V_{CC}$.

[5] $\Delta V_{OUT} = |V_{OUT+} - V_{OUT-}|$

[6] Channels 3 and 4 can only be set to mute or on by MODE2 when $V_{MODE1} > V_{CC} - 2.0$ V.

12. Dynamic characteristics

Table 9: Dynamic characteristics SE

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 4 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 12; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(SE)}$	SE output power	V_{CC} = 18 V; see Figure 8a					
		THD = 10 %; R_L = 4 Ω		7	8.5	-	W
		THD = 0.5 %; R_L = 4 Ω		-	6.5	-	W
		V_{CC} = 22 V					
		THD = 10 %; R_L = 4 Ω		-	14	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.1	0.5	%
G_v	voltage gain			25	26	27	dB
Z_i	input impedance			40	60	-	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	150	-	µV

Table 9: Dynamic characteristics SE...*continued*

V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 4 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 12; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	60	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	60	-	dB
$V_{o(mute)}$	output voltage in mute mode		[3]	-	-	150	µV
α_{cs}	channel separation	R_{source} = 0 Ω		50	60	-	dB
$\lvert G_v \rvert$	channel unbalance			-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with V_{MODE1} = V_{MODE2} = 7 V, and V_i = 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, including noise.

Table 10: Dynamic characteristics BTL

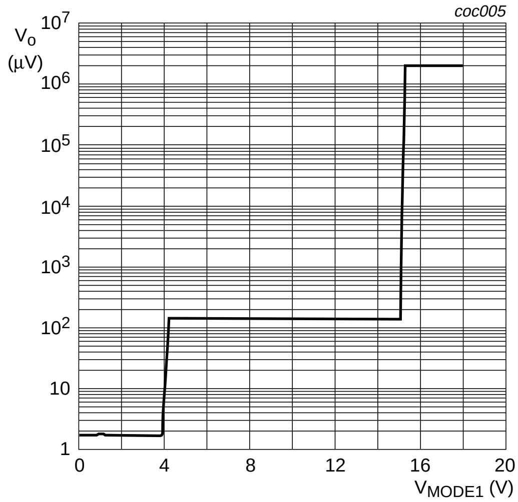
V_{CC} = 18 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 12; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(BTL)}$	BTL output power	V_{CC} = 18 V; see Figure 8b					
		THD = 10 %; R_L = 8 Ω		16	18	-	W
		THD = 0.5 %; R_L = 8 Ω		-	14	-	W
		V_{CC} = 22 V					
		THD = 10 %; R_L = 8 Ω		-	29	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.05	0.5	%
G_v	voltage gain			31	32	33	dB
Z_i	input impedance			20	30	-	kΩ
$V_{n(o)}$	noise output voltage		[1]	-	200	-	µV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	65	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	65	-	dB
$V_{o(mute)}$	output voltage in mute mode		[3]	-	-	250	µV
α_{cs}	channel separation	R_{source} = 0 Ω		50	65	-	dB
$\lvert G_v \rvert$	channel unbalance			-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{source} = 0 Ω at the input.

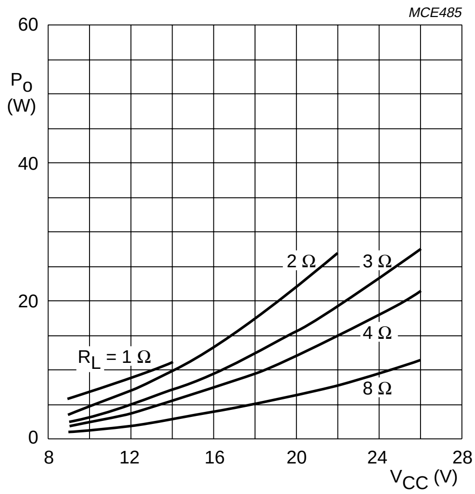
[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{source} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with V_{MODE1} = V_{MODE2} = 7 V, and V_i = 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, including noise.



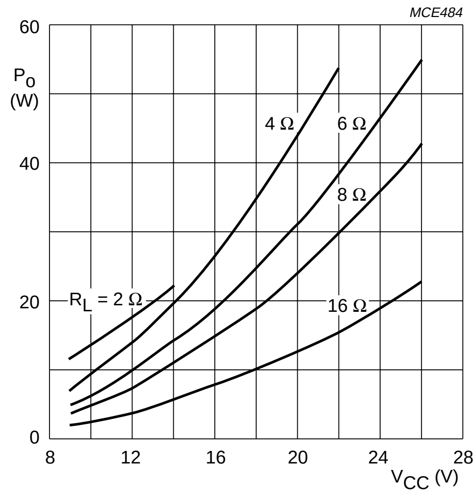
BTL; V_{CC} = 18 V; V_i = 50 mV.

Fig 4. AC output voltage as function of voltage on pin MODE1.



THD = 10 %; one channel.

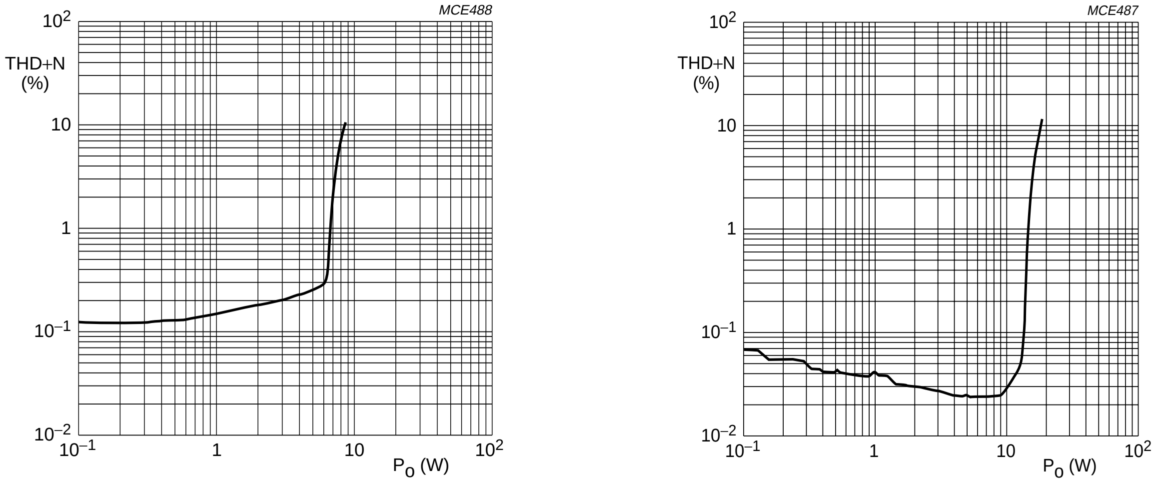
a. SE



THD = 10 %; one channel.

b. BTL

Fig 5. Output power as function of supply voltage at various loads



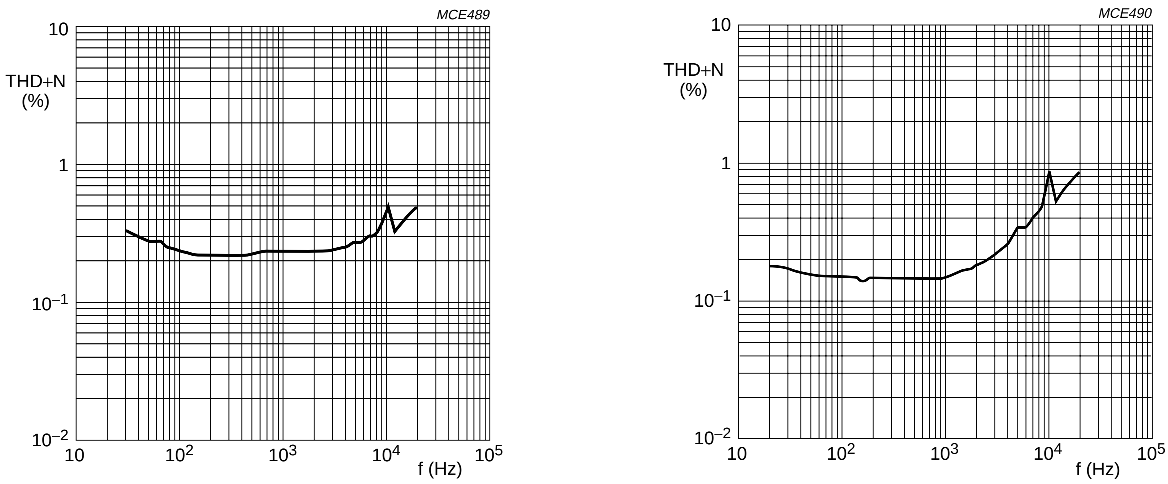
V_{CC} = 18 V; f = 1 kHz; R_L = 4 Ω.

a. SE

V_{CC} = 18 V; f = 1 kHz; R_L = 8 Ω.

b. BTL

Fig 6. Total harmonic distortion-plus-noise as function of output power.



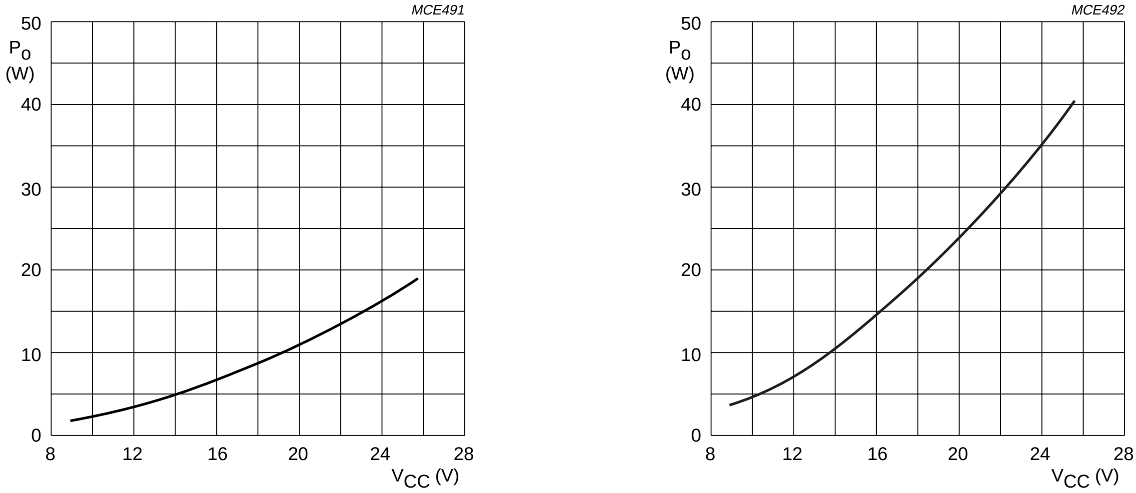
V_{CC} = 18 V; P_o = 1 W; R_L = 4 Ω.

a. SE

V_{CC} = 18 V; P_o = 1 W; R_L = 8 Ω.

b. BTL

Fig 7. Total harmonic distortion-plus-noise as function of frequency.



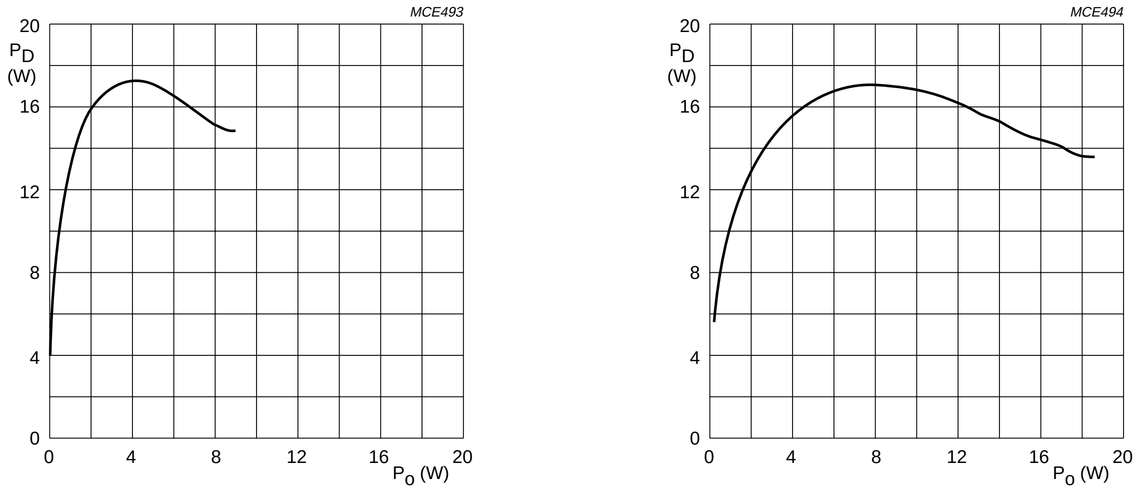
THD = 10%; R_L = 4 Ω; f = 1 kHz.

a. SE

THD = 10%; R_L = 8 Ω; f = 1 kHz.

b. BTL

Fig 8. Output power as function of supply voltage.



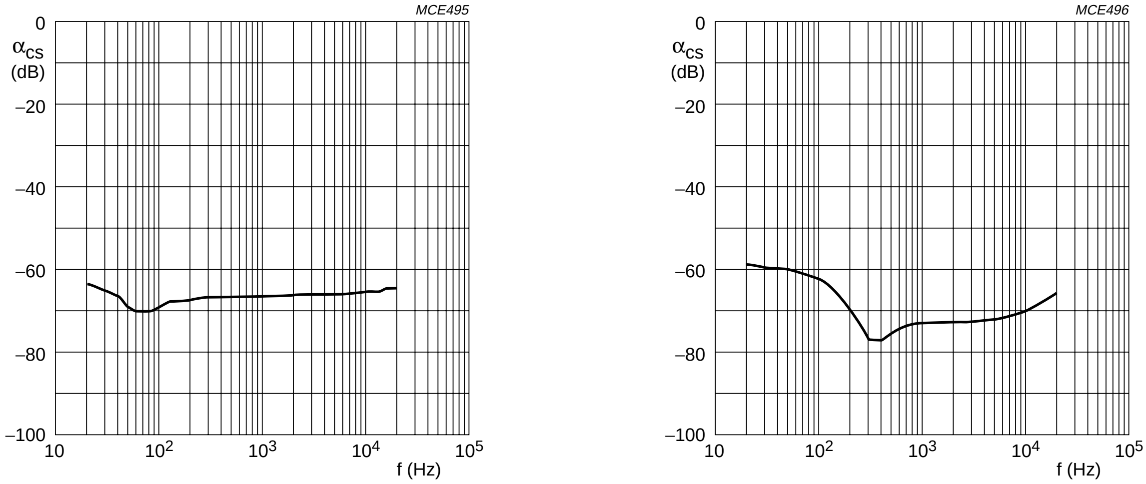
V_{CC} = 18 V; R_L = 4 Ω.

a. SE

V_{CC} = 18 V; R_L = 8 Ω.

b. BTL

Fig 9. Total power dissipation as function of channel output power per channel (worst case, all channels driven).



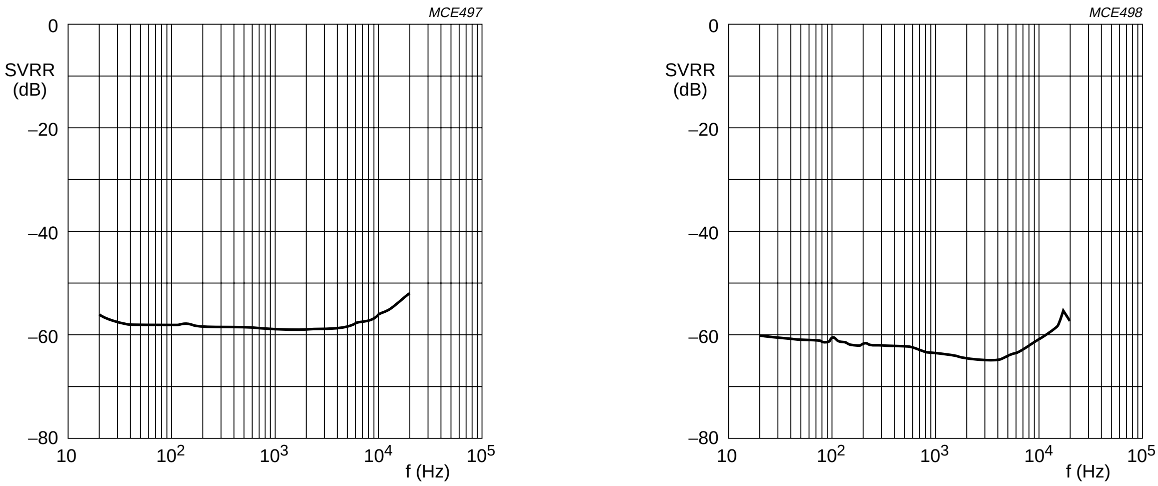
V_{CC} = 18 V; R_L = 4 Ω.

a. SE

V_{CC} = 18 V; R_L = 8 Ω.

b. BTL

Fig 10. Channel separation as function of frequency (no bandpass filter applied).



V_{CC} = 18 V; R_{source} = 0 Ω; V_{ripple} = 300 mV (RMS).
A bandpass filter of 20 Hz to 22 kHz has been applied.
Inputs short-circuited.

a. SE

V_{CC} = 18 V; R_{source} = 0 Ω; V_{ripple} = 300 mV (RMS).
A bandpass filter of 20 Hz to 22 kHz has been applied.
Inputs short-circuited.

b. BTL

Fig 11. Supply voltage ripple rejection as function of frequency.

13. Application information

13.1 Application diagrams

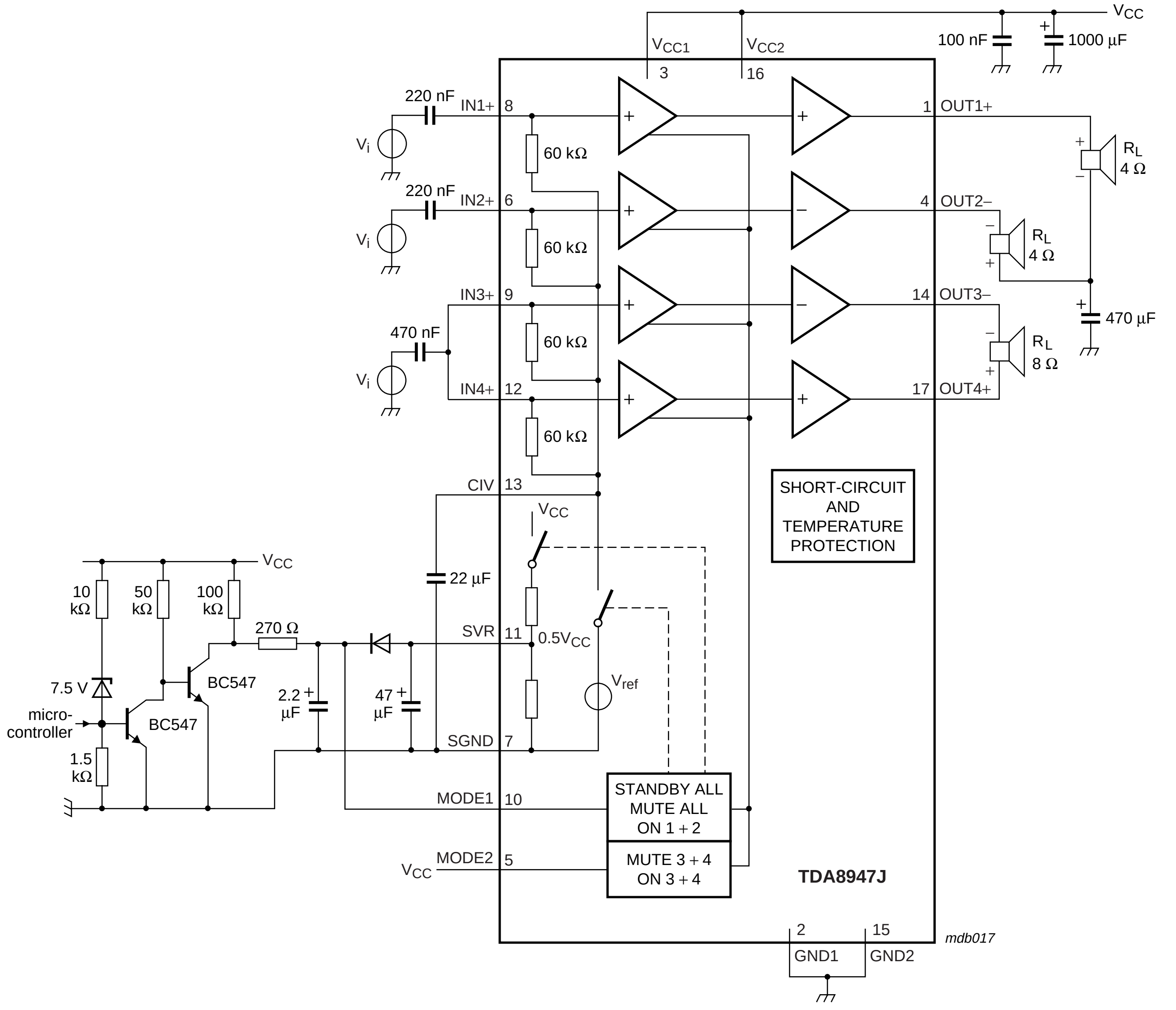


Fig 12. Typical application diagram without on/off switching plops.

Table 11: Amplifier selection by microcontroller

Microcontroller with open-collector output; see Figure 12

Microcontroller	Channels 1 and 2	Channels 3 and 4
LOW	on	on
HIGH	mute	mute

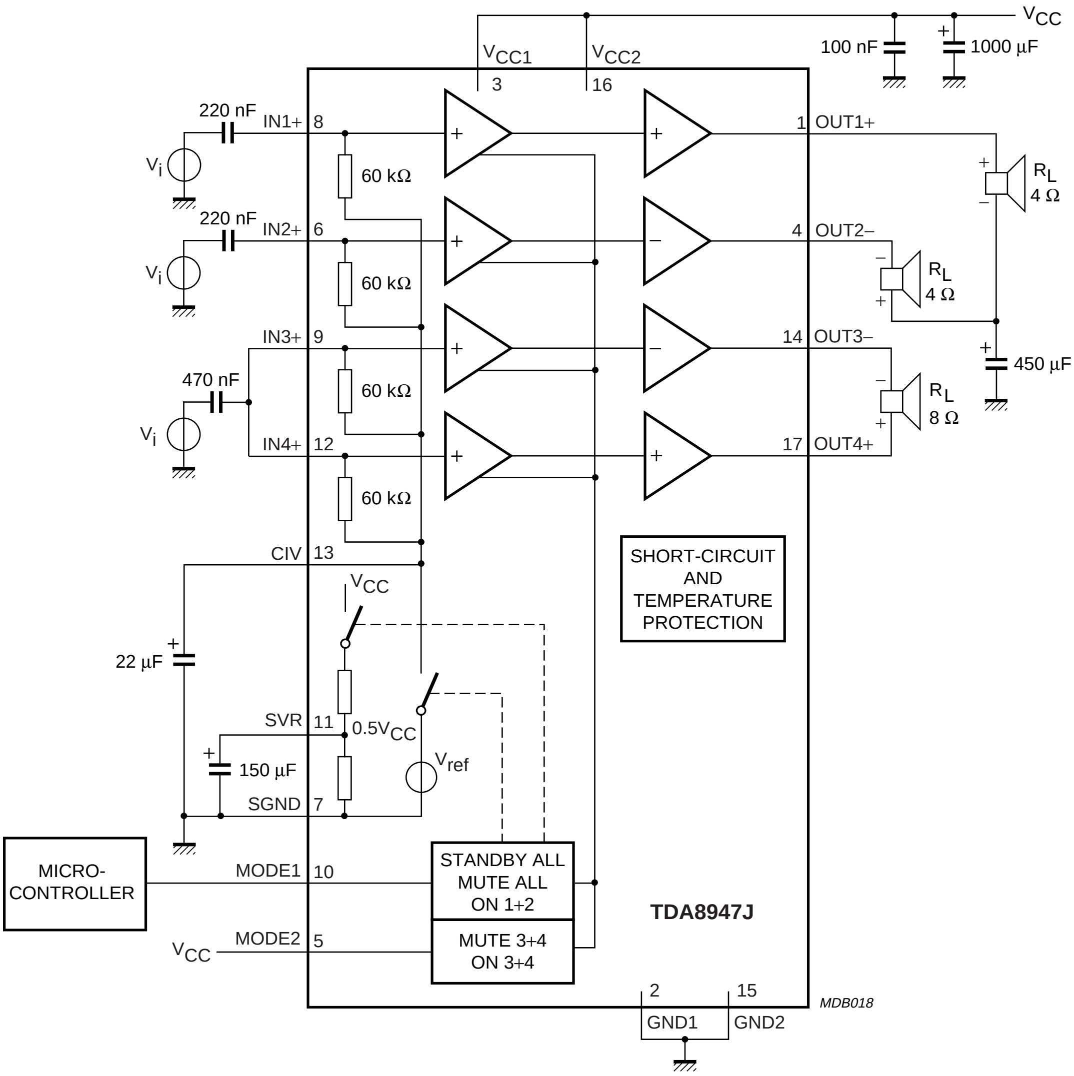


Fig 13. Application diagram with one pin control and reduction of capacitor.

Remark: Because of switching inductive loads, the output voltage can rise beyond the maximum supply voltage of 28 V. At high supply voltages, it is recommended to use (Schottky) diodes to the supply voltage and ground.

13.2 Printed-circuit board

13.2.1 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

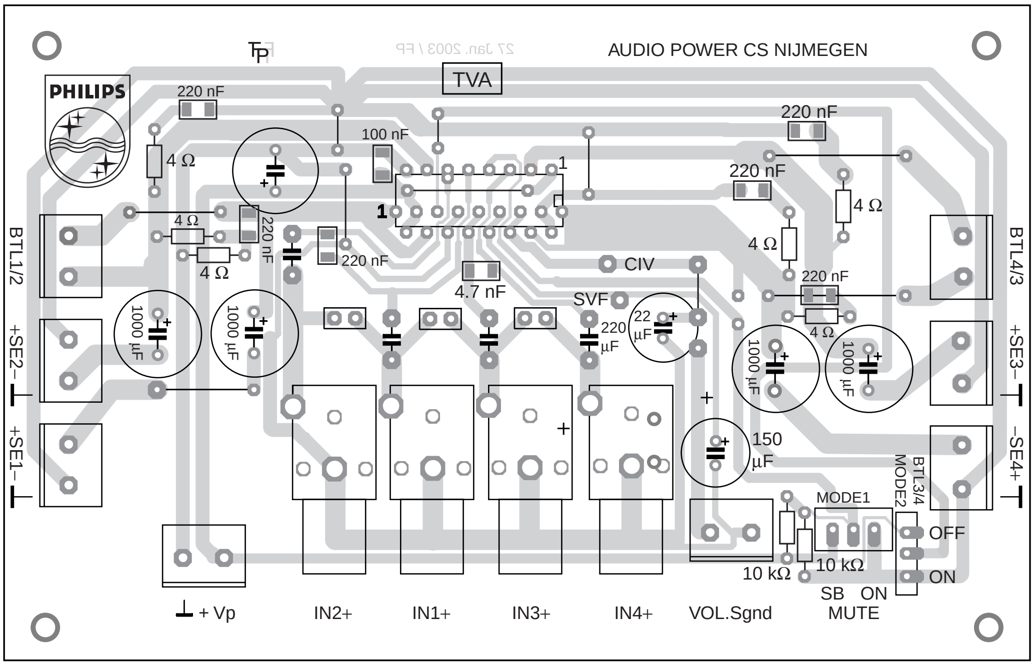


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Fig 14. Printed-circuit board layout (single-sided); components view.

13.2.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR, typical 100 nF, has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor, e.g. 1000 µF or greater, must be placed close to the device.

The bypass capacitor on pin SVR reduces the noise and ripple on the mid rail voltage. For good THD and noise performance a low ESR capacitor is recommended.

13.3 Thermal behavior and heatsink calculation

The measured maximum thermal resistance of the IC package, $R_{th(j-mb)}$, is 1.3 K/W. A calculation for the heatsink can be made, with the following parameters:

$T_{amb(max)} = 60$ °C (example)

$V_{CC} = 18$ V and $R_L = 4\ \Omega$ (SE)

$T_{j(max)} = 150$ °C (specification)

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient including the heatsink. This can be calculated using the maximum temperature increase divided by the power dissipation:

$$R_{th(tot)} = (T_{j(max)} - T_{amb(max)})/P_D$$

At $V_{CC} = 18$ V and $R_L = 4\ \Omega$ (4 × SE) the measured worst-case sine-wave dissipation is 17 W; see Figure 9. For $T_{j(max)} = 150$ °C the temperature raise, caused by the power dissipation, is: 150 – 60 = 90 °C:

$$P \times R_{th(tot)} = 90\ °C$$

$$R_{th(tot)} = 90/17 = 5.29\ K/W$$

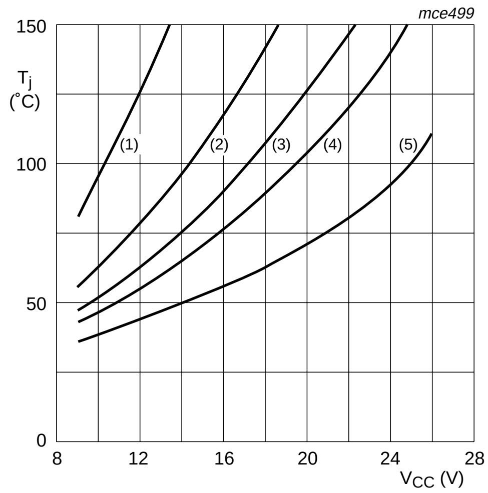
$$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 5.29 - 1.3 = 3.99\ K/W$$

This calculation is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation of 9 W (see Section 8.2.2). This allows for the use of a smaller heatsink:

$$P \times R_{th(tot)} = 90\ °C$$

$$R_{th(tot)} = 90/9 = 10\ K/W$$

$$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 10 - 1.3 = 8.7\ K/W$$



T_{amb} = 25 °C; external heatsink of 5 K/W.

(1) R_L = 1 Ω.

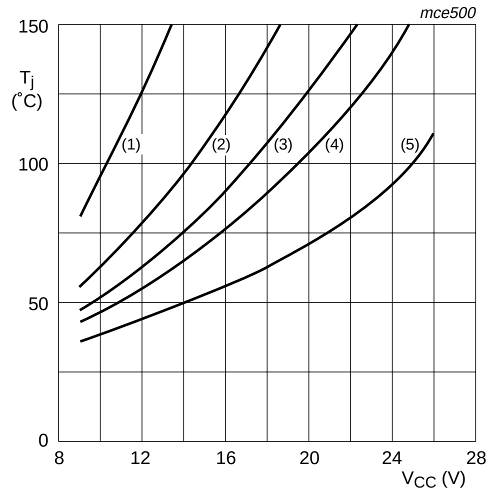
(2) R_L = 2 Ω.

(3) R_L = 3 Ω.

(4) R_L = 4 Ω.

(5) R_L = 8 Ω.

a. 4 times various SE loads with music signals.



T_{amb} = 25 °C; external heatsink of 5 K/W.

(1) R_L = 2 Ω.

(2) R_L = 4 Ω.

(3) R_L = 6 Ω.

(4) R_L = 8 Ω.

(5) R_L = 16 Ω.

b. 2 times various BTL loads with music signals.

Fig 15. Junction temperature as function of supply voltage for various loads with music signals.

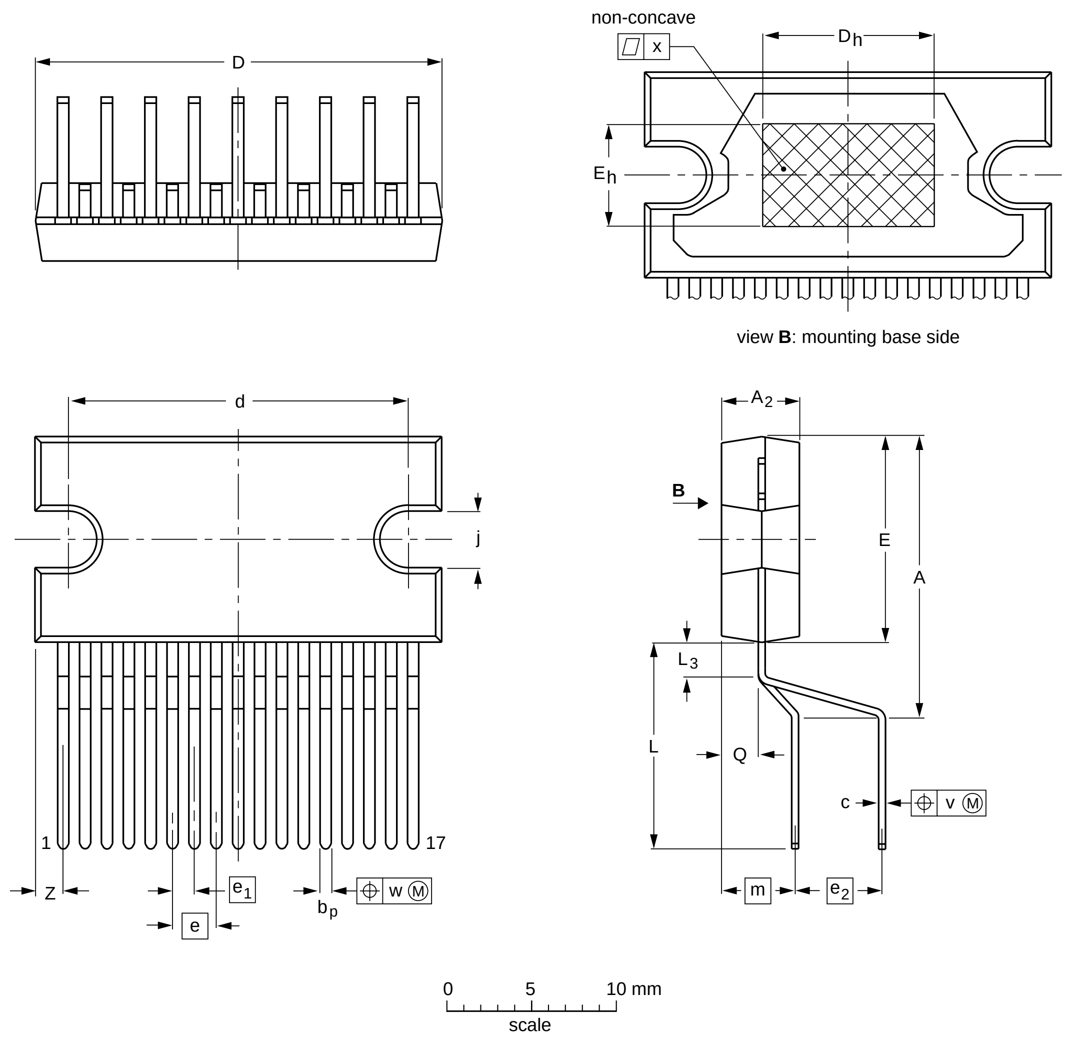
14. Test information

14.1 Quality information

The *General Quality Specification for Integrated Circuits, SNW-FQ-611* is applicable.

15. Package outline

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	D[1]	d	D_h	E[1]	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	Z[1]
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT243-1						~~99-12-17~~ 03-03-12

Fig 16. Package outline.

16. Soldering

16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

16.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.4 Package related soldering information

Table 12: Suitability of through-hole mount IC packages for dipping and wave soldering methods

Package	Soldering method	
	Dipping	Wave
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	–	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

17. Revision history

Table 13: Revision history

Rev	Date	CPCN	Description
01	20040206	-	Preliminary data (9397 750 10779)

18. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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