Home Low-cost ADC Photo Album of Electronic Projects

MiniDS

by Martin Clausen

Mini Digital Storage Scope, one channel, low cost ADC, 8 Bit, 20MHz, 32K RAM, for connection via parallel port

Table of contents:

Features

- Low cost, 20MHz, 8 Bit DAC
- 32K Bytes SRAM
- 20MHz, 2MHz and 200KHz sample rate via on board crystal oscillator and slower variable clock rates employing the PC
- Comfortable adjustable via PC software, single trimmer design
- Lines for measurement signal voltages on screen
- Bilingual user interface (German and English)
- Data can be streamed to hard disk.
- Helpfile included
- Communication protocol documentation
- Program is freeware for non-commercial use.

Systems Requirements

80386, VGA, some RAM, about 100kB harddiskspace, parallel port, one of the following operating systems: DOS, WIN95, WIN98, WIN98SE or WIN ME; WIN NT, WIN 2000 and WIN XP do not allow the required direct parallel port access

Usage

Simply type minids and press enter. If you start the program for the first time or changed something, please enter minids /setup so you can check the configuration.

Principle of Operation

The input signal amplitude is reduced by resistors. The impedance of the input signal is then reduced by an operational amplifier. To allow positive and negative input signals, the level of the signal shifted to the middle of the range of the analog-digital-converter (ADC). The input capacitance of the ADC is compensated through a capacitor in the level shifter.
The ADC is a flash converter. The PC selects a conversation frequency from the divider chain or generate one on its own. After the reset of the counter (74HC595), 32768 samples are taken by the circuit independently from the PC and stored in the SRAM. The data stream of 20MB per second could not be transferred through a parallel port. After the data acquisition is finished, the result is transferred in to the PC. The PC request the next byte by applying a clock cycle to the counter. Then the byte is transferred in two parts via the 74LS157 into the PC.
The 74LS14 is necessary to prevent latch-up and to reshape the signals. The 74HC390, 74HC251 and the quartz oscillator provide the clock signal for the counter. The 74HC251 is also used to stop data acquisition after the memory has been filled with data.
See Low-cost ADC for low cost design at lower sampling rates.

Parts

- Semiconductors:
- 6 1N4001
- 1 74LS14
- 1 74LS157

- 1 74HC107
- 1 74HC251
- 2 74HC390
- 1 74HC590
- 1 32*8 SRAM, 15ns
- 1 TDA8703
- 1 LT1227
- 1 7805
- 1 78L05
- 1 78L08
- 1 79L08
- 1 40MHz quartz oscillator, my MiniDS works also with 50MHz fine

Capacitors:

- 1 22pF cer SMD
- 1 47pF cer SMD
- 3 22nF cer SMD
- 19 100nF cer
- 2 4.7µF
- 9 10µF
- 2 220µF
- 1 1000µF

Resistors:

- 1 22
- 2 1k SMD
- 1 1.8k SMD
- 1 5k pot
- 1 15k SMD
- 1 100k SMD
- 1 27k*8 / 9 pin sil array

Mechanic:

- 1 9V / 3,6VA
- 1 sub-D socket, 25 pin
- 1 cabel, sub-D plug-plug, 25 pin
- 1 case

- 1 pbc
- 1 some thin wire

Building Hints

- Do not use a socket for TDA8703 nor LT1227
- Place 22nF capacitors as close as possible to the TDA8703
- SelRange is connected to a input of a gate but its output is not connected, because its use is at the moment not supported by the minidspreamp. However the software is already capable of handling that signal. You might modify the minidspreamp on your own to make use of this signal.

Download of Program and Circuit

- minids.exe program V1.01
- minids.ini ini-file
- minids.dat dat-file
- minids.bas source code V1.01
- minidscom.html communication protocol documentation
- minidsmain.gif main circuit V1.00
- minidspreamp.gif preamp circuit V1.00, please help to improve

The first three files are needed and expected to be placed in the same folder!

The part description in schematics is read as follows:
part type + value in exponential form + package description + subpart number in package
for example: C1040805,1 means Capacitor, 100nF, package SMD 0805, first subpart in package

Similar Projects

Description	Whom's work
DSO MK3, 2 channel DSO, employs expensive FIFO to get the same as this design, **input stage applicable to MiniDS**	David L. Jones
BitScope, combined DSO and logic analyzer, employs PIC and CPLD to get the same as this design, uses slow RS232 connection instead of parallel port, **input stage applicable to MiniDS**	BitScope

Disclaimer: No warranty at all!

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