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# Single Phase Bidirectional Dual Element Power/Energy Metering IC with Pulse Output



**sames**

## SA2007H

### FEATURES

- Two current sensor inputs
- Dual pulse and energy direction outputs
- No external crystal or resonator required
- Performs bi-directional power and energy measurement
- Meets the IEC 521/1036 Specification for Class 1 AC Watt hour meters
- Protected against ESD
- Total power consumption rating below 25mW
- Adaptable to different types of sensors
- Operates over a wide temperature range
- Precision voltage reference on-chip

### DESCRIPTION

The SAMES SA2007H is a single phase bidirectional dual element energy metering integrated circuit. It provides a simple analog interface to a micro-controller and is specifically designed for meter manufacturers to have full control over the meter functionality.

The SA2007H has two current sensor inputs. The power consumption on both inputs are continuously measured. A typical application would be to monitor Live and Neutral lines for tamper detection.

For each current sensor input the SA2007H integrated circuit has a corresponding pulse output, each generating a pulse rate with a frequency proportional to the power consumption measured on the specific channel.

The SA2007H performs active power measurement and takes the power factor into account. Energy consumption can be determined by the power measurement being integrated over time. The energy flow direction information is also available for each channel.

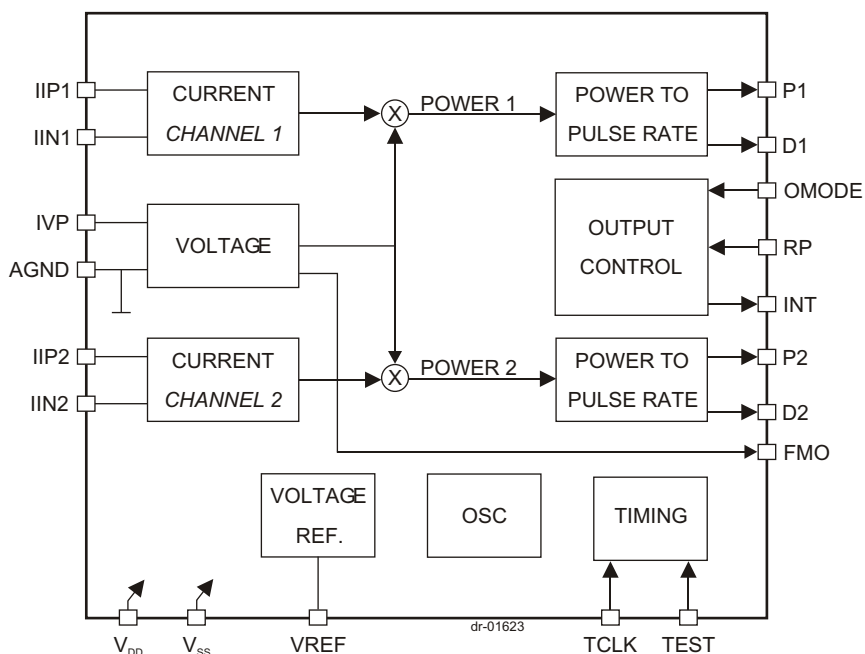


Figure 1: Block diagram

**ELECTRICAL CHARACTERISTICS**(V<sub>DD</sub> = 2.5V, V<sub>SS</sub> = -2.5V, over the temperature range -10°C to +70°C<sup>#</sup>, unless otherwise specified.)

| Parameter  | Symbol                             | Min                | Typ            | Max                | Unit           | Condition  |
|--|------------------------------------|--------------------|----------------|--------------------|----------------|--|
| Operating temp. Range  | T <sub>O</sub>                     | -25                |                | +85                | °C             |  |
| Supply Voltage: Positive   | V <sub>DD</sub>                    | 2.25               |                | 2.75               | V              |  |
| Supply Voltage: Negative   | V <sub>SS</sub>                    | -2.75              |                | -2.25              | V              |  |
| Supply Current: Positive   | I <sub>DD</sub>                    |                    | 5              | 6                  | mA             |  |
| Supply Current: Negative   | I <sub>SS</sub>                    |                    | 5              | 6                  | mA             |  |
| <b>Current Sensor Inputs (Differential)</b>                                |                                    |                    |                |                    |                |  |
| Input Current Range  | I <sub>II</sub>                    | -25                |                | +25                | µA             | Peak value   |
| <b>Voltage Sensor Input (Asymmetrical)</b>                                 |                                    |                    |                |                    |                |  |
| Input Current Range  | I <sub>IV</sub>                    | -25                |                | +25                | µA             | Peak value   |
| Pin VREF<br>Ref. Current<br>Ref. Voltage                                   | -I <sub>R</sub><br>V <sub>R</sub>  | 45<br>1.1          | 50             | 55<br>1.3          | µA<br>V        | With R = 24k<br>connected to V <sub>SS</sub><br>Reference to V <sub>SS</sub> |
| <b>Digital I/O</b>   |                                    |                    |                |                    |                |  |
| Pins P1, P2, D1, D2, FMO, INT<br>Output High Voltage<br>Output Low Voltage | V <sub>OH</sub><br>V <sub>OL</sub> | V <sub>DD</sub> -1 |                | V <sub>SS</sub> +1 | V<br>V         | I <sub>OH</sub> = -2mA<br>I <sub>OL</sub> = 5mA                              |
| Pins TCLK, TEST, OMODE, RP<br>Input High Voltage<br>Input Low Voltage      | V <sub>IH</sub><br>V <sub>IL</sub> | V <sub>DD</sub> -1 |                | V <sub>SS</sub> +1 | V<br>V         |  |
| Pulse Rate P1, P2  | f <sub>p</sub>                     | 5<br>0             | 1360           | 1600<br>3000       | Hz<br>Hz<br>Hz | At rated input conditions<br>Specified linearity<br>Min and Max frequency    |
| Pulse Width P1, P2   | t <sub>pp</sub><br>t <sub>pn</sub> |                    | 71.55<br>143.1 |                    | µs<br>µs       | Positive energy flow<br>Negative energy                                      |
| Pins TCLK, TEST, RP, OMODE<br>Pull down current                            | I <sub>IL</sub>                    | 48                 |                | 110                | µA             | V <sub>I</sub> = V <sub>DD</sub>   |

#Extended Operating Temperature Range available on request.

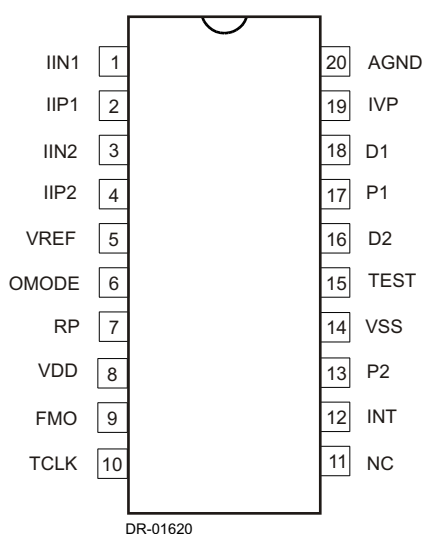
**ABSOLUTE MAXIMUM RATINGS\***

| Parameter             | Symbol                           | Min  | Max  | Unit |
|-----------------------|----------------------------------|------|------|------|
| Supply Voltage        | V <sub>DD</sub> -V <sub>SS</sub> | -0.3 | 6.0  | V    |
| Current on any pin    | I <sub>PIN</sub>                 | -150 | +150 | mA   |
| Storage Temperature   | T <sub>STG</sub>                 | -40  | +125 | °C   |
| Operating Temperature | T <sub>O</sub>                   | -25  | +85  | °C   |

\*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other condition above those indicated in the operational sections of this specification, is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

**PIN DESCRIPTION**

| PIN           | Designation              | Description  |
|---------------|--------------------------|--|
| 20            | AGND                     | Analog Ground. The voltage to this pin should be mid-way between $V_{DD}$ and $V_{SS}$ .   |
| 8             | $V_{DD}$                 | Positive supply voltage. The voltage to this pin is typically +2.5V if a shunt resistor is used for current sensing or in the case of a current transformer a +5V supply can be applied.   |
| 14            | $V_{SS}$                 | Negative supply voltage. The voltage to this pin is typically -2.5V if a shunt resistor is used for current sensing or in the case of a current transformer a 0V supply can be applied.  |
| 19            | IVP                      | Analog Input for Voltage. The current into the A/D converter should be set at $14\mu A_{RMS}$ at nominal mains voltage. The voltage sense input saturates at an input current of $\pm 25\mu A$ peak.   |
| 1, 2,<br>3, 4 | IIN1, IIP1<br>IIN2, IIP2 | Inputs for current sensor - Channel 1 and Channel 2. The shunt resistor voltage from each channel is converted to a current of $16\mu A_{RMS}$ at rated conditions. The current sense input saturates at an input current of $\pm 25\mu A$ peak. |
| 5             | VREF                     | This pin provides the connection for the reference current setting resistor. A 24k resistor connected to $V_{SS}$ sets the optimum operating condition.  |
| 6             | OMODE                    | This logic input is used to select between latched or unlatched condition for the pulse and direction outputs.   |
| 7             | RP                       | A logic input is used to reset the latched outputs which is required after an interrupt has occurred.  |
| 9             | FMO                      | The zero crossover of the voltage sense input is signaled on this pin.   |
| 10, 15        | TCLK, TEST               | Configure / Test inputs. For normal operations these pins must be connected to $V_{SS}$ .  |
| 12            | INT                      | This logic output will indicate a change in status of the pulse or direction outputs.  |
| 17, 13        | P1, P2                   | Pulse outputs. The P1 and P2 outputs give instantaneous pulse outputs of channel 1 and channel 2 respectively. The pulse is active low with a pulse width of 71.5 $\mu s$ for positive energy and doubles for reverse energy.                    |
| 18, 16        | D1, D2                   | Direction output. These outputs indicate the energy flow direction of each channel.  |
| 11            | NC                       | No Connection.   |

**ORDERING INFORMATION**

| Part Number | Package |
|-------------|---------|
| SA2007HPA   | DIP-20  |
| SA2007HSA   | SOIC-20 |

Figure 2: Pin connections: Package: DIP-20, SOIC-20



### FUNCTIONAL DESCRIPTION

The SA2007H is a CMOS mixed signal analog/digital integrated circuit, which performs power/energy calculations across a power range of 1000:1, to an overall accuracy of better than Class 1.

The integrated circuit includes all the required functions for 1-phase power and energy measurement such as oversampling A/D converters for the voltage and current sense inputs, power calculation and energy integration. Internal offsets are eliminated through the use of cancellation procedures.

Referring to the block diagram (figure 1) the SA2007H has two current sense channels and a voltage sense channel. The voltage measured is multiplied with the current measured on the two channels. The multiplied signals from each current channel is fed to separate power to pulse rate blocks.

The power to pulse rate blocks generate pulses at a frequency proportional to the instantaneous active power measured. Pulses on output P1 represent energy measured on current channel 1. The pulses on output P2 represent energy measured on current channel 2. Counting the pulses generated represents the energy measured.

A typical application would be to simultaneous measure energy/power consumption in both Live and Neutral lines. A meter tamper condition could be detected when an imbalance exists between the live and neutral energy/power measured.

Two modes of operation is available on the SA2007H, in one mode the device is functionally the same as two SA2002H devices sharing a common voltage channel. Alternatively the pulse output is latched and an interrupt is generated on any change of the pulse outputs.

### POWER CALCULATION

In Figure 8, the voltage drops across the current transformers terminating resistors are converted to currents for each current sense input, by means of resistors  $R_{10}$  and  $R_{11}$  (channel 1) as well as  $R_{12}$  and  $R_{13}$ . (channel 2). The current sense input saturates at an input current of  $\pm 25\mu A$  peak.

The mains voltage (230VAC) is divided down through a divider to  $14V_{RMS}$ . The current into the A/D converter input is set at  $14\mu A_{RMS}$  at nominal mains voltage, via resistor  $R_7$  (1M).

In this configuration, with a mains voltage of 230V and a current of 80A, the output frequency measured on P1 or P2 pin is 1360Hz. In this case the energy associated with a single pulse is  $18.4kW/1360Hz = 13.5Ws$  per pulse.

### ANALOG INPUT CONFIGURATION

The input circuitry of the current and voltage sensor inputs are illustrated in figure 3. These inputs are protected against electrostatic discharge through clamping diodes.

The feedback loops from the outputs of the amplifiers  $A_1$  and  $A_v$  generate virtual shorts on the signal inputs. Exact duplications of the input currents are generated for the analog signal processing circuitry.

### ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The SA2007H integrated circuit's input's/outputs are protected against ESD.

### POWER CONSUMPTION

The power consumption rating of the SA2007H integrated circuit is less than 30mW.

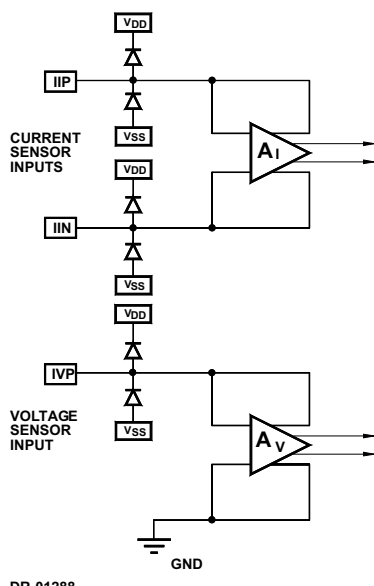


Figure 3: Analog input internal configuration



### INPUT SIGNALS

#### Voltage reference (VREF)

A bias resistor of 24k sets optimum bias conditions on chip. Calibration of the SA2007H should be done in the micro-controllers software.

#### Output Mode (OMODE)

The output behavior of the SA2007H is selectable between fixed width outputs or latched outputs. In fixed width mode the P1 and P2 output pulses stay at a fixed width. In latched mode the status of P1 and P2 are cleared with a logic 1 on the RP pin.

Refer to the "Output signals in latched mode" section (Page 6) for further information.

| OMODE | Description      |
|-------|------------------|
| 0     | Fixed width mode |
| 1     | Latched mode     |

#### Clear Interrupt (RP)

A logic 1 on the RP input is used to clear the interrupt generated by the SA2007H when a pulse is generated on P1 or P2, while operating in latched mode. By clearing the interrupt in latched mode the status of the pulse outputs will also be cleared.

#### Test Inputs (TEST, TCLK)

For normal operations these pins must be connected to V<sub>SS</sub>.

### OUTPUT SIGNALS

#### Pulse outputs (P1, P2)

The output on P1 and P2 is a pulse density signal representing the instantaneous power/energy measurement as shown in figure 4. The pulse width  $t_p$  on P1 and P2 change with the direction of energy measurement  $t_p$  is 71.5µs for positive energy and doubles (143µS) if negative energy is measured. The output frequency may be calculated using the following formula:

$$f = 11.16 \times F_{OUT} \times (I_L \times I_V) / I_R^2$$

Where:

F<sub>OUT</sub>= Typical rated output frequency (1360Hz)

I<sub>L</sub> = Input current on current sense input (16µA at rated conditions)

I<sub>V</sub> = Input current on voltage sense input (14µA at rated conditions)

I<sub>R</sub> = Reference current on VREF typically 50µA

An integrated anti-creep function does not allow output pulses on P1 or P2 if no power is measured by the device.

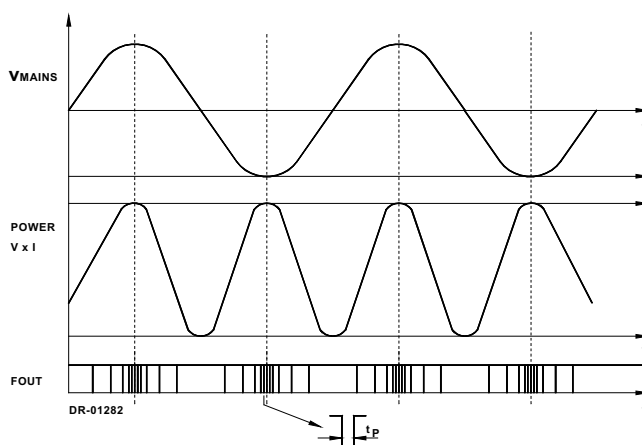


Figure 4: FOUT instantaneous pulse output

#### Direction indication (D1, D2)

The SA2007H provides information about the energy flow direction of both current channels separately on pins D1 and D2.

Logic 0 on pin D1 or D2 indicates reverse energy flow of that particular channel. Reverse energy flow is defined as the condition where the voltage sense input and current sense input are out of phase (greater than 90 degrees).

Positive energy flow, when voltage sense and both current sense input are in phase, is indicated on pin D1 or D2 as a logic 1.

Figure 5 shows the behavior of D1 and D2, when energy reversal takes place. The time period for the direction signal to change state,  $t_{DIR}$ , is the time it takes for the internal integrator to count (down) from its present value to zero. Thus the energy consumption rate determines the speed of change on the direction outputs.

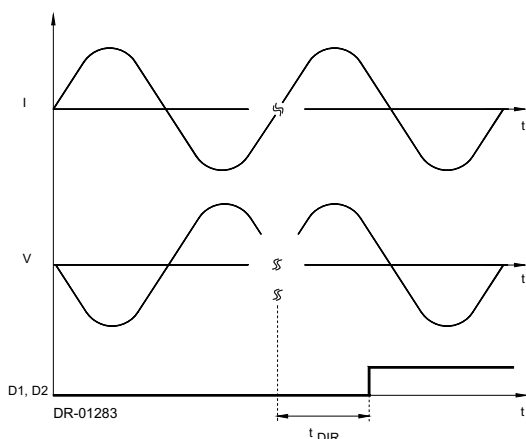


Figure 5: Measured energy direction on D1 or D2

#### Mains zero crossing indication (FMO)

The square wave signal of FMO indicates the polarity of the mains voltage. Due to comparator offsets, the FMO low to high transition can occur within a range as shown in figure 6. The time between successive low to high transitions will be equal to the mains voltage period.

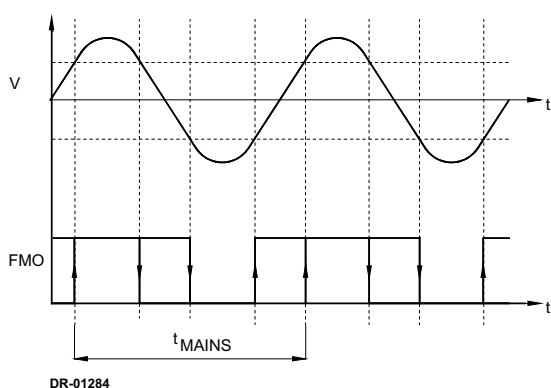


Figure 6: Mains zero crossing on FMO

#### Interrupt (INT)

While the SA2007H is operating in latched mode (see Output mode description) an interrupt is generated with the falling edge of the pulse outputs P1 and P2 (see figure 7). INT is cleared with a logic 1 on the RP input.

#### OUTPUT SIGNALS IN LATCHED MODE

Latched mode is selected by setting the OMODE input to logic 1. This mode is used with a micro controller to ensure that any simultaneous pulses on P1 and P2 are not missed. The functionality of the latched mode is shown in figure 7.

An interrupt is generated with a falling edge on any of the pulse output signals P1 and P2. The micro controller needs to scan the status of the pulse outputs as well as the direction signals D1 and D2 during its interrupt service routine. The micro controller clears the interrupt by setting the RP input to a logic 1. The pulse outputs P1 and P2 are cleared along with the interrupt. Note that energy pulses are inhibited when the interrupt output is set (during latched mode).

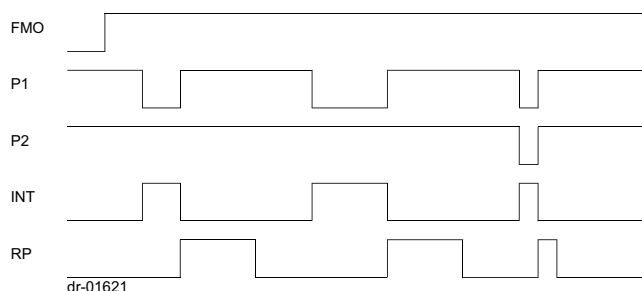


Figure 7: Output signals in latched mode

**TYPICAL APPLICATION**

The analog (metering) interface shown in figure 8, is designed for measuring 230V/60A with precision better than Class 1. The most important external components for the SA2007H integrated circuit are the current sense resistors, the voltage sense resistors and the bias setting resistor. The resistors used in the metering section should be of the same type so temperature effects are minimized.

**Current Input IIN1, IIP1, IIN2, IIP2**

Two current transformers are used to measure the current in the live and neutral phases. The output of the current transformer is terminated with a low impedance resistor. The voltage drop across the termination resistor is converted to a current that is fed to the differential current inputs of the SA2007H.

**CT Termination Resistor**

The voltage drop across the CT termination resistor at rated current should be at least 20mV. The CT's have low phase shift and a ratio of 1:2500. The CT's are terminated with a 3.6 resistor giving a voltage drop of 86.4mV across each termination resistor at rated conditions ( $I_{max}$  for the meter).

**Current Sensor Input Resistors**

The resistors R10, R11 and R12, R13 define the current level into the current sense inputs of the SA2007H. The resistor values are selected for an input current of 16µA at rated conditions. For a 60A meter and a CT Ratio of 2500:1 the resistor values are calculated as follows:

$$\begin{aligned} R10 = R11 &= (I / 16\mu A) \times R_{SH} / 2 \\ &= 60A / 2500 / 16\mu A \times 3.6 / 2 \\ &= 2.7k \end{aligned}$$

$I_L$  = Line current

$R_{SH}$  = CT Termination resistor

2500 = CT ratio

The two current channels are identical so R10 = R11 = R12 = R13.

**Voltage Input IVP**

The voltage input of the SA2007H (IVP) is driven with a current of 14µA at nominal mains voltage. This voltage input saturates at approximately 17µA. At a nominal voltage current of 14µA allows for 20% overdriving. The mains voltage is divided with a voltage divider to 14V that is fed to the voltage input pins via a 1M resistor.

**Voltage Divider**

The voltage divider is calculated for a voltage drop of 14V. Equations for the voltage divider are:

$$\begin{aligned} RA &= R1 + R2 + R3 \\ RA &= R7 \parallel (R5 + P1) \end{aligned}$$

Combining the two equations gives:

$$(RA + RB) / 230V = RB / 14V$$

Values for resistors R4 = 10 , R5 = 22k and R7 = 1M is chosen.

Substituting the values result in:

$$\begin{aligned} RB &= 21.526k \\ RA &= RB \times (230V / 14V - 1) \\ RA &= 332.12k \end{aligned}$$

Standard resistor values for R1, R2 and R3 are chosen to be 100k , 100k and 120k .

The capacitor C1 is used to compensate for phase shift between the voltage sense inputs and the current sense inputs of the device, in cases where CTs with phase errors are used. The phase shift caused by the CT may be corrected by inserting a capacitor in the voltage divider circuit. To compensate for a phase shift of 0.18 degrees the capacitor value is calculated as follows:

$$\begin{aligned} C &= 1 / (2 \times \text{Mains frequency} \times R5 \times \tan(\text{Phase shift angle})) \\ C &= 1 / (2 \times 50 \times 1M \times \tan(0.18 \text{ degrees})) \\ C &= 1.013\mu F \end{aligned}$$

**Reference Voltage Bias resistor**

R6 defines all on chip and reference currents. With R6 = 24k optimum conditions are set. Calibration should be done in the micro controller software.



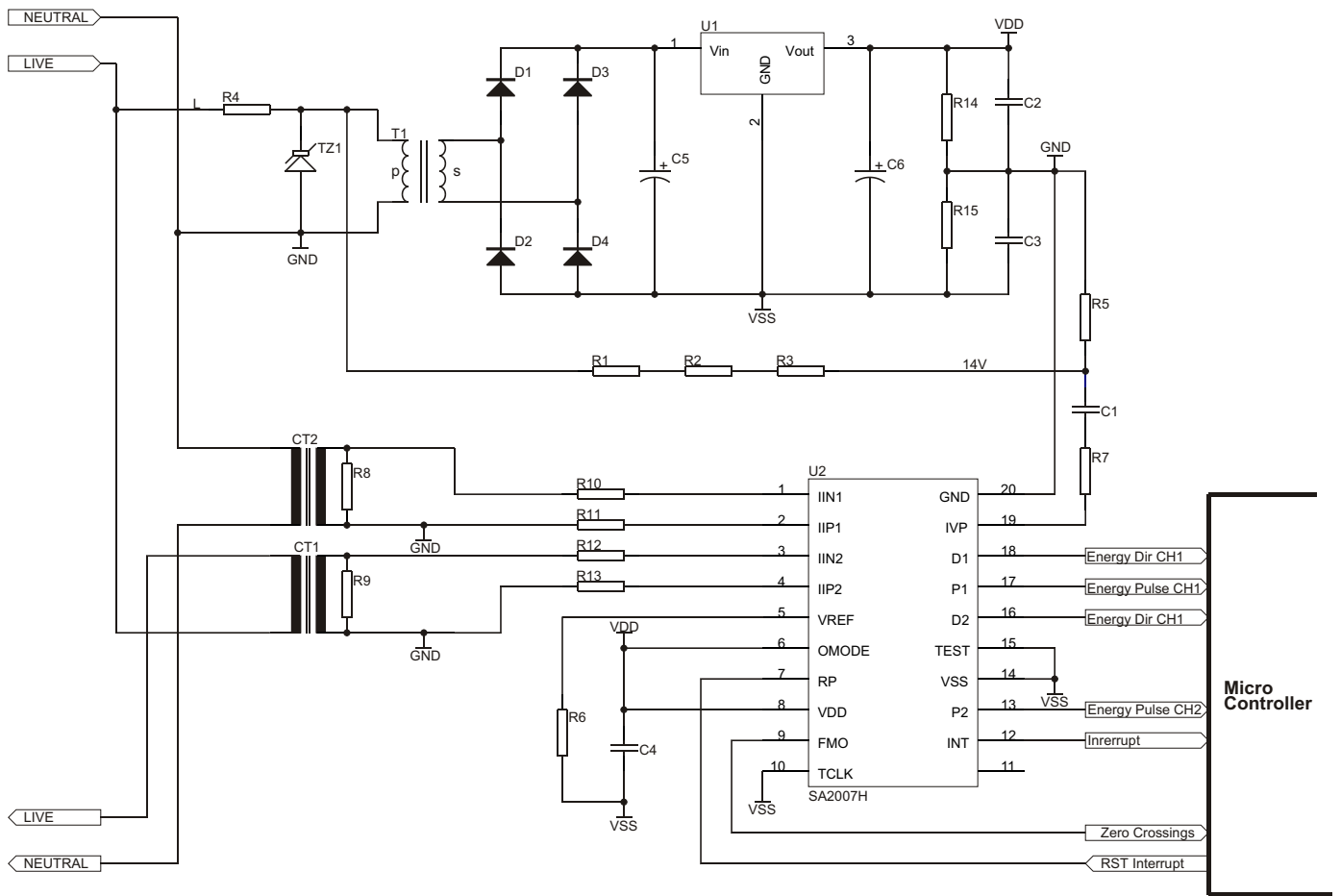


Figure 8: Application circuit showing metering section



## Parts List for Application Circuit: Figure 8

| Item | Symbol | Description                                | Detail         |
|------|--------|--|----------------|
| 1    | U2     | SA2007H                                    | DIP-20/SOIC-20 |
| 2    | D1     | Diode, Silicon 1N4148                      | or Similar     |
| 3    | D2     | Diode, Silicon 1N4148                      | or Similar     |
| 4    | D3     | Diode, Silicon 1N4148                      | or Similar     |
| 5    | D4     | Diode, Silicon 1N4148                      | or Similar     |
| 6    | R1     | Resistor, 100k, 1/4W, 1%, metal            |                |
| 7    | R2     | Resistor, 100k, 1/4W, 1%, metal            |                |
| 8    | R3     | Resistor, 120k, 1/4W, 1%, metal            |                |
| 9    | R4     | Resistor, 10 , 2W, Wire wound              |                |
| 10   | R5     | Resistor, 24k, 1/4W, 1%, metal             |                |
| 11   | R6     | Resistor, 24k, 1/4W, 1%, metal             |                |
| 12   | R7     | Resistor, 1M, 1/4W, 1%, metal              |                |
| 13   | R8     | Resistor, 3.6 , 1/4W, 1%, metal            | Note 2         |
| 14   | R9     | Resistor, 3.6 , 1/4W, 1%, metal            | Note 2         |
| 15   | R10    | Resistor, 2.7k, 1/4W, 1%, metal            | Note 1         |
| 16   | R11    | Resistor, 2.7k, 1/4W, 1%, metal            | Note 1         |
| 17   | R12    | Resistor, 2.7k, 1/4W, 1%, metal            | Note 1         |
| 18   | R13    | Resistor, 2.7k, 1/4W, 1%, metal            | Note 1         |
| 19   | R14    | Resistor, 1k, 1/4W                         |                |
| 20   | R15    | Resistor, 1k, 1/4W                         |                |
| 21   | C1     | Capacitor                                  | Note 4         |
| 22   | C2     | Capacitor, 220nF                           |                |
| 23   | C3     | Capacitor, 220nF                           |                |
| 24   | C4     | Capacitor, 820nF                           | Note 3         |
| 25   | C5     | Capacitor, 2200 $\mu$ F, 25V, electrolytic |                |
| 26   | C6     | Capacitor, 100 $\mu$ F, 16V, electrolytic  |                |
| 27   | CT1    | Current Transformer                        |                |
| 28   | CT2    | Current Transformer                        |                |
| 29   | T1     | Transformer, 230V/9V                       |                |
| 30   | U1     | 78LC05, Voltage regulator                  |                |
| 31   | TZ1    | 400V, Metal oxide varistor                 |                |

**Note 1:** Resistor (R10, R11, R12 and R13) values are dependent upon the selected value of R8 and R9

**Note 2:** See TYPICAL APPLICATION when selected the value of R8 and R9.

**Note 3:** Capacitor (C4) to be positioned as closed to Supply Pins ( $V_{DD}$  &  $V_{SS}$ ) of U-1, as possible.

**Note 4:** Capacitor (C1) selected to minimize phase error introduced by current transformer (typically 1.5 $\mu$ F for normal CTs)



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**SA2007H**

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