The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7532 chips it is possible to produce 4X, 3X, 2X step-ups of the V_{DD2}-V_{SS} voltage levels.

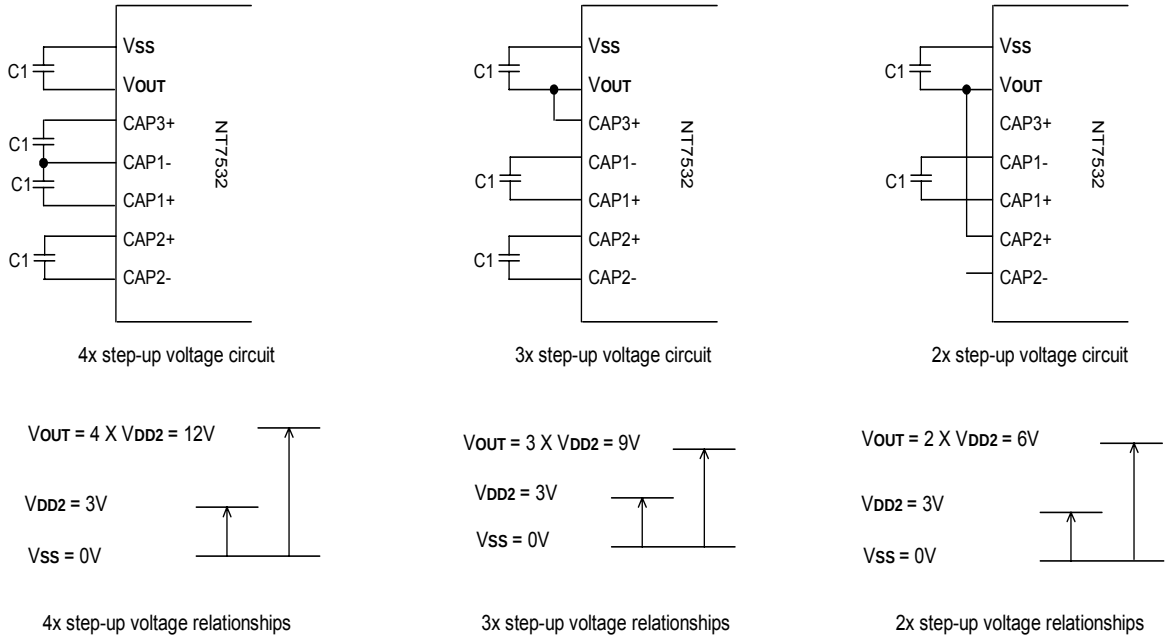


Figure. 7

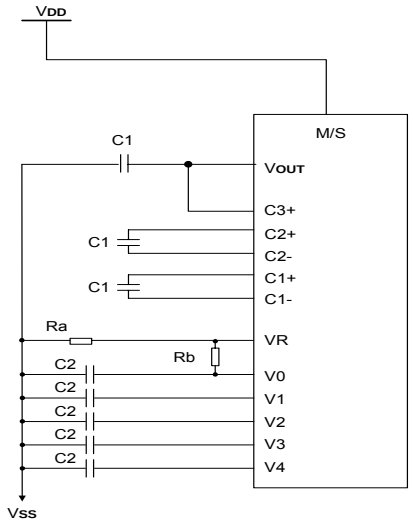
The Voltage Regulator Circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7532 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

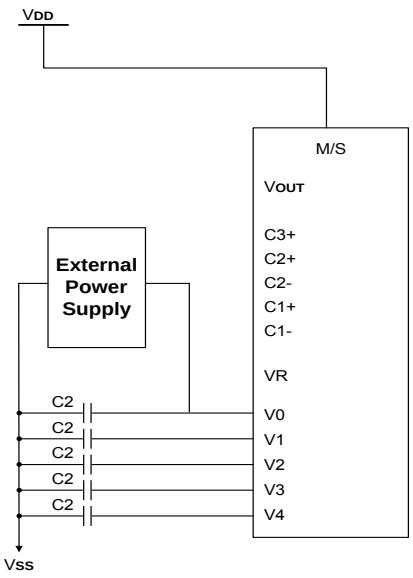
Moreover, in the NT7532, two types of thermal gradients have been prepared as VREG options: (1) approximately –0.05%/℃and (2) external input (supplied to the VEXT terminal).

Reference Power Supply Circuit for Driving LCD Panel

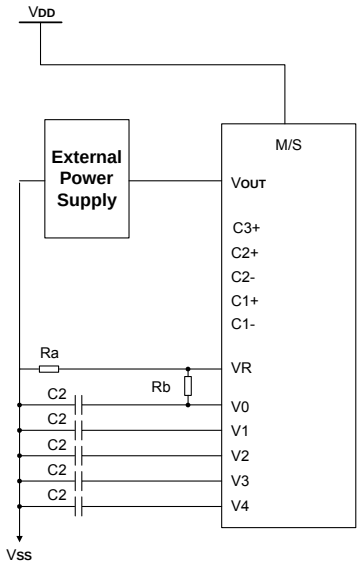
-When using all LCD power circuits
(Voltage converter regulator and follower)
(In case of 3X boosting circuit)



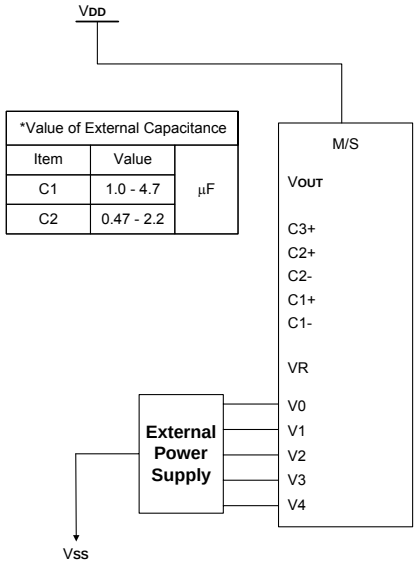
-When only using voltage follower



-When not using voltage booster circuits



-When not using internal LCD power supply circuits



Reset Circuit

When the /RES input falls to “L”, these LSI reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/55, 1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF
   Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address 0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:
    V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0 = “L”)
17. Output condition of COM, SEG
    COM: V1
    SEG: V2

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect.The MPU interface (Reference Example)”, the /RES terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RES terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition; therefore, take measures to prevent the input terminal from entering a high impedance state.
In the NT7532, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the /RES terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the /RES terminal is “L,” the display timing generator circuit is stopped, and the FR, FRS, and /DOF terminals are fixed to “H,” and the CL pin is fixed to “H” only when the intermal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

Commands

The NT7532 uses a combination of A0, /RD(E) and /WR (R/W) signals to identify data bus signals. As the chip analyzes and executes each command using the internal timing clock only, regardless of the external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the /RD pad and a write status when a low pulse is input to the /WR pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/W pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics). Accordingly, in the command explanation and command table, (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is the only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands are explained below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Display ON/OFF
   Alternatively turns the display on and off.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1 0	Display ON Display OFF

   When the display OFF command is executed when in the display all points ON mode, the power save mode is entered. See the section on the power saver for details.

2. Set Display Start Line
   Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of the LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. This command changes when the line address, smooth scrolling or a page change take place.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

Specifies the page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

4. Set Column Address

It specifies column address of display RAM. It divides the column address into 4 higher bits and 4 lower bits. Set each of them in succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7532 is busy due to the internal operation or reset. Any command is rejected until BUSY becomes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address “131-n” corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates that the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after the column address setup. Refer to the display RAM section of the FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure4. When display data is written or read, the column address is incremented by 1 as shown in Figure4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, rotation is to the right (normal direction)
When D is high, rotation is to the left (reverse direction)

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)

When D is high, the RAM data is low, being LCD ON potential (reverse display)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

11. Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Duty			
											1/33	1/49	1/55	1/65
0	1	0	1	0	1	0	0	0	1	0	1/6 bias	1/8 bias	1/8 bias	1/9 bias
										1	1/5 bias	1/6 bias	1/6 bias	1/7 bias

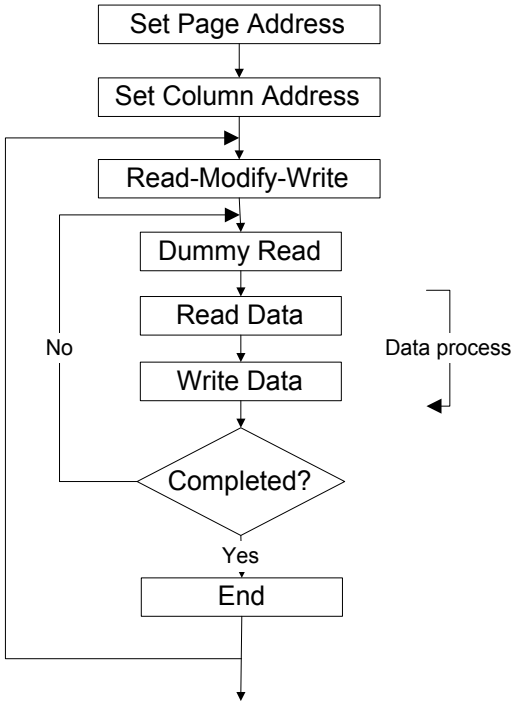
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, the column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until the End command is issued. When the End is issued, the column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed when the cursor is blinking or other events.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

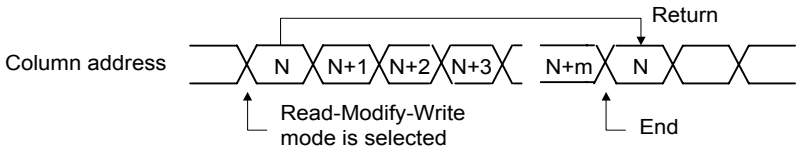
Cursor display sequence



13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued).

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



14. Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize the LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

15. Output Status Select Register
Applicable to the NT7532. When D is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pad
D = 0: Normal (COM0 → COM63/53/47/31)
D = 1: Reverse (COM63/53/47/31 → COM0)
*: Invalid bit

16. Set Power Control
Selects one of eight-power circuit functions using a 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to the Power Supply Circuit section of the FUNCTIONAL DESCRIPTION for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 is low, the voltage follower turns off. When A0 is high, it turns on.
When A1 is low, the voltage regulator turns off. When A1 is high, it turns on.
When A2 i low, the voltage booster turns off. When A2 is high, it turns on.

17. V0 Voltage Regulator Internal Resistor Ratio Set
This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “The Power Supply Circuits”.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb / Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									:		:
								1	1	0	
								1	1	1	Large

18. The Electronic Volume (Double Byte Command)
This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply.
This command is a double byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	V0
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
0	1	0	*	*			:				:
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator registers, and these commands must be executed one after the other. (The static indicator OFF command is a single byte command.)

Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W/ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D = 0: Static Indicator OFF

D = 1: Static Indicator ON

Static Indicator Register Set

These commands set two bits of data into the static indicator register and are used to set the static indicator into a blinking mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately 0.5 second intervals
									1	0	ON (blinking at approximately 1 second intervals
									1	1	ON (constantly on)

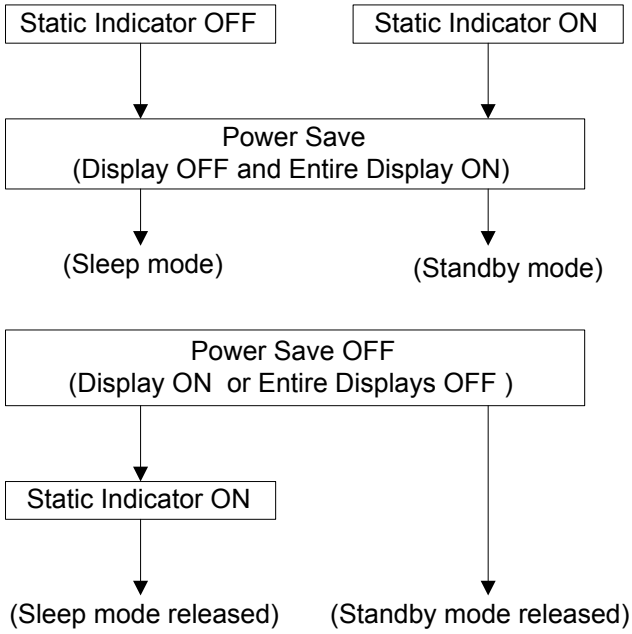
* Disabled bit

20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicators are off, the Power Save command makes the system enter sleep mode. If it is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD drives and outputs the V_{SS} level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access the built-in display RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for the static drive.
The ON operation of the static drive system indicates that the NT7532 is in standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the V_{SS} level as the segment / common driver output. However, the static drive system still operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access the built-in display RAM.

When the RESET command is issued in the standby mode, the sleep mode is set.

- When an external resistive driver gives the LCD driving voltage level, the current of this resistor must be cut so that it may be fixed to floating or V_{SS} level, prior to or concurrently with causing the NT7532 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or V_{SS} level, prior to or concurrently with causing the NT7532 to go into sleep mode or standby mode.

21. NOP

Non-Operation Command

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently set the /RES input to low or issue the Reset command to release the test mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

Cautions: The NT7532 maintains an operation status specified by each command. However, a high level of ambient noise may change the internal operation status. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended.

The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command Table

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display on/off	0	1	0	1	0	1	0	1	1	1	D	Turns on the LCD panel when high, and turns it off when low
(2) Set display start line	0	1	0	0	1	Display start address						Specifies RAM display line for COM0
(3) Set page address	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register
(4-1) Set column address 4 higher bits	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits of column address of display RAM in register
(4-2) Set column address 4 lower bits	0	1	0	0	0	0	0	Lower column address				Sets 4 lower bits of column address of display RAM in register
(5) Read status	0	0	1	Status				0	0	0	0	Reads the status information
(6) Write display data	1	1	0	Write data								Writes data in display RAM
(7) Read display data	1	0	1	Read data								Reads data from display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets the display RAM address SEG output correspondence
(9) Normal/Reverse display	0	1	0	1	0	1	0	0	1	1	D	Normal indication when low, but full indication when high
(10) Entire display on/off	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1)
(11) Set LCD bias	0	1	0	1	0	1	0	0	0	1	D	Sets LCD drive voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions
(15) Common output mode select	0	1	0	1	1	0	0	D	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set power control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb / Ra) mode
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Sets the V0 output voltage electronic volume register
Electronic Volume Register set	0	1	0	*	*	Electronic control value						
(19) Set static indicator On/Off	0	1	0	1	0	1	0	1	1	0	D	Sets static indicator On/Off 0: OFF 1: ON
Set Static indicator register	0	1	0	*	*	*	*	*	*	Mode		Sets the flashing mode

Command Table (Continued)

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(20) Power save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!
(23)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

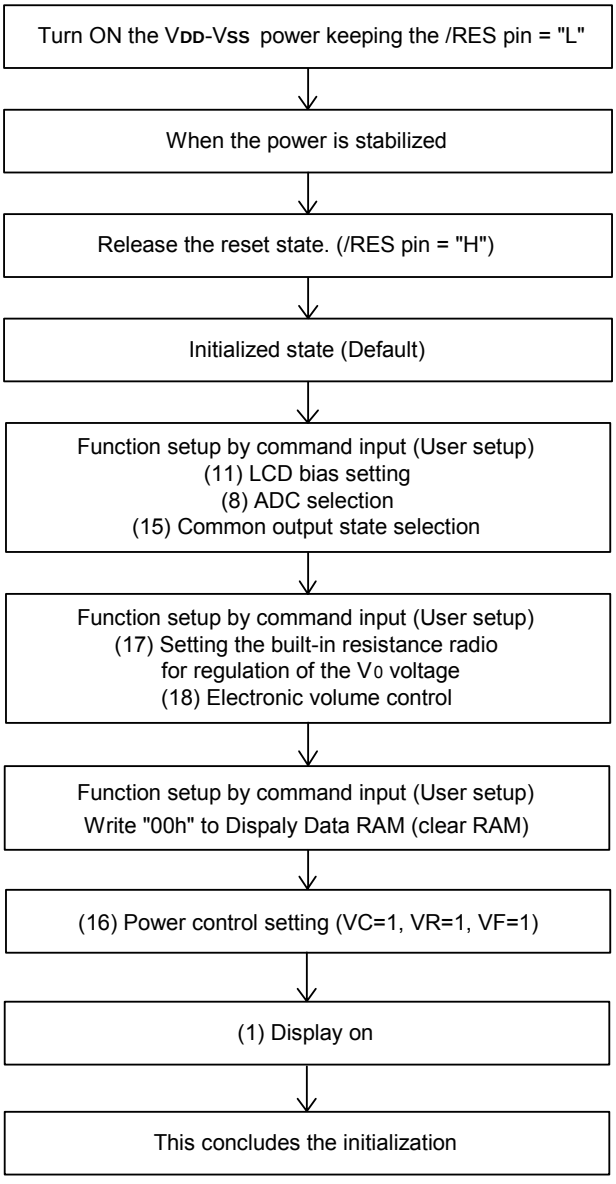
Command Description

Instruction Setup: Reference

1. Initialization

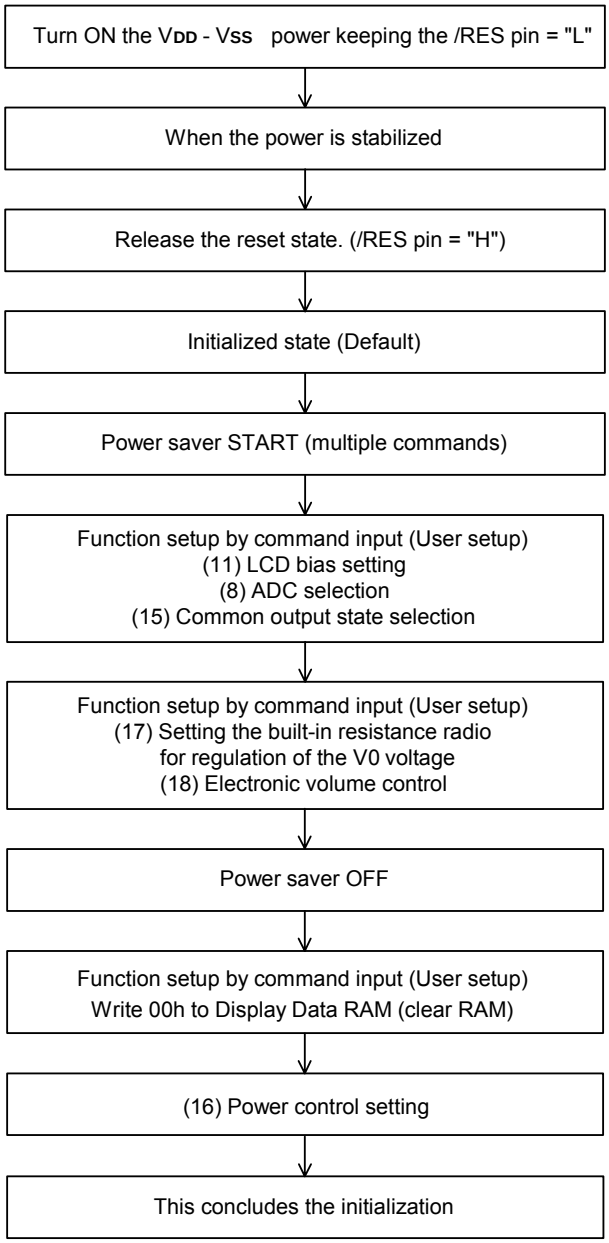
Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the V_{DD} pin, the picture on the display may instantaneously become totally dark when the power is turned on. To avoid such failure, we recommend the following flow sequence when turning on the power.

1.1. When the built-in power is being used immediately after turning on the power:



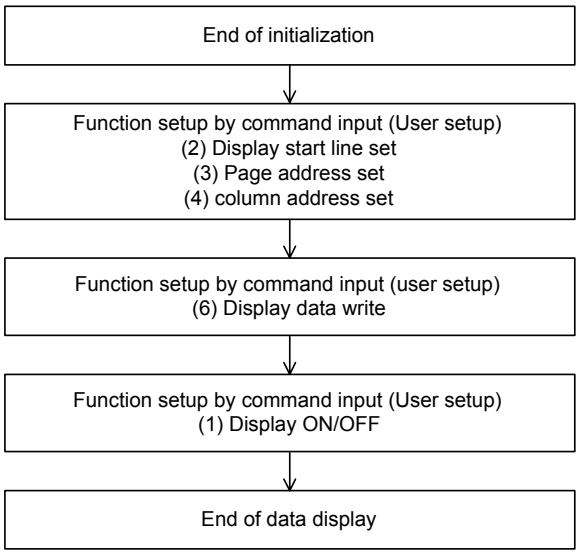
The time of initialization will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

1.2. When the built-in power is not used immediately after turning on the power

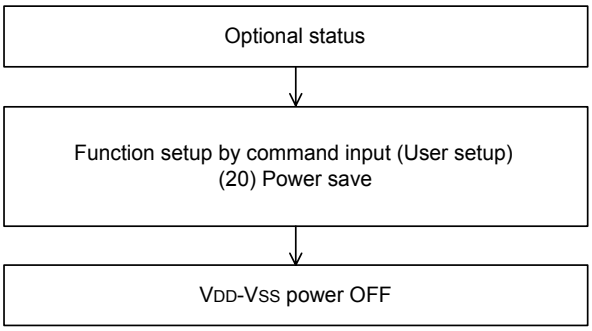


The target time of 5ms will vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you conduct an operation check using the actual equipment.

1. Data Display



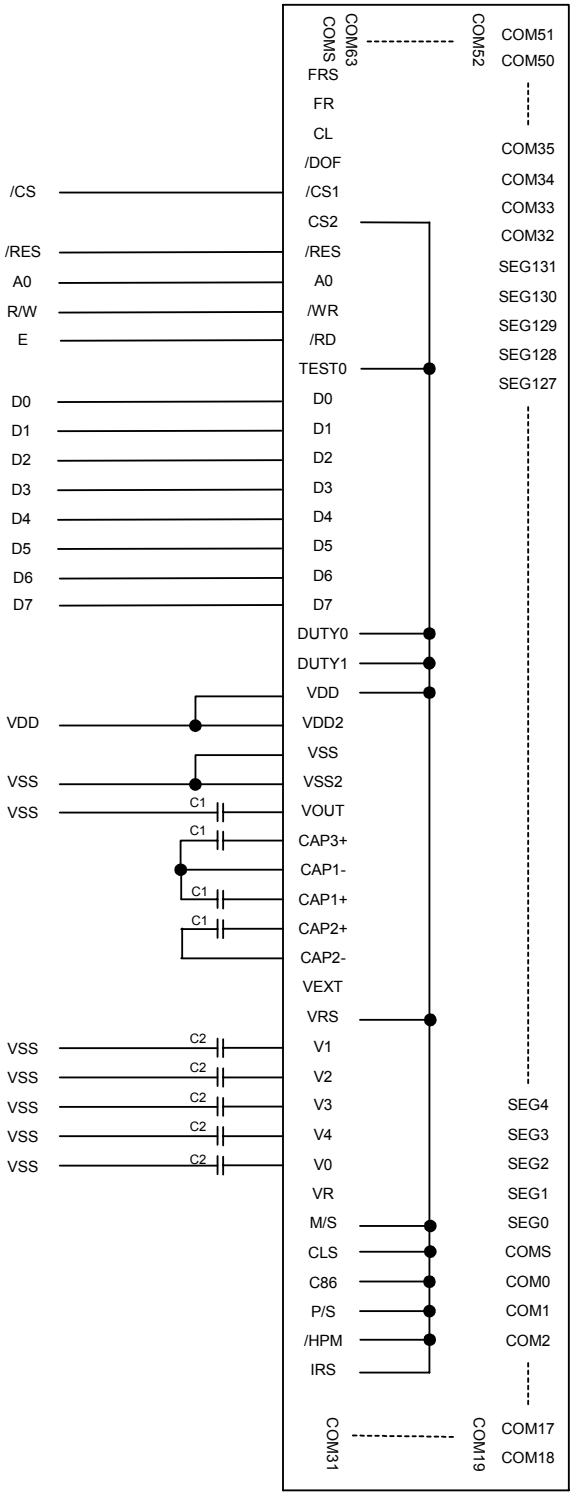
2. Power OFF



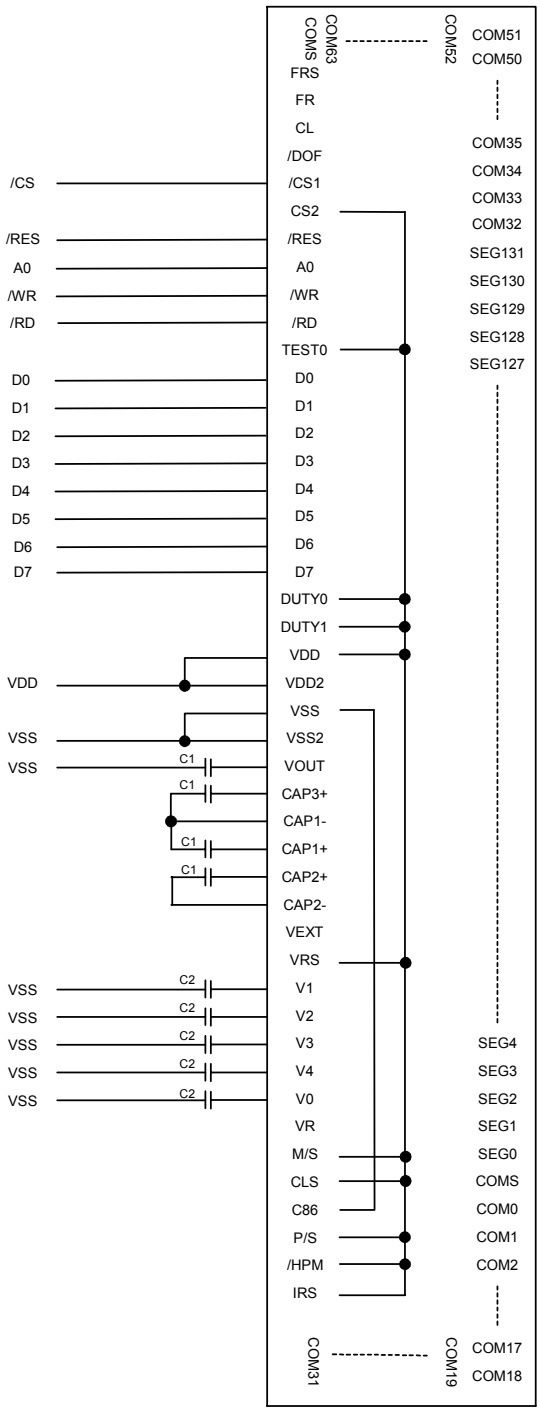
The target time will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you conduct an operation check using the actual equipment.

Reference Connection to MPU

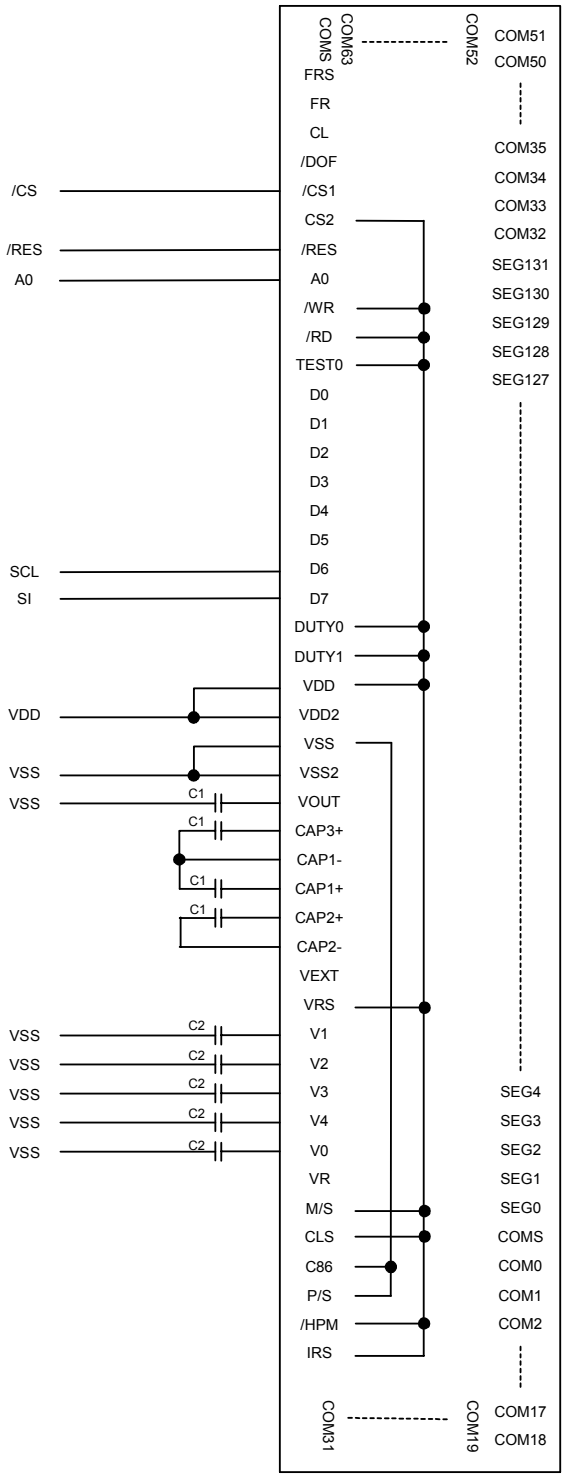
6800 series interface (1/65 duty; internal oscillator, Ra & Rb; normal mode)



8080 series interface (1/65 duty; internal oscillator, Ra & Rb; normal mode)

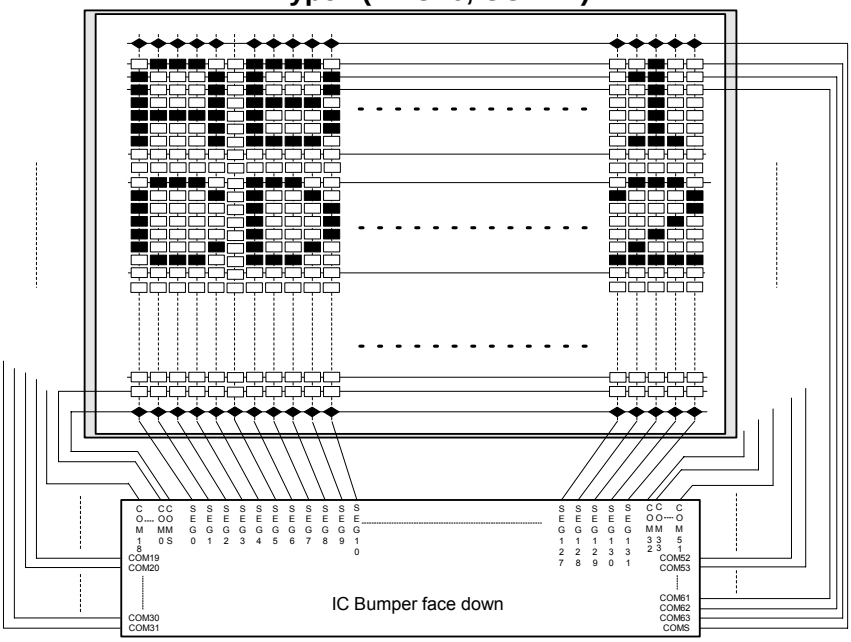


Serial interface (1/65 duty; internal oscillator, Ra & Rb; normal mode)

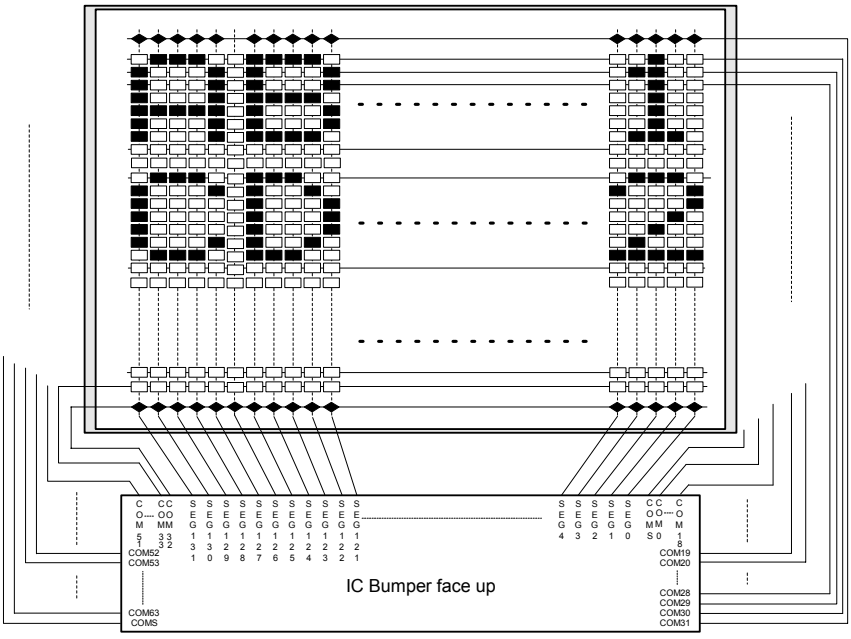


Examples for LCM layout

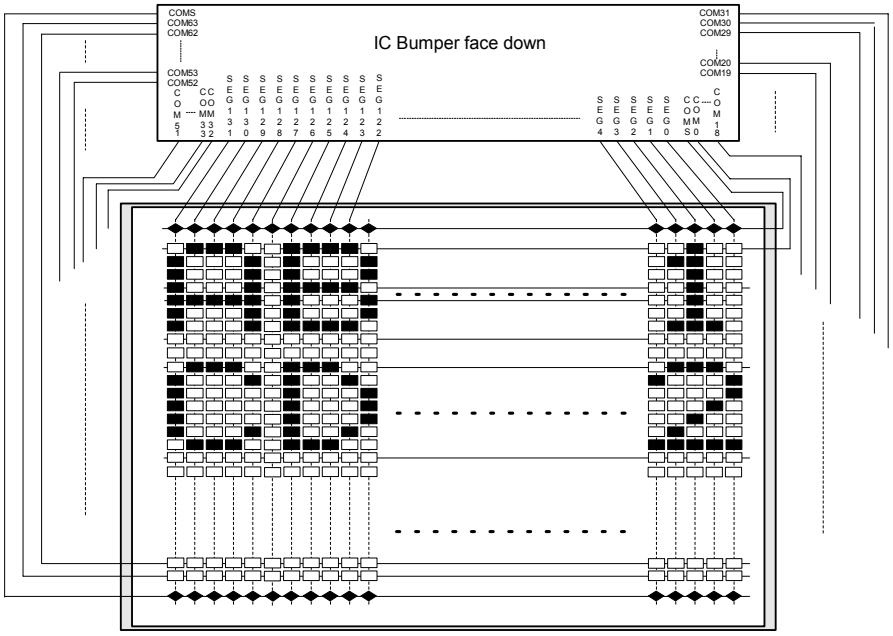
Type I (ADC=0, COM=1)



Type II (ADC=1, COM=1)



Type III (ADC=1, COM=0)



Type IV (ADC=0, COM=0)