NEC

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC2533

AM TUNER FOR ELECTRONIC TUNING CAR RADIOS

The μPC2533 is an IC developed as an AM tuner for car stereos and car radios.

It employs an up-conversion type double super-heterodyne configuration (IF1 = 10.71 MHz, IF2 = 450 kHz).

The internal configuration consists of the MIX1 block (MIX1, OSC1, Buff1), MIX2 block (MIX2, OSC2, Buff2), IF amplifier, detection circuit, AGC circuit, signal meter circuit, SD (station detector) circuit, and Lo/DX (short range/long range) circuit.

Features

- Possible to select stations using only one varactor diode with narrow variable capacitance range
- Tracking adjustment unnecessary
- Coil switching between LW (long wave) and MW (middle wave) unnecessary
- Less sensitivity deviation due to tracking error
- High S/N: 60 dB
- Signal meter output with good linearity
- Signal meter output voltage inclination setting possible by external resistor.
- Can be used with IF (intermediate frequency) counter turning system or high/low tuning system.

Type Number	SD Sensitivity Setting		Signal Meter Voltage Inclination Setting	Remarks
	IF Counter Output	High/Low Output		
μPC2533GS-01	Set by pin No. 7	Set by pin No. 9	Depends on SD sensitivity setting	SD sensitivity of IF counter system and high/low system can be set independently.
μPC2533GS-02	Set by pin No. 7		Set by pin No. 9	Tilt of the signal meter voltage can be set without regard to SD sensitivity.

- Lo/DX function on-chip
- Since IFT (intermediate frequency transformer) turn ratio is free from limitation for matching of ceramic filter impedance, it is easy to design MIX gain with IFT.

The information in this document is subject to change without notice.

Document No. S11989EJ4V0DS00 (4th edition)
Date Published August 1998 N CP(K)
Printed in Japan

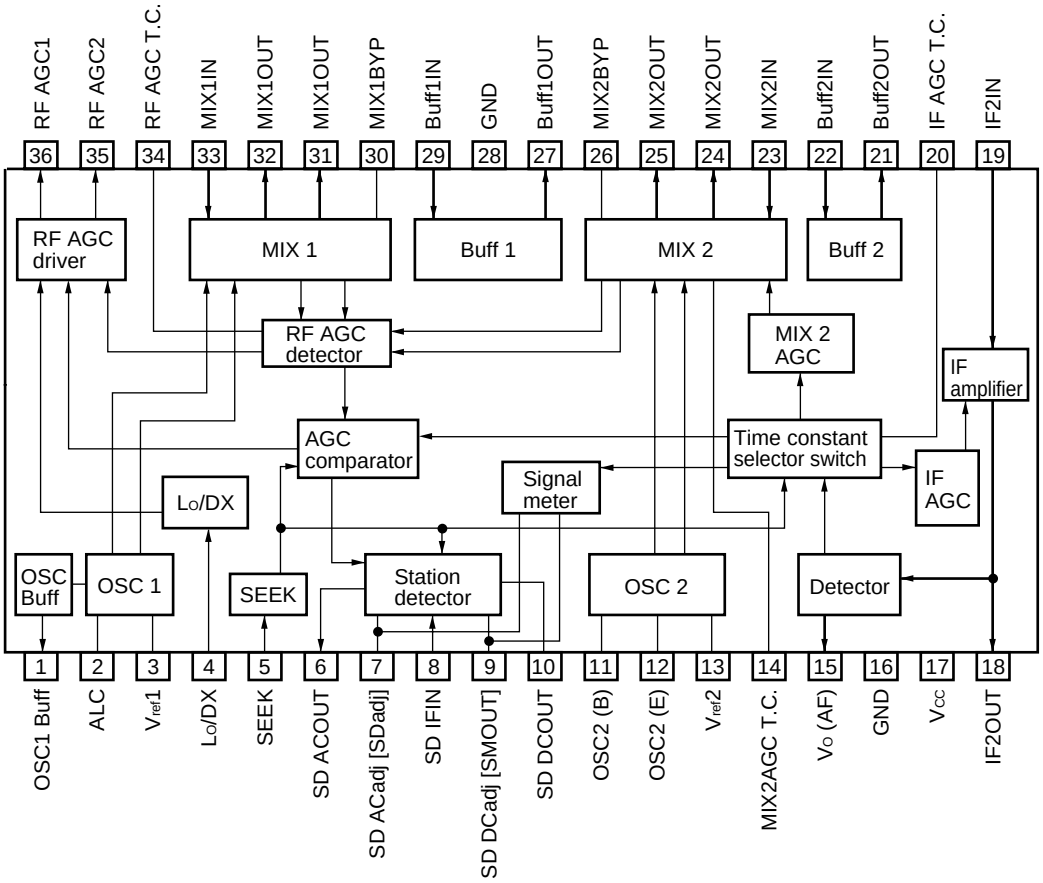
The mark ★ shows major revised points.

© NEC Corporation 1993

Ordering Information

Part Number	Package
μPC2533GS-01	36-pin plastic shrink SOP (300 mil)
μPC2533GS-02	36-pin plastic shrink SOP (300 mil)

Block Diagram



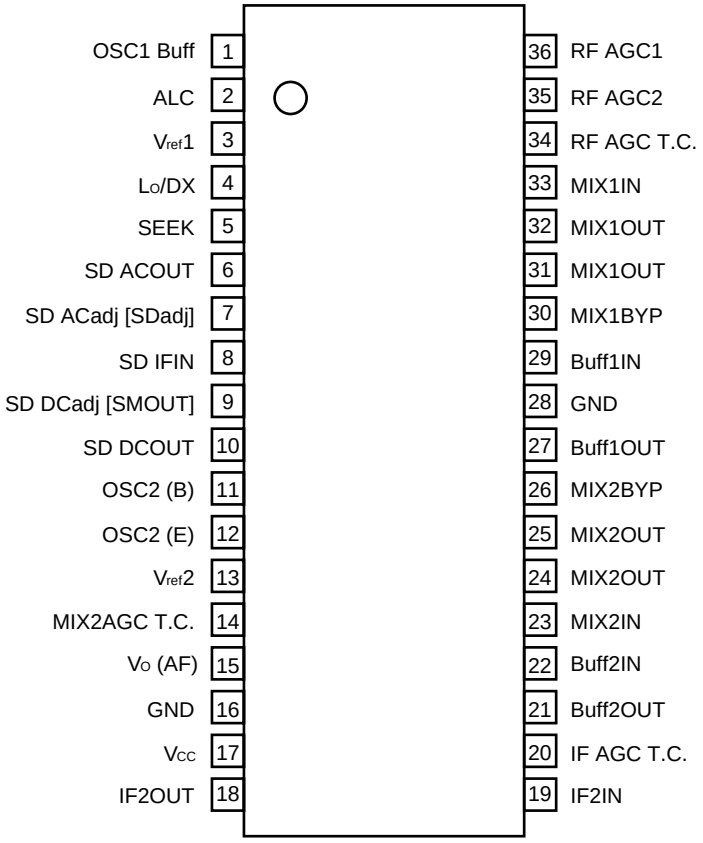
Remarks 1. Bold lines indicate flow of audio signal.

2. μPC2533GS-02 pin names are in parentheses. Pins not in parentheses are used in both the μPC2533GS-01 and μPC2533GS-02.

Pin Configuration (Top View)

36-pin plastic shrink SOP (300 mil)

- **μPC2533GS-01**
- **μPC2533GS-02**

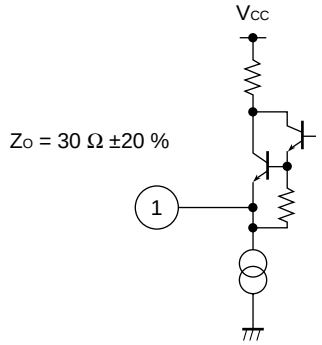
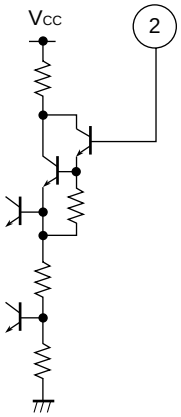
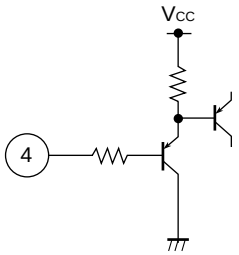
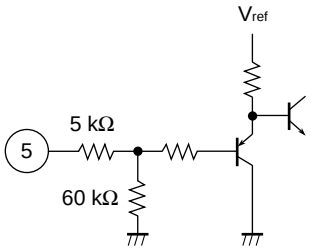


Remark μPC2533GS-02 pin names are in parentheses. Pins not in parentheses are used in both the μPC2533GS-01 and μPC2533GS-02.

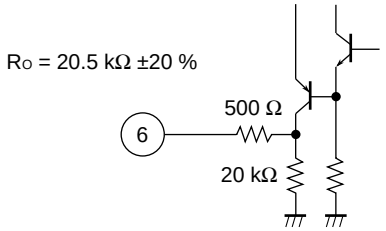
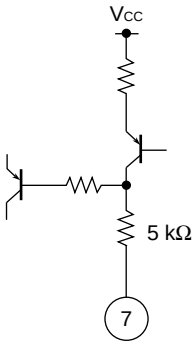
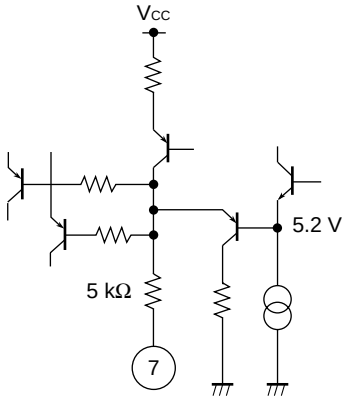
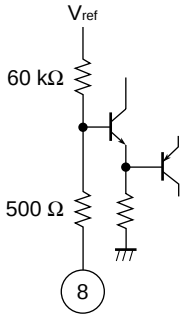
1. Pin Description

Names and symbols in parentheses indicate pin names for μPC2533GS-02. Names and symbols not in parentheses are pin names used in both the μPC2533GS-01 and μPC2533GS-02.

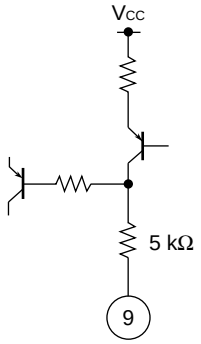
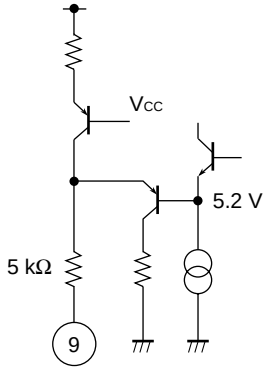
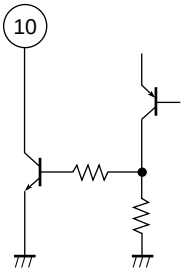
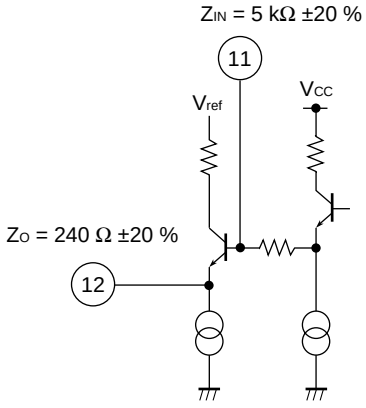
(1/7)

Pin No.	Symbol	Name	Equivalent Circuit
1	OSC1 Buff	OSC1 Buff output	
2	ALC	OSC1 ALC	
3	Vref1	Reference voltage	Reference voltage (5.3 V)
4	LO/DX	LO/DX control	
5	SEEK	Seek request	

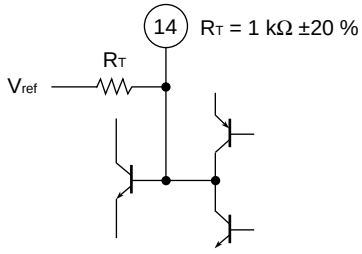
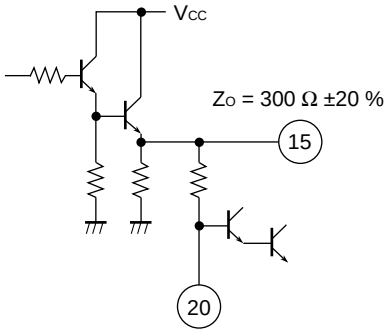
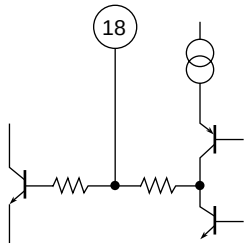
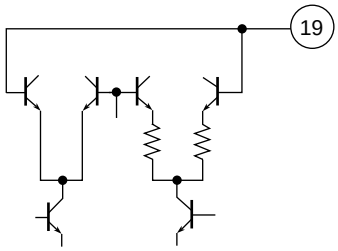
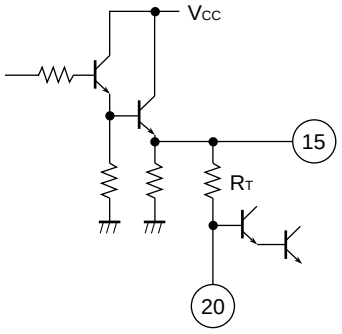
(2/7)

Pin No.	Symbol	Name	Equivalent Circuit
6	SD ACOUT	SD AC output	
7	SD ACadj	SD AC sensitivity setting (and signal meter ouput)	(μPC2533GS-01) 
	[SDadj]	[SD AC sensitivity and SD DC sensitivity setting]	(μPC2533GS-02) 
8	SD IFIN	SD IF input	

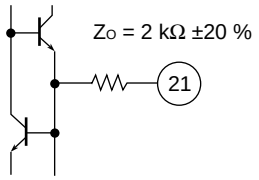
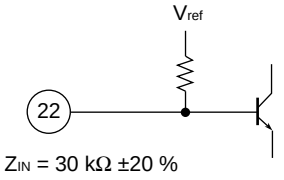
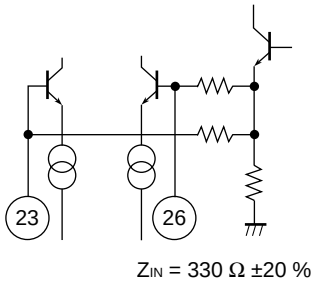
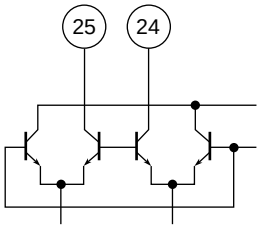
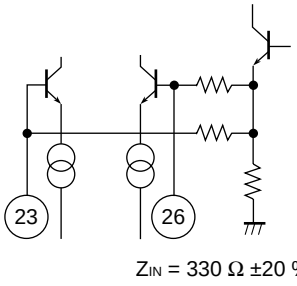
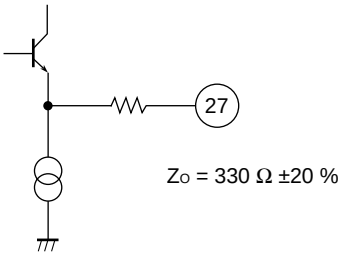
(3/7)

Pin No.	Symbol	Name	Equivalent Circuit
9	SD DCadj	SD DC sensitivity setting (and signal meter output)	(μPC2533GS-01) 
	[SMOUT]	[Signal meter output]	(μPC2533GS-02) 
10	SD DCOUT	SD DC output (Active high)	
11 12	OSC2 (B) OSC2 (E)	OSC2 (base) OSC2 (emitter)	
13	Vref2	Reference voltage	Reference voltage (6.0 V)

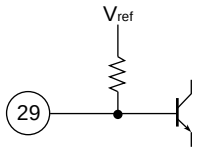
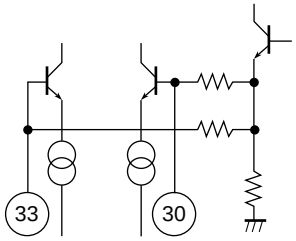
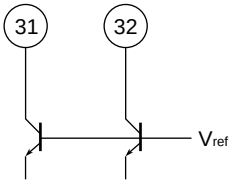
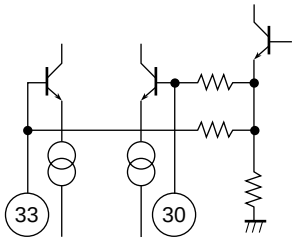
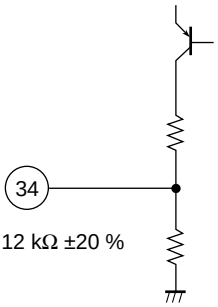
(4/7)

Pin No.	Symbol	Name	Equivalent Circuit
14	MIX2AGC T.C.	MIX2 AGC smoothing	
15	V_O(AF)	Audio output	
16	GND	Ground	GND (low frequency)
17	V_{CC}	Power supply voltage	V_{CC}
18	IF2OUT	IF amplifier output	
19	IF2IN	IF amplifier input	
20	IF AGC T.C.	IF AGC input	

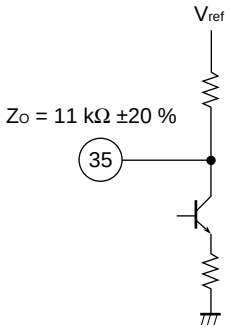
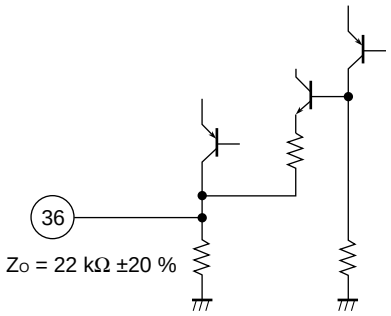
(5/7)

Pin No.	Symbol	Name	Equivalent Circuit
21	Buff2OUT	2nd IF burffer output	
22	Buff2IN	2nd IF buffer input	
23	MIX2IN	MIX2 input	
24 25	MIX2OUT MIX2OUT	MIX2 output MIX2 output	
26	MIX2BYP	MIX2 bypass	
27	Buff1OUT	1st IF buffer output	

(6/7)

Pin No.	Symbol	Name	Equivalent Circuit
28	GND	Ground	GND (high frequency)
29	Buff1IN	1st IF buffer input	 Z_{IN} = 15 kΩ ±20 %
30	MIX1BYP	MIX1 bypass	 Z_{IN} = 1.2 kΩ ±20 %
31 32	MIX1OUT MIX1OUT	MIX1 output MIX1 output	
33	MIX1IN	MIX1 input	 Z_{IN} = 1.2 kΩ ±20 %
34	RF AGC T.C.	RF AGC smoothing	 Z_O = 12 kΩ ±20 %

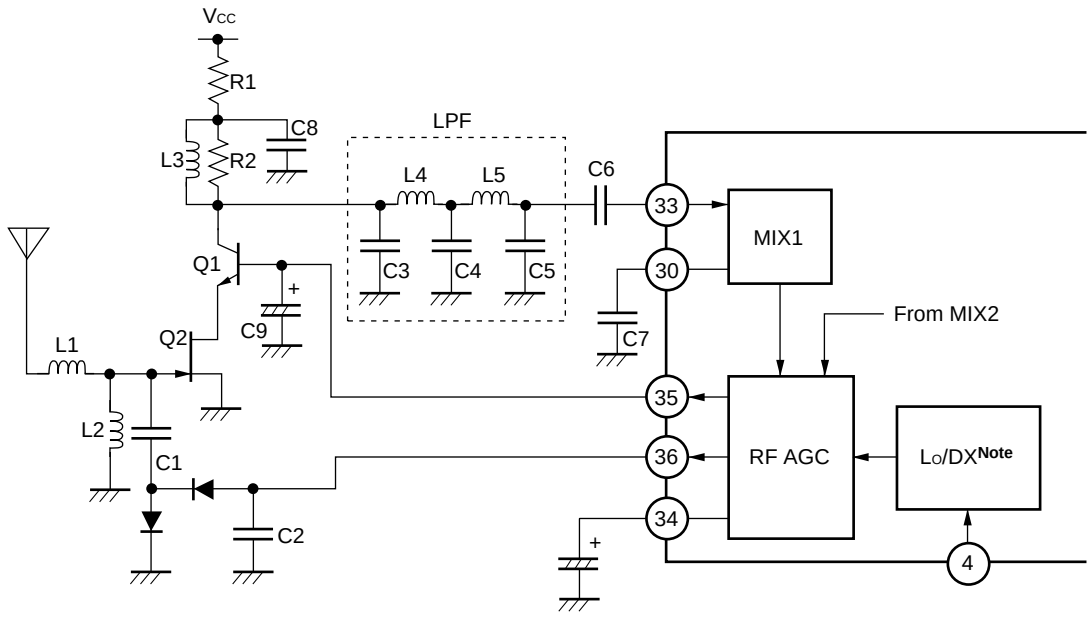
(7/7)

Pin No.	Symbol	Name	Equivalent Circuit
35	RF AGC2	RF AGC output (cascade base)	
36	RF AGC1	RF AGC output (PIN diode)	

2. Operation of Each Block

2.1 FR Amplifier Circuit Block

Fig. 2-1 RF Ampliier Circuit



Note LO : 3 V or higher
DX : 1 V or lower

In the AM band, the capacitance of a car radio antenna depends on its length, diameter, cable length, etc. Therefore, J-FET is used in the μPC2533 to raise RF input impedance.

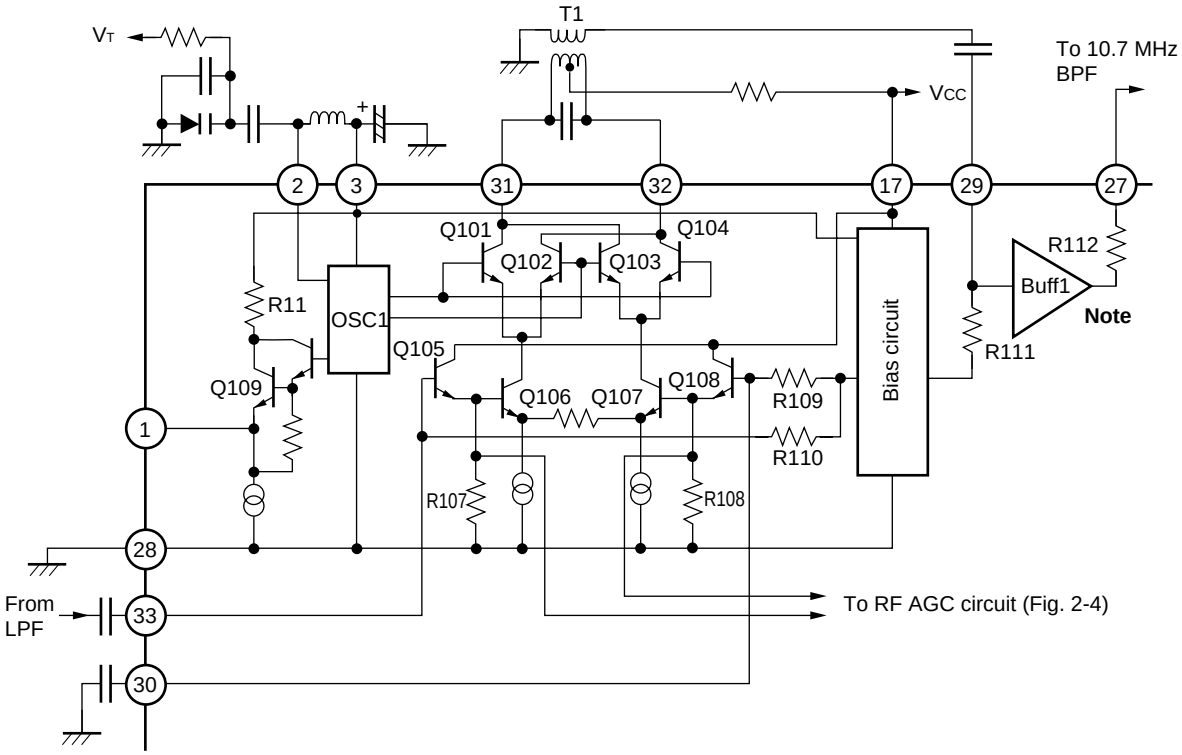
Since the μPC2533 raises the first IF (intermediate frequency) to 10.71 MHz, there is no need for a tuning circuit between the RF amplifier circuit and MIX1. Instead, it employs an LPF (about 6 MHz) consisting of L4, L5 and C3 to C5 between the RF amplifier circuit and MIX1 in order to cut image frequency (21.4 MHz or higher). Because this allows a wide-band RF amplifier circuit to be configured without using a tuning circuit, frequency sensitivity deviation can be minimized to a high degree.

The AGC circuit consists of RF AGC1 by the PIN diode connected to the FET gate and RF AGC2 by the cascade transistor Q1. Use a low-noise transistor even with low current for the cascade transistor Q1 (if a high-noise one is used, the S/N ratio deteriorates).

Remark Set bias voltage for cascade transistor Q1 to $V_C > V_B$.

2.2 MIX1 Block

Fig. 2-2 MIX1 Block



Note Output impedance and input impedance of Buff1 are 330 Ω and 15 kΩ, respectively.

MIX1 (Q101 to Q108) is a DBM (double balanced mixer).

MIX1 output is supplied to 10.7 MHz ceramic filter via Buff1 (output impedance: 330 Ω) for impedance matching.

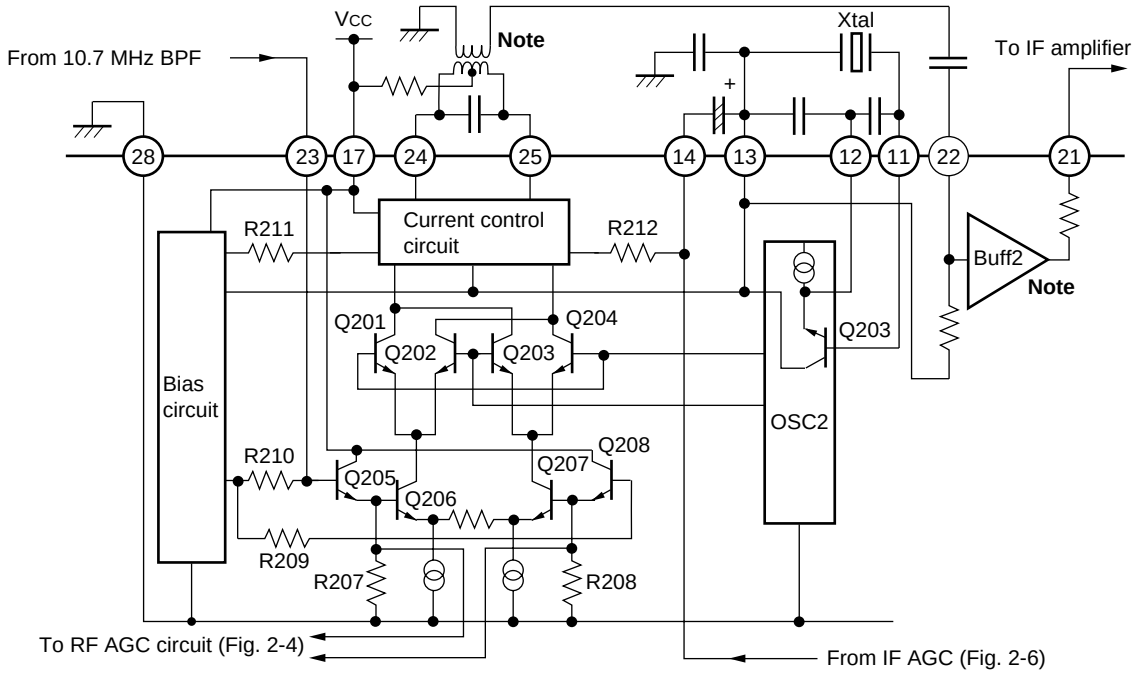
The local oscillation signal is applied to the bases of Q101 to Q104, and the RF signal to the base of Q105. MIX1 (Q101 to 108) multiplies the local oscillation signal by RF signal, and converts to the resonance frequency of IFT T1 for output.

The local oscillation signal is output from pin 1 via Q109 (OSC Buff). It has an amplitude of 110 dBμV and can be directly input to CMOS LSI for use by the PLL synthesizer.

The RF signal applied to the base of Q105 is also input to the detector of the RF AGC circuit.

2.3 MIX2 Block

Fig. 2-3 MIX2 Block



Note Output impedance and input impedance of Buff2 are 2 kΩ and 30 kΩ, respectively.

MIX2 (Q201 to Q208) is a DBM with a configuration similar to that of MIX1.

The major difference from the MIX1 is that MIX2 is equipped with a current control circuit for output and is controlled by the AGC.

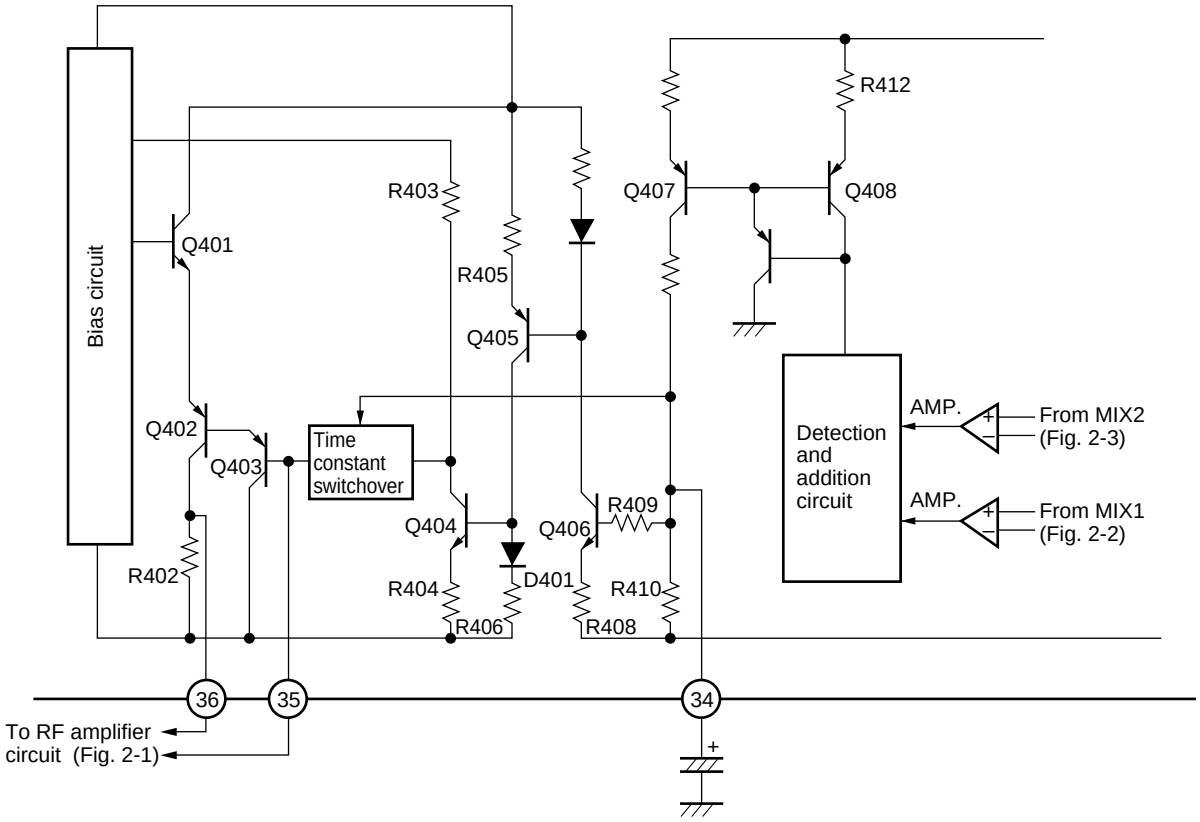
Input impedance of MIX2 is 330 Ω to match the 10.7 MHz ceramic filter. Output impedance of Buff2 is 2 kΩ to match the 450 kHz ceramic filter.

IF signal input from pin 23 is also input to the detector of the RF AGC. The RF AGC is detected by both MIX1 and MIX2 blocks.

The Buff1 and Buff2 ensure impedance matching between MIX1 and MIX2 outputs and each ceramic filter. As a result, IFT design is not restricted by the need to match ceramic filter impedance. For turn ratio, etc., only conversion gain need be taken input account, so it is easy to design.

2.4 RF AGC Block

Fig. 2-4 RF AGC Block



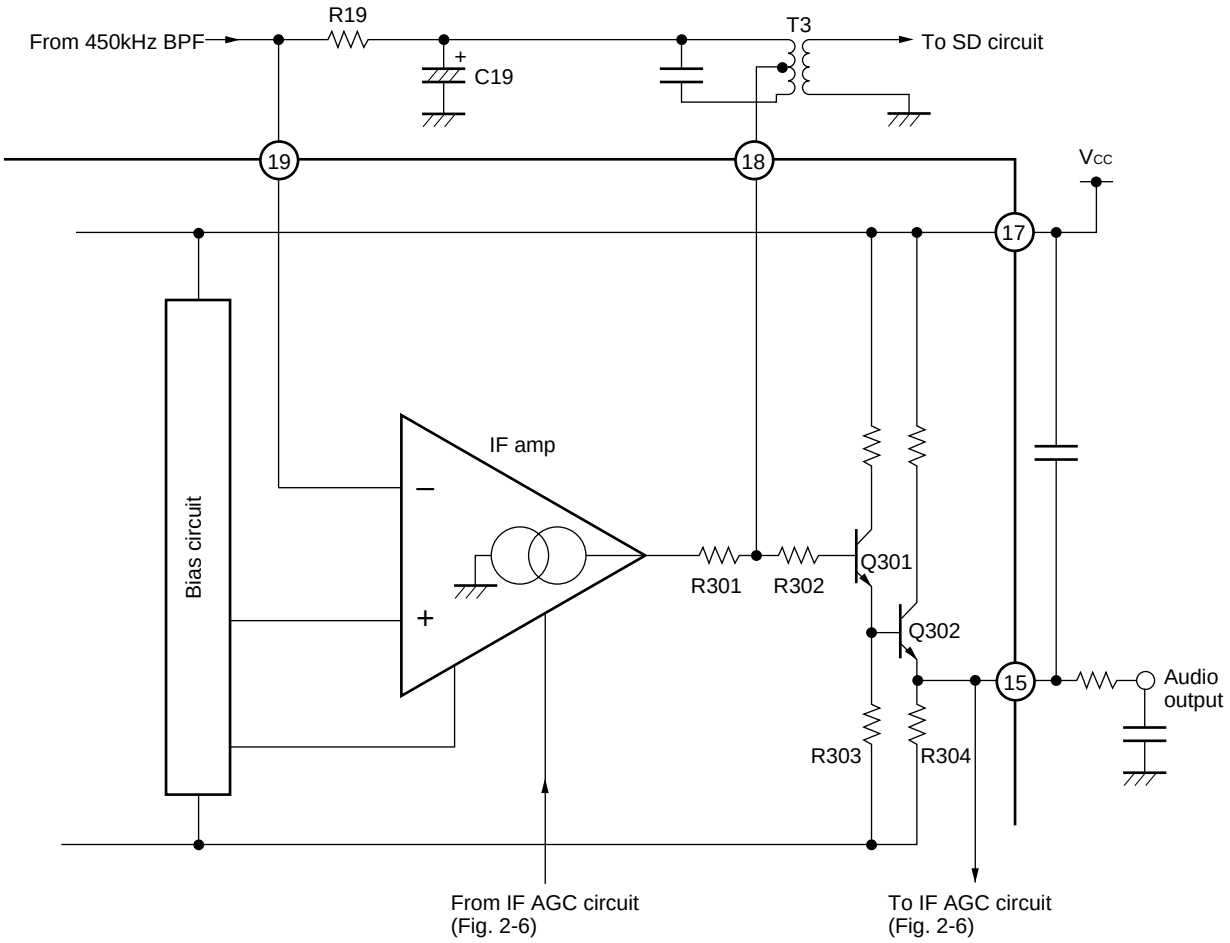
The configuration of the RF AGC is shown in Fig. 2-4. After being detected by the RF AGC detector and added, the input signal from MIX1 and MIX2 is smoothed by external capacitor of pin 34, and its DC voltage controls the RF AGC.

RF AGC output controls the PIN diode from pin 36 and controls base voltage of cascade transistor which determines FET V_{DS} from pin 35. In addition, by detecting sudden fluctuation of pin 34 voltage and switching over time constants, RF AGC response convergence when the electric field suddenly changes is improved.

Operation start time of the RF AGC can be delayed slightly by connecting a resistor parallel to the external capacitor of pin 34.

2.5 IF Amplifier Block and Detection Block

Fig. 2-5 IF Amplifier and Detection Block



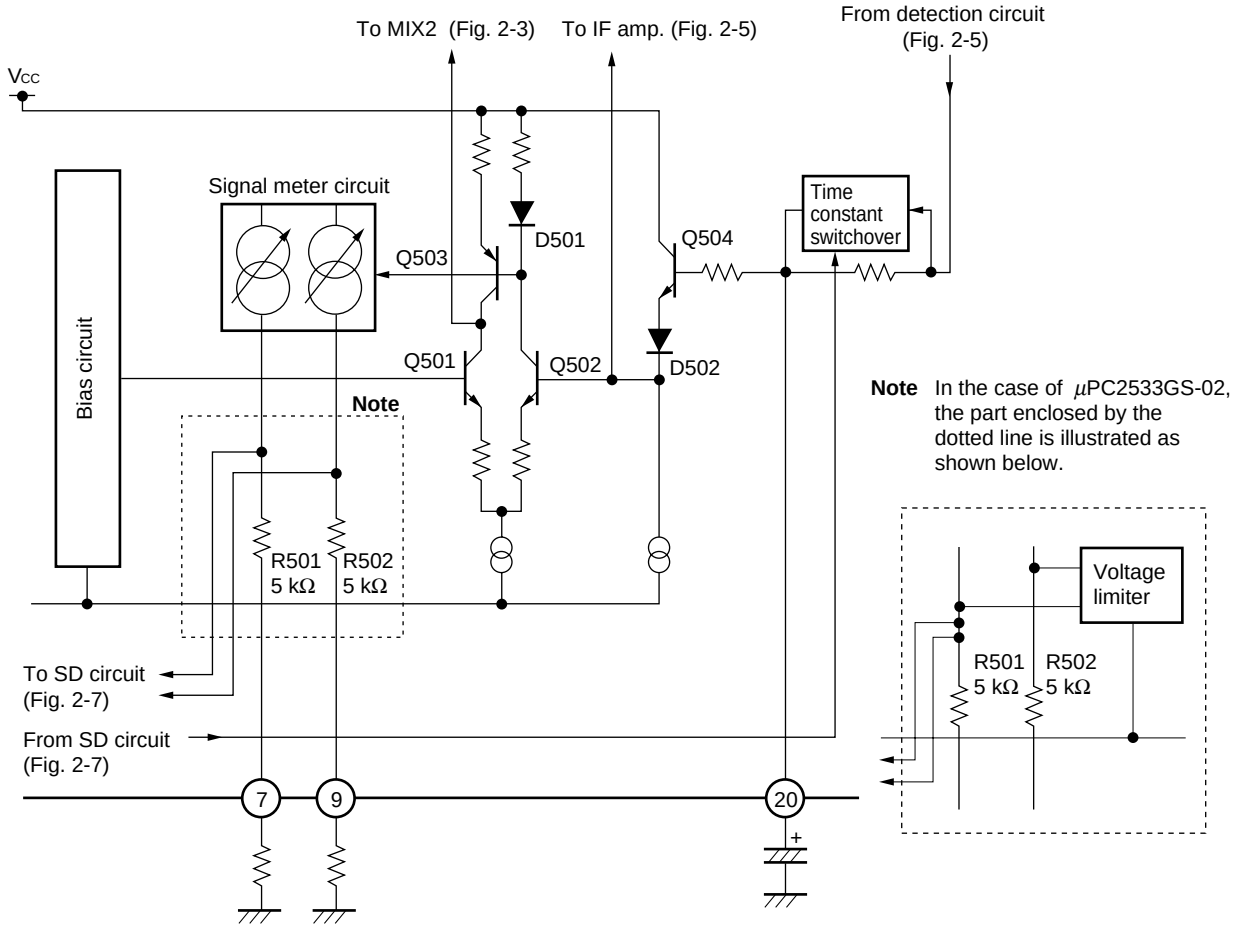
In the IF amplifier block, DC feedback is carried to pin 19 via an external low pass filter (composed of T_3 and C_{19}) from pin 18, an output pin. The DC electric potential of pin 18 is designed to be fixed approximately equal to the (+) side input of the IF amplifier. The value of R19 is the input impedance, so impedance matching to 450 kHz ceramic filter is possible.

The output signal current of the IF amplifier is converted to signal voltage by being resonated by T3 and input to the detection circuit after frequency selection.

Emitter follower detection by Q302 is adopted for the detection circuit block.

2.6 IF AGC Block

Fig. 2-6 IF AGC Block (for μPC2533GS-01)



IF AGC block configuration is shown in Fig. 2-6. The signal detected from pin 15 is smoothed by the capacitor of pin 20, and its DC voltage controls the IF AGC.

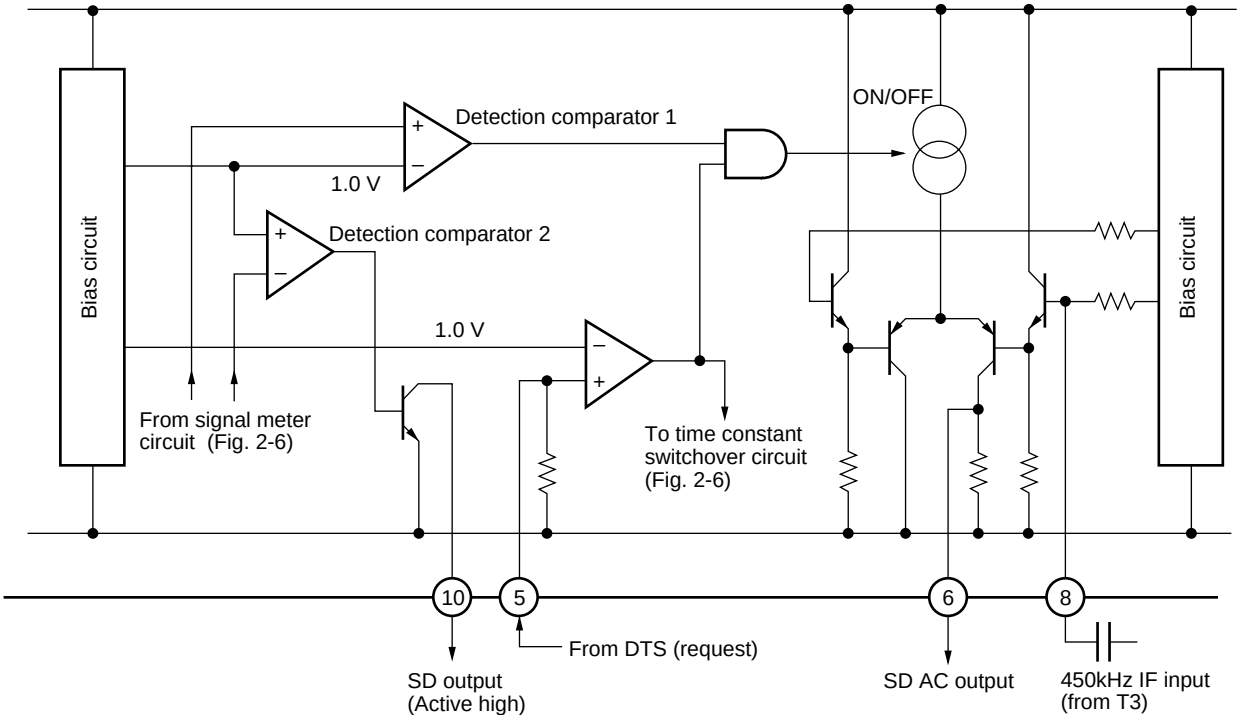
The IF AGC controls the IF amplifier and MIX2. In the operation sequence, it first controls the gain of the IF amplifier, then controls the gain of MIX2.

The signal meter circuit output (current output) is in proportion to the DC voltage smoothed by pin 20, and converted to voltage by the external resistor of pin 7 or 9. Therefore, output voltage value and gain can be set by the value of the external resistor. **Note**

Note For relation between the external resistor and the signal meter, refer to **Signal meter output voltage (adjustment by resistor between pin 9 and GND)** in section **4. Characteristic Curves**.

2.7 Station Detector Circuit Block

Fig. 2-7 Station Detector Circuit Block



The configration station detector (SD) circuit block is shown in Fig. 2-7.

The SD circuit stops scanning or seeking when a broadcast wave is received when auto scanning or seek tuning. Since the μPC2533 has two outputs (DC high/low signal (open collector) and AC IF signal (f = 450 kHz)), it can be used according to DTS (digital tuning system) type. Input the SD request signal from DTS to pin 5.

The SD sensitivity setting methods of the μPC2533GS-01 and μPC2533GS-02 differ.

With the μPC2533GS-01, SD sensitivities in the IF counter output system and in the high/low output system are set by external resistor between pin 7 and GND and by external resistor between pin 9 and GND.

With the μPC2533GS-02, SD sensitivities in both the IF counter output system and high/low output system are set by external resistor between pin 7 and GND (refer to Fig. 2-6).

Table 2-1 SD Sensitivity Setting Examples

Value of Resistor between Pin 9 or Pin 7 and GND	SD Sensitivity (AC, DC)
51 kΩ	27 dBμV
24 kΩ	29 dBμV
10 kΩ	33 dBμV

The reference voltage of the μPC2533-01 and μPC2533-02 detection comparator has been internally fixed at 1.0 V.

Under the influence of R501 (5 kΩ) and R502 (5 kΩ) of the siganl meter circuit (Fig. 2-6), signal meter output voltage and detection comparator input voltage do not perfectly coincide. For SD sensitivity setting, refer to the following formula.

Detection comparator input voltage =

$$\text{Signal meter output voltage} \times \left(1 + \frac{\text{R501}}{\text{Value of resistor between pin 7 and GND}}\right)$$

Remark Because DC output is open-collector type (Active high), connect pull-up resistor to pin 10 to use.

3. Electical Characteristics

Absolute Maximum Ratings (T_A = 25 °C)

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	10	V
Power dissipation	P_D	600	mW
Operating ambient temperature	T_A	–40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions (T_A = 25 °C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{CC}		7.5	8.0	8.5	V
Input voltage	V_{IN}				132	dBμV

Electrical Characteristics

(Unless specified, T_A = 25 °C, V_{CC} = 8 V, f_{IN} = 999 kHz, f_{MOD} = 400 Hz, AM_{MOD} = 30 %, R_{SD1} (resistor between pin 7 and GND) = R_{SD2} (resistor between pin 9 and GND) = 24 kΩ, 15-pin measurement load = 100 kΩ)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit current	I_{CC}	No input (excluding FET)	–	45	55	mA
Detection output	V_O	V_{IN} = 74 dBμV	150	180	210	mVrms
Signal-to-noise ratio	S/N	V_{IN} = 74 dBμV	53	60	–	dB
Total harmonic distortion 1	THD1	V_{IN} = 74 dBμV	–	0.3	1.0	%
Total harmonic distortion 2	THD2	V_{IN} = 74 dBμV, AM_{MOD} = 80 %	–	0.7	1.0	%
Total harmonic distortion 3	THD3	V_{IN} = 130 dBμV, AM_{MOD} = 80 %	–	0.7	1.5	%
Signal meter output voltage 1	V_{S1}	No input	–	0	0.2	V
Signal meter output voltage 2	V_{S2}	V_{IN} = 30 dBμV	0.5	1.5	2.5	V
Signal meter output voltage 3 **Note**	V_{S3}	V_{IN} = 74 dBμV	4.8 (4.3)	5.5 (5.0)	6.7 (5.5)	V
Local buffer output 1	V_{OSC}	1-pin load: 20 pF or less	106	110	114	dBμV

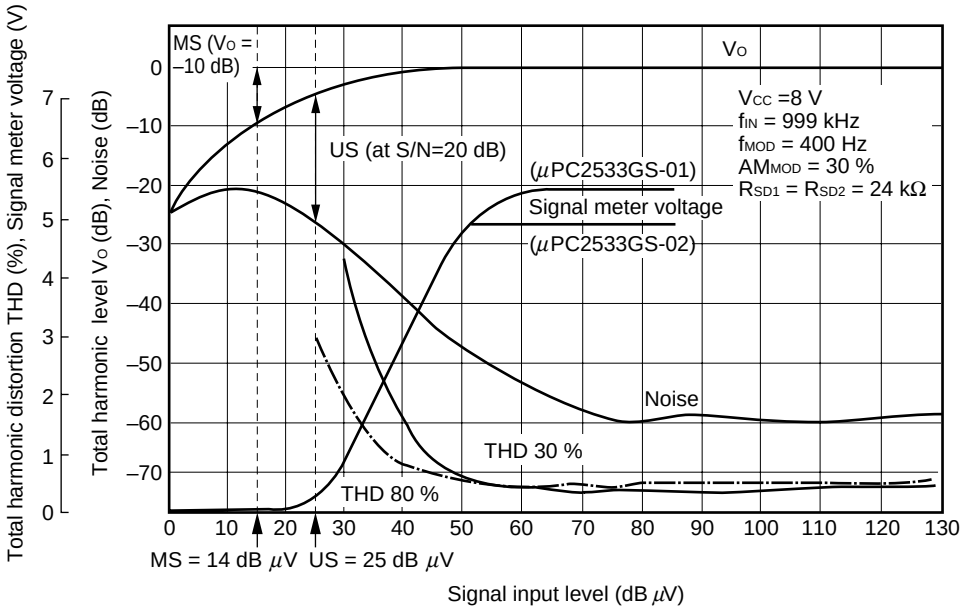
Note Specifications in parentheses for signal meter output voltage 3 are for μPC2533GS-02. Values of other items are the same for μPC2533GS-01 and μPC2533GS-02.

Reference Characteristics

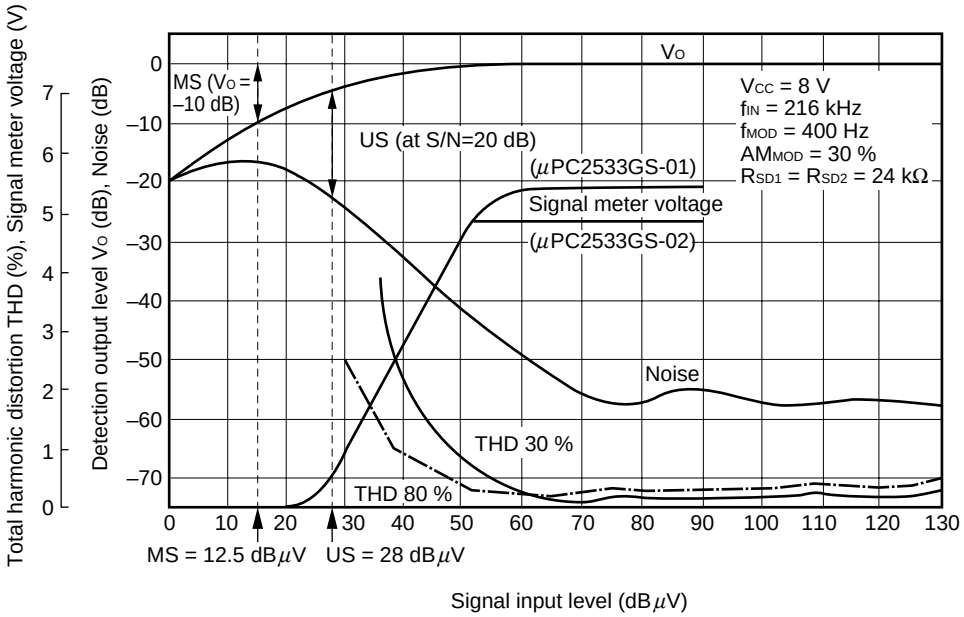
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum sensitivity	MS	V_{IN} making V_O –10 dB, where V_O = 0 dB at V_{IN} = 74 dBμV	–	13	–	dBμV
S/D sensitivity (AC)	SS(AC)	V_{IN} making SEEK, SD AC OUT level 101 dBμV or more	–	29	–	dBμV
S/D sensitivity (DC)	SS(DC)	V_{IN} making SEEK, SD AC OUT voltage 4.8 V or more	–	29	–	dBμV
S/D output time	T-SD	Delay time from the time when changing SEEK V_{IN} = 0 → 40 dBμV to the time when pin 10 voltage becomes 4.8 V or more	0	5	25	ms
Vo stabilization time	T-V_O	V_{IN} = 60 → 100 dBμV, V_O = ±3 dB	60	160	260	ms
Tweet	TW	V_{IN} = 74 dBμV, 2IF	–	60	–	dB
2nd local buffer negative impedance	Z_{OSC}2	Maximum value of a series resistor with which the crystal can oscillate	400	–	–	Ω
Usable sensitivity	US	V_{IN} making S/N = 20 dB	–	25	–	dBμV

4. Characteristic Curves

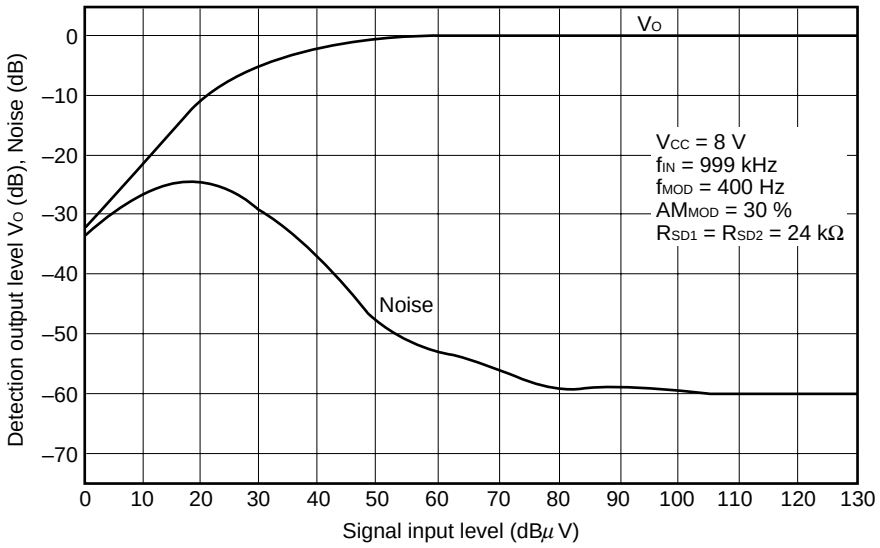
Input/Output Characteristics (1)



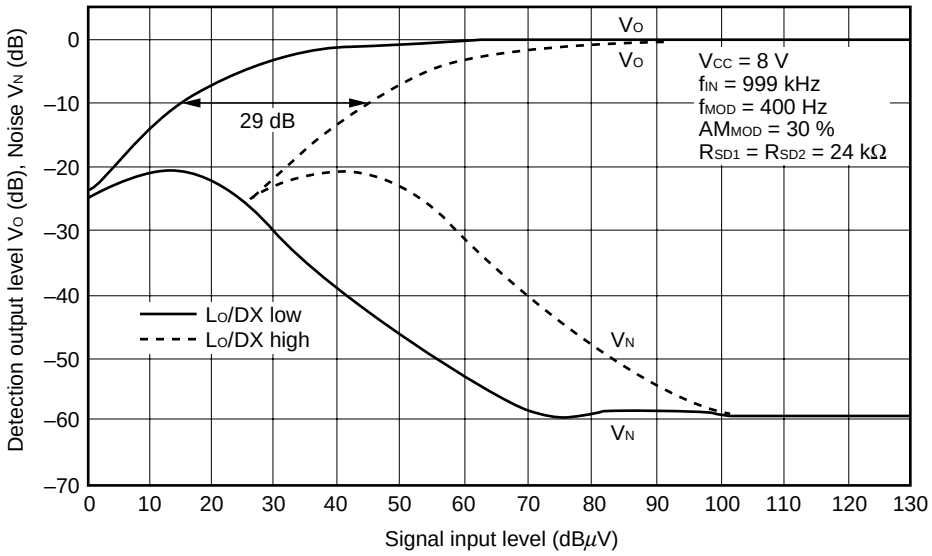
Input/Output Characteristics (2)



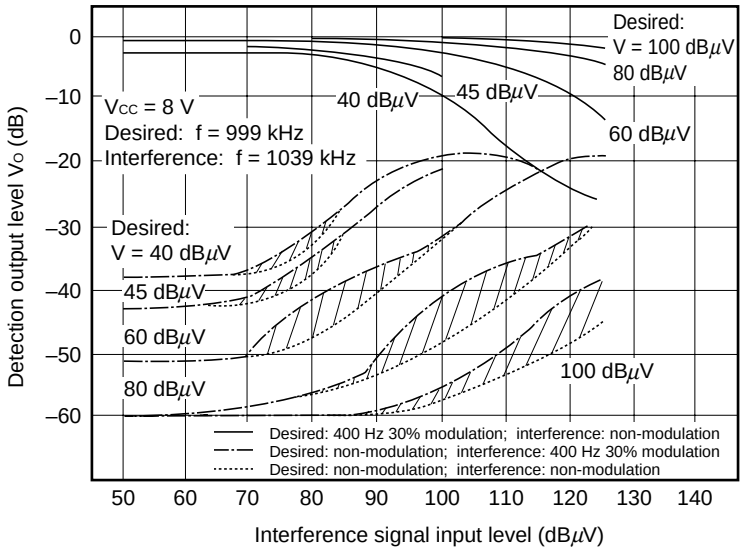
Input/Output Characteristics (3) (FET Load: 255 Ω) (Reference Only)



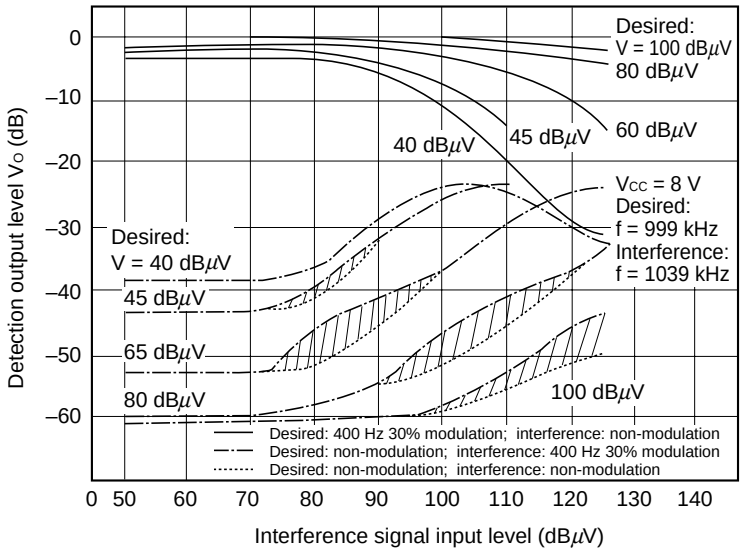
Input/Output Characteristics (4)



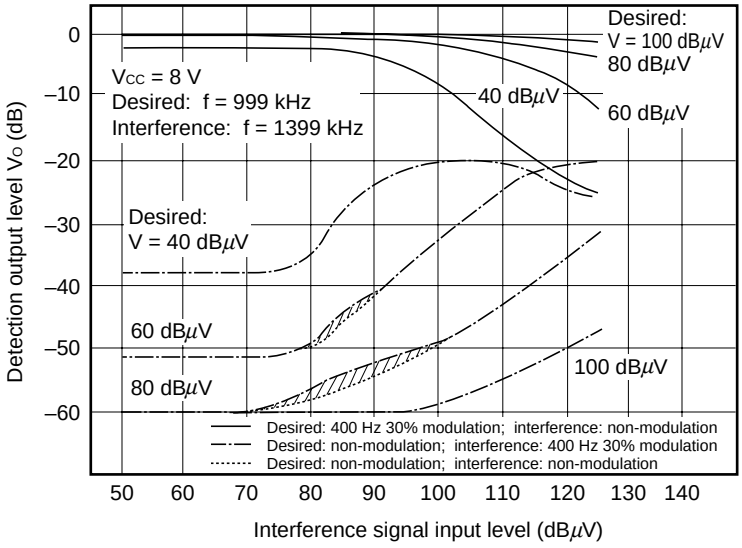
Cross-Modulation Characteristics (40 kHz Detuning)



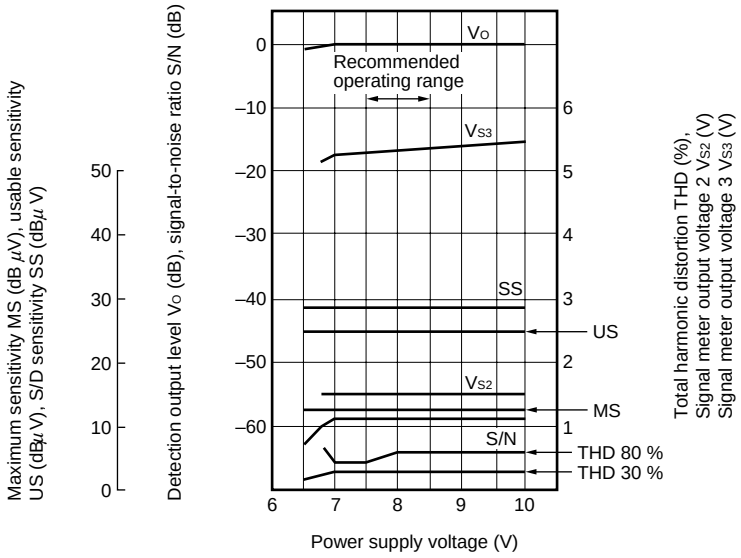
Cross-Modulation Characteristics (40 kHz Detuning, FET Load 255 Ω) (Reference Only)



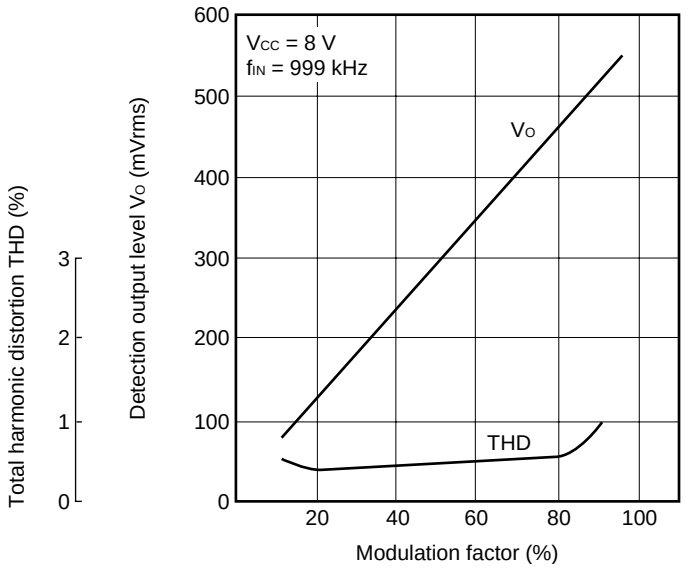
Cross-Modulation Characteristics (400 kHz Detuning)



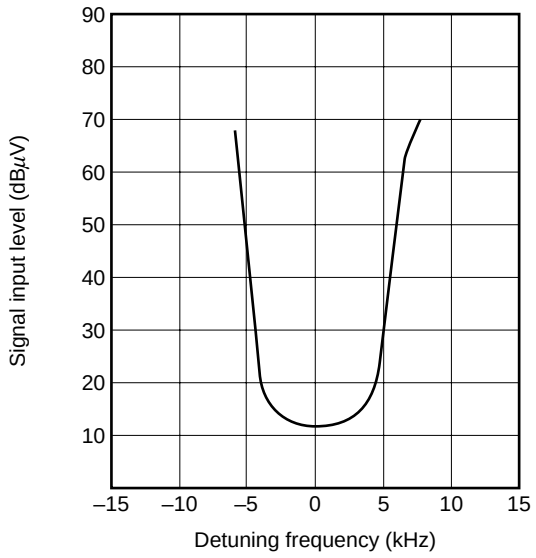
Power Supply Voltage Characteristics



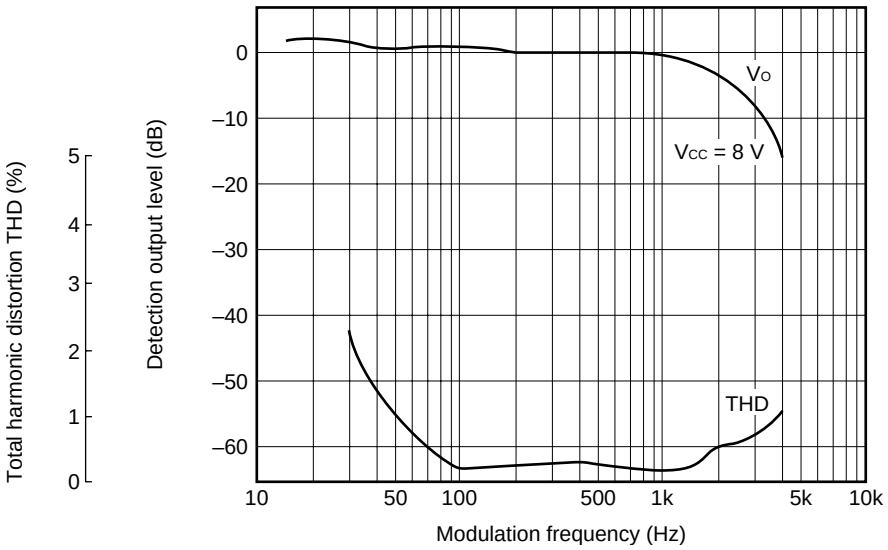
Modulation Factor Characteristics



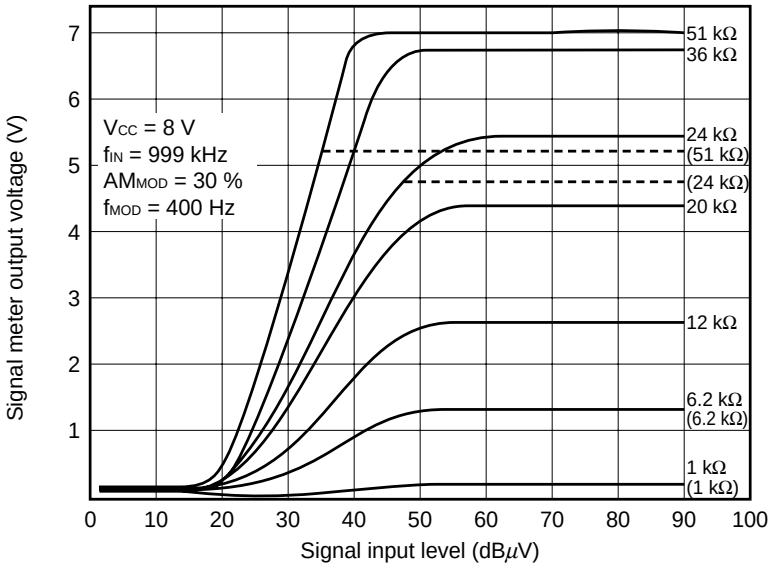
Detuning Frequency Characteristics (Maximum Sensitivity), Signal Selectivity Characteristics



Modulation Frequency Characteristics

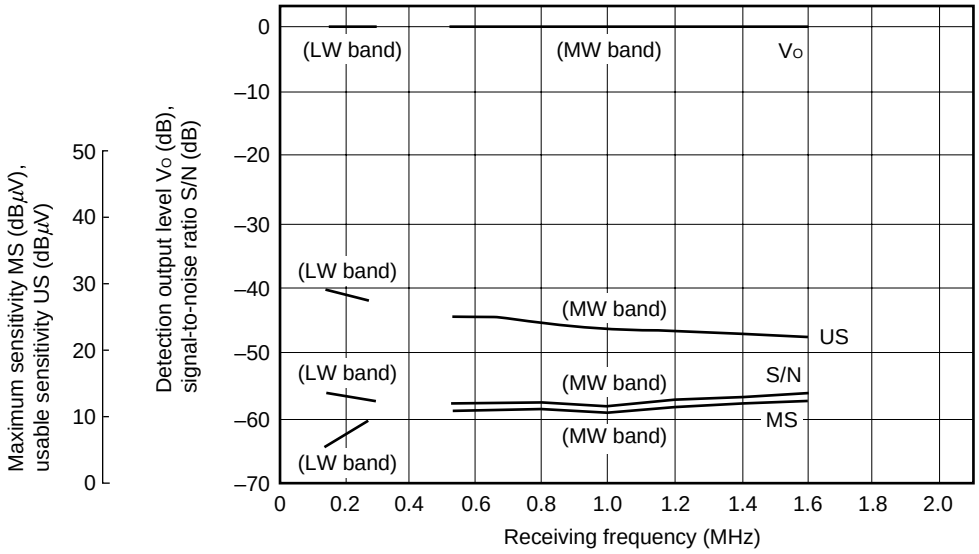


Signal Meter Output Voltage (Adjustment by Resistor between Pin 9 and GND)

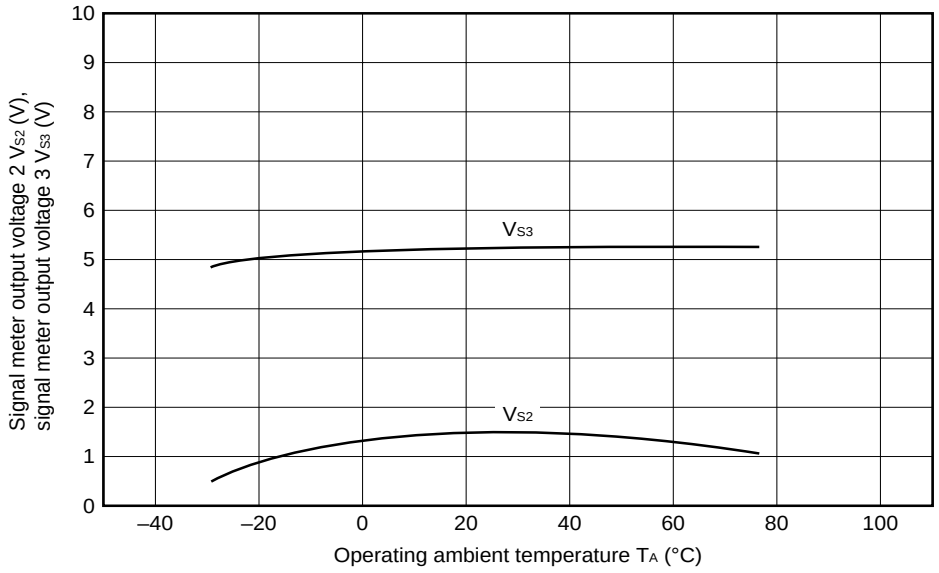


Remark Figures in parentheses indicate setting value (resistor between pin 9 and GND) for μPC2533GS-02. A circuit that restricts output current from pin 9 is mounted on μPC2533GS-02.

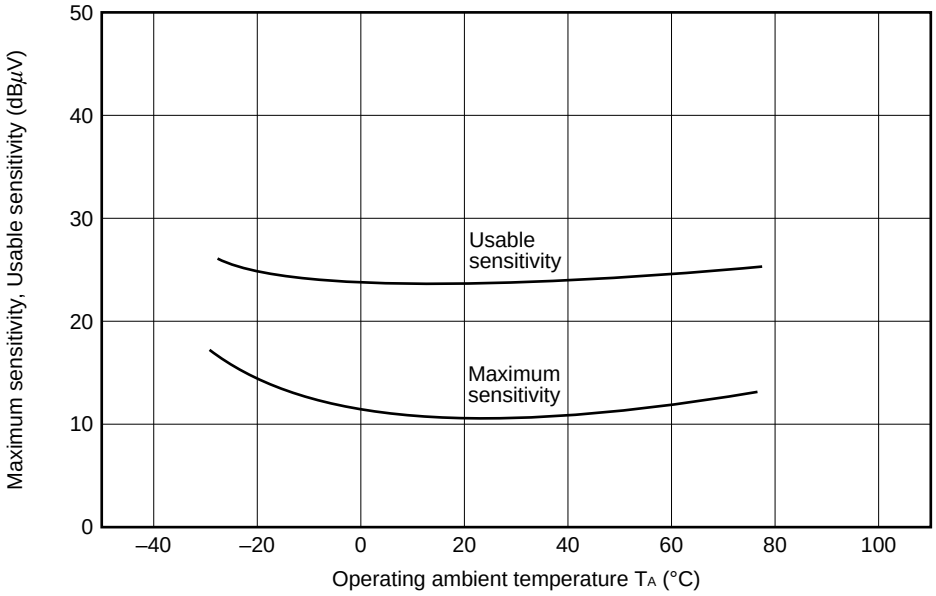
Receiving Frequency Characteristics



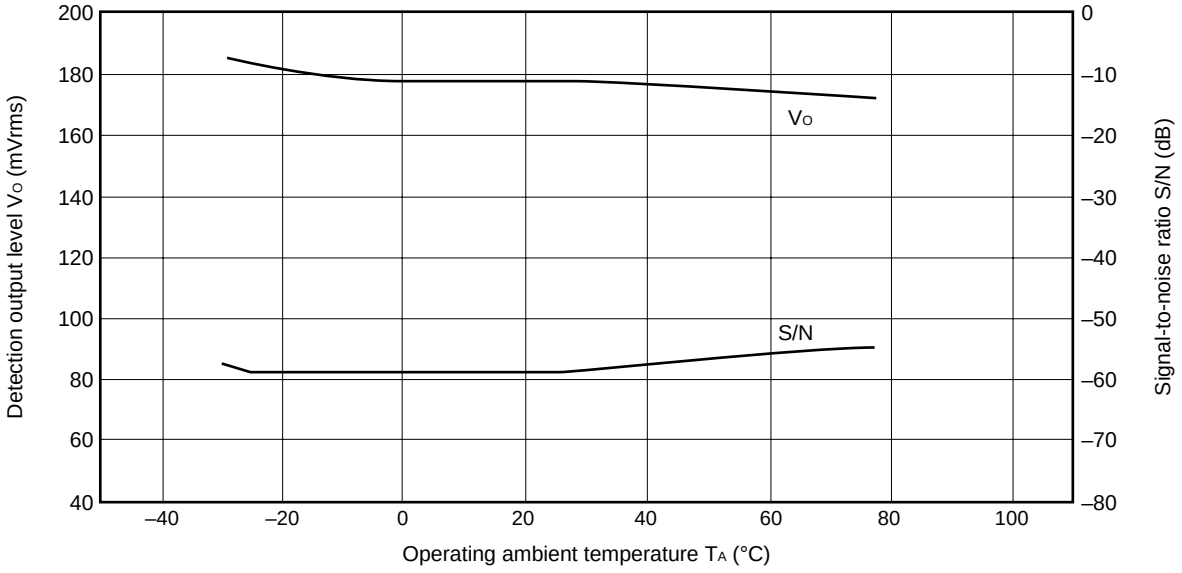
Temperature Characteristics (Signal Meter Voltage vs. Operating Ambient Temperature)



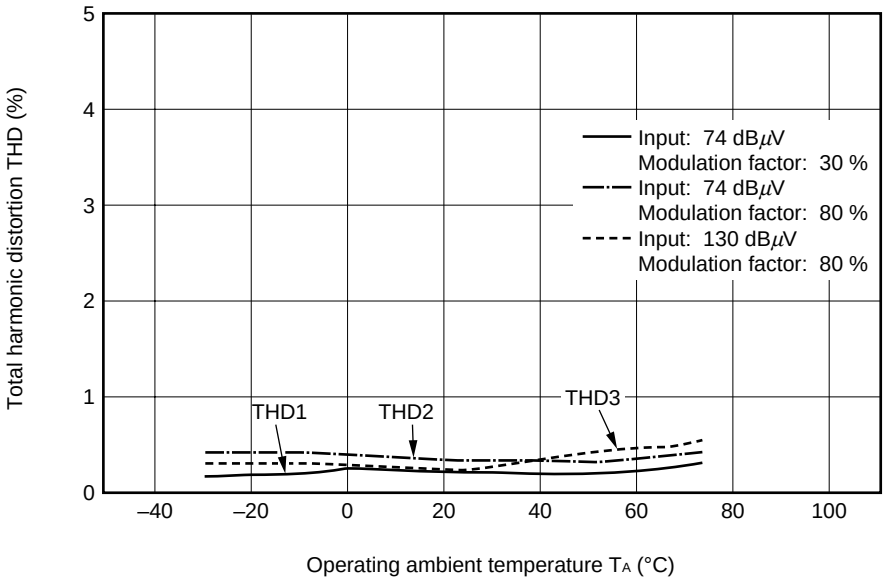
Temperature Characteristics (Maximum Sensitivity, Usable sensitivity vs. Operating Ambient Temperature)



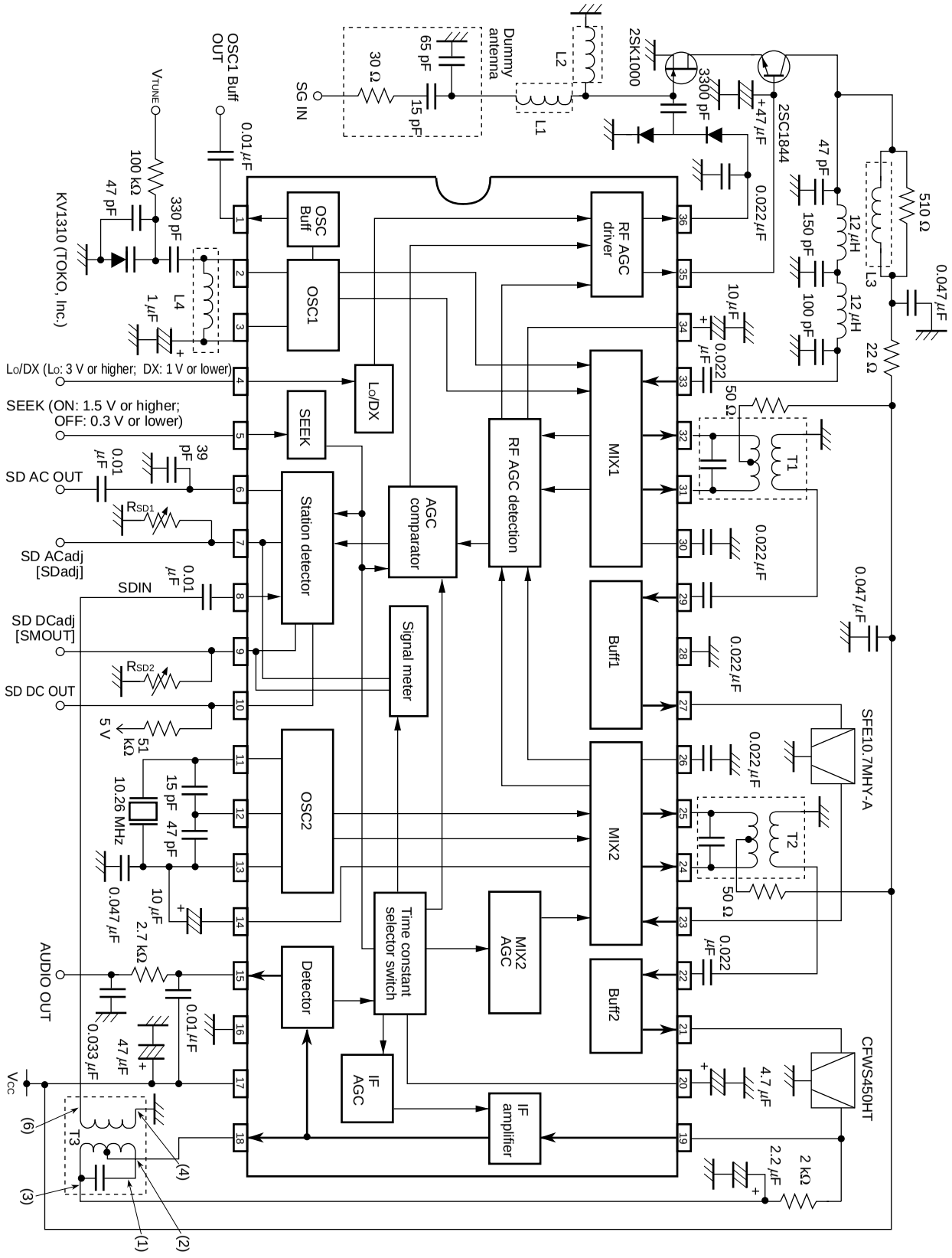
Temperature Characteristics (Detection Output Level, Signal-to-Noise Ratio vs. Operating Ambient Temperatue)



Temperature Characteristics (THD vs. Operating Ambient Temperatue)

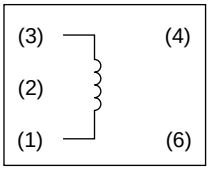
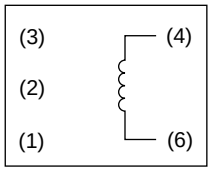
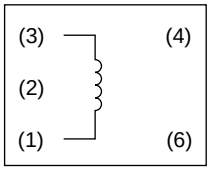
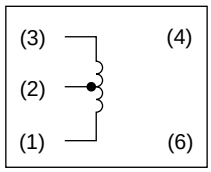
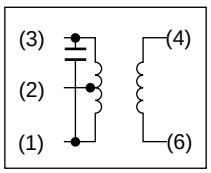
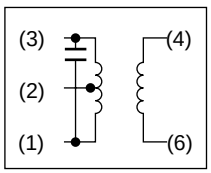
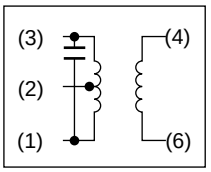


★ 5. Measurement Circuit



Remark Pin names in parentheses are those of μPC2533GS-02.

Coil Specifications (TOKO, Inc.)

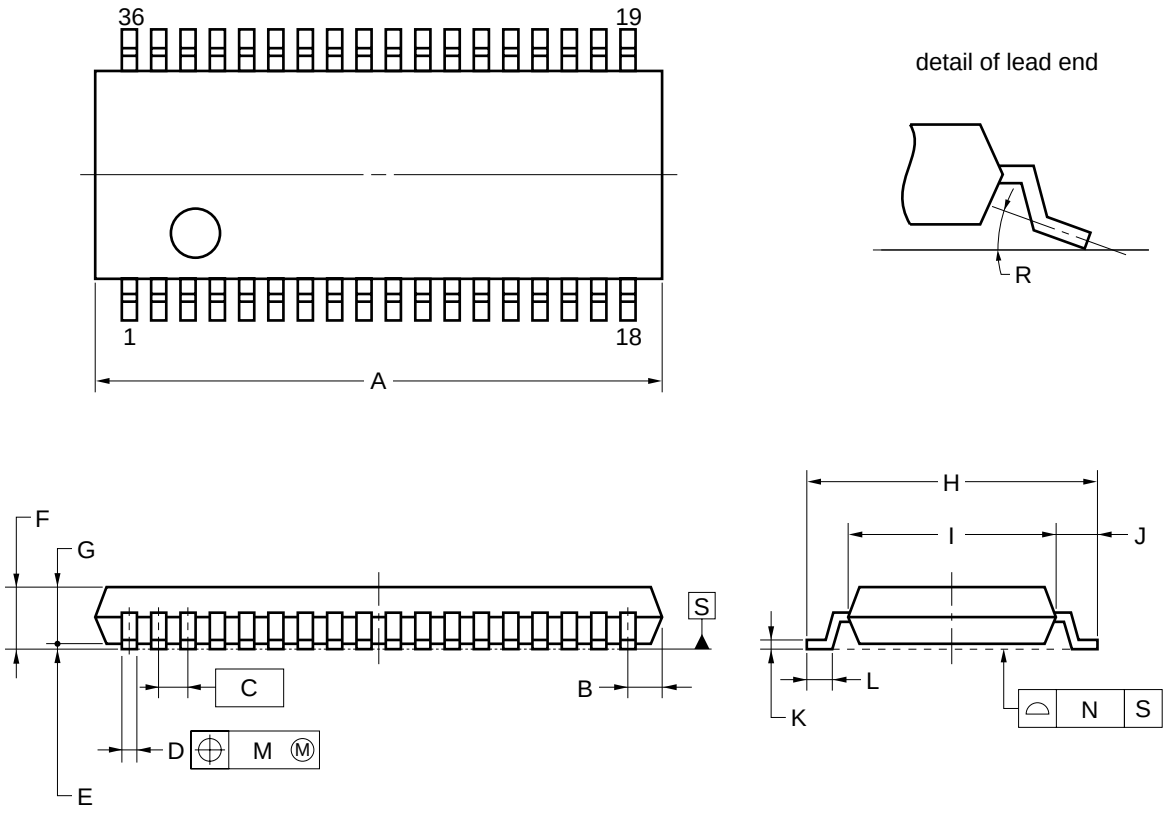
Product No.	Connection Diagram	Prototype No.	Specifications
L1		X119FNS-16314Z	(1) - (3) 15T L = 4.7 μH Qu > 60
L2		388DN-1043BS	(4) - (6) 1440T L = 100 mH Qu > 45
L3		247BR-0147Z	(1) - (3) 274T L = 2 mH Qu > 50
L4		392AN - 1871Y	(1) - (3) (1) - (2) (2) - (3) 8T 4T 4T L = 1.8 μH Qu > 70
T1		392AC-1883N	(1) - (3) (1) - (2) (2) - (3) 14T 7T 7T (4) - (6) C = 43 pF 3T Qu > 50 f_O = 10.7 MHz
T2		7PSYC-1779N	(1) - (3) (1) - (2) (2) - (3) 152T 76T 76T (4) - (6) C = 180 pF 40T Qu > 25 f_O = 450 kHz
T3		CX7YCS-8986N	(1) - (3) (1) - (2) (2) - (3) 148T 43T 105T (4) - (6) C = 180 pF 30T Qu > 40 ±20 % f_O = 450 kHz

- BPF SFE10.7 MHY-A (MURATA mfg. Co., Ltd.)
  CFWS450HT (MURATA mfg. Co., Ltd.)

- RF FET 2SK1000 (NEC)

6. Package Drawing

36 PIN PLASTIC SSOP (300 mil)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	15.3±0.24
B	0.97 MAX.
C	0.8 (T.P.)
D	$0.37^{+0.08}_{-0.07}$
E	0.125±0.075
F	$1.675^{+0.125}_{-0.175}$
G	1.55
H	7.7±0.3
I	5.6±0.15
J	1.05±0.2
K	$0.22^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.10
N	0.10
R	5°±5°

P36GM-80-300B-4

7. Recommended Soldering Conditions

When soldering this product, it is highly recommended to observe the conditions as shown below. If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E)**.

Surface mount device

μPC2533GS-01, 2533GS-02: 36-pin plastic shrink SOP (300 mil)

Process	Conditions	Symbol
Infrared ray reflow	Peak temperature: 235 °C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210 °C or higher), Maximum number of reflow processes: 2 times.	IR35-00-2
VPS	Peak temperature: 215 °C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200 °C or higher), Maximum number of reflow processes: 2 times.	VP15-00-2
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120 °C or below (Package surface temperature).	WS60-00-1
Partial heating method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

[MEMO]

[MEMO]

[MEMO]

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
NEC devices are classified into the following three quality grades:
"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

- Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
- Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
- Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.
Anti-radioactive design is not implemented in this product.

M4 96.5

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.